TRANSMISSION GATE BASED 8T SRAM CELL FOR BIOMEDICAL APPLICATIONS

PROJECT REPORT

submitted by,

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To
the APJ Abdul Kalam Technological University

in partial fulfillment of the requirements for the award of the Degree

of *Bachelor of Technology in Electronics & Communication*

under the guidance of

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TKM COLLEGE OF ENGINEERING, KOLLAM 691005

MAY 2024

DECLARATION

We, hereby declare that the main project report "**TRANSMISSION GATE BASED 8T SRAM CELL FOR BIOMEDICAL APPLICATIONS"** submitted for partial fulfillment of the requirements for the award of degree of Bachelor of Technology in Electronics and Communication Engineering of APJ Abdul Kalam Technological University, Kerala , is a bonafide work done by us under the supervision of Prof. Amal mole S (Assistant Professor of the Dept of ECE, TKM College of Engineering), Prof. Nishanth N (HOD, Dept. of ECE, TKM College of Engineering, Kollam), Prof. Vishnu D (Assistant Professor, Dept. of ECE, TKM College of Engineering, Kollam), This submission represents our ideas in our own words, and where ideas or words of others have been included, we have adequately and accurately cited and referenced the original sources. We also declare that we have adhered to ethics of academic honesty and integrity and have not misrepresented or fabricated any data or idea or fact or source in our submission. We understand that any violation of the above will be a cause for disciplinary action by the institute and/or the University and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission hats not been obtained.

Place: KOLLAM

Date: 05/5/2024

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CERTIFICATE

This is to certify that the major project report entitled "**TRANSMISSION GATE BASED 8T SRAM CELL FOR BIOMEDICAL APPLICATIONS" is bonafide record of the work presented by C J ADITHYAN (TKM20EC039), ANAGHA V (LTKM20EC132) ROHITH S (TKM20EC048), MOHAMMED SANOOF T (TKM20EC104)** to APJ Abdul Kalam technological university in partial fulfillment of the requirement for the award of degree bachelor of Technology in Electronics and Communication Engineering during the academic year 2023-2024 under our guidance and supervision. This report in any form has not been submitted to any other University or Institute for any purpose.

Prof. Amal mole S	**Prof. Vishnu D**	**Prof. Nishanth N**
Project Guide	project coordinator	Head of department

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ABSTRACT

There is an immense necessity for several kilobytes of embedded memory for Biomedical systems which typically operate in the sub-threshold domain with perfect efficiency. SRAMs dominates the total power consumption and the overall silicon area, as 70% of the die has been occupied by them. This brief proposes the design of a Transmission gate-based SRAM cell for Biomedical applications eliminating the use of peripheral circuitry during the read operation. This topology offers a smaller area, reduced delay, low power consumption, and improved data stability in the read operation. Static random-access memories mostly contribute to the performance, area, and power dissipation of digitally integrated systems. The mentioned implantable and wireless applications require low-power circuits operating for a long time, occupying less area without degrading the performance, as it provides inconvenience and may even be risky especially while considering the implantable devices.

CONTENTS

LIST OF ABBREVIATIONS

SRAM	STATIC RANDOM ACCESS MEMORY
9T,6T	9 TRANSISTOR /6 TRANSISTOR
BL	BIT LINE
WWL	WRITE WORD LINE

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CHAPTER 1

INTRODUCTION

Static Random-Access Memory is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance but is still volatile in a conventional sense, that data is eventually lost when memory is not powered. The continuous scaling down of bulk CMOS creates major issues due to its base material. The primary obstacles to the scaling of bulk CMOS to 32nm gate lengths include short channel effects Sub-threshold leakage gate-dielectric leakage and device-to-device variations. Due to the sudden increase in threshold voltage oscillation produced by overall and general process variations occur in ultra-short channel devices, 6T SRAM cell and their modifications cannot be operated at advance scaling of supply voltages without functional and parametric failure causing yield loss. The design of a standard 6T SRAM cell undergoes a lot of problems with write delay. The design of Low power 6T SRAM cell could decrease the write power and access delay but could not improve their stability. In deep submicron ranges, none of the earlier works has studied about the improvement of variability in SRAM cells at the schematic level.

CHAPTER 2

LITERATURE REVIEW

[1] G. Pasandi and S. M. Fakhraie, "An 8T Low-Voltage and Low-Leakage Half-Selection Disturb-Free SRAM Using Bulk-CMOS and FinFETs," in IEEE Transactions on Electron Devices, vol. 61, no. 7, pp. 2357-2363, July 2014, doi: 10.1109/TED.2014.2321295.

In this paper, present a new 8T design for static random access memory (SRAM) cell that is based on traditional Si technology and reduces leakage power considerably compared with a conventional design. Proposed design can be fully functional at smaller supply voltages over the conventional 6T SRAM cell. To verify the proposed design, a 32 kb SRAM is designed and simulated in 90 nm CMOS technology using the proposed 8T and conventional 6T SRAM cells. Operating at their VDDmin, simulations show improvement of 58% and 67% for write and read power per operation, respectively, for our design. To address the challenge of half-selection during write operation, a new low-power internal write-back scheme is presented. Finally, designing proposed cell using fin-shaped field effect transistors shows less sensitivity to variations and also improvement of 2.08× in read static noise margin at VDD = 1.0 V over bulk-CMOSbased SRAM cell.

[2] S. Gupta, K. Gupta, B. H. Calhoun and N. Pandey, "Low-Power Near-Threshold 10T SRAM Bit Cells With Enhanced Data-Independent Read Port Leakage for Array Augmentation in 32-nm CMOS," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 3, pp. 978-988, March 2019, doi: 10.1109/TCSI.2018.2876785.

The conventional six-transistor static random-access memory (SRAM) cell allows high density and fast differential sensing but suffers from half-select and read-disturb issues. Although the conventional eight-transistor SRAM cell solves the read-disturb issue, it still suffers from low array efficiency due to deterioration of read bit-line (RBL) swing and Ion/Ioff ratio with increase in the number of cells per column. Previous approaches to solve these issues have been afflicted by low performance, data dependent leakage, large area, and high energy per access. Therefore, in this paper, we present three

iterations of SRAM bit cells with nMOS-only based read ports aimed to greatly reduce data dependent read port leakage to enable 1k cells/RBL, improve read performance, and reduce area and power over conventional and 10T cell-based works. We compare the proposed work with other works by recording metrics from the simulation of a 128-kb SRAM constructed with divided-word line-decoding architecture and a 32-bit word size. Apart from large improvements observed over conventional cells, up to 100-mV improvement in read-access performance, up to 19.8% saving in energy per access, and up to 19.5% saving in the area are also observed over other 10T cells, thereby enlarging the design and application gamut for memory designers in low-power sensors and battery-enabled devices.

[3] J. P. Kulkarni and K. Roy, "Ultralow-Voltage Process-Variation-Tolerant Schmitt-Trigger-Based SRAM Design," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 20, no. 2, pp. 319-332, Feb. 2012, doi: 10.1109/TVLSI.2010.2100834.

Analyze Schmitt-Trigger (ST)-based differential-sensing static random-access memory (SRAM) bitcells for ultralow-voltage operation. The ST-based SRAM bitcells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bitcell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bitcell. The proposed ST bitcells incorporate a built-in feedback mechanism, achieving process variation tolerance—a must for future nano-scaled technology nodes. A detailed comparison of different bitcells under iso-area condition shows that the ST-2 bitcell can operate at lower supply voltages. Measurement results on ten test-chips fabricated in 130-nm CMOS technology show that the proposed ST-2 bitcell gives 1.6 higher read static noise margin, 2 higher write-trip-point and 120-mV lower read- compared to the iso-area 6T bitcell.

[4] G. Pasandi and S. M. Fakhraie, "A 256-kb 9T Near-Threshold SRAM With 1k Cells per Bitline and Enhanced Write and Read Operations," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 23, no. 11, pp. 2438-2446, Nov. 2015, doi: 10.1109/TVLSI.2014.2377518.

In this paper, present a new 9T SRAM cell that has good write ability and improves read stability at the same time. Simulation results show that the proposed design increases read static noise margin and ION/IOFF of read path by 219% and 113%, respectively, at supply voltage of 300-mV over conventional 6T SRAM cell in a 90-nm CMOS technology. The proposed design lets us reduce the minimum operating voltage of SRAM (VDD min) to 350 mV, whereas conventional 6T SRAM cannot operate successfully with an acceptable failure rate at supply voltages below 725 mV. We also compared our design with three other SRAM cells from recent literature. To verify the proposed design, a 256-kb SRAM is designed using new 9T and conventional 6T SRAM cells. Operating at their minimum possible VDDs, the proposed design decreases write and read power per operation by 92% and 93%, respectively, over the conventional rival. The area of the proposed SRAM cell is increased by 83% over a conventional 6T one. However, due to large ION/IOFF of read path for 9T cell, we are able to put 1k cells in each column of 256-kb SRAM block, resulting in the possibility for sharing write and read circuitries of each column between more cells compared with conventional 6T. Thus, the area overhead of 256- kb SRAM based 0n new 9T cell is reduced to 37% compared with 6T SRAM.

CHAPTER 3

EXISTING SRAM'S

The SRAM cell is designed to perform read, write, and hold operations as long as power is applied. Although an ordinary flip-flop could fulfil this requirement, it would result in a larger cell size. However, in large RAM arrays where memory cells dominate the area, this trade-off may be acceptable. The smaller cell size of the 6T SRAM cell, as shown in Figure 1, offers shorter wires, which in turn reduces dynamic power consumption. The 6T SRAM cell contains a pair of weak cross-coupled inverters that hold the state, along with a pair of access transistors for reading or writing the state. This compact design enables efficient reading and writing of the cell, while the positive feedback mechanism corrects disturbances caused by leakage or noise.

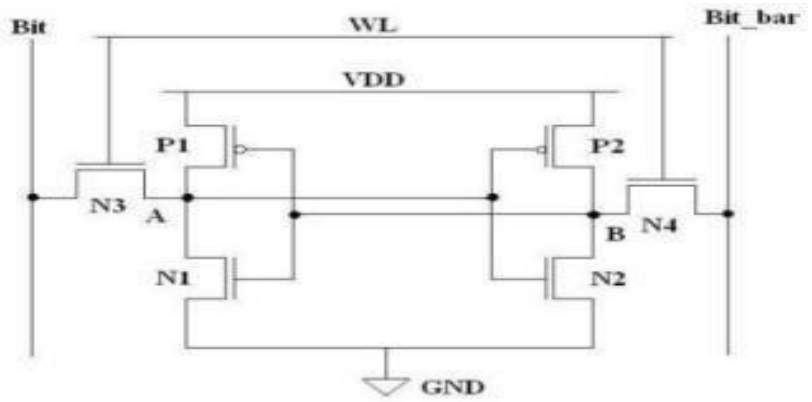

Fig 1: 6T SRAM Cell

Operation

Standby Mode (the circuit is idle):

When in standby mode, the word line will be set to 0, causing transistors N3 and N4 to be activated and connect the 6T cell. As a result, the cell will not be accessible. Meanwhile, the cross-coupled inverters N1 and N2 will continue to provide feedback as long as they remain connected to the power supply, data, and hold signals in the latch.

Read Mode:

During the read mode, the word line signal will be set to 1, enabling both transistors N1 and N2. The values stored in nodes a and b are then transferred to the bit lines. If a logic 1 is stored at node a, the bit line bar will discharge through the driver transistor N1, while the bit line will be pulled up towards VDD through the load transistor P1.

Write Mode:

During the write mode, if we want to write either a 0 or a 1, the bit line needs to be lowered to 0V, while the bit bar is raised to VDD, and the cell is selected by raising the word line to VDD. If we want to write a 0 at node a, transistor N3 operates in saturation, with its source voltage at 1V. The drain terminal of N3 starts at 1V and is pulled down by N3 because N3 is stronger than N1. As a result, N2 turns on and P1 turns off, allowing the new value to be written, forcing the bit line to be lowered to 0V and the bit bar to be raised to VDD.

CHAPTER 4

8T SRAM CELL

To address the limitations of the conventional 6T SRAM cell, several alternative designs have been proposed, starting with the 8T SRAM cell, as shown in Fig. 2. This modified cell includes a decoupled read path with two additional NMOS transistors to mitigate the read stability issue. However, one drawback of this design is increased leakage current due to the additional transistors that depend on the stored information in the cell. This added complexity may result in reduced reliability, particularly in sub-micron technology, where process parameter variations are more pronounced.

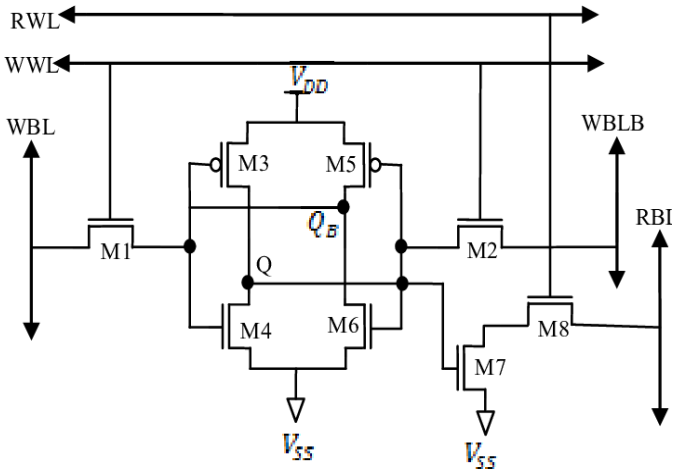

Fig 2**:** 8T SRAM Cell

The primary driving force behind aggressive device scaling is to achieve enhanced performance and increased integration in modern semiconductor technology. However, these improvements come at the cost of increased sensitivity to standby leakage and delay, especially in area-constrained circuits like SRAM that require minimum-sized devices. In this work, an effort has been made to address these challenges in the conventional 6T SRAM cell by considering the implications of minimum area requirements and incorporating a fully differential architecture.

CHAPTER 5

METHODOLODY

SIMULATION TOOL

Use of cadence tool to design and implement transmission gate-based 8T SRAM cell to achieve high data integrity, energy efficiency, less noise etc. Cadence Virtuoso is a widely used electronic design automation (EDA) tool suite in the semiconductor industry. It provides a platform for designing and simulating integrated circuits (ICs), including SRAM (Static Random Access Memory) circuits.

PROCEDURES FOR SIMULATION

Design Entry: Begin by creating or importing your VLSI circuit design into the Cadence tool. This may involve using schematic entry tools like Virtuoso Schematic Composer

Library Setup: Ensure that the necessary technology libraries and models are available and linked appropriately. Cadence tools rely on technology files and libraries to understand the characteristics of the semiconductor process being used.

Simulation Setup: Choose the appropriate simulation tool within the Cadence suite based on the nature of your circuit. Specify simulation parameters such as simulation type (transient, DC, AC, etc.), simulation time, and any other relevant settings.

Netlist Generation: Generate the simulation netlist from your design. This netlist represents the circuit in a format that the simulator can understand.

Simulation Execution: Run the simulation using the chosen simulator. Cadence tools provide a range of simulation types, including transient simulations, DC sweeps, AC analyses, and more. Monitor the simulation progress and check for any error messages or warnings.

Results Analysis: After the simulation completes, analyze the results to evaluate the performance of your circuit. This may involve plotting waveforms, extracting specific data points, or performing statistical

analyses. Cadence tools often provide waveform viewers and data analysis tools to help interpret simulation results.

Optimization and Debugging: Based on the simulation results, optimize your design for performance, power, or other relevant metrics. Use debugging features in the Cadence tool to identify and resolve any issues or unexpected behavior in the circuit.

Verification: Perform additional verification steps to ensure that the simulated behavior aligns with the intended design. This may involve comparing simulation results with specifications or other reference models.

Documentation: Document the simulation setup, results, and any design changes made during the optimization process. This documentation is valuable for future reference and collaboration

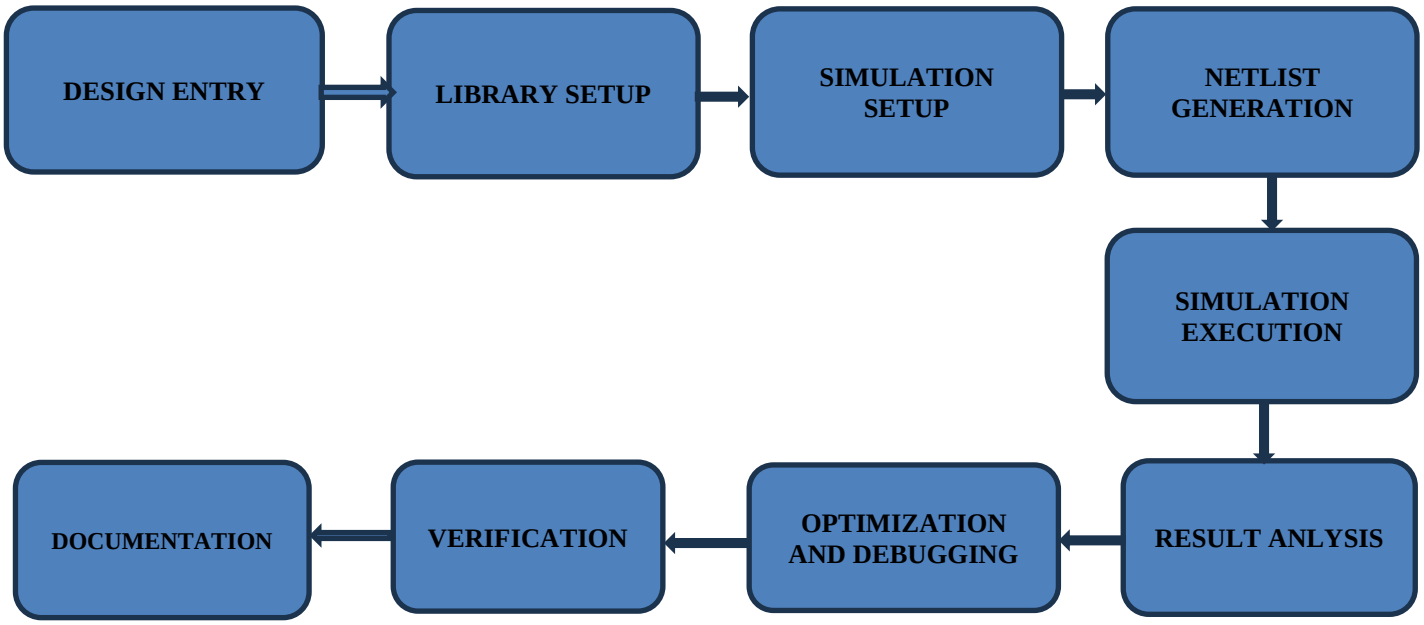

Fig 3: Block Diagram

CHAPTER 6

CIRCUIT DIAGRAM

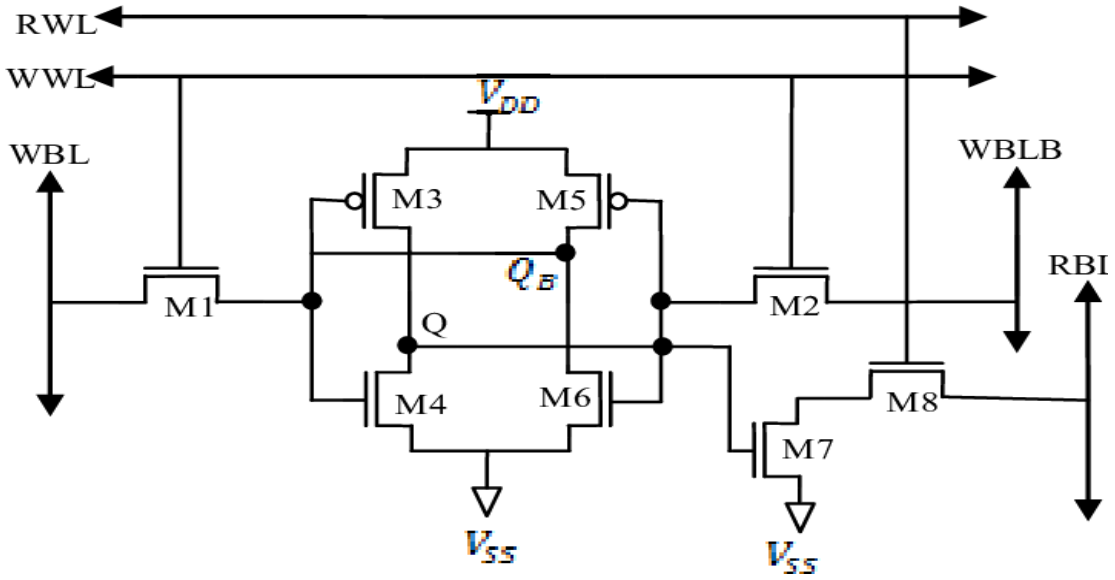

Fig 4: Initially Proposed 8T SRAM Circuit

Working:

Read operation: To read the data stored in the cell, the word line (WL) signal is asserted high. This turns on the two access transistors (M1 and M2), which connect the bit lines (BL and BLB) to the storage nodes (Q and CB). The bit lines are then precharged to VDD or GND, depending on the state of the cell. If Q is at VDD and CB is at GND, then BL will be precharged to VDD and BLB will be precharged to GND. Otherwise, BL will be precharged to GND and BLB will be precharged to VDD.

Write operation: To write data to the cell, the write word line (WWL) signal is asserted high and the word line (WL) signal is asserted low. This turns on the two write transistors (M3 and M5), which connect the bit line (BL) to the storage nodes (Q and CB). The voltage on BL will then be written to the storage nodes.

Standby mode: When the cell is not being read or written to, both the word line (WL) and write word line (WWL) signals are deasserted low. This turns off all of the transistors in the cell, and the data stored in the cell is retained.

CHAPTER 7

SCHEMATIC CIRCUIT

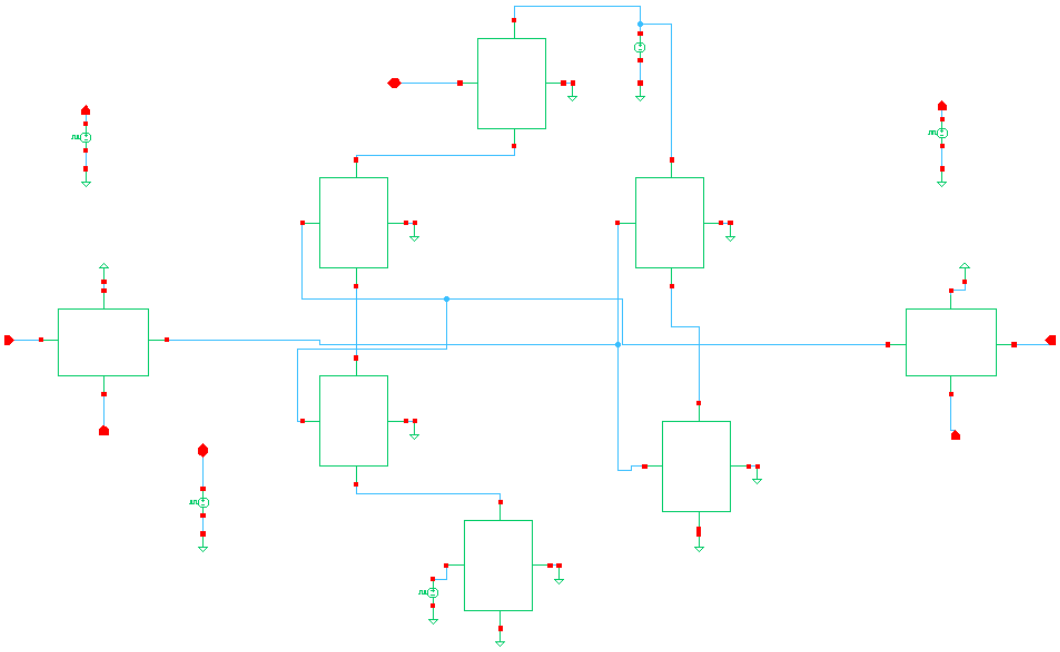

Fig 5: Final Proposed SRAM Circuit Using 8 Transmission Gates

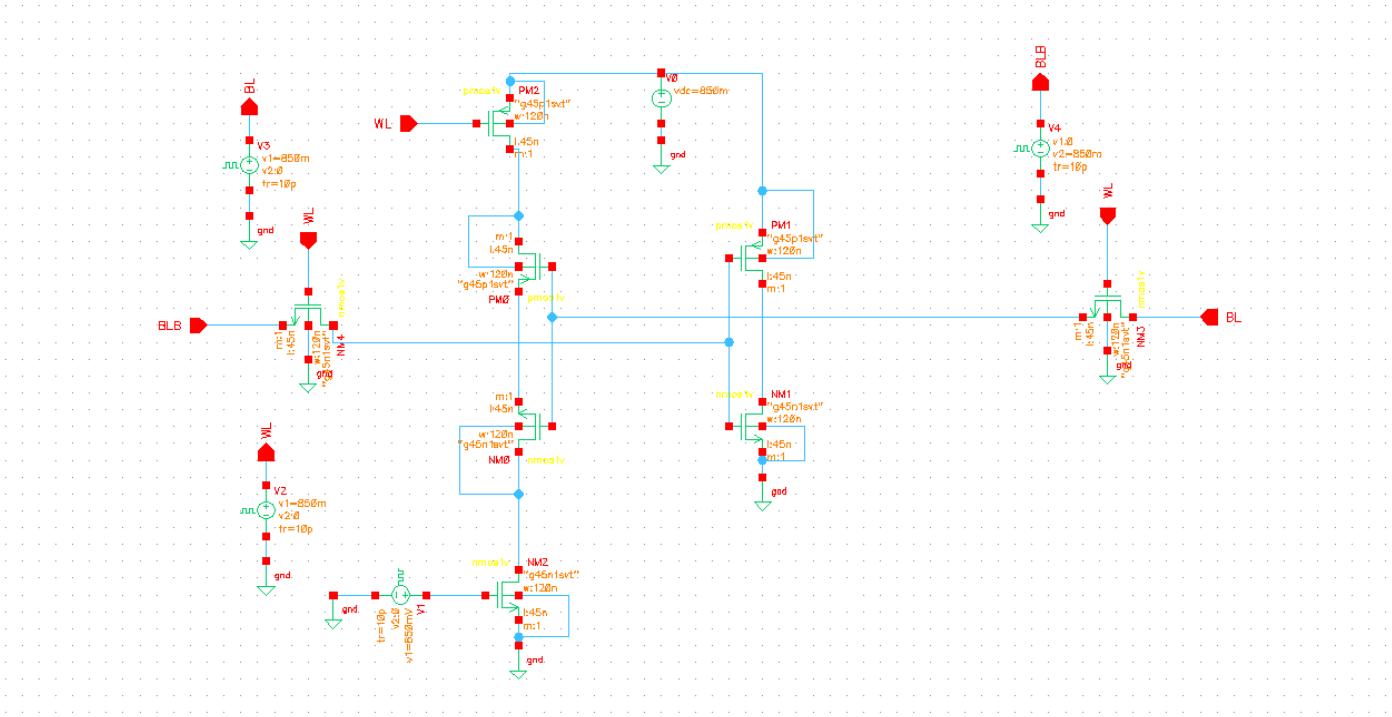

Fig 6: 8 T SRAM Circuit Diagram

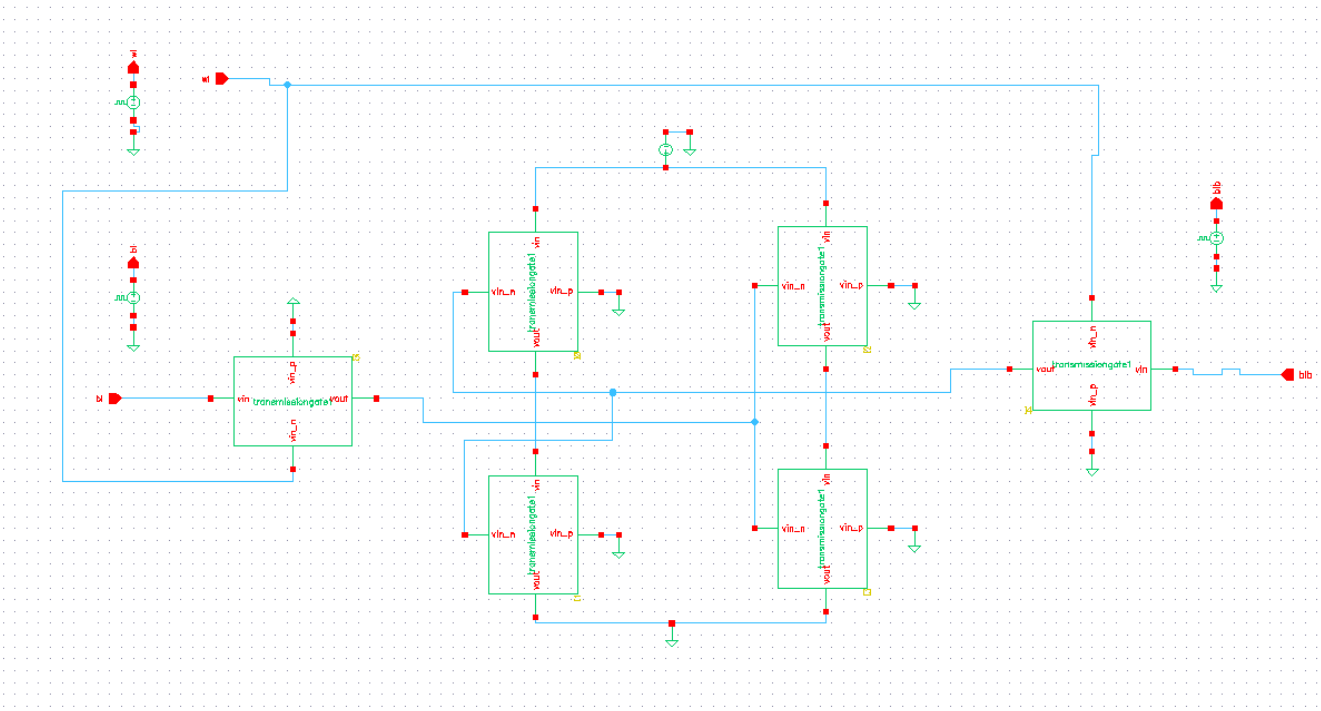

Fig 7: SRAM Circuit Using 6 Transmission Gates

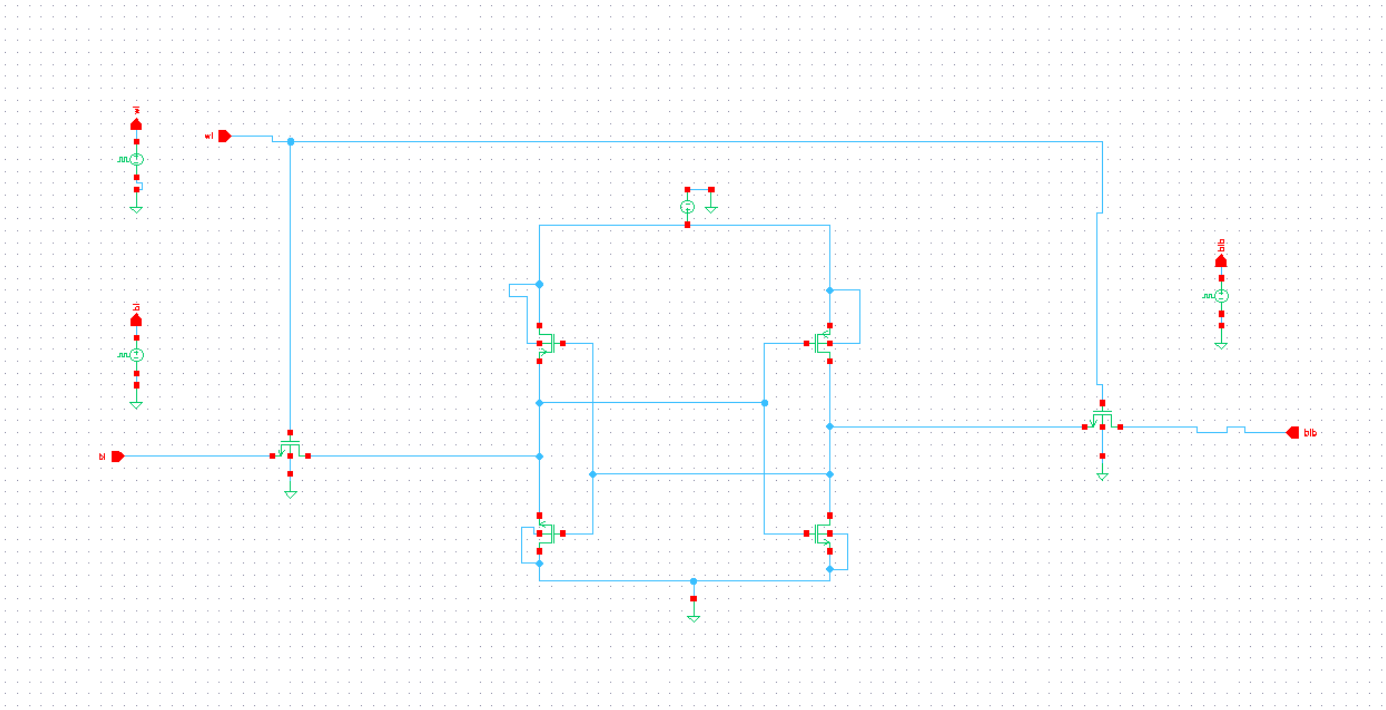

Fig 8: 6T SRAM Circuit Diagram

CHAPTER 8

EXPERIMENTAL RESULT AND ANALYSIS

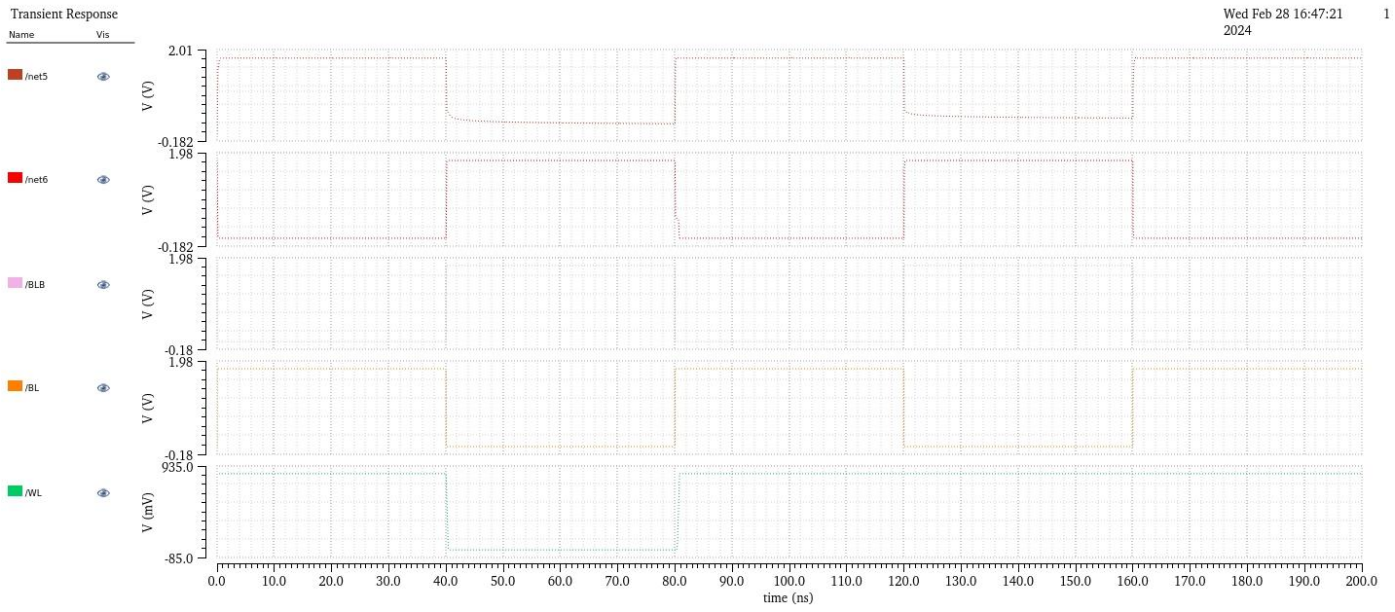

Fig 9: Output Proper Working

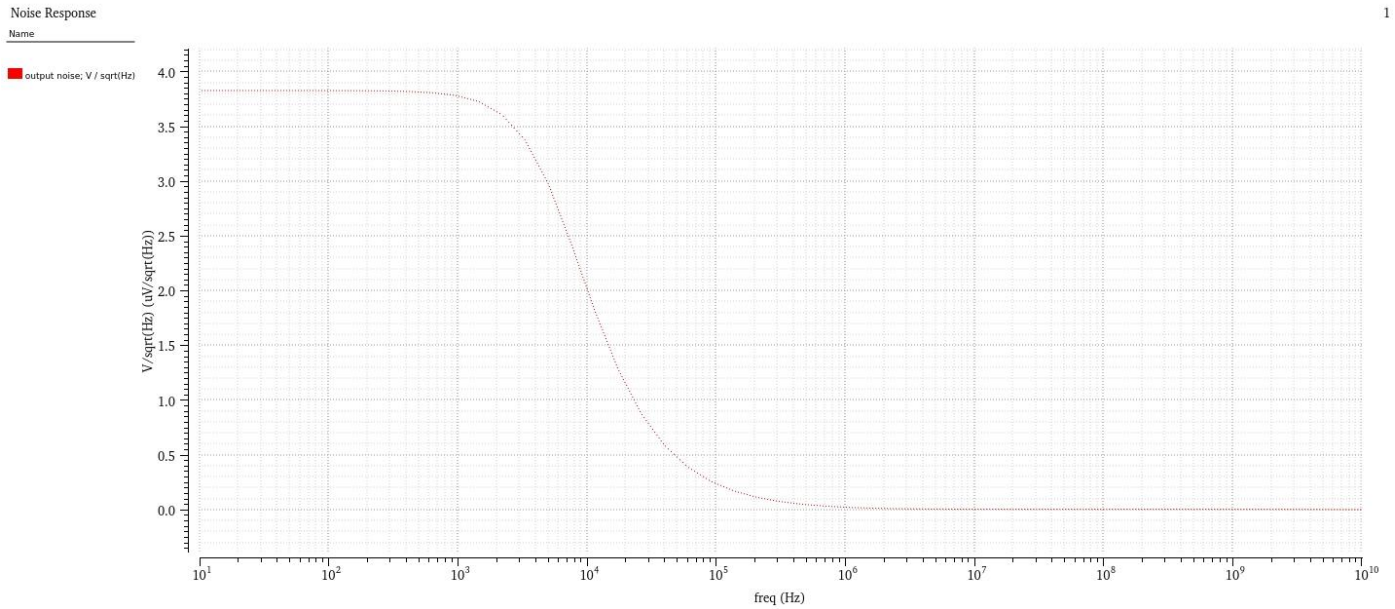

Fig 10: Output Noise Graph of SRAM Circuit Using 8 Transmission Gate

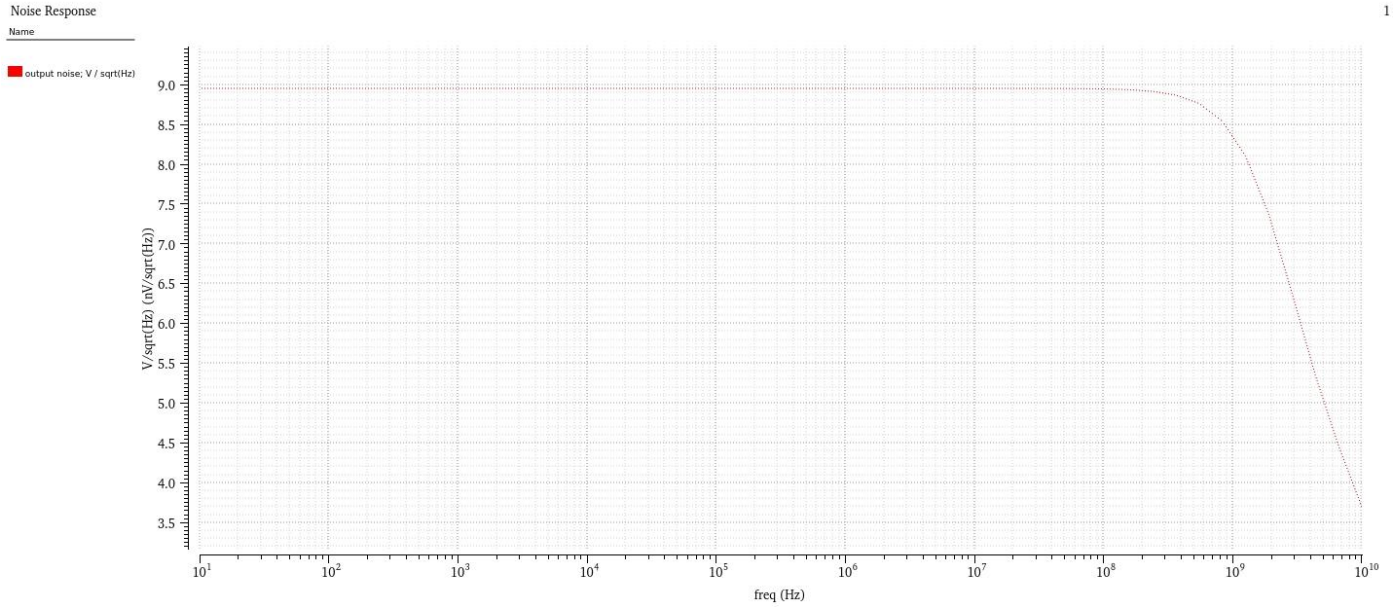

Fig 11: Output Noise Graph of SRAM Circuit Using 6 Transmission Gate

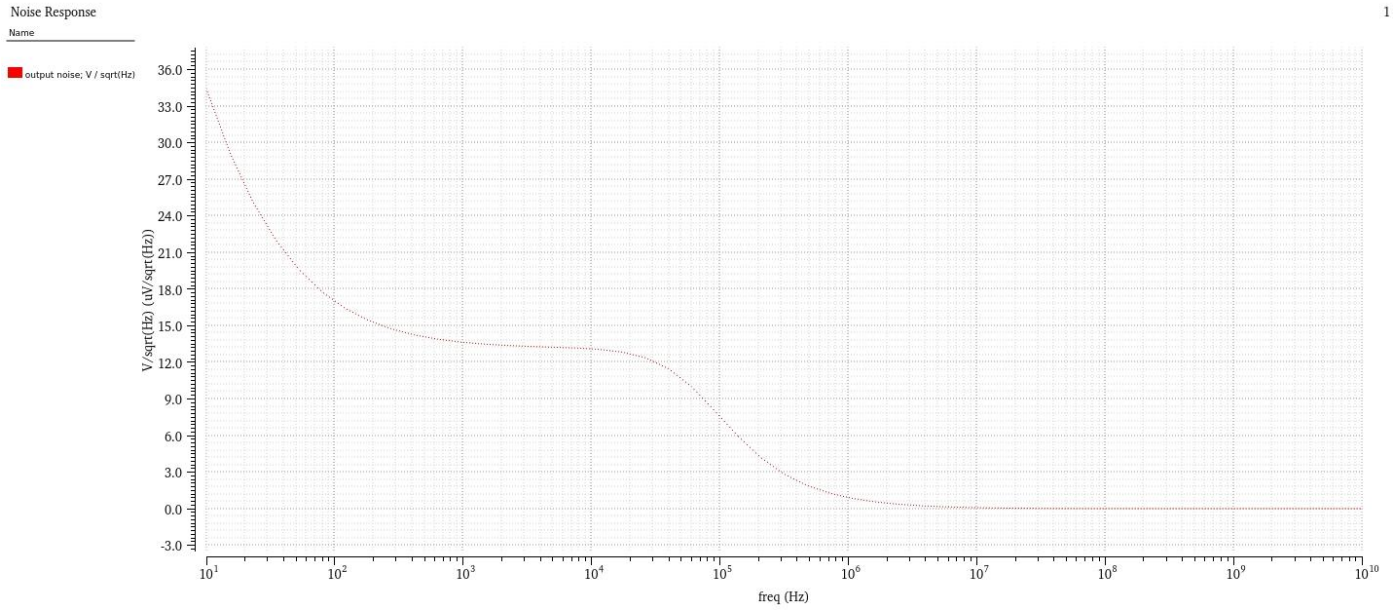

Fig 12: Output Noise Graph of 8T SRAM CMOS Circuit

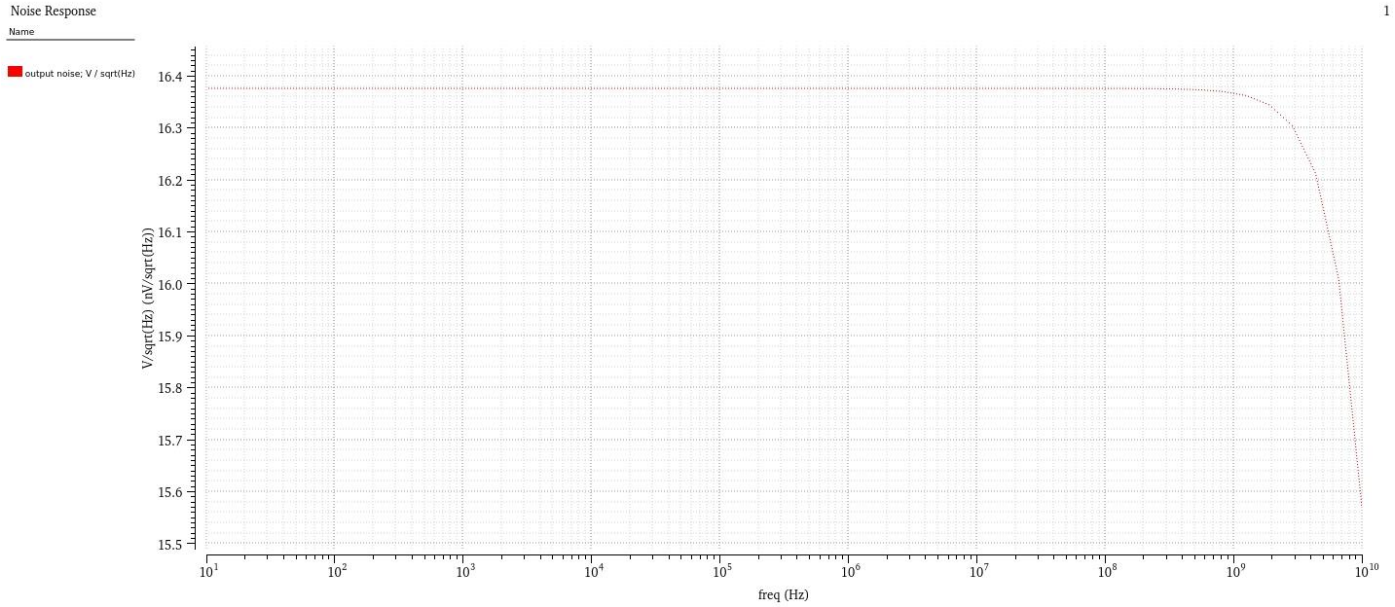

Fig 13: Output Noise Graph of 6T SRAM CMOS Circuit

	8T TRANSMISSION	8T CMOS	6T TRANSMISSION	6T CMOS
TECHNOLOGY	45	45	45	45
NOISE	4.40E-09	15.1E-09	5.62E-09	16.1E-09

Table 1: Comparison Result

The output waveforms indicate that the 8T SRAM cell is functioning correctly. The storage nodes are able to store and maintain a differential voltage, indicating the state of the stored data (logic 0 or 1). The transistor currents (M1 and M2) are highest during the write operation and very low during the idle state.

CHAPTER 9
ADVANTAGES & FUTURE SCOPE

1. Introduction to Noise Reduction in SRAM for Biomedical Applications

SRAM (Static Random-Access Memory) plays a critical role in biomedical devices, where reliability and performance are paramount. However, the operation of SRAM circuits can be susceptible to various noise sources, which can compromise device functionality and accuracy. Therefore, there is a growing need to develop advanced noise reduction techniques tailored specifically for SRAM used in biomedical applications.

2. Advanced Noise Modeling and Analysis

The future holds promising advancements in noise modeling and analysis techniques for SRAM circuits in biomedical applications. Researchers are exploring sophisticated simulation tools capable of accurately predicting and analyzing noise sources within SRAM cells. These tools leverage advanced algorithms, including machine learning approaches, to improve the efficiency and reliability of noise prediction and mitigation.

3. Low-Noise SRAM Design Techniques

Emerging design methodologies focus on reducing noise in SRAM circuits to enhance their performance in biomedical devices. These techniques encompass innovative layout strategies to minimize coupling effects and optimize signal integrity. Additionally, optimization of transistor sizing and biasing schemes aims to mitigate thermal noise and improve overall circuit performance. Integration of advanced materials with reduced intrinsic noise properties also holds promise for enhancing noise immunity in SRAM designs.

4. Integration with Noise-Canceling Technologies

The integration of noise-canceling technologies into SRAM designs represents a significant advancement in noise reduction for biomedical applications. Adaptive noise cancellation circuits can actively suppress noise sources and improve the signal-to-noise ratio within SRAM cells. Feedback mechanisms and dynamic biasing schemes are being explored to adaptively mitigate noise in real-time. Furthermore, digital signal processing techniques are being utilized to enhance noise resilience and improve overall system performance in biomedical devices.

5. Biomedical Signal Processing

Noise reduction in SRAM circuits is crucial for enhancing the accuracy and reliability of biomedical signal processing applications. Low-noise SRAM designs play a vital role in improving the quality of biosignal acquisition, medical imaging, and bioinformatics. These advancements have significant implications for wearable health monitoring devices, implantable medical devices, and diagnostic equipment, ultimately improving diagnosis, treatment, and patient outcomes in clinical settings.

6. Cross-Disciplinary Collaborations

Collaboration between semiconductor engineers, biomedical researchers, and healthcare professionals is essential for addressing noise-related challenges in SRAM for biomedical applications. These collaborations leverage expertise from multiple disciplines to develop innovative noise reduction solutions tailored to specific biomedical use cases. Successful partnerships have led to breakthrough advancements in noise reduction technology for biomedical devices, facilitating the translation of research findings into clinical practice.

7. Quantification of Noise Performance

Standardized methodologies for quantifying the noise performance of SRAM circuits in biomedical applications are essential for evaluating noise reduction techniques. Industry benchmarks, metrics, and testing procedures ensure compliance with stringent noise requirements in medical device regulations. Reliable characterization techniques enable the assessment of noise reduction strategies under varying operating conditions, facilitating the development of robust and reliable SRAM solutions for biomedical devices.

8. Clinical Translation and Adoption

The translation of noise-reduced SRAM technologies into clinical practice and commercial biomedical devices requires careful consideration of regulatory pathways, validation studies, and market adoption strategies. Ensuring safety, efficacy, and reliability are paramount in deploying noise-reduced SRAM circuits in healthcare settings. These advancements have the potential to significantly impact patient care, healthcare outcomes, and the advancement of biomedical engineering, ultimately improving the quality of life for patients worldwide.

CHAPTER 10
CONCLUSION

In this paper, Cadence virtuoso tool along with 45nm technology is used to observe the behaviors of different types of SRAM Circuits. This design provides a virtuous improvement in Noise parameter. This proposed work enlarges the overall performance of the system by reducing complexity and cost. By analyzing overall performance, the proposed SRAM has more advantages. In future research, it is important to focus on developing SRAM architectures and memory designs that are even more power efficient and have minimized noise requirements. With technology scaling, efforts should be made to further reduce the operating voltage, while optimizing speed and delay considerations for the system. By integrating these research advancements, the proposed SRAM design can be further improved in terms of noise reduction, speed, and area efficiency. The goal is to achieve a higher level of efficiency that considers noise, stability, and data storage as critical factors, building on the significant reduction in noise is achieved in the proposed design. In the future, additional optimization of the layout design can lead to further reductions in area overhead and improvements in the performance of the 8T SRAM cell. This may involve exploring various techniques for noise reduction techniques, transistor sizing, positioning, and routing to minimize parasitic capacitance and enhance signal integrity. By carefully optimizing the layout, it is possible to reduce noise requirements and improve the overall performance of the SRAM cell, leading to more efficient and effective memory designs. Continued research and development in this area can result in advanced layout design methodologies that push the boundaries of SRAM performance and area optimization.

CHAPTER 11

REFERENCES

[1] N. Maroof and B.-S. Kong, "10T SRAM using Half- VDD precharge and row-wise dynamically powered read port for low switching power and ultralow RBL leakage," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 4, pp. 1193–1203, Apr. 2017.

[2] Liang Wen, Xu Cheng, Keji Zhou, Shudong Tian, and Xiaoyang Zeng, " Bit-Interleaving-Enabled 8T SRAM With Shared Data-Awareand Reference-Based Sense Amplifier", IEEE Transactions on Circuits and Systems, vol. 63, No. 7, July 2016.

[3] J. P. Kulkarni and K. Roy, "Ultralow-voltage process- variation tolerant Schmitt-trigger-based SRAM design," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 319–332, Feb. 2012.

[4] J.-J. Wu, Y.-H. Chen, M.-F. Chang, P.-W. Chou, C.-Y. Chen, H.-J. Liao, M.-B. Chen, Y.-H. Chu, W.-C. Wu, and H. Yamauchi, "A large VTH/VDD tolerant zigzag 8T SRAM with area-efficient decoupled differential sensing and fast write-back scheme," IEEE J. Solid-State Circuits, vol. 46, no. 4, pp. 815–827, Apr. 2011

[5] J. P. Kulkarni, A. Goel, P. Ndai, and K. Roy, "A read- disturb-free, differential sensing 1R/1W port, 8T bitcell array," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 9, pp. 1727–1730, Sep. 2011.

[6] M.-H. Tu, J.-Y. Lin, M.-C. Tsai, S.-J. Jou, and C.-T. Chuang, "Single- ended subthreshold SRAM with asymmetrical write/read-assist," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 12, pp. 3039–3047, Dec. 2010

[7] G. Chen, M. Fojtik, D. Kim, D. Fick, J. Park, M. Seok, M.-T. Chen,Z. Foo, D. Sylvester, and D. Blaauw, "Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells," in proc. of IEEE Int. Solid State Circuits Conf. Dig. Tech. Papers, Feb. 2010, pp. 288– 289

[8] M. E. Sinangil, N. Verma, and A. P. Chandrakasan, "A reconfigurable 8T ultra-dynamic voltage scalable (U-DVS) SRAM in 65 nm CMOS," IEEE J. Solid-State Circuits, vol. 44, no. 11, pp. 3163– 3173, Nov. 2009.

[9] T.-H. Kim, J. Liu, and C. H. Kim, "A voltage scalable 0.26 V, 64 kb 8T SRAM with Vmin lowering techniques and deep sleep mode," IEEE J. Solid-State Circuits, vol. 44, no. 6, pp. 1785–1795, Jun. 2009.

[10] N. Verma and A. P. Chandrakasan, "A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy," IEEE J. Solid-State Circuits, vol. 43, no. 1, pp. 141–149, Jan. 2008.

[11] A. P. Chandrakasan, D. C. Daly, J. Kwong, and Y. K. Ramadass, "Next generation micro-power systems," in proc. of IEEE Symp. VLSICircuits, Jun. 2008, pp. 2–5.

[12] T.-H. Kim, J. Liu, J. Keane, and C. H. Kim, "A 0.2 V, 480 kb subthreshold SRAM with 1k cells per bitline for ultra-low-voltage computing," IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 518–529, Feb. 2008.

[13] Z. Liu and V. Kursun, "Characterization of a novel nine-transistor SRAM cell," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 16, no. 4, pp. 488–492, Apr. 2008.

[14] B. H. Calhoun and A. Chandrakasan, "A 256 kb sub- threshold SRAM in 65 nm CMOS," in proc. of IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2006, pp. 628–629.

[15] K. Nii, S. Shimada, K. Yanagisawa, and T. Kawahara, "Low-power embedded SRAM modules with expanded margins for writing," in proc. of IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2005, pp. 480– 481.

PO MAPPING

- **PO1 Engineering Knowledge**: The project was successfully executed by applying VLSI, Linear Integrated Circuits, and Analog Circuits knowledge
- **PO2 Problem Analysis**: The objective was to enhance efficiency of a SRAM circuit by reducing the noise parameter since noise parameter is an integral part in memory circuits used in biomedical applications.
- **PO3 Design/Development of solutions**: Transmission gate-based circuit is designed, SRAM circuit using 8 transmission gate is designed and developed to reduce the noise in memory circuit.
- **PO4 Conduct investigations of complex problems**: A comparative analysis was done for four different topologies in which one circuit is already existing, one is a circuit mentioned in a research paper and another design is designed by our team. Noise parameter values were determined.
- **PO5 Modern tool usage**: CADENCE VIRTUOSO was utilized as the simulation tool.
- **PO6 The Engineer and Society**: The future application of this project involves noise modeling and analysis techniques for SRAM circuits in biomedical applications.
- **PO7 Environment and Sustainability**: This project is software-based, promoting environmental sustainability.
- **PO8 Ethics**: The work is completely original and free from any instances of plagiarism. All external content used is appropriately referenced.
- **PO9 Individual and team work**: The project was completed through the collective effort and hard work of all team members.
- **PO10 Communication**: The project idea and its novelty were effectively communicated.
- **PO11 Project Management and Finance**: The project was efficiently completed by successfully managing time through the development of a timeline and strict adherence to it. The licensed version of CADENCE VIRTUOSO was employed for this project.
- **PO12 Lifelong learning**: Successful completion of the project involved a detailed study about various topologies, proposing a novel topology and gaining familiarity with the simulation tools used, through a self-learning process.