TRANSMISSION GATE-BASED 8T SRAM CELL FOR BIOMEDICAL APPLICATIONS

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Date: 6-05-24

CONTENTS

INTRODUCTION

- Noise is an integral parameter of memory circuits used in biomedical applications
- Biomedical devices often handle critical data.Noise in SRAM cells can corrupt this data, leading to errors in analysis, diagnosis, or treatment.
- Transmission gate based SRAM circuit is designed and simulated that reduces noise to a great extend.

OBJECTIVES

- To design, simulate, and evaluate a transmission gate-based 8T SRAM cell optimized for biomedical applications.
- To develop a robust and low-noise SRAM cell.
- To reliably store and retrieve data in scenarios relevant to biomedical devices.
- To achieve high data integrity and energy efficiency

METHODOLOGY

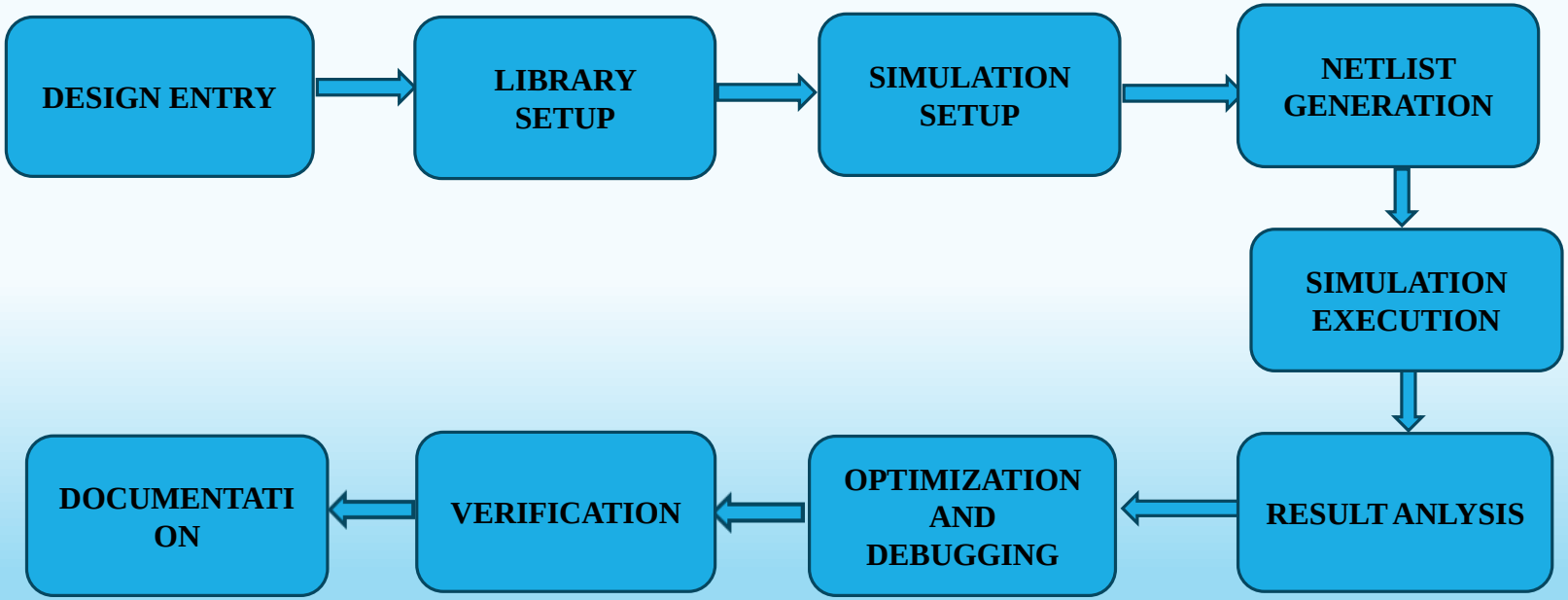

fig no.1:Block diagram

WORK FLOW

- Initially we designed the circuit in LTSPICE using cmos, referring the research paper we referred.
- We designed the circuit successfully and ensured its proper working using simulation.
- We could only evaluate the parameters at the nodes and couldn’t evaluate as a whole, also we couldn’t do different simulations in LTSPICE.Thus we switched to CADENCE virtuoso tool.

WORK FLOW

- In cadence, we designed a transmission gate using nmos and pmos of 45 nm technology.
- We decided to build and design a new circuit using this transmission gate similar to our initial design.
- We designed SRAM circuit using 8 transmission gates. Also designed a SRAM circuit using 6 transmission gates for comparison.
- To make the comparison more precise we designed a 8T SRAM circuit and 6T SRAM circuit using CMOS.

WORK FLOW

- We compared the noise,power and dc analysis as parameters using the 4 circuits designed.
- With the data values received , we concluded that the circuit is efficient in terms of Noise . Thus we concluded noise as our final parameter.The proposed circuit is thus proposed as an efficient SRAM circuit that could be used in biomedical applications.

INITIAL CIRCUIT DIAGRAM

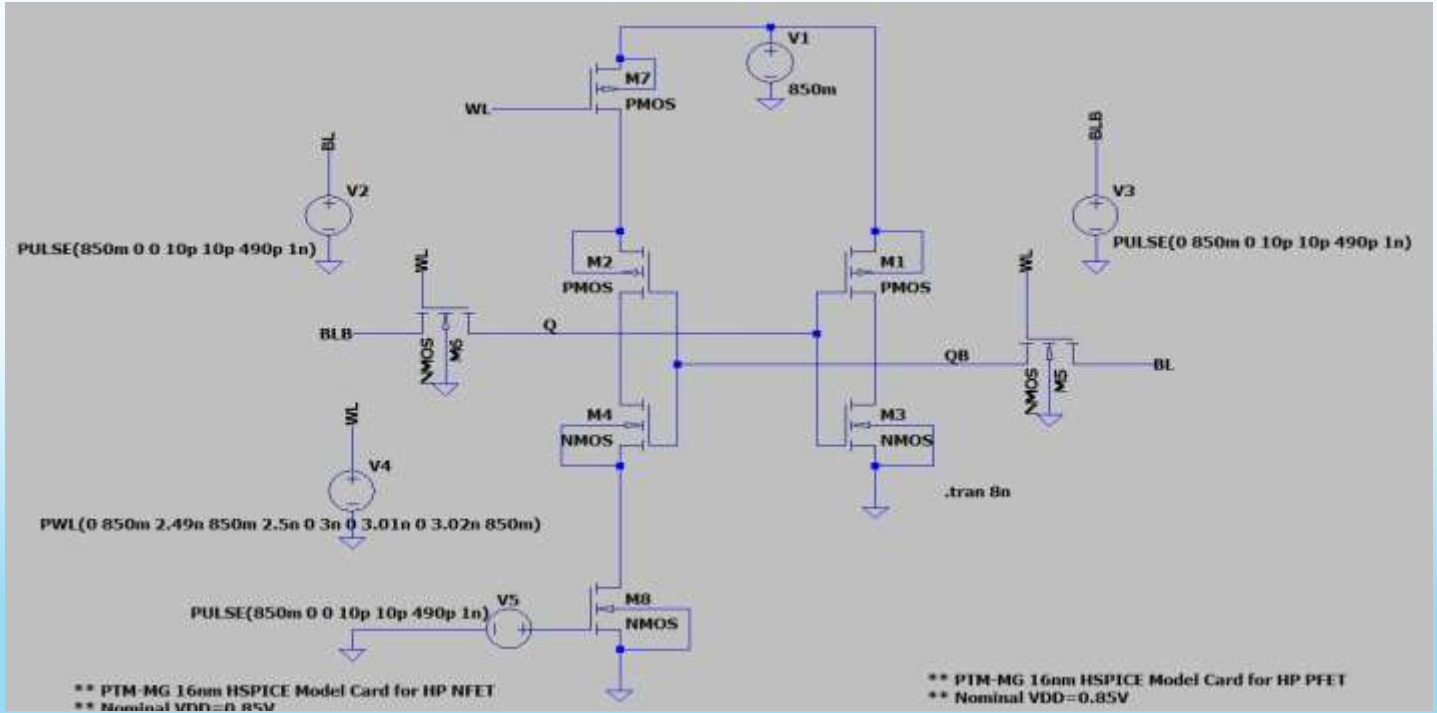

fig no.2:Circuit diagram

PROPOSED CIRCUIT DIAGRAM

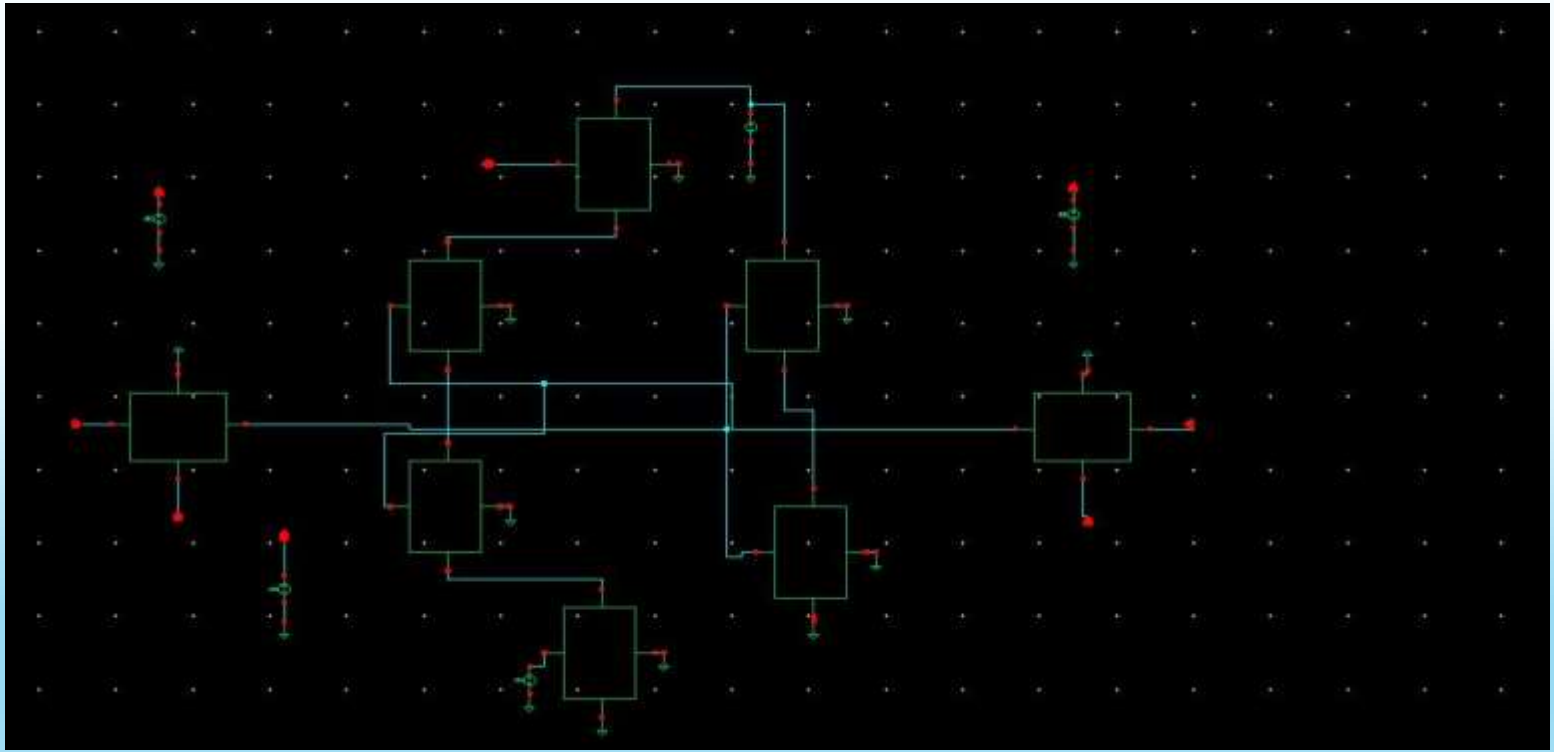

fig no.3 : SRAM circuit using 8 transmission gates

COMPARISON CIRCUITS

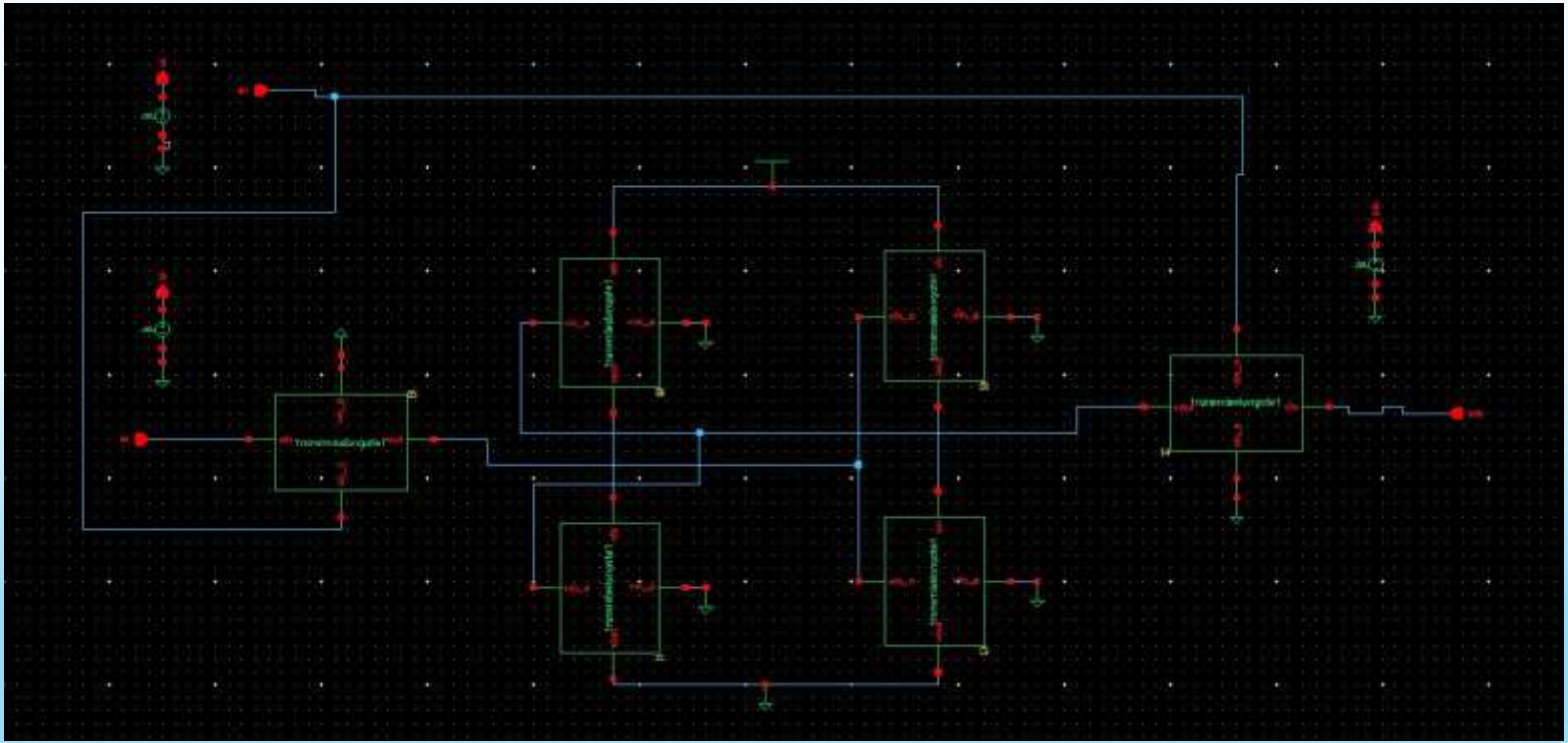

fig no.4 : SRAM circuit using 6 transmission gates

COMPARISON CIRCUITS

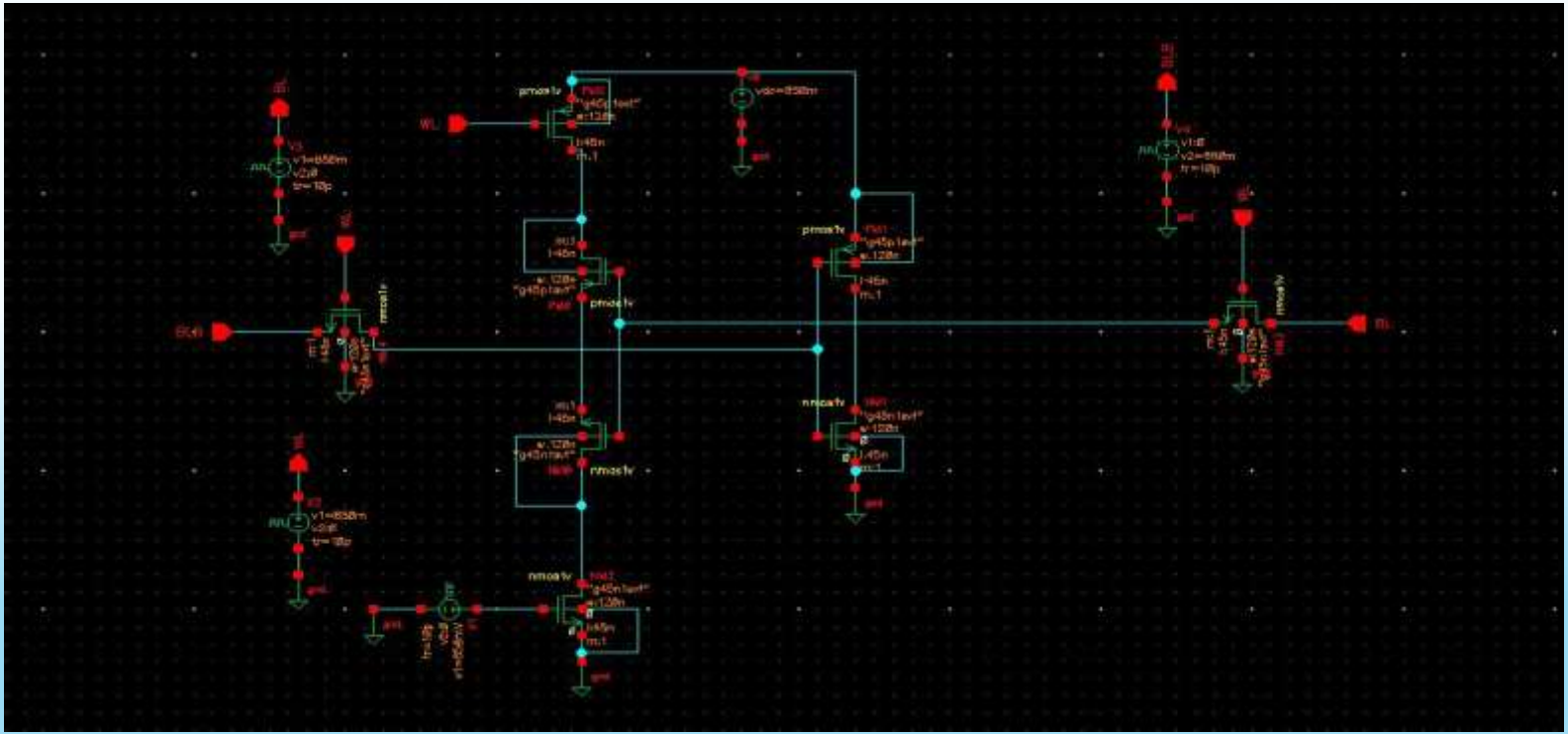

fig no.5 : 8T SRAM circuit using CMOS

COMPARISON CIRCUITS

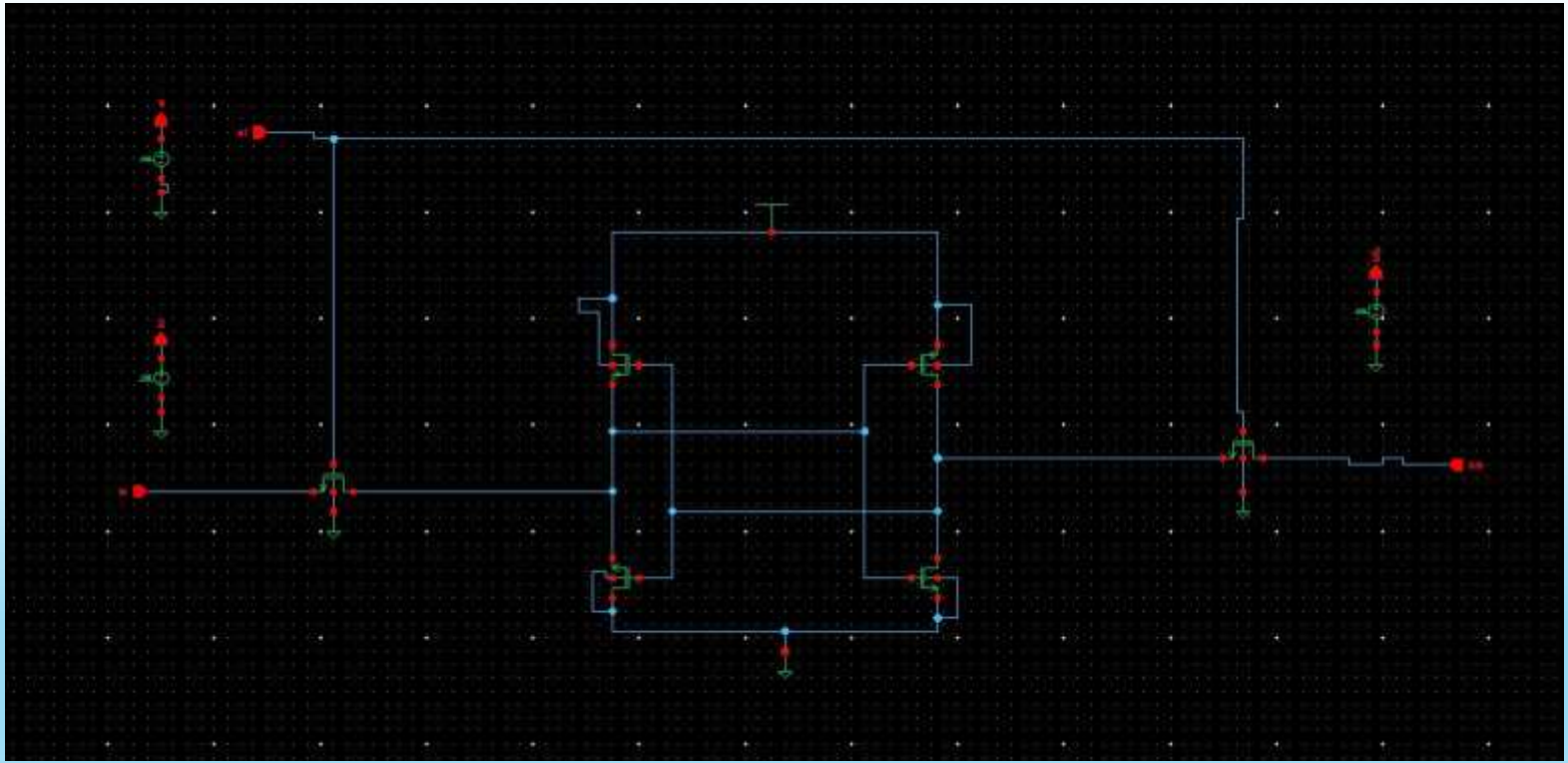

fig no.6 : 6T SRAM circuit using CMOS

OUTPUT OF PROPER WORKING

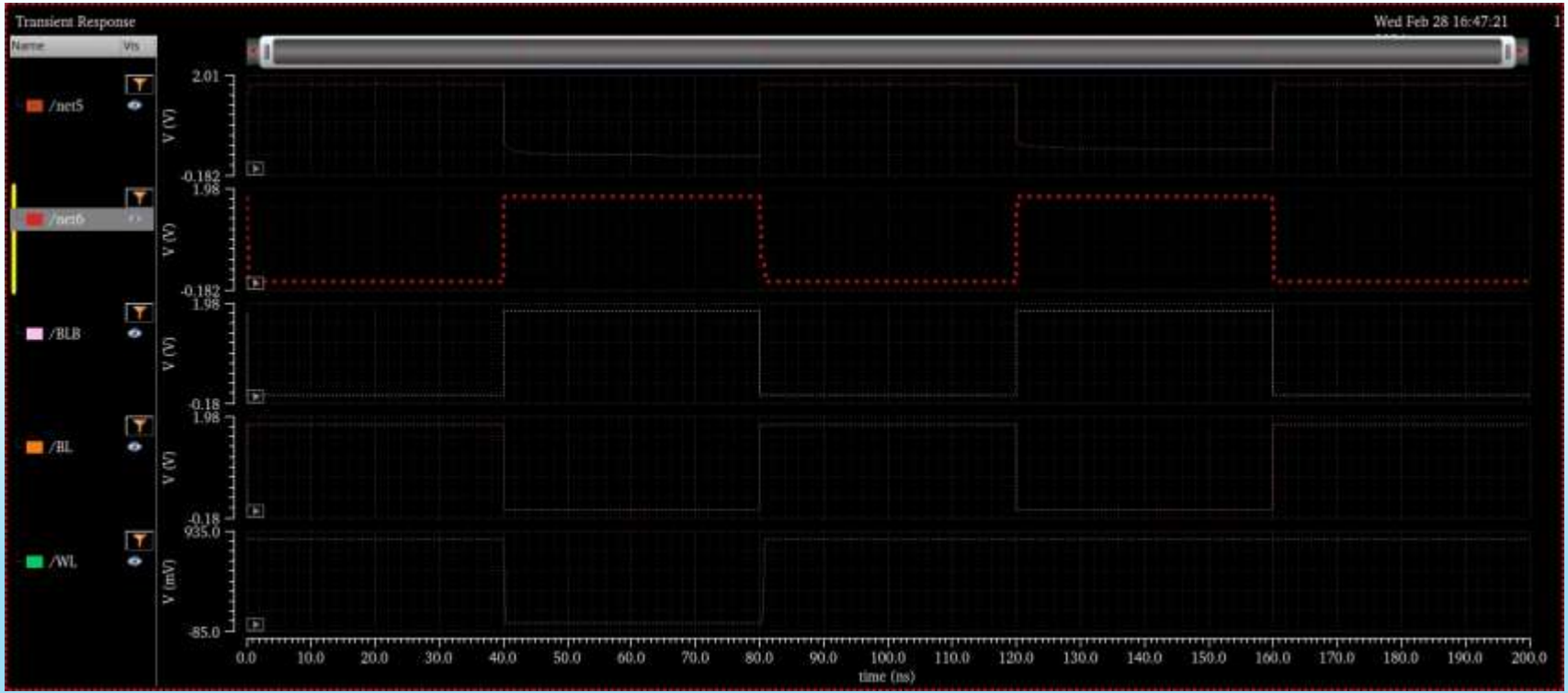

fig no.7 :CADENCE result

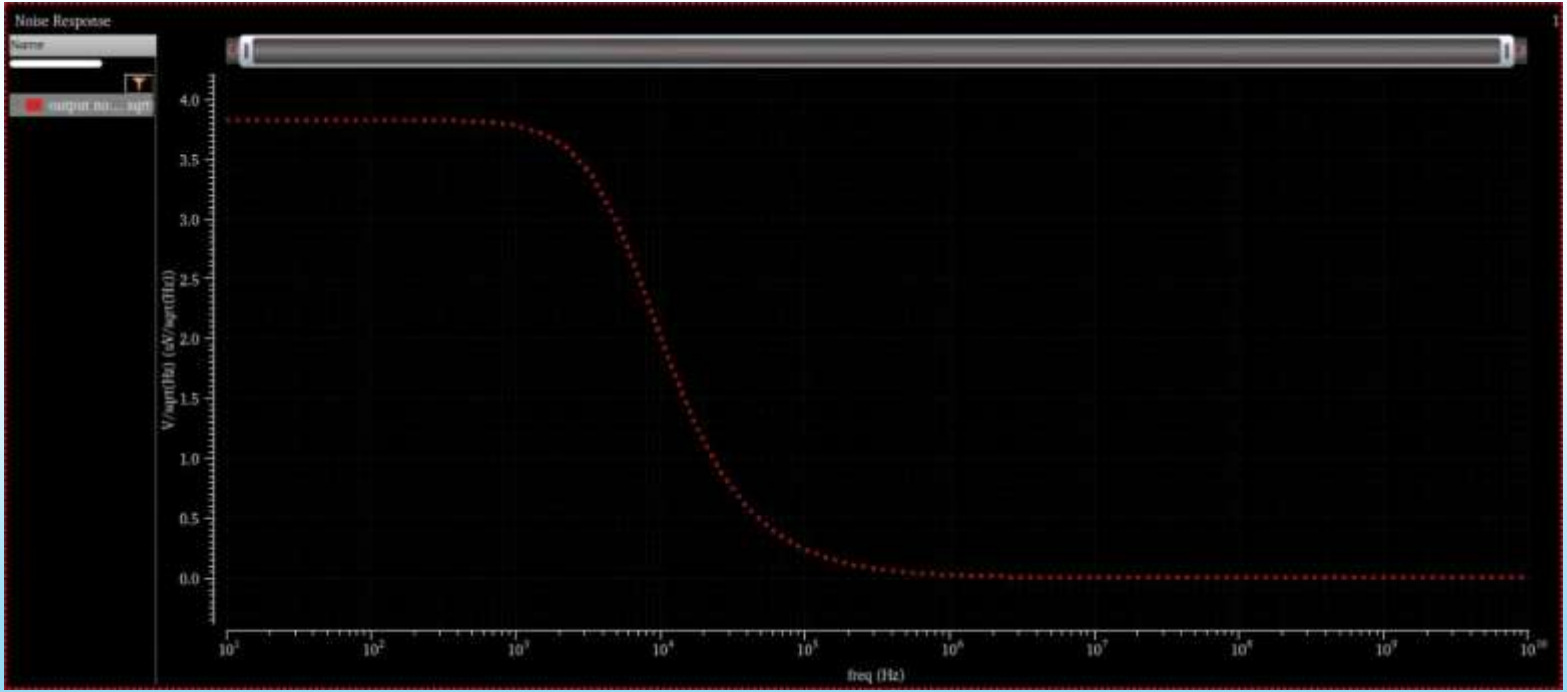

fig no.8 : 8T transmission gate based circuit noise output graph

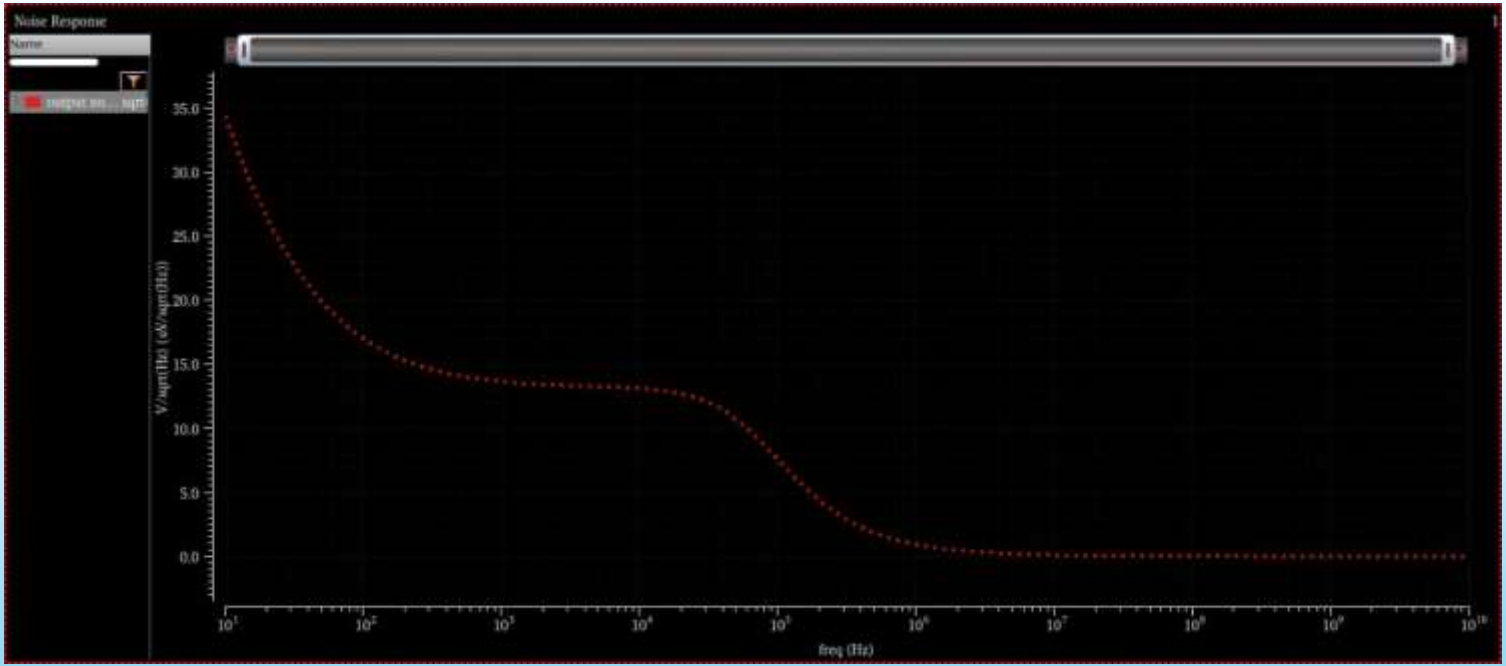

fig no.9: 8T CMOS gate based circuit noise output graph

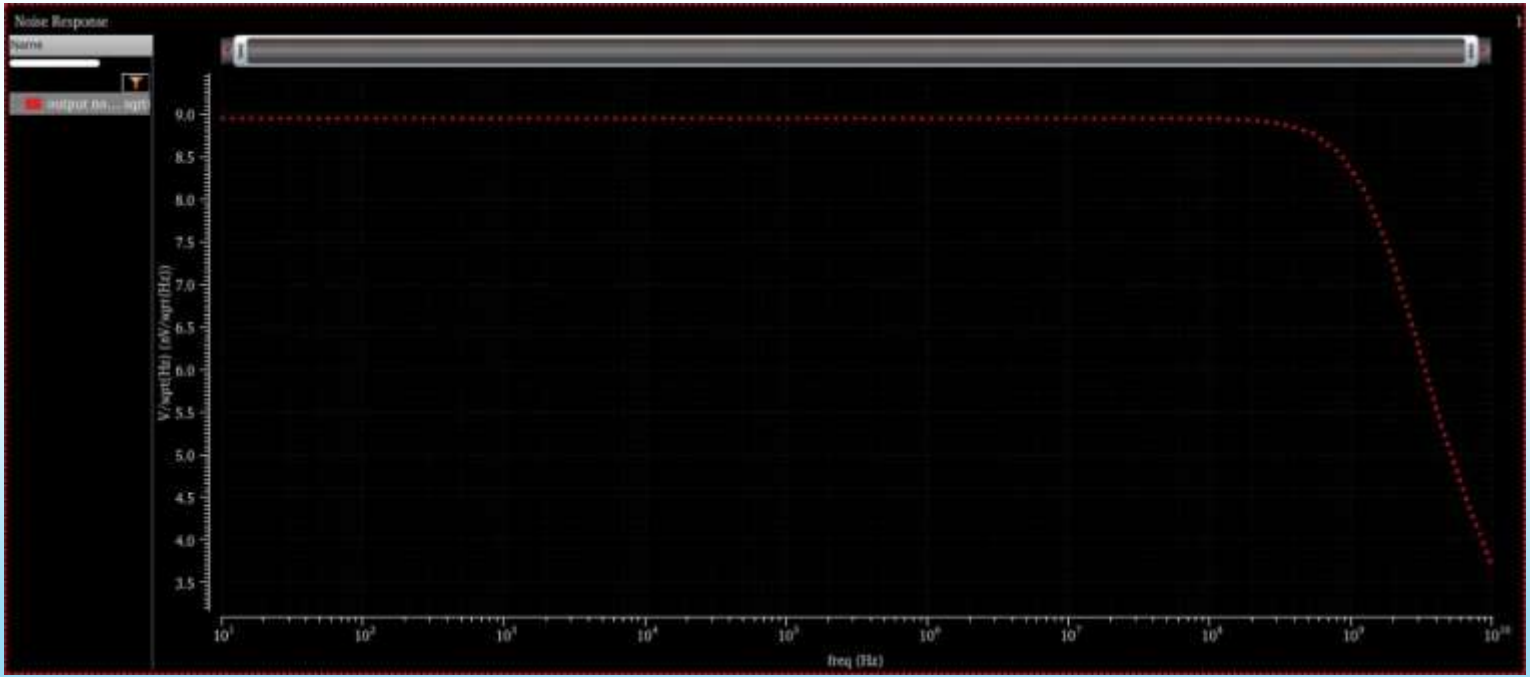

fig no.10 :6T transmission gate based circuit noise output graph

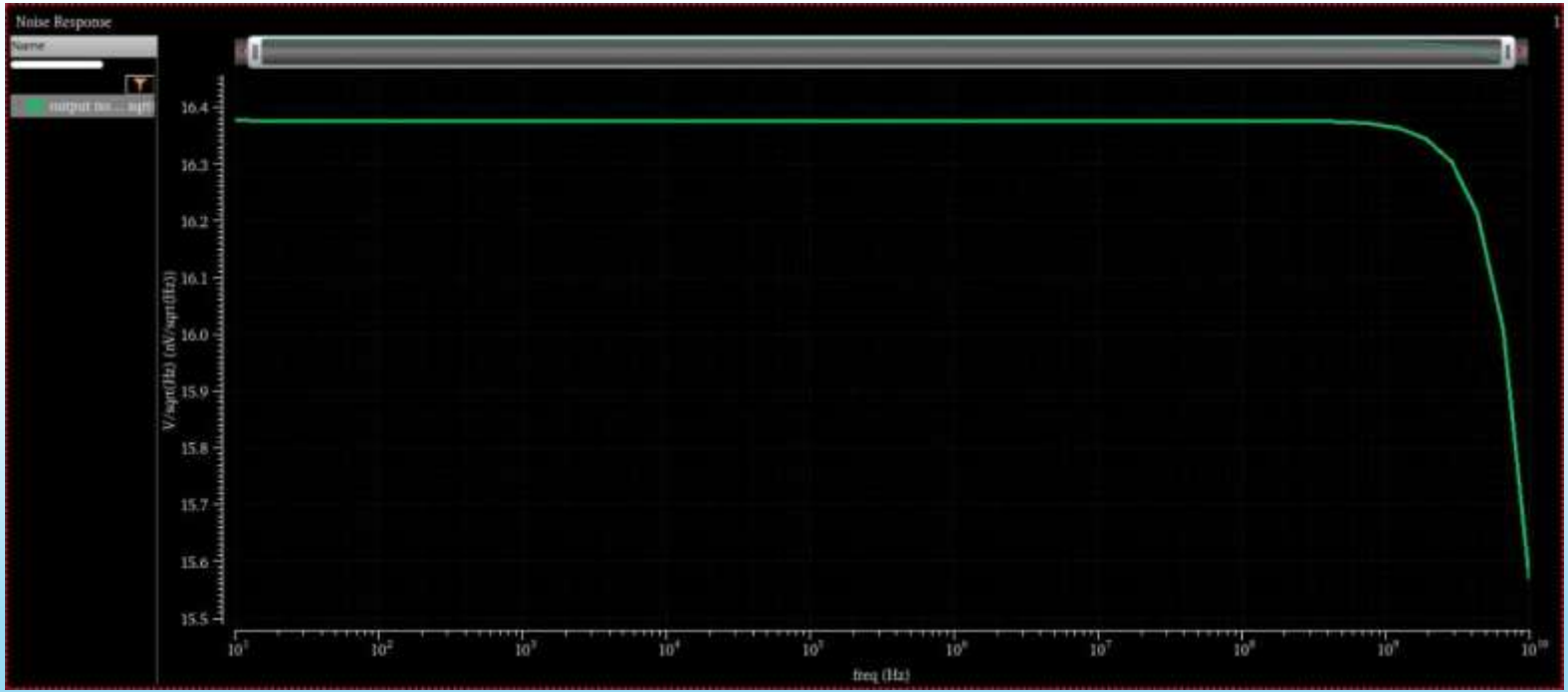

fig no.11 : 6T CMOS gate based circuit noise output graph

COMPARISON RESULT

PARAMETER	8T TRANSMISSION	6T TRANSMISSION	8T CMOS	6T CMOS
NOISE average(getData("/out" ?result "noise"))	4.40E-09	5.62E-09	15.1E-09	16.1E-09
POWER average(getData(":pwr" ?result "tran"))	354.9E-6	134.5E-6	10.95E-9	5.088E-09

From the comparison values obtained from the cadence virtuoso , we concluded that the circuit is efficient in terms of noise parameter .Also other parameters are not changed to a great extend.

CONCLUSION

- Effective SRAM with 8 transmission gate based circuit
- Performance Assessment with Cadence tool
- Less Noise and Data stability
- Thus increasing the efficiency of memory circuit

MAPPING

MAPPING OF COURSE OUTCOMES WITH PROGRAM OUTCOMES

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
C01	X	X									
C02	X	X	X		X	X					
C03										X	
C04								X		X	X
C05								X		X	X

PO1 & PO2

- Area of technology for project development has been identified.
- Significant problems in ECE domains has been recognized.

PO3

- Changes has been incorporated into the existing technology

PO5

- Studied and gained sufficient knowledge in the software used for implementation.

PO6

- Applied the domain knowledge to address societal issues.

PO8

- Has valued the intellectual property rights and avoided the use of other’s work.

PO9

- Accomplished team coordination for the completion of the assigned tasks.
- Achieved effective sharing of technical information and ideas in presentations throughout the project.

PO10

- Appropriate organization of papers has been achieved.

PO11

- Efficient and detailed planning, job division and scheduling the work.
- Accomplished proper budget estimation and planning.

PO12

- Satisfactory presentation of literature review and formulation of problem based on literature gap.

REFERENCES

[1] N. Maroof and B.-S. Kong, “10T SRAM using Half- VDD precharge and row-wise dynamically powered read port for low switching power and ultralow RBL leakage,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 4, pp. 1193–1203, Apr. 2017.

[2] Liang Wen, Xu Cheng, Keji Zhou, Shudong Tian, and Xiaoyang Zeng, “ Bit-Interleaving-Enabled 8T SRAM With Shared Data-Awareand Reference-Based Sense Amplifier”, IEEE Transactions on Circuits and Systems, vol. 63, No. 7, July 2016.

[3] J. P. Kulkarni and K. Roy, “Ultralow-voltage process- variation tolerant Schmitt-trigger-based SRAM design,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 319–332, Feb. 2012.

THANK YOU