CONTROLS...

	R	W	A_1	A_2	A_3	O3	T1	T2	alu-a	alu-b	ALU	PC	t5	M-add	RW RF	C	Z	IR	T4
MR-state	1	0	X	X	XX	XX	X	X	0	1	00	1	11	01	X	0	0	00	0	0	1	X
bring_regd	0	0	1	1	X	X	0	0	0	0	00	0	00	00	X	X	X	10	0	0	0	X
ALU_op_c3	0	0	X	X	XX	XX	X	X	1	0	01	0	10	00	X	X	X	00	1	1	0	X
write_back	0	0	X	X	00	01	X	X	0	0	00	0	00	00	X	X	X	01	0	0	0	X
write_back2	0	0	X	X	01	01	X	X	0	0	00	0	00	00	X	X	X	01	0	0	0	X
bring_imm	0	0	1	X	XX	XX	0	1	0	0	00	0	00	00	X	X	X	10	0	0	0	X
store_mem	0	1	1	X	XX	XX	X	X	0	0	00	0	00	00	X	0	1	00	0	0	0	X
load_frommem	1	0	X	X	10	11	X	X	0	0	00	0	00	00	X	0	1	01	0	0	0	X
ALU_op_z3	0	0	X	X	XX	XX	X	X	1	0	01	0	10	00	X	X	X	00	0	1	0	X
store_PC	0	0	X	X	10	10	X	X	0	1	00	1	01	00	X	X	X	01	0	0	0	X
dec_PC	0	0	X	X	XX	XX	X	X	0	1	00	1	01	01	X	X	X	00	0	0	0	X
PC_offset_6	0	0	X	X	XX	XX	X	X	0	1	01	1	11	01	X	X	X	00	0	0	0	X
PC_offset_9	0	0	X	X	XX	XX	X	X	0	1	10	0	11	01	X	X	X	00	0	0	0	X
t2_PC	0	0	X	X	XX	XX	X	X	0	0	00	0	00	10	X	X	X	00	0	0	0	X
LM_load reg	1	0	X	X	11	11	X	X	0	0	00	0	00	00	1	1	0	01	0	0	0	1
check_z2	0	0	X	X	XX	XX	X	X	0	0	00	0	00	00	0	X	X	00	0	0	0	0
SM_storemem	0	1	0	X	XX	XX	X	X	0	0	00	0	00	00	1	1	0	10	0	0	0	1
priority_out	0	0	X	X	XX	XX	X	X	0	0	00	0	00	00	X	X	X	00	0	0	0	1
data_ext	0	0	X	X	10	00	X	X	0	0	00	0	00	00	X	X	X	01	0	0	0	X
bring_imm2	0	0	X	1	XX	XX	1	1	0	0	00	0	00	00	X	X	X	10	0	0	0	X