ELECENG 2EI4

Design Project 4

Instructor: Dr.Haddara

Suchir Ladda - laddas - 400517569

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by [**Suchir Ladda, laddas, 400517569**]

Circuit Schematic

In order to determine the circuit schematic to use for this project, I had to use a combination of boolean algebra and DeMorgan's theorem to do the following:

$$Y = A \oplus B$$
$$Y = \overline{A}B + A\overline{B}$$
$$Y = \overline{\overline{A}B + A\overline{B}}$$
$$Y = \overline{(A + \overline{B}) \bullet (\overline{A} + B)}$$
$$Y = \overline{AB + \overline{A}\overline{B}}$$

Based on the final equation it is evident that the circuit schematic will have a pull down network (PDN) where A is in series with B and $\overline{A}$ is in series with $\overline{B}$. The PDN will be implemented with 4 N-type MOSFETs as seen in the bottom portion of the diagram in figure 2. We then mirror the PDN and make a pull up network (PUN) using P-type MOSFETs. The 2 parallel networks are then connected to make our CMOS XOR gate. The final schematic will use 4 transistors to implement the PDN and another 4 to make the PUN, in addition to that we need 2 inverters, 1 for $\overline{A}$ and 1 for $\overline{B}$. In total, 12 transistors will be used to create our XOR gate.

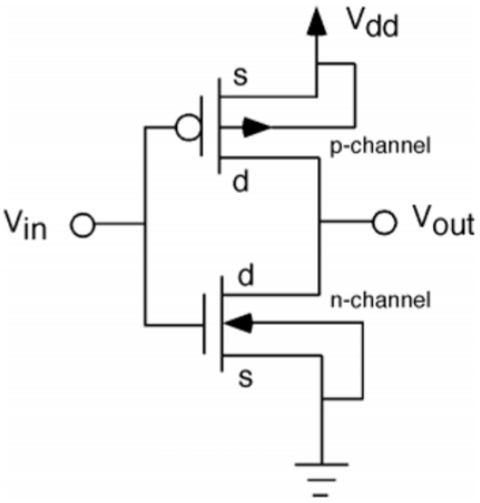


Figure 1: CMOS XOR Inverter

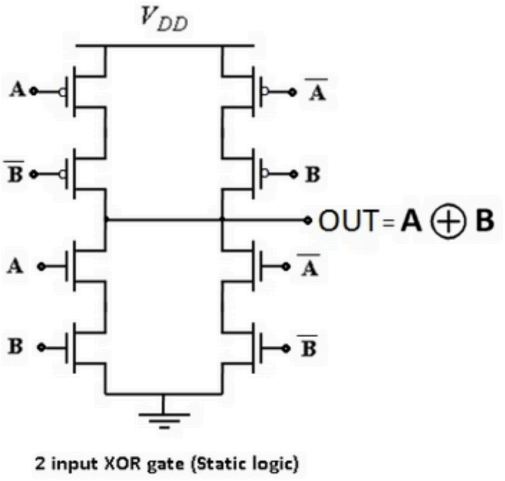


Figure 2: CMOS XOR gate

Ideal Sizing

The ideal sizing for a PMOS is assumed to be $(\frac{W}{L})_P$ = 5/1 and for an NMOS we know that the ideal sizing is $(\frac{W}{L})_N$ = 2/1. Based on the circuit schematic shown above, the longest path

in both the PDN and PUN goes through 2 transistors. This means that R_{eq} is going to be n/2 for the NMOS and p/2 for the PMOS. Before moving forward, it is important to know that the ratio of the PDN and PUN need to be symmetric in order to get the fastest switching time. What this tells us is that the ratio should be 1:1. We also know that the sizing of both the N and P MOSFET should be doubleled because R is inversely proportional to sizing. Using this information it can be stated that the ideal sizing ratio is:

$$\frac{2(Pmos)}{2(Nmos)} = \frac{5}{2} = 2.5$$

Implementation of Ideal Sizing

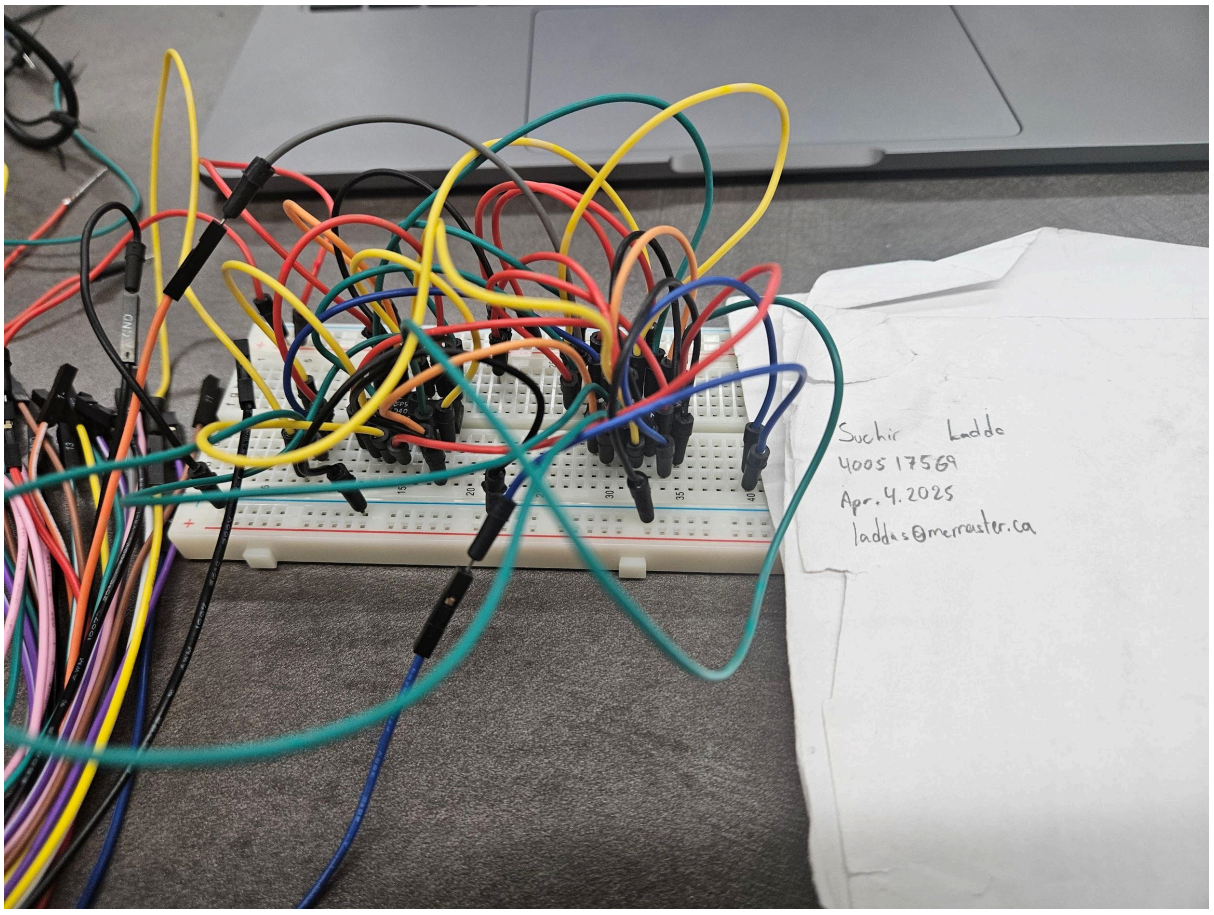


Figure 3: Physical Implementation of Circuit

In the picture above, it can be seen that the longest path in the circuit goes from Vdd all the way to GND. In this path we go past 2 PMOS and 2 NMOS telling us the sizing is $\frac{2(Pmos)}{2(Nmos)} = \frac{5}{2} = 2.50$. This lines up with what we calculated in the earlier section, therefore confirming that it is possible to implement the ideal sizing in our circuit.

Functional Testing

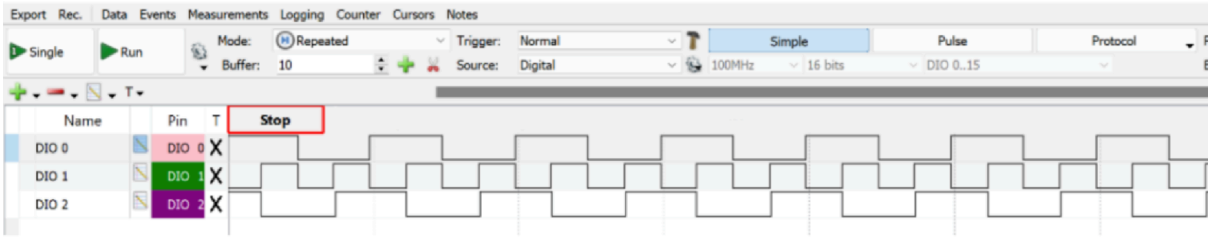
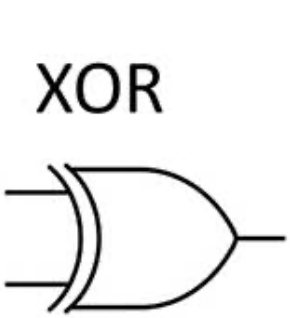


Figure 4: Logic test of CMOS XOR gate (DIO 1 is output)



A	B	Output
0	0	0
1	0	1
0	1	1
1	1	0

Figure 5: Truth table of XOR gate

After using the AD3 digital IO pins, the above waveform was generated. It can be seen that the output DIO1 is only high when either DIO 0 or DIO 2 is active, matching the truth table above.

Static Level Testing

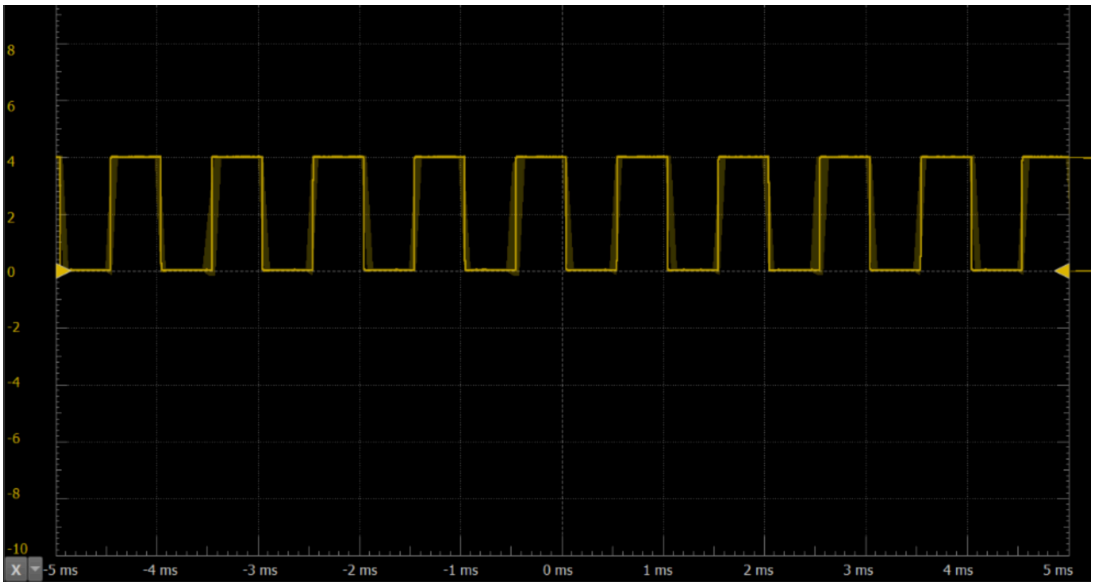


Figure 6: First generated graph

In the initial testing the AD3 measured $V_H = 4.2411\ V$ and $V_L = -8.8435\ mV$

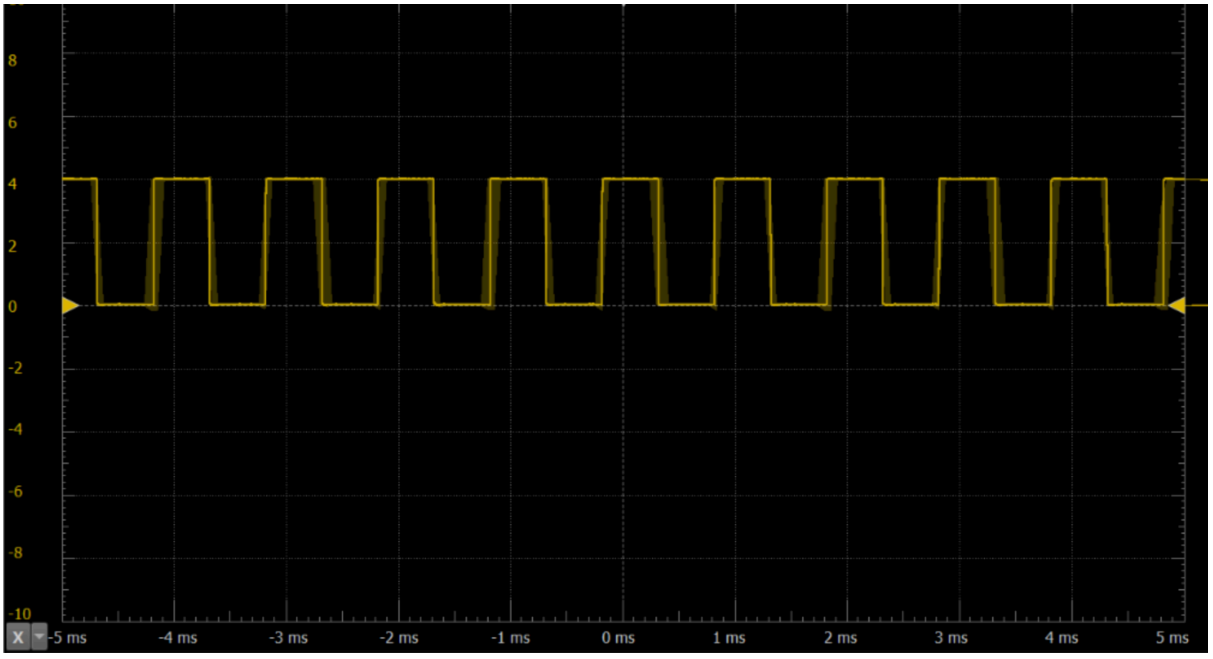


Figure 7: Second generated graph

In the secondary testing the AD3 measured $V_H = 4.2407\ V$ and $V_L = -9.0217\ mV$
The measurements in both measurements were very close, in fact V_H only had a difference of approximately 0.0004 V.

Timing

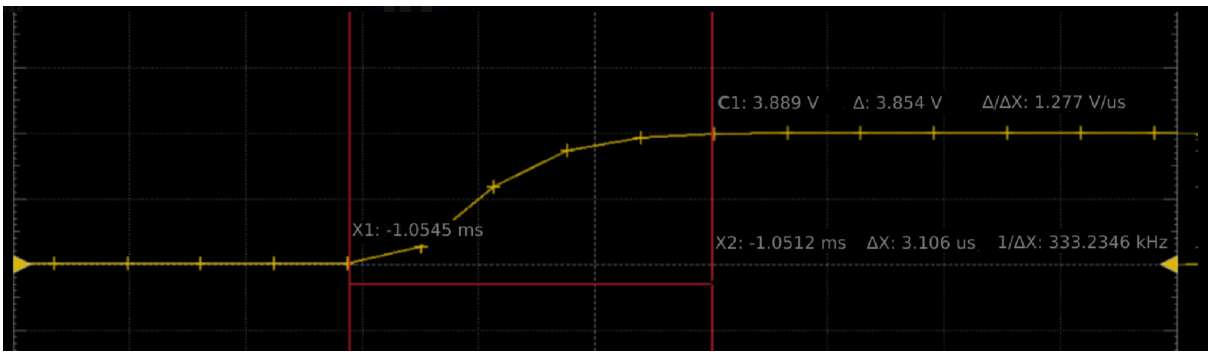


Figure 8: Rise time

Above it can be seen how the rise time was determined using the cursors on the AD3. After taking careful measurements it was determined that the times were:

Rise time = 1.6452 us
Fall time = 1.1876 us

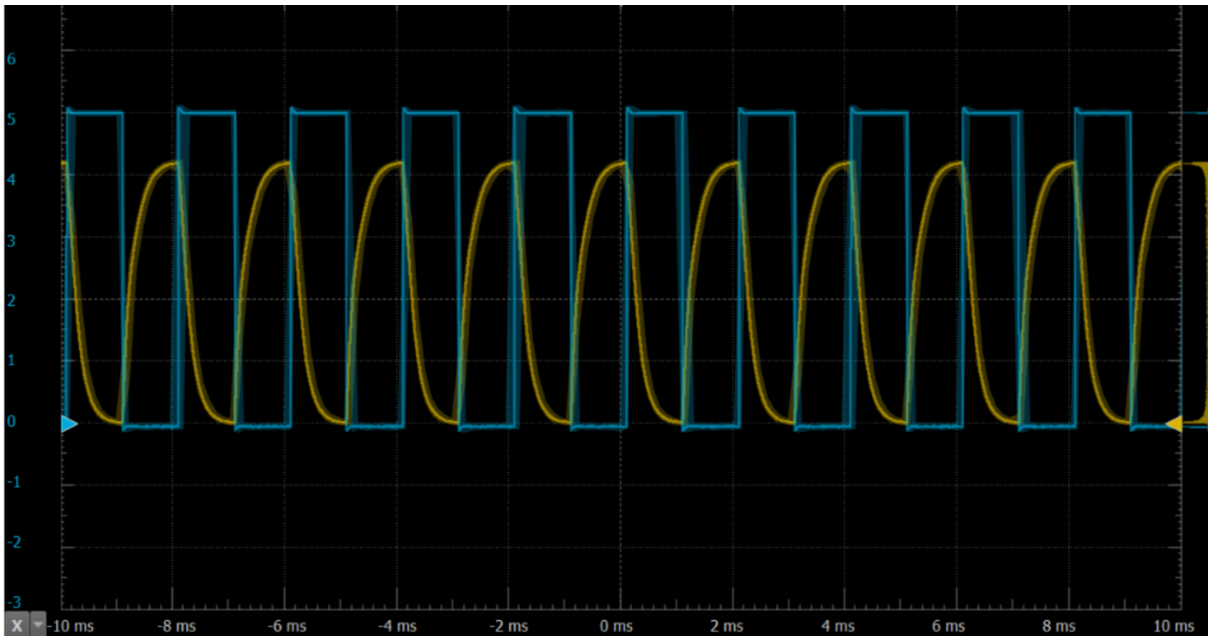


Figure 9: Timing analysis to find parameters

The last portion of this project was to determine τ_{PHL}, τ_{PLH}, and τ_P. In order to find the high-to-low propagation delay, I measured from 50% of the time taken for the input pulse to go low-to-high to 50% of the time it takes for the output to go from high-to-low. After reading the graph values I found that $\tau_{PHL} = 158\,us$. For low-to-high I did the opposite of what was mentioned from before resulting in $\tau_{PLH} = 110\,us$. Lastly, to find the overall propagation delay I used $\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} = \frac{158+110}{2} = 134\,us$