Indian Institute of Technology Tirupati
Department of Electrical Engineering

VLSI Circuits for Signal Processing
(EE5037) Instructor: Dr. Vikramkumar Pudi

Assignment – 4

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EE5037 VLSI Circuits for Signal Processing

Assignment - IV

EE19B043
EE19B047
EE19B049

The Verilog HDL File for Source code is named as **"DX.v"**. Other required files are **"DTX.v"**, **"ROM.v"**, **"Add_Sub_Nbit.v"**, "**Half_Adder.v**", "**Full_Adder.v**", "**OR_2in.v**"

To implement 1x8 x 8x1, we used 1 Adder, Shifter, ROM and called it sequentially for all 8 bits. (**Refer DTX.v, ROM.v**).
Later for 8x8 x 8x1, we called DTX.v module sequentially 8 times(once for each row of D Matrix). (Refer DX.v)
For test bench, go to file named **"Test_Bench_DX.v"**
Here is the Result of Test Bench:
(Look into Transcripts after pressing Run All)

```
X=[   1   13    9   99   13 -115  101   18], Y=[   48    -2    -2   -85    43    85  -119    32]
X=[ -27  119  -19 -116   -7  -58  -59  -86], Y=[  -89   103    30    19   -77  -113   -62    25]
X=[  45  101  -14  -50  -24  -59   92  -67], Y=[    8    69    73    30   -76    20  -113    39]
X=[  13   83 -128   32  -86  -99 -106   19], Y=[  -96    78    77   -40    80   -49   -78  -124]
X=[ -54   60    2  -82   29  -49   35   10], Y=[  -18   -18    30   -23   -51   -72   -64    62]
X=[ -58  -82   65  -40  120 -119  -21  -74], Y=[  -74    19  -107   -34    36   -15   -18   173]
X=[ 126   21   11  113 -123   79   59   58], Y=[  118    20    87    -2     1   129    40  -128]
X=[ -97   92   98   76  -97 -113   -8  -73], Y=[  -43   105   -51  -172   -92    35   -74   -29]
X=[ -62  -56   73  -48  -41   81 -106   12], Y=[  -52   -19   -42   -30   -47   -50   152   -21]
X=[-123  120   18  126  109   57   31  -45], Y=[  103   -11  -172   -27   -56   -63  -111   -57]
```

Final Verdict: Total Area used – 1 Adder, Shifter.
Total Delay : 8 clk cycles for inputting X, 64 clk cycles for final output.