Project (Deadline: 7th June)

For the 3 tasks, use the PDK of a UMC 0.13µm technology:

Task #1:

For an NMOS core high speed HS transistor (N_12_HS_L130E), with Drain and Gate connected to $V_{DD} = 1.2V$ and Source connected to a current source $I_{REF} = 200\mu A$ to GND and Bulk connected to GND. Fix L=L$_{min}$ and sweep W from W=L to W=100L:

- **Sketch** V_{TH} versus W/L
- **Sketch** g_m versus W/L
- **Sketch** r_o versus W/L
- **Sketch** V_{ov} (V_{GS}-V_{TH})
- **Sketch** $g_m.r_o$ versus W/L
- **Repeat** for L=2L$_{min}$, L=4L$_{min}$ and L=8L$_{min}$ (plot the **4** curves for different values of L for each of the required parameters mentioned above in the same figure).
- **Mention** the long channel equation for each of the above simulated parameters. Is the trend of the simulations similar to the equations?

Task #2:

Use the NMOS core high speed HS transistor (N_12_HS_L130E) to design a MOS accurate high swing current mirror (according to the architecture shown) operating at $V_{DD} = 1.2V$ with the following specifications:

- $I_{out} = 2I_{REF} = 20\mu A$, and
- $V_{comp} \leq 300mV$,
- $R_{out} \geq 1M\Omega \ @ \ V_{out} = 500mV$
- You may generate V_b using an ideal voltage source with any value of your choice

The documentation of your design must include the following:

1- DC operating point annotation on the schematic with dimensions

2- Simulation results to verify V_{comp} and R_{out} specifications

3- Measure the value of the systematic offset versus V_{out}
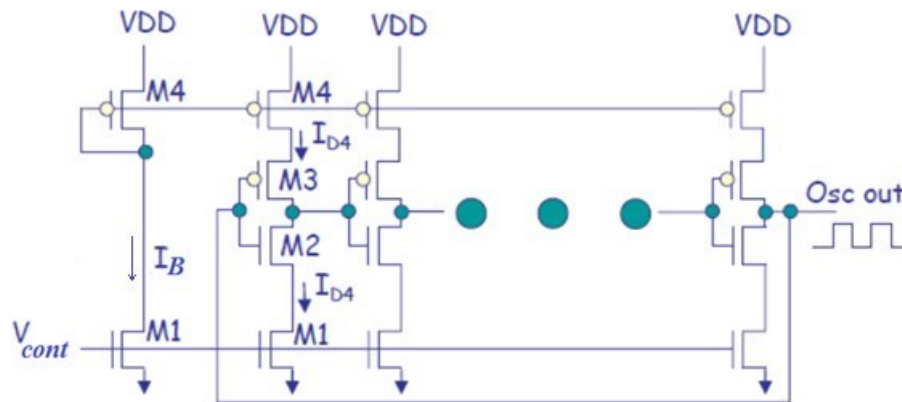
4- Provide your observations and conclusion.

Task #3:

Design the CMOS ring oscillator shown with $V_{DD} = 1.2V$. The unit cell (stage) consists of a CMOS inverter (M_2 and M_3), an NMOS current source (M_1), and a PMOS current source (M_4). This is called a "Voltage Controlled Oscillator (VCO)".

- Explain why this is called a Voltage Controlled Oscillator (VCO).
- Determine the dimensions of all the transistors (Use 1.2V devices N_12_HSL130E or P_12_HSL130E) to generate an output frequency of **20MHz** using **7-stages** with $V_{cont} = V_{DD}/2$.

The documentation of your design must include the following:

1- Schematic diagram showing dimensions of all transistors and bias current (I_B)
2- Simulate the ring oscillator and plot the transient waveforms at all inverter outputs showing the output frequency (you might need to add an initial condition to start the oscillation).
3- Vary V_{cont} from 0 to V_{DD} and record the output frequency versus V_{cont} in steps of 0.1V. Plot the oscillator output for 3 different steps.
4- Repeat (2) after doubling the width (W) and length (L) of the inverters (M_2 & M_3) of all stages.
5- Provide your observations and conclusion.

Assessment:

- The total grade of this project is 15 points.
- Maximum number of students per group is 2.
- You are required to deliver a pdf report that clearly describes your work, including all the required items.
- Report size should not exceed 15 pages.
- Delivery details will be shared with you later.