Cairo University
Faculty of Engineering
Electronics and Electrical Communications Engineering Department

Course Code **ELC2060**

Course Title **Electronic circuits**

Electronics project

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Name	Section	B.N

Task 1:

The characteristics graphs for the N_12_HS_L130E at 200 μA bias current .

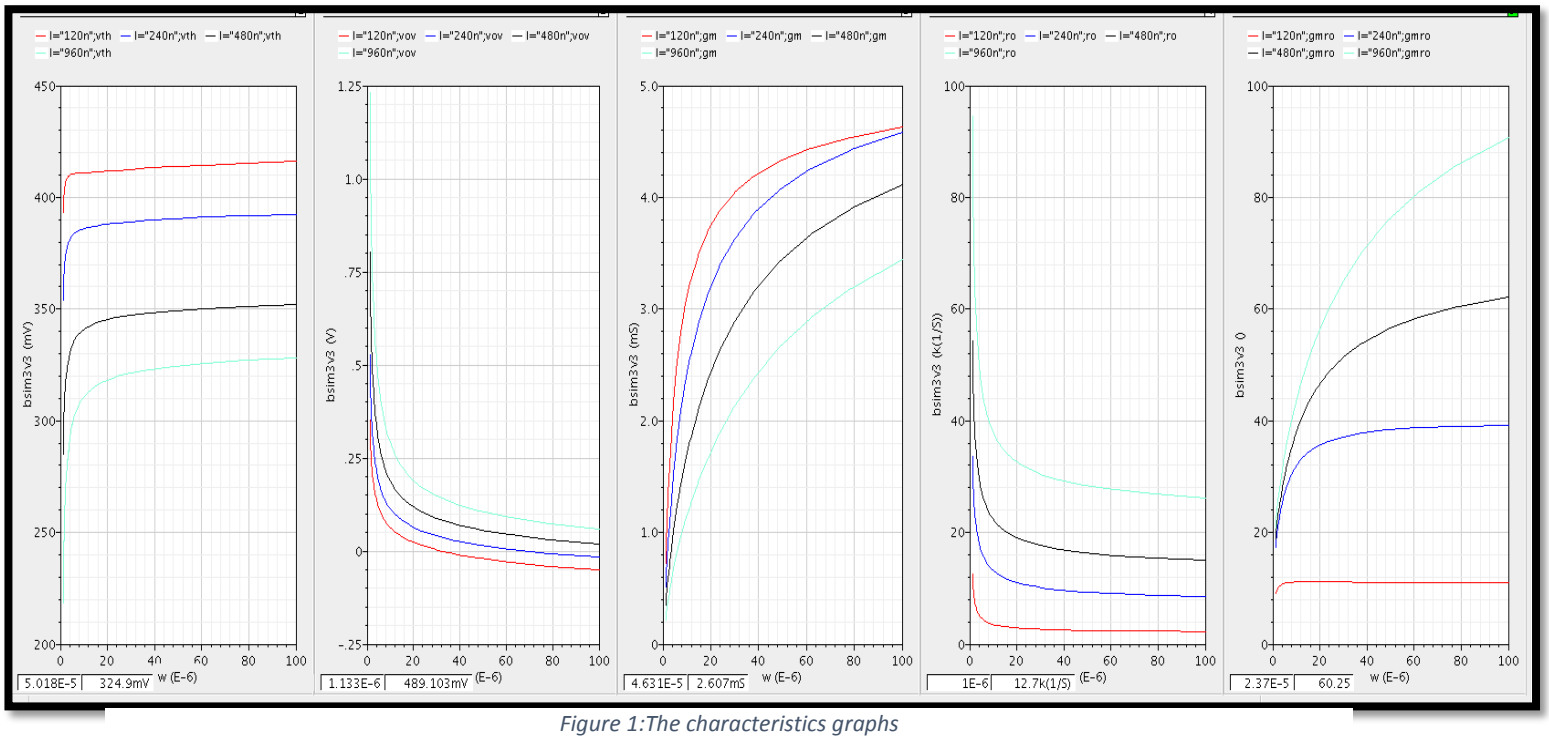


Figure 1:The characteristics graphs

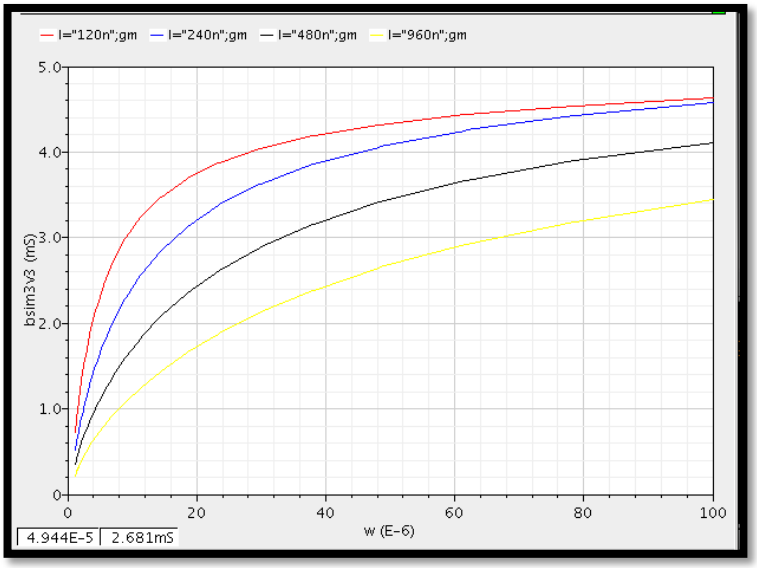
The long channel equation for each of the above simulated parameters:

1. gm

$$gm = \sqrt{2kI_d} = \sqrt{\frac{2\mu c_{ox} W}{l}\, I_d}$$

$$gm \propto \sqrt{w}$$

Which is similar to the obtained results in the simulation.

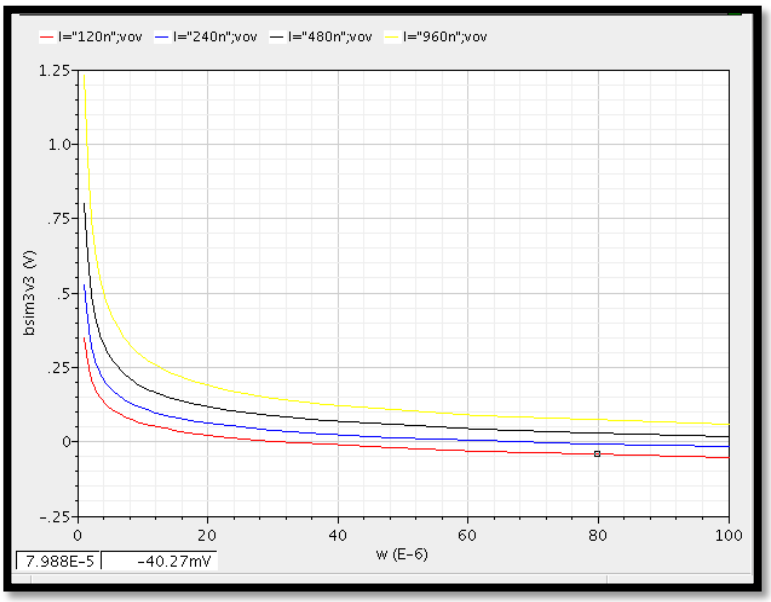


2. V_{ov}

$$V_{ov} = \sqrt{2I_d \frac{l}{\mu_n C_{ox} W}}$$

$$V_{ov} \propto \sqrt{\frac{1}{w}}$$

Which is similar to the obtained results in the simulation.

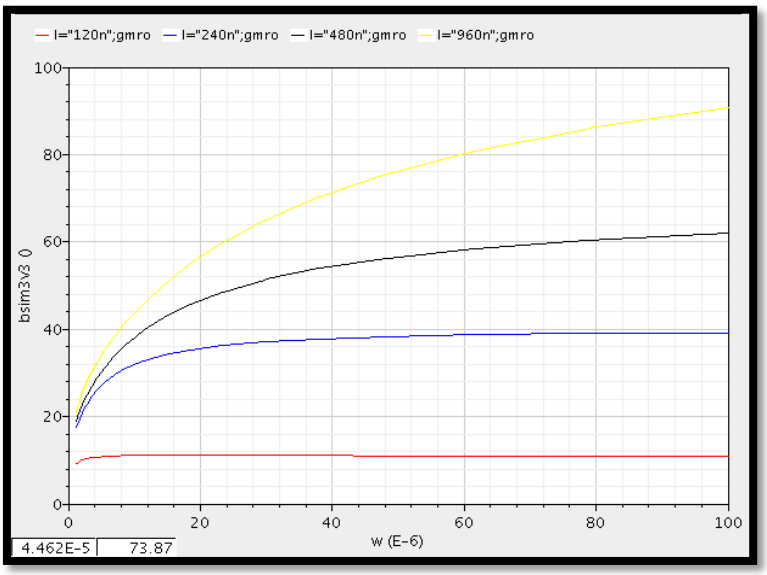


3. $gm\ \ r_o$

$$gm\, r_o = \frac{1}{\lambda}\sqrt{\frac{2kw}{l\, I_d}}$$

$$gm\, r_o \propto \frac{1}{\lambda}\sqrt{w}$$

Which is similar to the obtained results in the simulation.

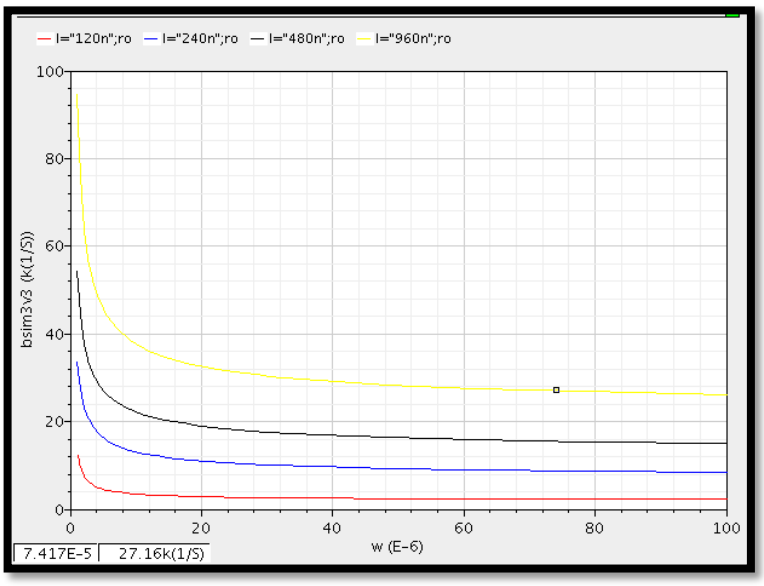


4. r_o

$$r_o = \frac{1}{\lambda I_d}$$

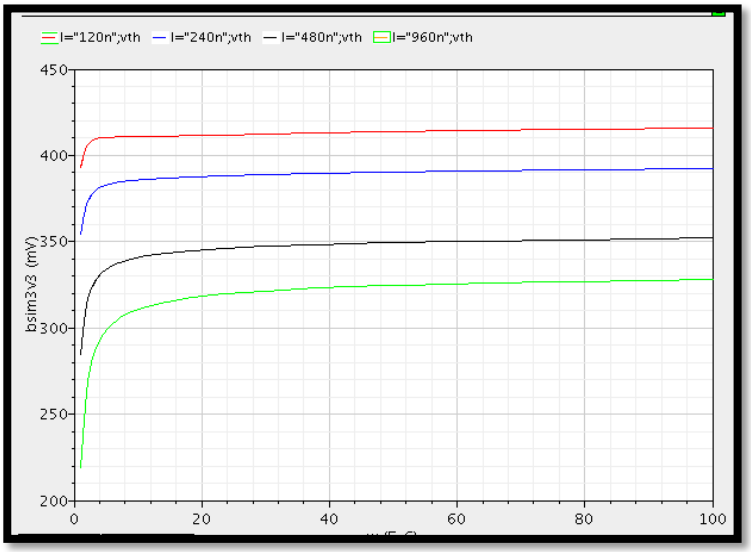
$$thus : r_o \propto \frac{1}{w}$$

Which is similar to the obtained results of the simulation.



5. v_{th}

as seen from the results that V_{th} almost constant(slitly increase) with the width of the transistor and it decreases with the increase of the process technology and it increases with temprature



Task 2:

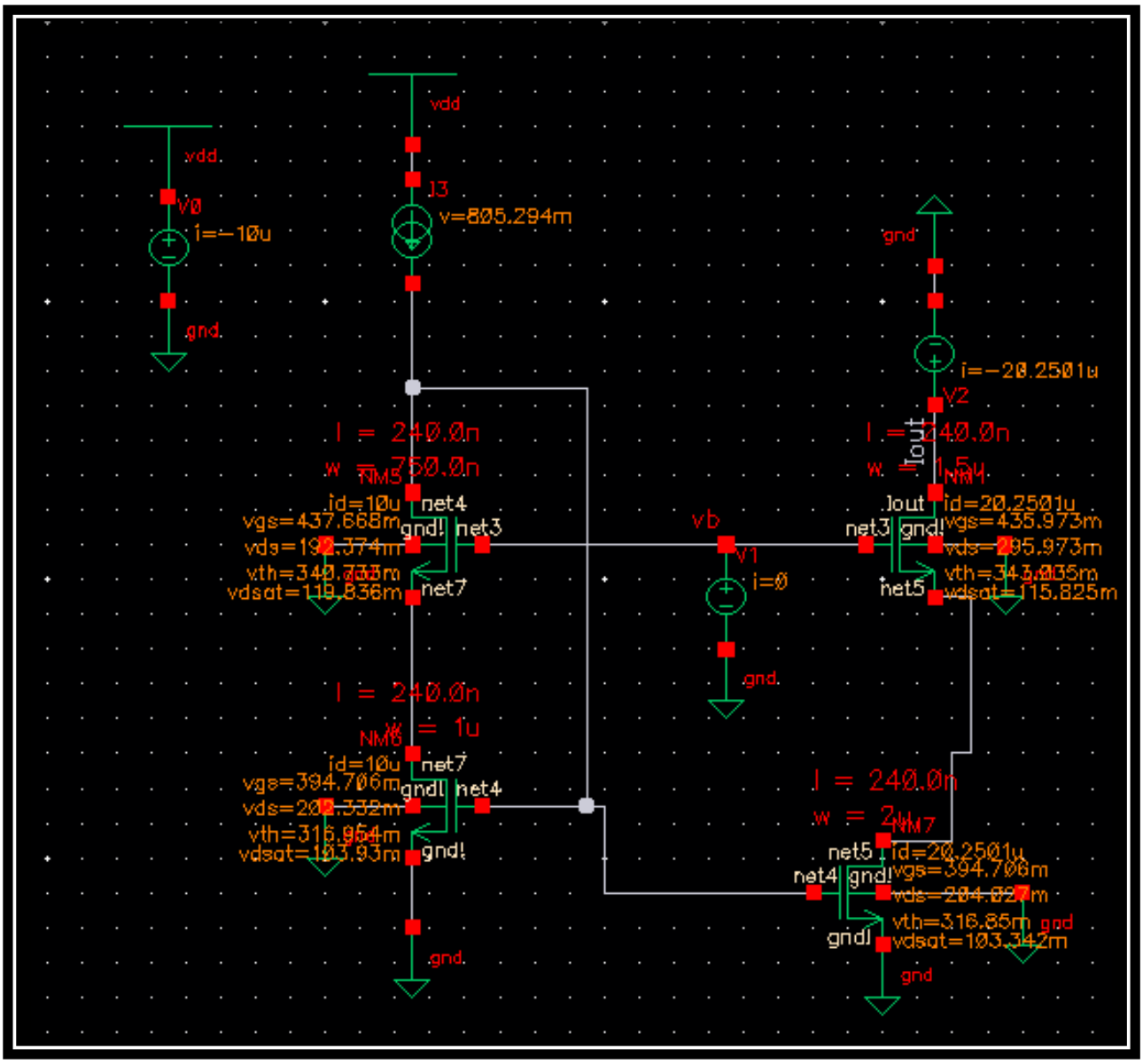


Figure 2:DC operating point annotation with dimensions

R_{out}

Using AC analysis we obtained the value Of the output resistance from frequency 1:2 Hz which is considered DC and with AC magnitude = 1 v

$Rout = 2.55\ M\Omega$

Which is much more the the required value in the design specifications.

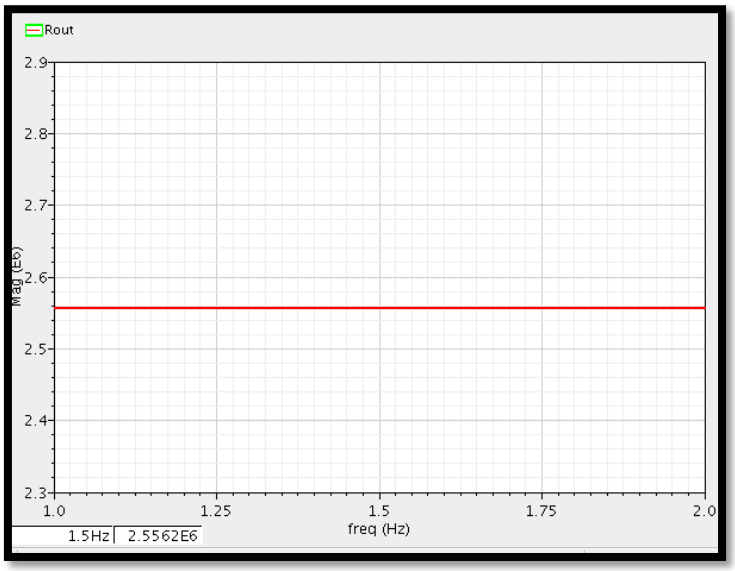


Figure 3:output resistance.

V_{comp}

From the operating point the value of $V_{comp} = 640 - 343 = 297\ V$ which is valid by the design specifications.

Systematic offset

$$Systematic\ offset = \frac{|I_{out} - I_{ref}|}{I_{ref}}\ x\ 100\%$$

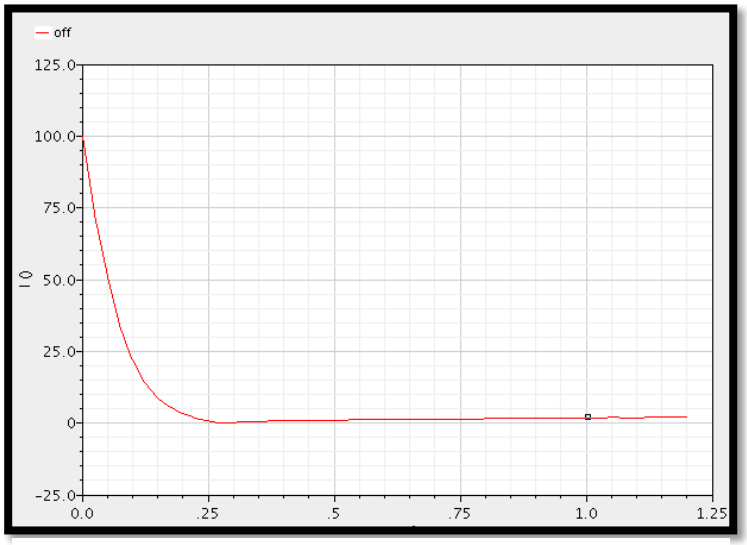


Figure 4:Iout with Vout from 0 to 1.2

Observations and conclusions:

In this design we found it hard to work with $L_{\min}$ as the values for r_o was so small and the value for the V_{th} was large that we couldn't accomplish the design specifications so we used a process technology of $2L_{\min}$.

For the mirroring ratio to be 1:2 , we used the widths of the transistors of the reference part of the current mirror half the width of the widths of the output part.

And after choosing the values of w_3, w_2 from the characteristics graphs obtained in the first task, we observed that changing the value of W_2 changes the value of V_{comp} as it changes the value of V_{ds} and also changes the accuracy of the mirroring ratio.The value of the output resistance changes with the value of W_3.

The systematic offset of the current mirror increases dramatically with decreasing the V_{out} of it, and at approximately $0.2\ v$, it starts to saturate approaching 0, and although the systematic offset is very low below the achieved V_{comp}, the output resistance still very low compared with it's values close to V_{comp}.

The results obtained from the hand analysis were not accurate and the results in the simulation were slightly different from the hand analysis as the equations we use is derived from a simplified model of the transistor, so simulating the values we obtained from the hand analysis we changed the values of the parameters of the transistor to achieve design requirements .

Task 3:VCO

The voltage controlled oscillator is an oscillator which its output frequency is controlled with the input voltage V_{cont}.

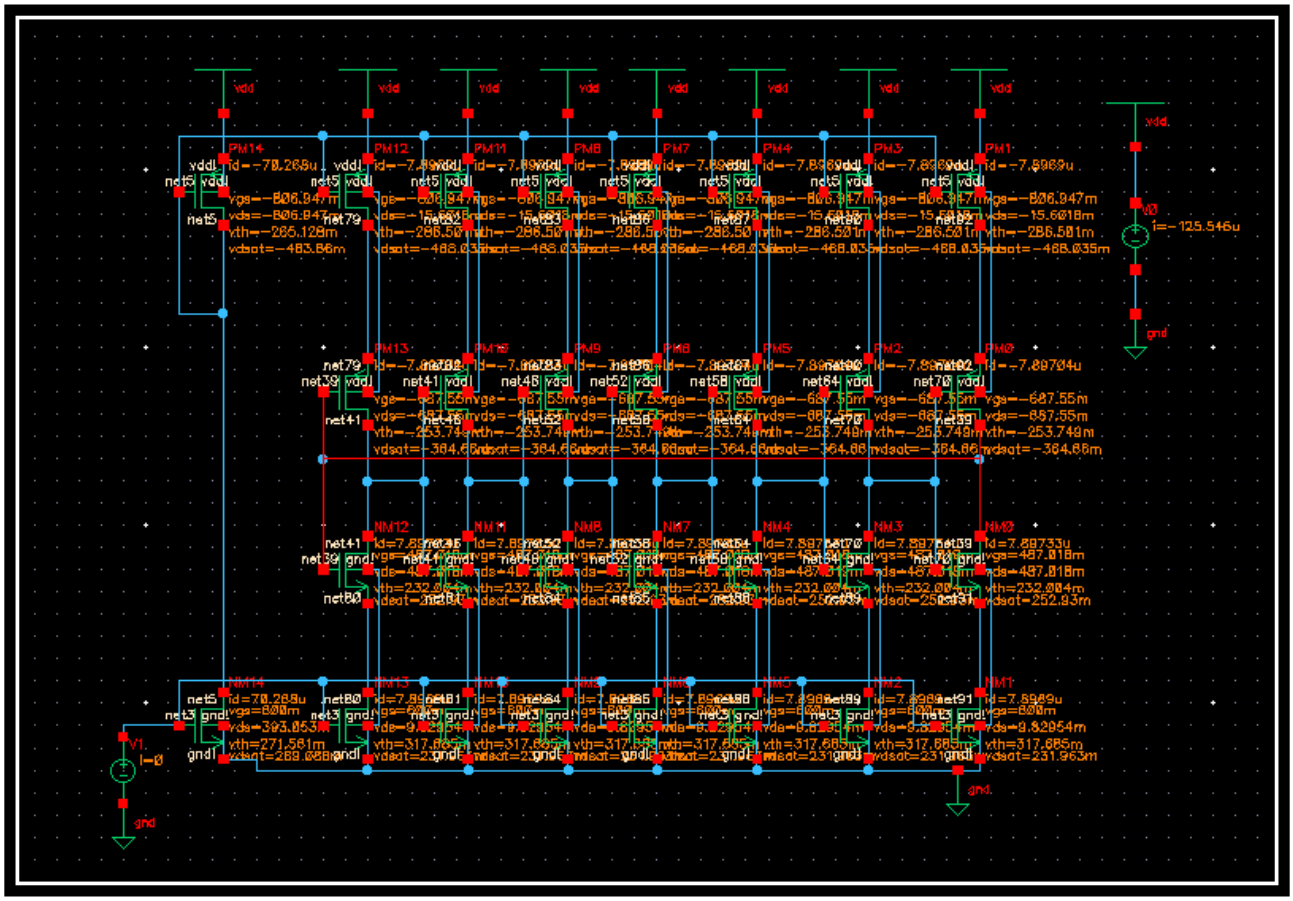


Figure 5:schematic with bias current

To ease modifying the dimensions of the transistors we put theme as variables and the values we used to obtain the required frequency as shown .

The bias current $I_B = 70.268u$.

For the oscillations to start we needed to seed an initial condition for the output of the last inverter $Vout = 1.2V$.

Design Variables

	Name	Value
1	LCMOS	2.76u
2	Lmirror	480n
3	Wnmirror	1.5u
4	WNCMOS	Wnmirror
5	WNS	Wnmirror
6	LS	0.5*Lmirror
7	Wpmirror	2*Wnmirror
8	WPCMOS	2*WNCMOS
9	WPS	2*WNS

Figure 6:transistor parameters used in the simulation.

The output frequency

1. the output of the last inverter with frequency $f_{osc} = 20.0251\ Mhz$.
   The error = 0.126%.

Waveforms of all inverter outputs:

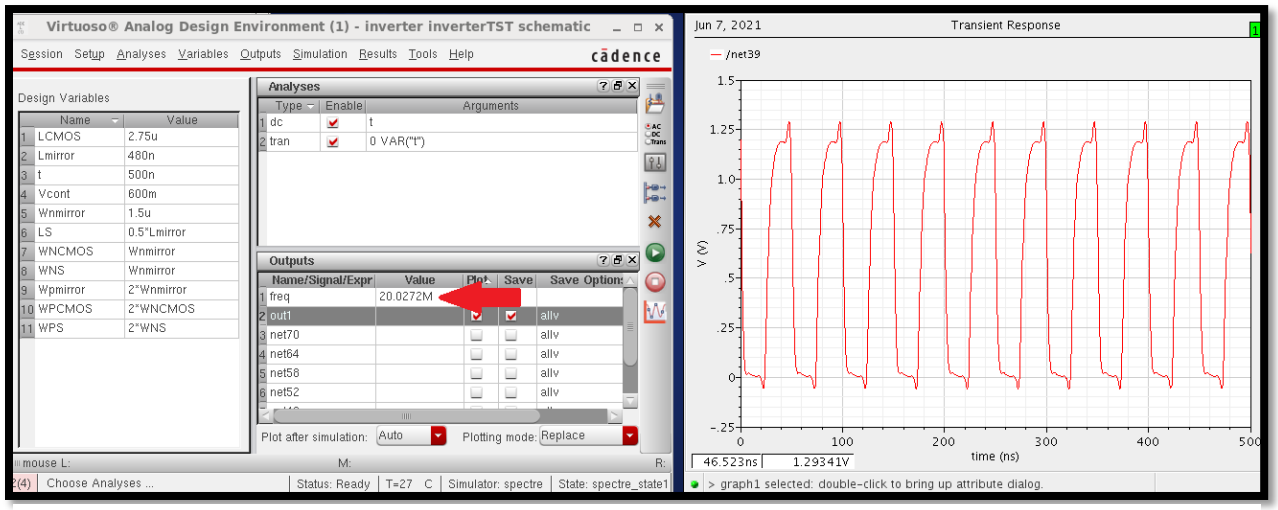


Figure 7:out of first inverter

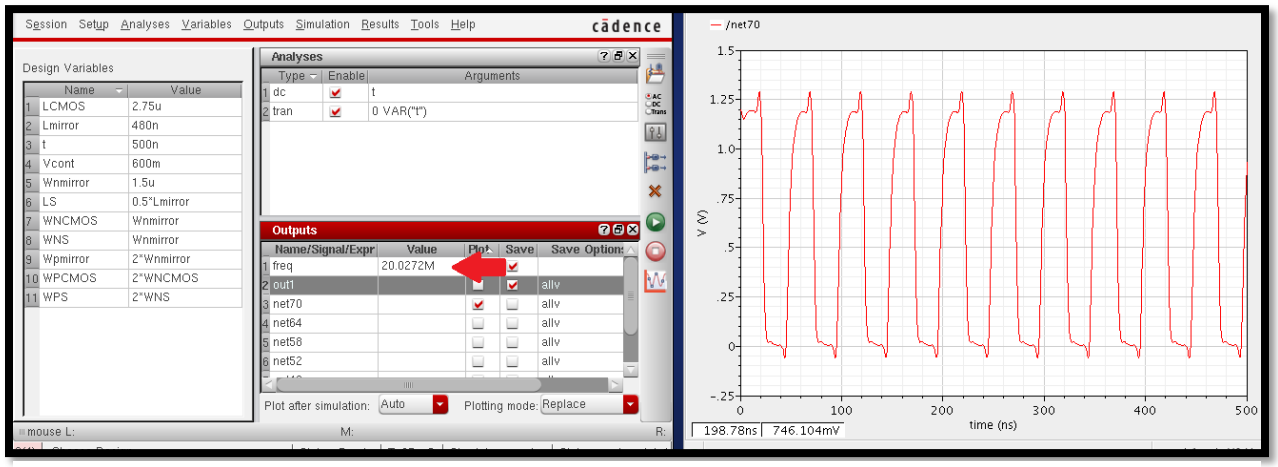


Figure 8:output of second inverter

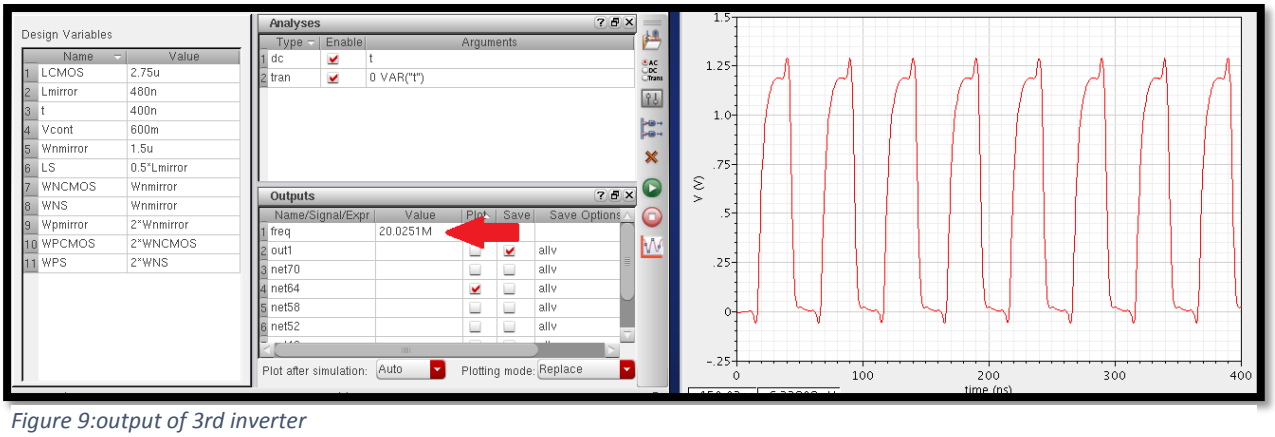


Figure 9:output of 3rd inverter

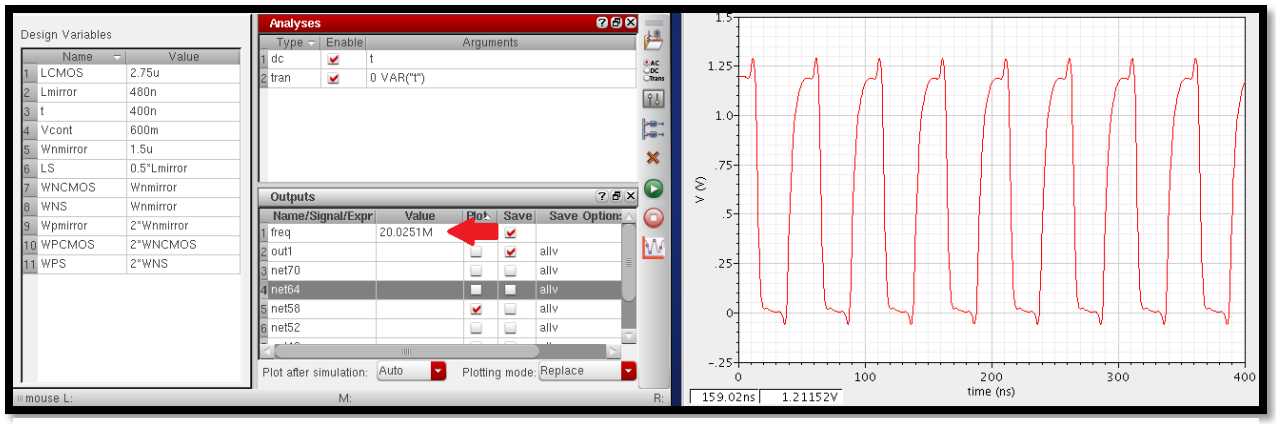


Figure 10:output of 4th inverter

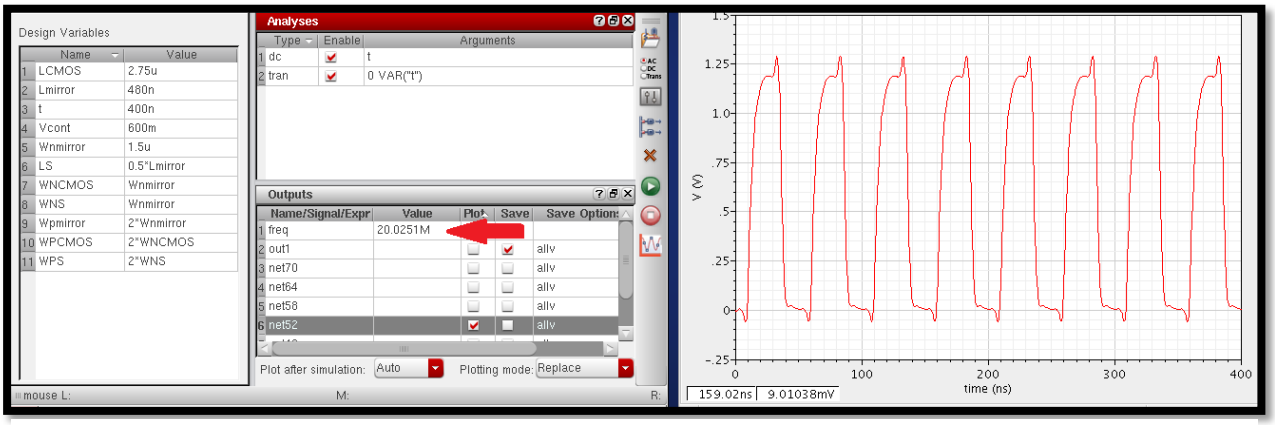


Figure 11:output of 5th inverter

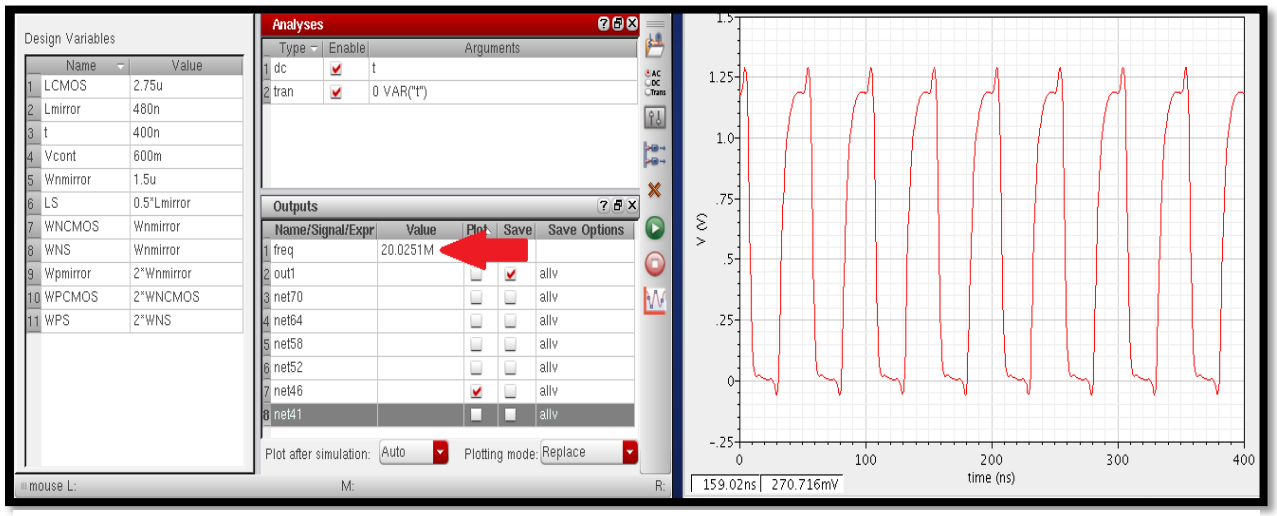


Figure 12:output of inveter no. 6

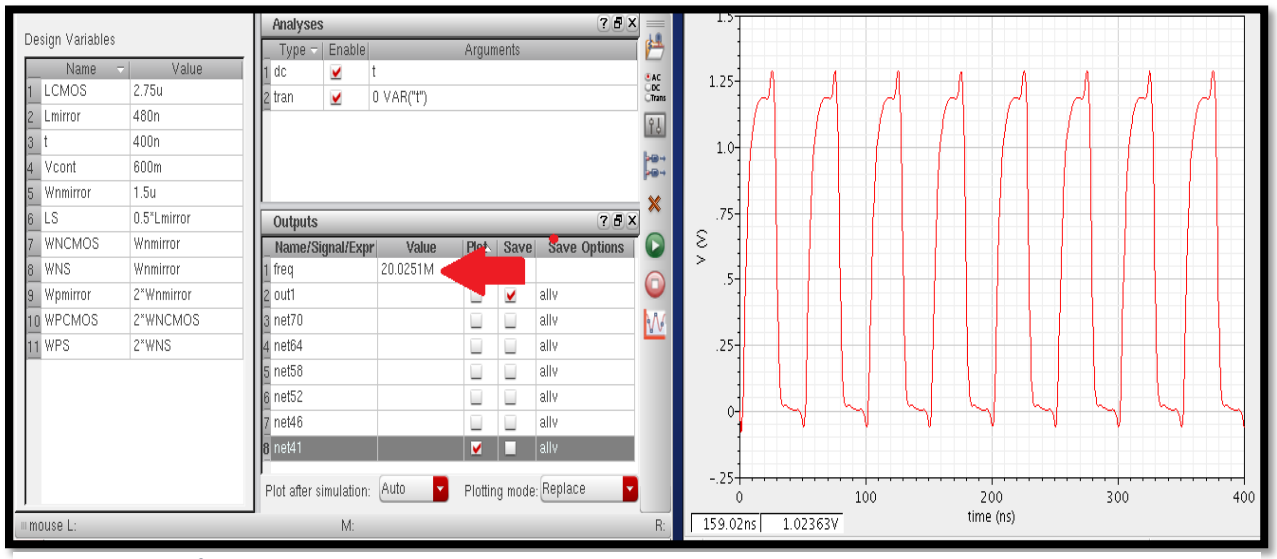


Figure 13:output of inverter no. 7

Varying $Vcont$ with frequency:

as seen from the schematic the frequency increases with the increase in Vcont.
to plot the frequency we used the parametric analysis to swap Vcont for output expression:
frequency(v("/net39" ?result "tran-tran"))

V_{cont}	$Frequency$
0	796.6
1.00E-01	1.45E+04
2.00E-01	2.66E+05
3.00E-01	2.98E+06
4.00E-01	1.28E+07
5.00E-01	1.88E+07
6.00E-01	2.00E+07
7.00E-01	2.06E+07
8.00E-01	2.08E+07
9.00E-01	2.10E+07
1.00E+00	2.11E+07
1.10E+00	2.12E+07
1.20E+00	2.12E+07

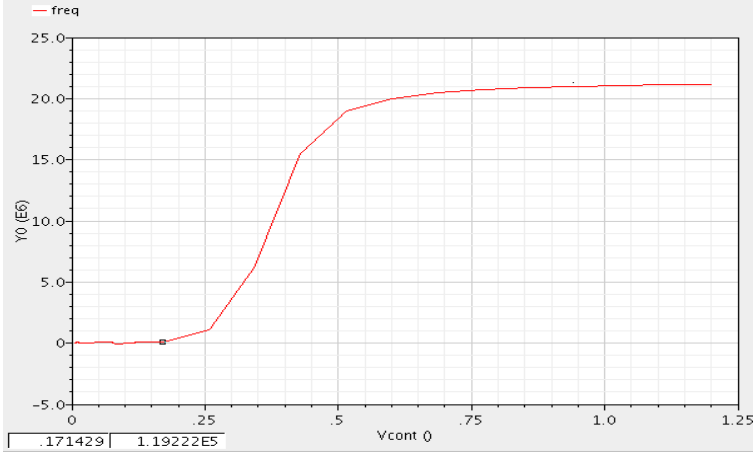


Figure 14:frequency of the ouput oscillations with the change in V_{cont}

Out for three steps:

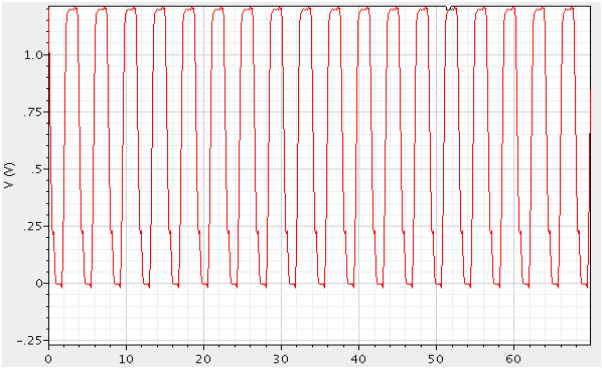


Figure 6:Vcont = 0.2v

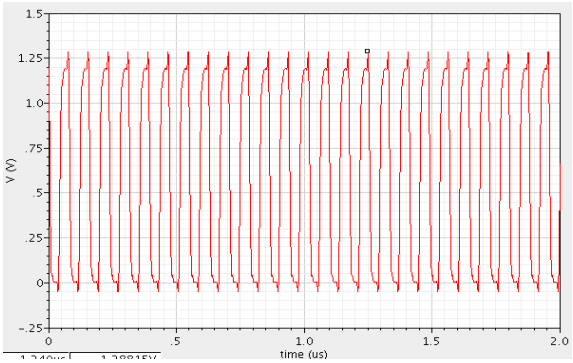


Figure 7:Vcont = 0.4v

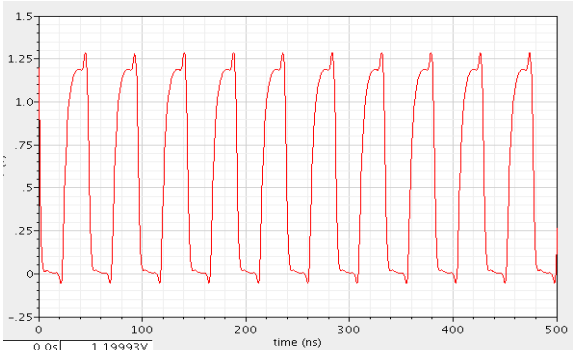


Figure 8:Vcont = 0.9v

Conclusion and observations:

1. For increasing V_{cont} of the oscillator, the frequency of the output signal increases. It's shown from the results that the rate of increase of the frequency is low and after approximately $V_{cont} = 0.25v$, the rate of increase increases dramatically, and it decreases again before reaching $V_{cont} = \frac{V_{dd}}{2} = 0.6v$, and almost constant as closing to $20Mhz$.

2. For the length of the transistors of the reference side of the current mirror, decreasing the length results in increasing the reference current I_B significantly, which means consuming more power from the source of the circuit, and it doesn't affect the frequency of the output signal of the oscillator.

3. For the width of the reference side of the current mirror: decreasing the width results in decreasing the reference current significantly, and have a small effect of the output frequency of the oscillator.

4. After changing each parameter and keeping others constant (L, W) of each transistor, we observed that the length of the CMOS inverter transistors has the greatest effect on the frequency of the output.