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BATCH : DI – 44

COURSE : VLSI DESIGN INTERNSHIP

PROJECT : AHB2APB BRIDGE

FACULTY : Sathya Priya Mam

ABOUT AMBA BUS ARCHITECTURE :

- AMBA stands for **Advanced Microcontroller Bus Architecture** . It is developed by ARM as an interface for their microprocessors . It is available in three standards – APB , AHB, AXI , ASB.
- The AMBA specification defines an on-chip communications standard for designing high – performance embedded microcontrollers .
- AHB stands for **Advanced High – Performance Bus**.
- ASB stands for **Advanced System Bus**.
- APB stands for **Advanced Peripheral Bus** .

ABOUT AHB BUS :

- It is for high – performance ,high clock frequency system modules .
- It acts as high – performance system **backbone bus** .
- It supports efficient connection of processors , on -chip memories and off – chip external memory interfaces with low- power peripheral .
- The ASB is an alternative to the AHB where some high-performance features are not needed.

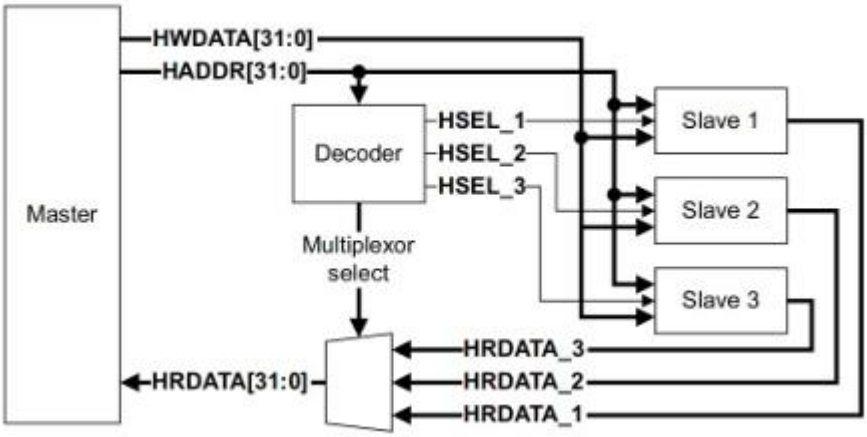
ABOUT APB BUS :

- It is for **low – power peripherals** .
- It is optimised for minimal power consumption and reduced interface complexity to support peripheral functions .
- It consists of a single bus master called the **APB bridge**, which acts as a slave on the AHB/ASB.
- Thus, the bridge is the interface between the high-performance bus(AHB) and the low-frequency peripherals(APB) .

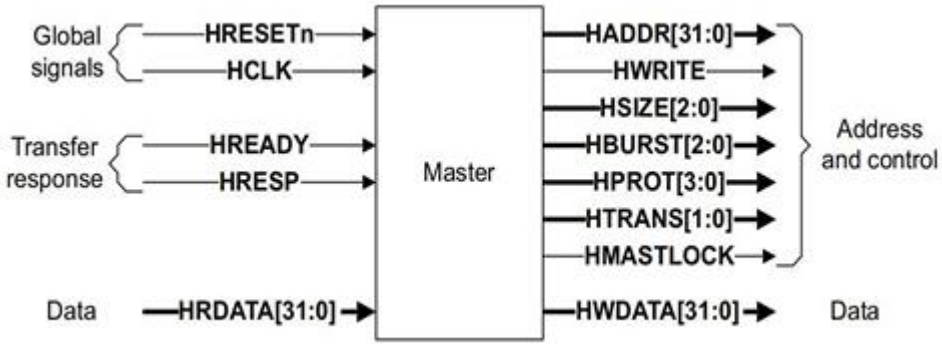
BLOCK DIAGRAM AND ARCHITECTURE

- Block Diagram

1.**AHB Master**

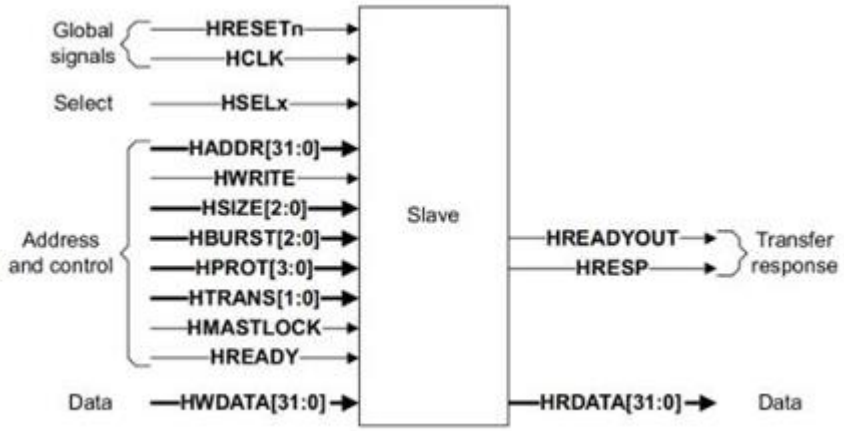


AHB Block Diagram

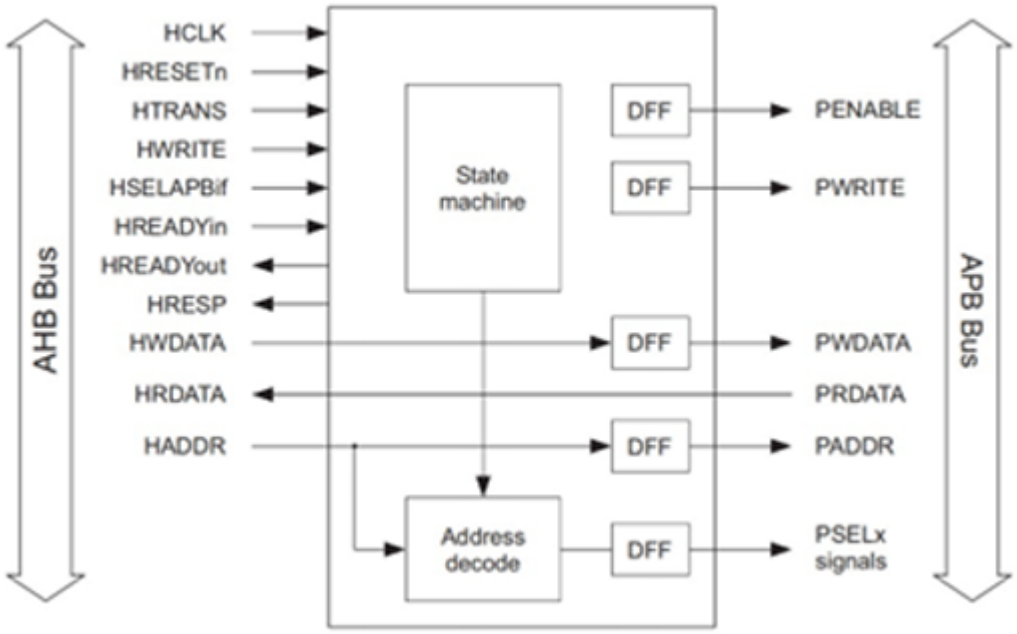


AHB Master Interface

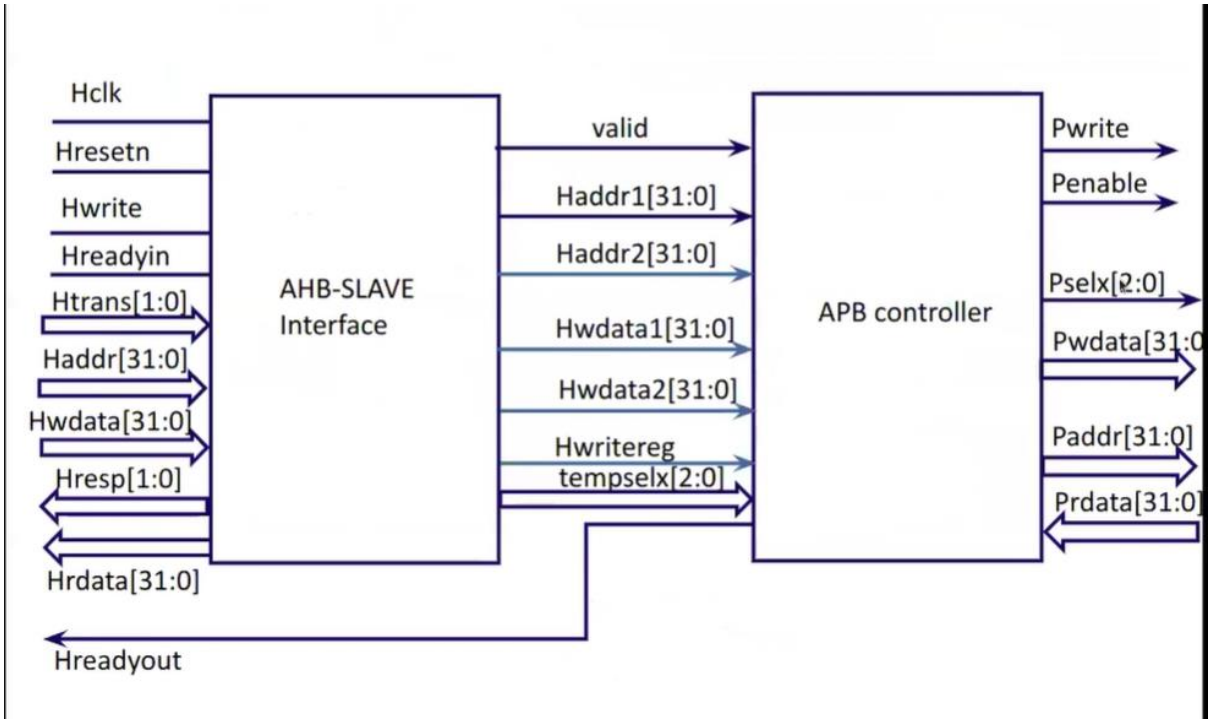
2.**AHB Slave Interface**



3.**AHB 2 APB Bridge Block Diagram**



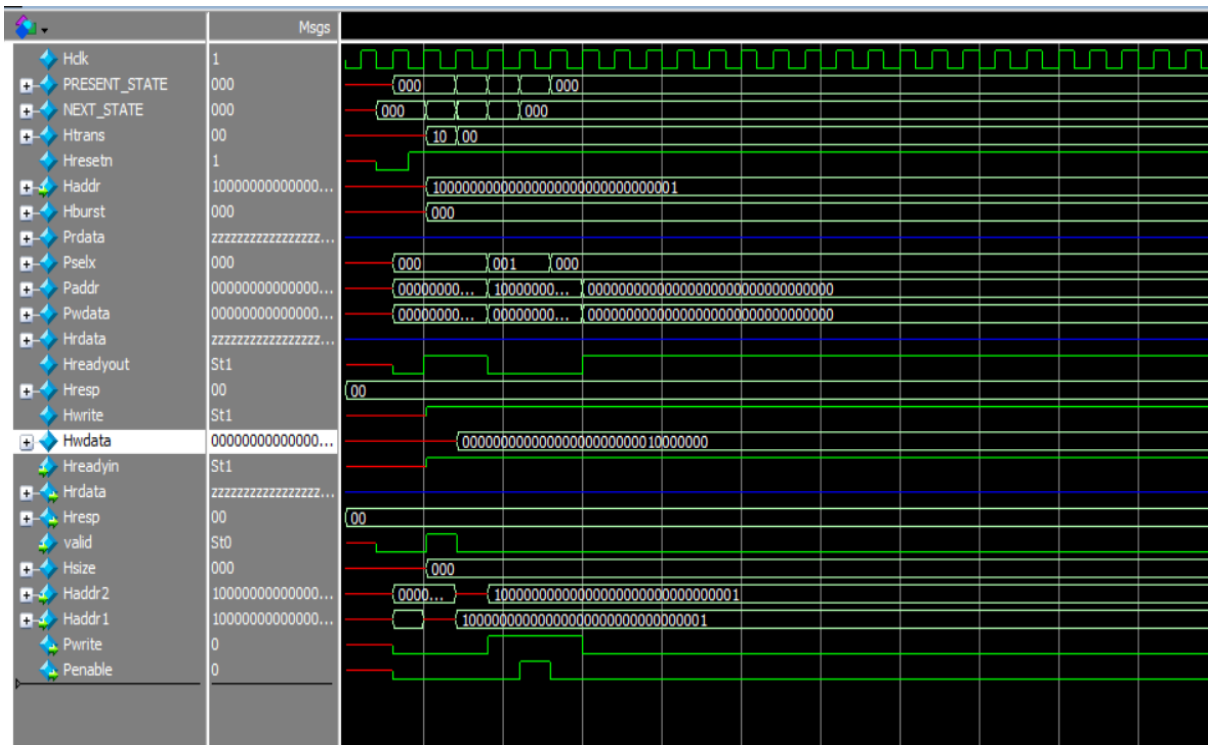
4.**Bridge Module**



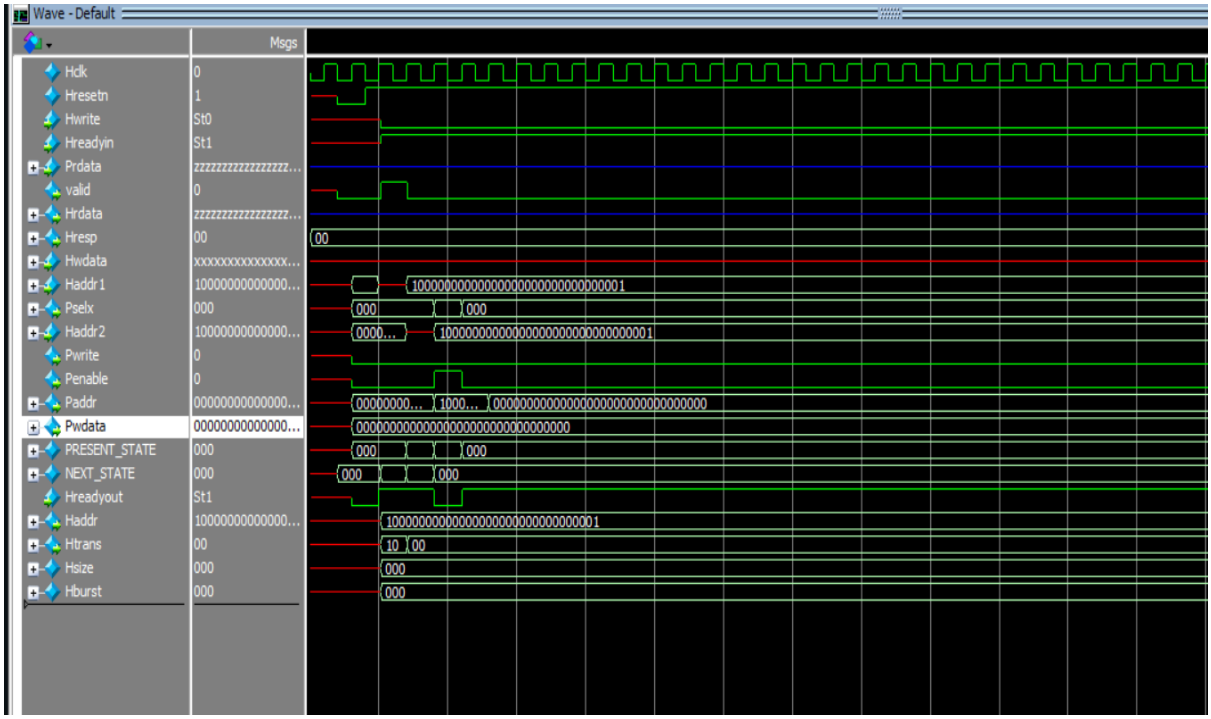
- The above figure shows the connection between **AHB slave interface and APB controller within the bridge .**

SIMULATION RESULTS OF ALL TRANSFERS :

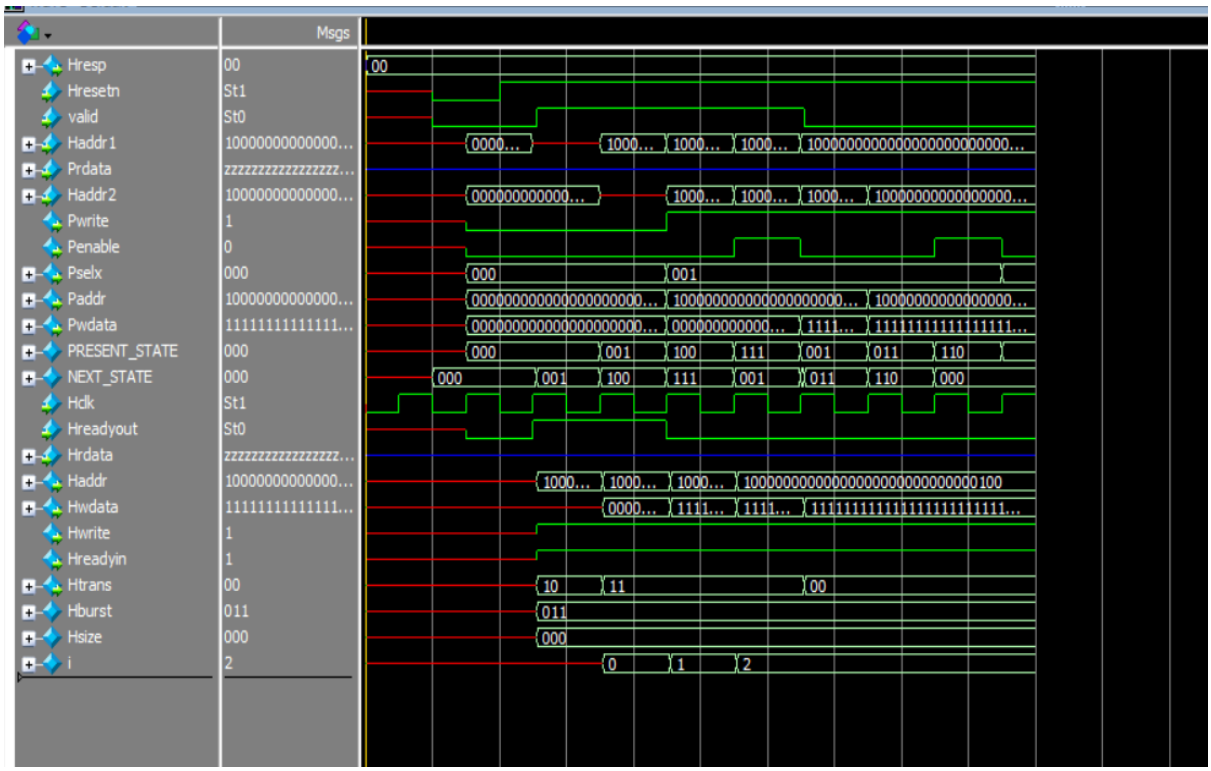
1.SINGLE_WRITE_TRANSFER



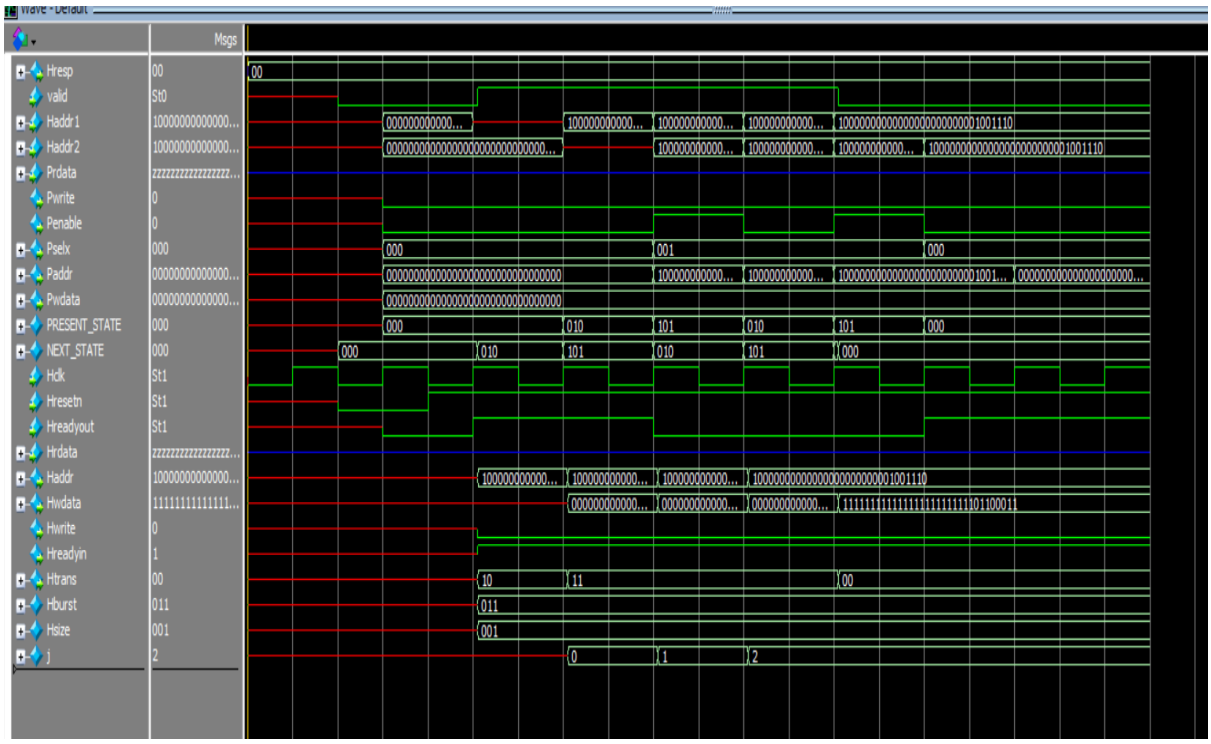
2.SINGLE_READ_TRANSFER



3.**BURST_WRITE_TRANSFER**

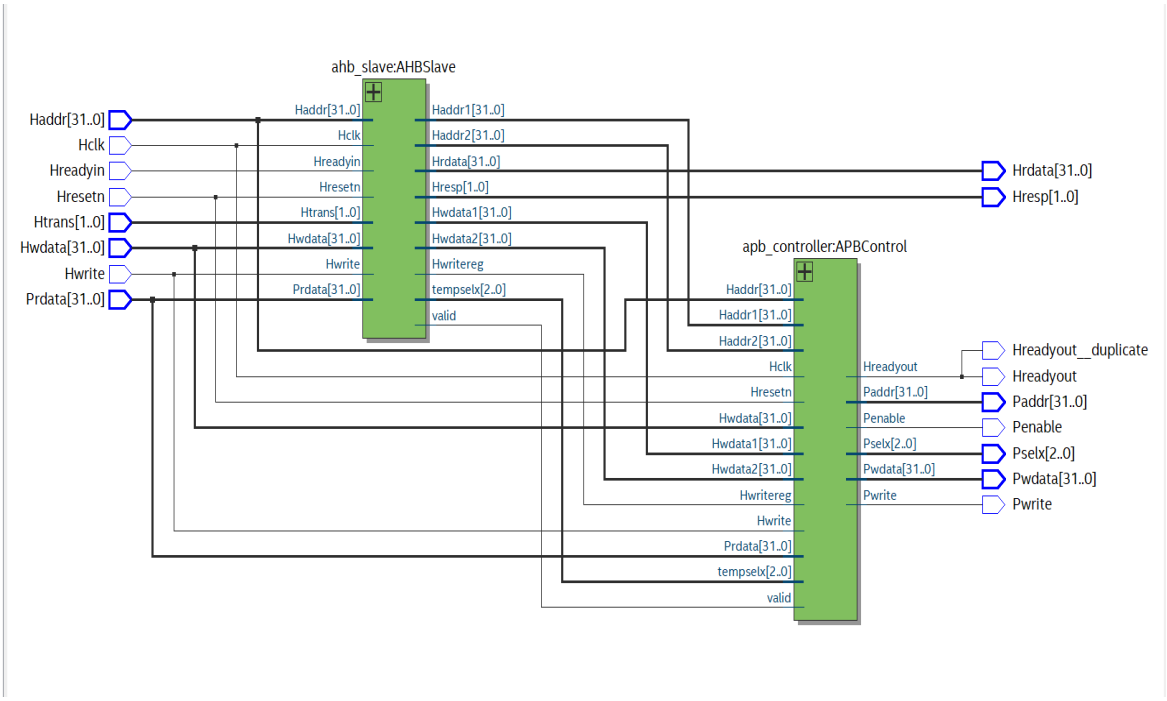


4. **BURST_READ_TRANSFER**

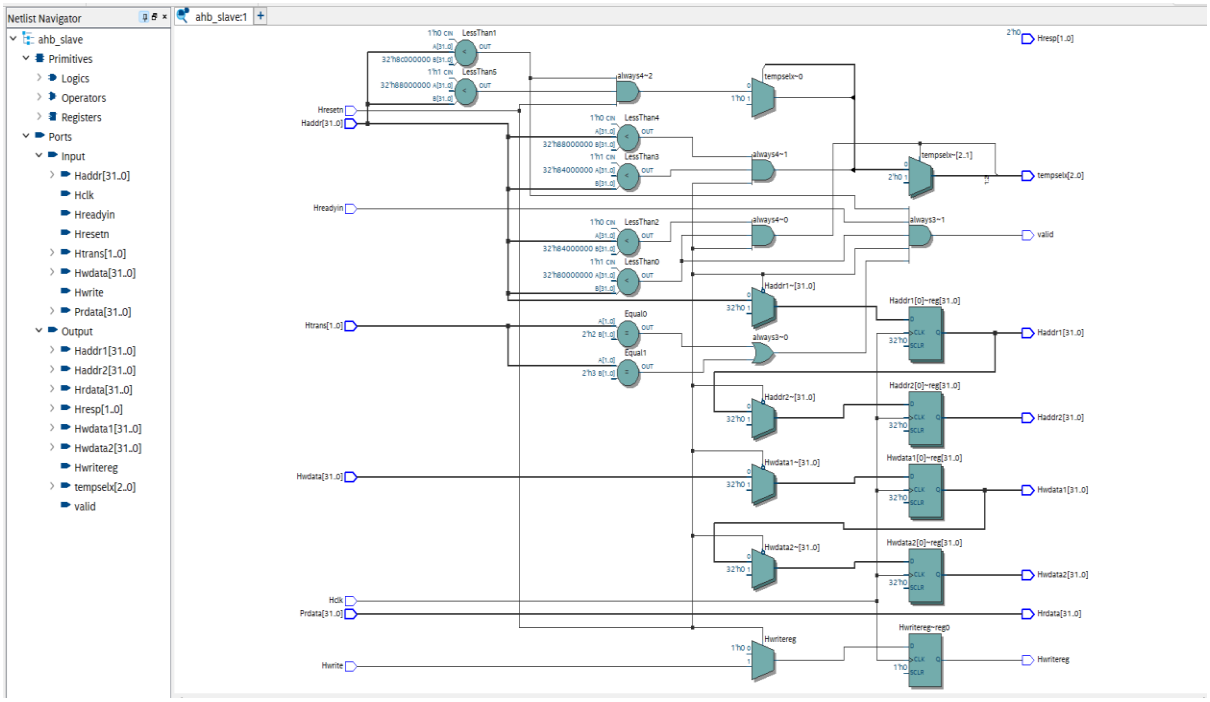


SYNTHESIS :

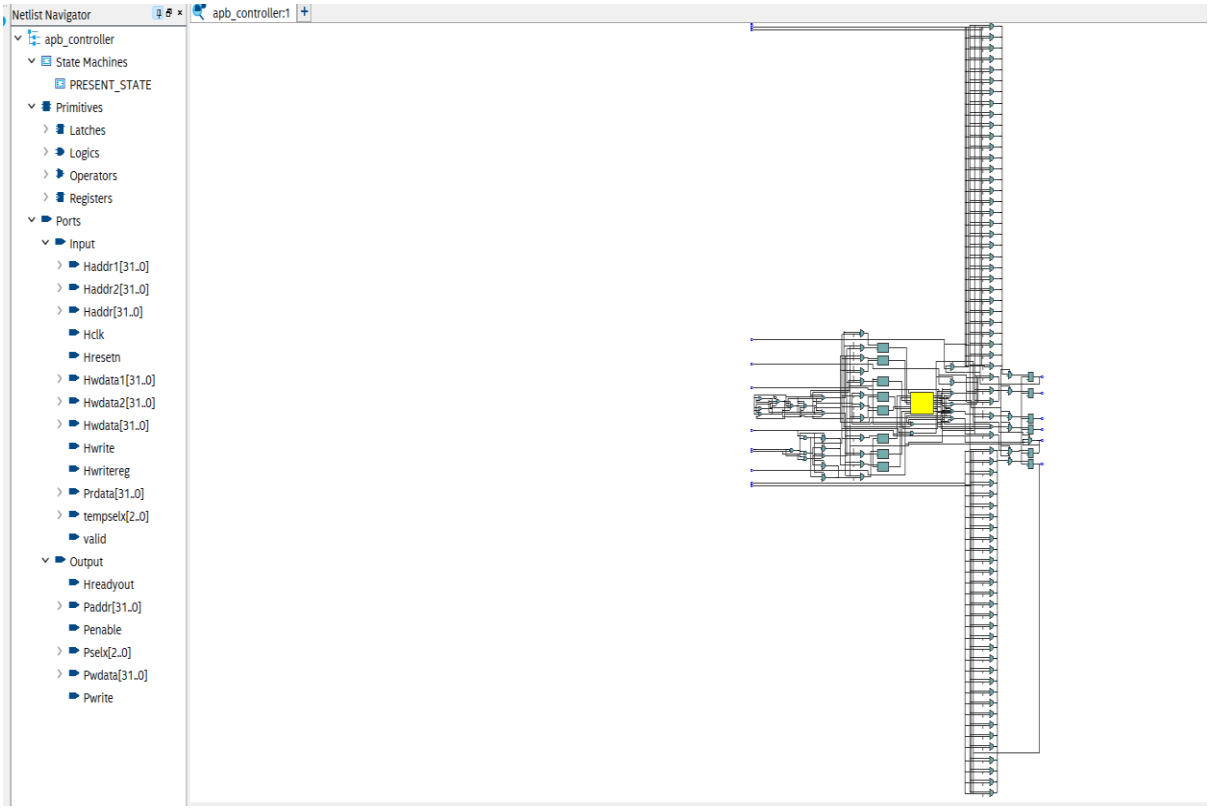
1. BRIDGE_TOP_MODULE



2.AHB_SLAVE_INTERFACE



3.**APB_FSM_CONTROLLER**



CONCLUSION :

My RTL design internship provided a springboard for developing practical skills. I designed, integrated, and verified modules, solidifying my understanding of the design flow. Troubleshooting simulations and synthesis in ModelSim and Quartus Prime honed my problem-solving abilities. I mastered Verilog HDL syntax for complex digital circuit modelling and honed my signal analysis skills, enabling accurate design verification. This internship fueled my passion for VLSI design and equipped me with the necessary analytical and problem-solving skills to excel.

The AHB2APB Bridge project showcases my ability to integrate high-performance AHB and low-power APB buses within AMBA architecture. This bridge facilitates seamless communication and efficient data management across different bus systems. Synthesis results confirm the bridge's robustness, ensuring optimal performance with minimal power consumption. This project highlights the importance of bridging for efficient and versatile embedded systems in modern VLSI design.