🔧 Mini Project Challenge – Phase 1

Title: Traffic Light Controller (Smart Variant)

Problem Statement:

Design a traffic light controller for a **4-way intersection** (North, South, East, West) using either **Verilog or VHDL**.

The controller should:

- Alternate green light priority between NS and EW directions.
- Handle **pedestrian crossing requests** via push-button inputs: ped_NS, ped_EW.
- Use a **finite state machine (FSM)** with clearly defined timing sequences for green, yellow, and red phases.
- Show a **blinking "WAIT"** signal when a pedestrian is waiting during a red phase.
- Assume a system clock of **50MHz**.

📥 **Inputs:**

- clk – System clock (50MHz)
- reset – Active-high synchronous reset
- ped_NS, ped_EW – Pedestrian crossing requests

📤 **Outputs:**

- NS_red, NS_yellow, NS_green
- EW_red, EW_yellow, EW_green
- pedestrian_wait – Blinking signal indicating pedestrian is waiting

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🧩 **Requirements:**

- Use either **Verilog** or **VHDL** or **System Verilog**
- **Upto simulation is only needed, you may test if a board is available to you.**
- Implement modular design:

    - FSM module
    - Timer/counter module (if needed)
    - Pedestrian control module
- Use clean, synchronous coding practices
- Comment your code

Google forms will be shared soon for uploading your responses.