1. Difference b/w SISD, SIMD and MIMD? Can given an explame for each type of computer

A) Based on specfic classification of parallel Computer Architecture, classifications are based on no of concurrent instruction (single or multiple) & data stream (single or multiple) avaliable in architecture

SISD:- 1. Single unicore processor executes a single instruction stream to operate on data stored in a single memory

2. The hardware in such process is such Process is configured to carry operands for only one instruction at a time

SIMD:- 1. Executes a single equivalent operation on multiple data pieces at the same time. There is a single control unit and several processing unit

2. A single instruction can be used to fech multiple files

MIMD:- While most modern desktop are MIMD each processor system can execute asynchronously different set of instruction

independently on a different set of data units which means that each of them can do something different at any given time.

2) What are the factors that determine the profit of CPU fabrication? How to improve the profit?

A) a) Chip size & production cost of chip
b) Size of memory in CPU
c) Supply & demand of machine
d) Architecture used in CPU

3) What is LRU? How to improve the performance of computer with LRU?

LRU → Least Recently used

A) This technique is used to remove/replace some blocks in the cache which are recently used with the new ones coming from main memory. Whenever CPU reads the data from memory it stores in cache but when cache is full it needs to replace the old ones with the new ones. The least recently used data is removed so that most used data is in cache, by this it need not

always move the frequently used data from main memory to cache. By this it improves performance

4. What are the advantages and disadvantages of write through ~~and~~ cache compared with write back cache

A) Using the write through policy data is written to the cache and the backing store location at the same time.

Advantages:- Ensure fast retrieval while making sure the data is in the backing store & is not lost in case the cache is disrupted

Disadvantages:- Writing data will experience latency as you have to write to two places at a time

• write through	Write back
1. Main memory always contain same data as cache	Main ~~mary~~ memory and ache memory may have different data
2. When I/O ~~data~~ device communicated through DMA would recive most recent data	When I/O device communicated through DMA would not recive most receat data

5.) What are the factors that determine the average memory access time? Please list at least 3 solution that can help reduce AMAT?

A) The factor that determine the average memory access time is

1) To reduce hit time :- a) pipeline cache access to improve band width
   b) Multiported caches
   c) Multi banked caches
2) To reduce miss Rate:- a) Compiler optimization
   b) ~~Compiler~~ Large blocks, Large caches, Higher Associativity
   c) prefectching
3) To reduce miss penality:- 1) Non blocking cache
   2) victim caches
   3) Multi level caches
   4) Merging write buffer

6.) What is victim cache? What's the relationship b/w victim cache and data cache

A) Victim cache is a small fully associative cache buffer for dirty blocks. Cache miss can look into victim cache first It is perfect between L_1 & L_2 cache Whenever block is dirty it can be flushed to victim cache

7) What is TLB? How does TLB help speed up computer performace

A) TLB → Translation lookaside buffer is a fast Address Translation place page table in RAM. It keep translation in hardware MMU.

The TLB can be placed at different positions in memory hierachy to speed up the computer performace. When CPU is looking for the process that can be searched in TLB instead of page in ~~ram~~ memory

As TLB is stored in cache it is much faster to access

8) What are the difference b/w virtual memory and physical memory? What are the adv of virtual memory

A) Virtual memory is a combination of some blocks from physical memory that only process / program uses to store all the data that is needed by it. Physical memory is the real memory which is known by CPU. It is seen in CPU perspective

Adva of virtual memory:- Virtual memory is not perfect physically only required

data is stored in it and we can delete the data from virtual memory as it is present in main memory

Problem 2 :-

a) Die size = $120mm^2 = 1.2cm^2$ N = 14

defect Rate = 0.04, Wafer yeild = 100% = 1

$$\text{Die yield} = \text{wafer yield} \times \frac{1}{(1 + \text{Defect per unit} \times \text{Die area})}$$

$$= \frac{1}{(1+0.04 \times 1.2)^{14}} = \frac{1}{(1.048)^{14}} = 0.5187$$

Die diameter = 450mm = 45cm

No. of die per wafer :-

$$= \frac{\pi (\text{wafer diameter}/2)^2}{\text{Die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$

$$= \frac{\pi \left(\frac{45}{2}\right)^2}{1.2} - \frac{\pi \times 45}{\sqrt{2 \times 1.2}}$$

$$= 45\pi \times \left(\frac{45}{4.8} - \frac{1}{1.5}\right)$$

$$\simeq 1233$$

Profit = Die per wafer × profit per wafer × yeild

$$= 1233 \times 10 \times 0.518$$

$$\simeq 6386.94$$