Design of 6T SRAM Array

Instructor : Dr Anuj Grover

Independent Project

Nikhil Pratap Singh MT21199
Sudhanshu Trivedi MT21212

INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Problem Statement

Problem Statement:

Icell >= 50uA at wc, 1.0V
Ileak < 100pA at nom,1.1V,25C
Vmin=0.95V
Case-1: 6T Cell based BL=512 rows
Case-2: 6T Cell based BL=32 rows/ bank (16 banks)

Understanding:

Icell >= 50uA at Worst case condition at 1V, 125C and Ileak < 100pA at Nominal condition at 1.1V, 25C.

For calculating FOMs (Write margin, Write time, SNM, Retention Voltage) at Vmin = 0.95V.

We have 2 cases with different total Bit line capacitance one with 512 rows and Second with 32 rows/bank with total such 16 banks

Challenges

Various Conflicting Parameters -

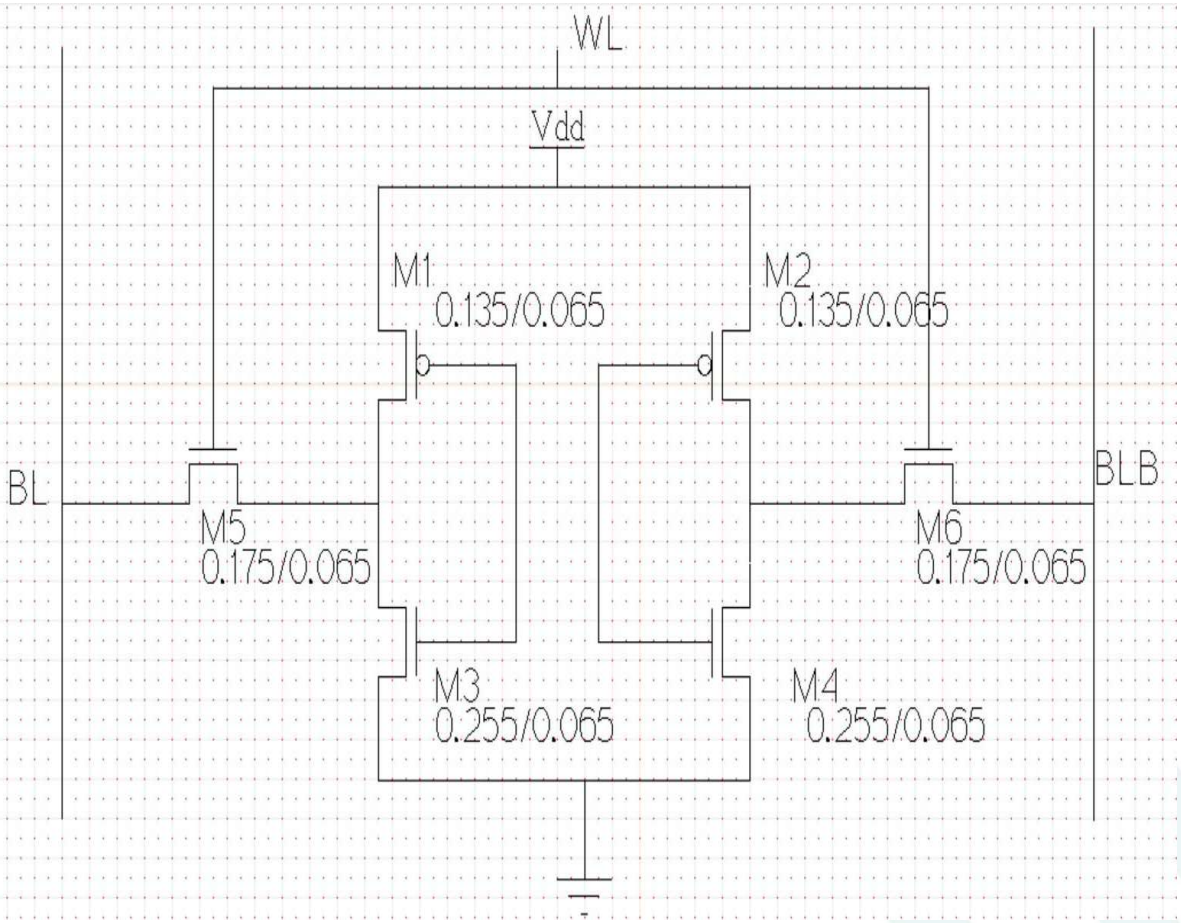
For high cell current we need to increase the size of PG and PD but that leads to an increase in the leakage current too. We need to reach a sizing such that both the specifications can be met.

Verification Plan -

We tried different Vt devices with the width constraint and low voltage but were unable to achieve it. So, cell current specification was met at PVT of TT/25/1.08v with Standard Voltage devices.

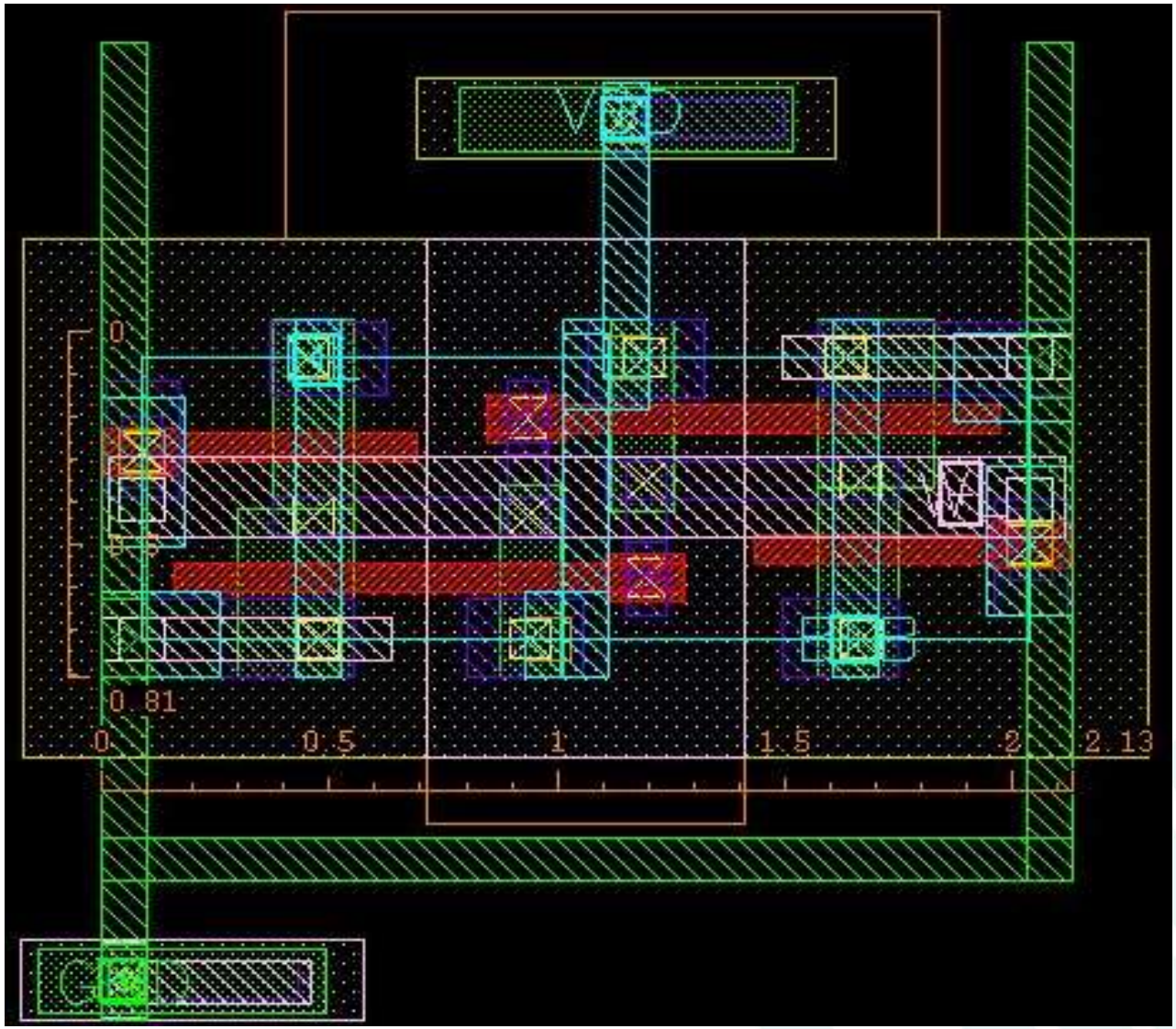
Design Schematic(s)

Cell Ratio (CR)	**1.46**
Pull up ratio (PR)	**0.7**
W/L of PU	**0.135/0.065**
W/L of PD	**0.255/0.065**
W/L of PG	**0.175/0.065**

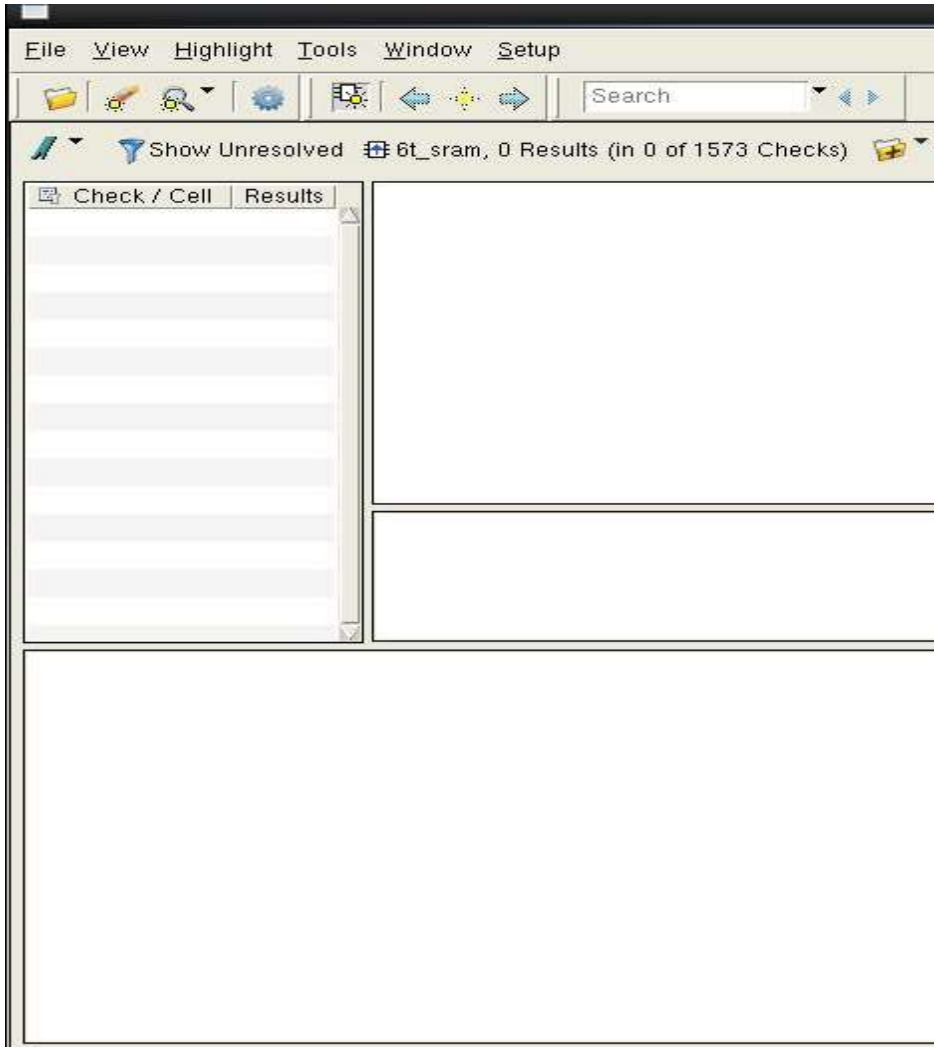


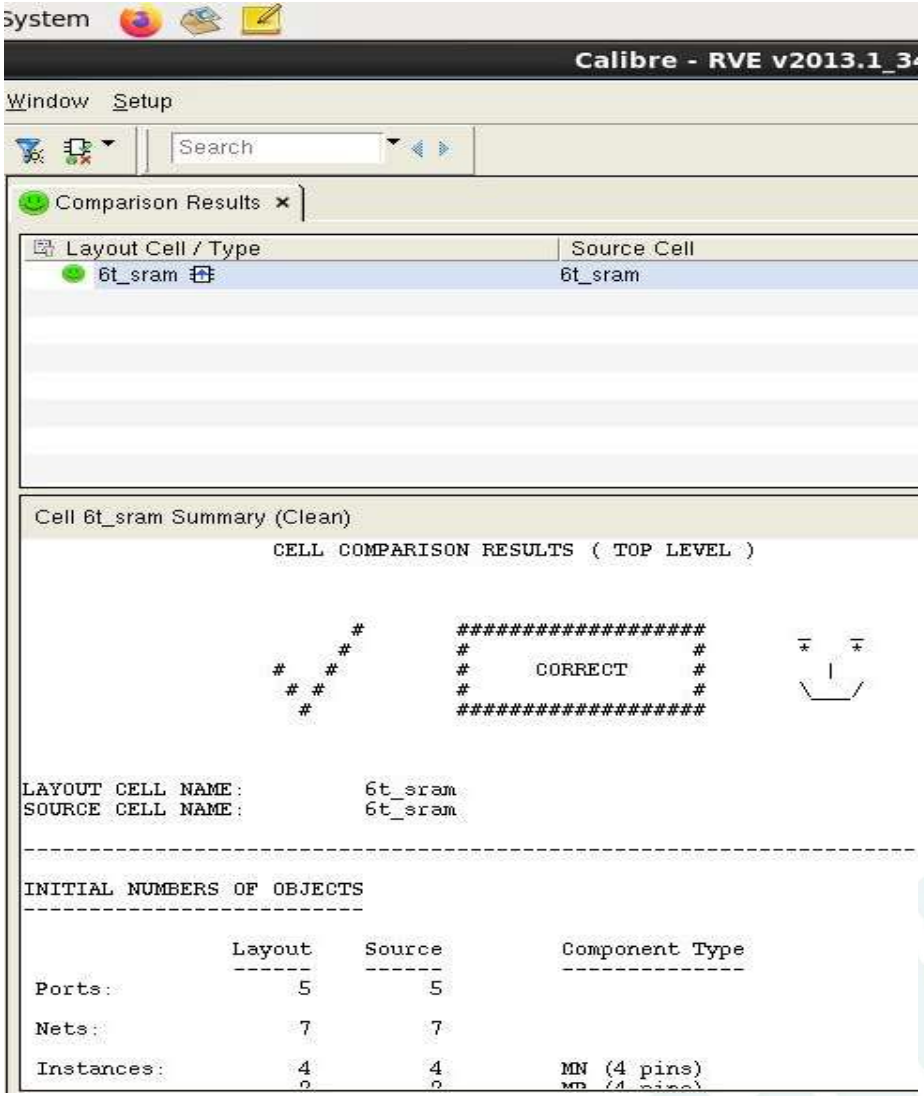
6T SRAM Cell Layout

AREA = 1.7um^2

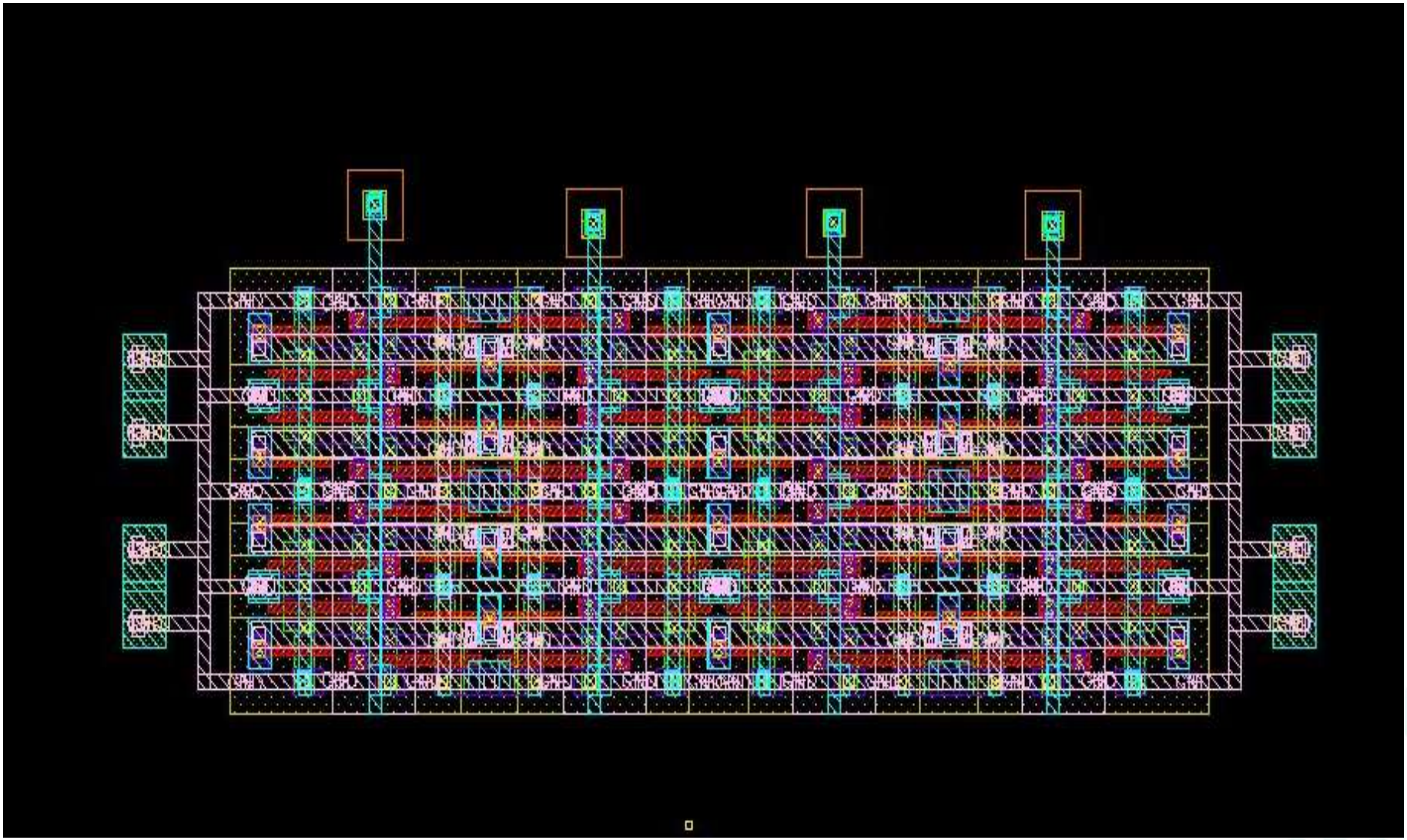


DRC/LVS clean





6T SRAM Array (4*4)



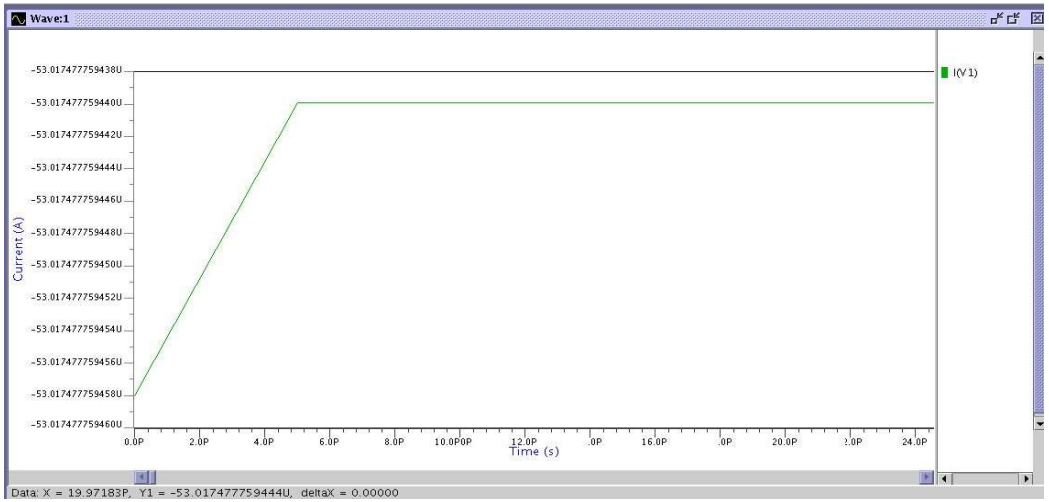
Verification Plan (& Justification)

- **Cell Current**: SS Corner, taking BL,BLB,WL and VDD all equal to 1V, Temp=125C
- **Leakage Current:** TT Corner, taking BL,BLB,WL and VDD all equal to 1.1V and Temp =25C

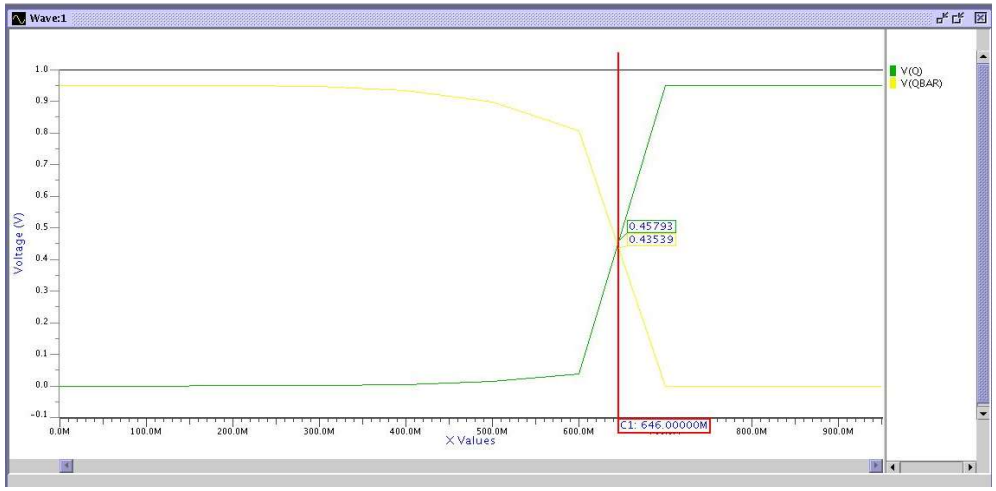
FOMs-

- **Cell Current:** taking BL,BLB,WL,VDD,Q all equal to 1V and QB=0V then while doing DC Analysis, the current flowing through Pass Gate is Cell Current.
- **Leakage Current:** taking BL,BLB,WL, VDD and Q all equal to 1.1V and QB=0 then while doing DC Analysis, current flowing through VDD and BLB is Leakage Current.
- **Write Margin:** Taking WL=0, DC analysis and varying BL 0 to voltage at which Q and QB flips.
- **Write Time:** Time at which both 1s and 0s written inside the memory cell.
- **SNM:** Cross point of Q and QB in DC Analysis, keeping WL=0
- **6-Sigma:** Monte Carlo is run and see the HISTO graph.

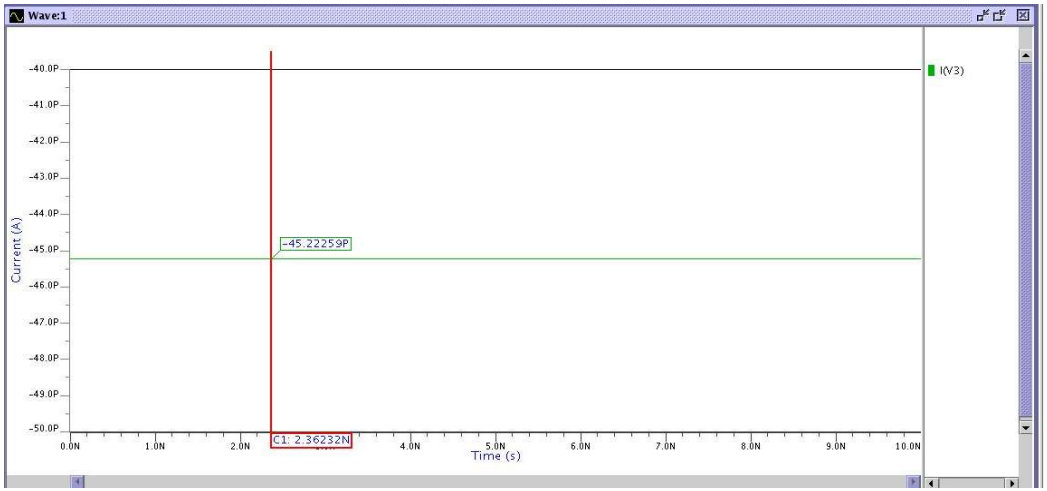
Results – FOMs



Cell Current



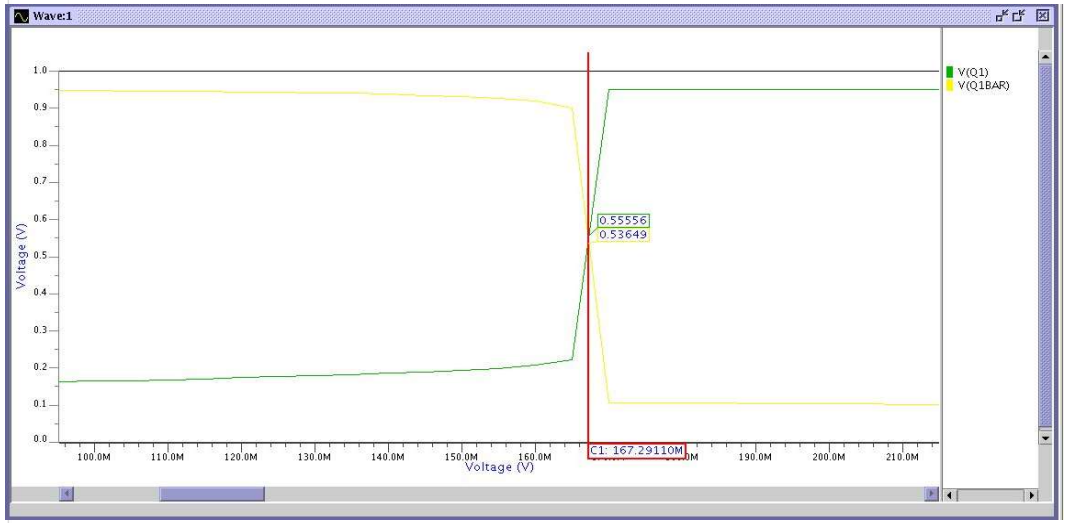
Write margin

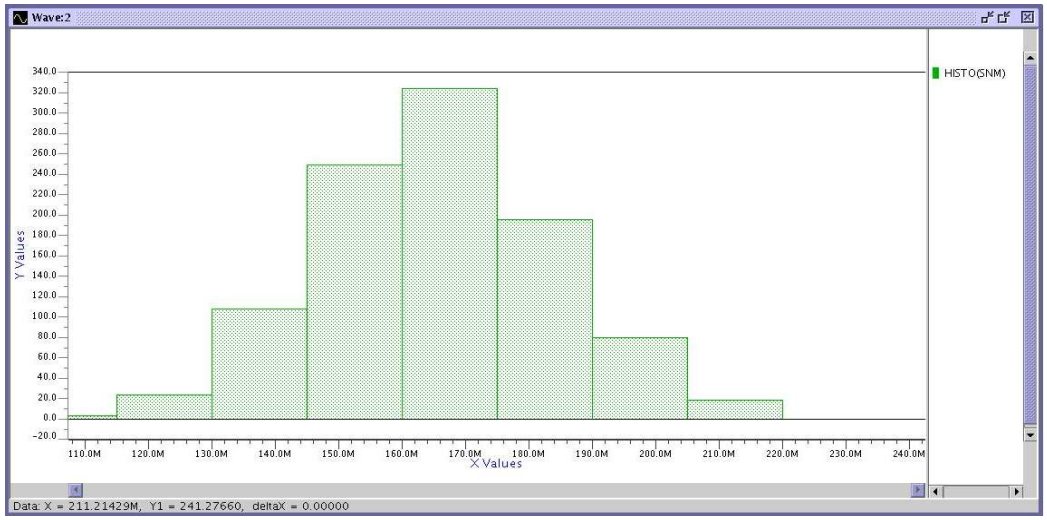


Leakage Current

Write Time

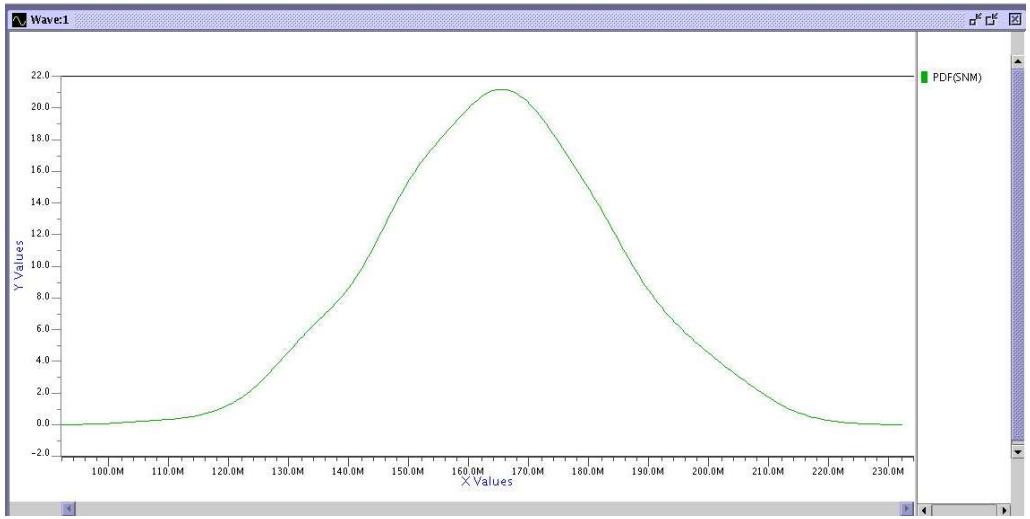
SNM, 6sigma qualification (1/1)

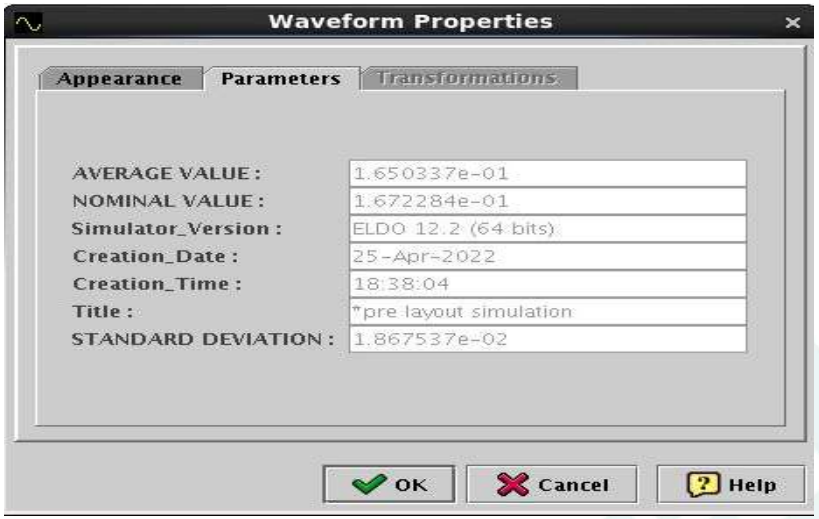




SNM

HISTO





PDF

6 sigma qualified

Results

FOM	Value
Cell Current	53.06uA
Leakage Current	45.22pA
Write Margin	0.44volt
Write Time	77psec
SNM	0.54volt
Monte Carlo	6 sigma qualified

PVTs	Cell current
SS/25/1v	32.29uA
SS/125/1v	28.89uA
SS/-40/1v	35.95uA
TT/25/1v	41.89uA
TT/125/1v	37.2uA
TT/-40/1v	46.66uA
FF/25/1v	54.89uA
FF/125/1v	48.54uA
FF/-40/1v	61.03uA

Conclusions and Future Plans

- Technical Conclusions
  - We were able to design a memory cell with the specified constraints and mirror it to obtain the memory cell.
    - It got difficult for us to convert into a 512x512 memory array.
- Learnings from the project

  - We learnt to calculate different Figure of Merits and how to figure out the sizing using the Pull Up Ratio and Cell Ratio.
  - We learnt what voltage of devices to use such that the design can be obtained for the given specification.
  - The project helped us in better understanding of the theory portion taught in class by giving us a hands-on experience on the same for example the concept of mirroring.

- Future plans
  - In SRAM Cell high Read current is needed so that it is sufficiently stable so in that process, while increasing the cell size, the leakage current also increases causing huge power overhead so ways can be looked at which does not lead to this.
  - Memories having separate Read Write port can be explored
  - Publication Scope in conferences like IOP Conference Series Materials Science and Engineering can be explored.

References

https://www.academia.edu/30689972/High_Read_Stability_and_Low_Leakage_Cache_Memory_Cell?email_work_card=view-paper

https://eecs.wsu.edu/~daehyun/teaching/2017_EE466/labs/EE586_CadTutorials_Ver2.pdf

https://www.academia.edu/17157991/Design_of_6T_5T_and_4T_SRAM_Cell_on_Various_Performance_Metrics?email_work_card=view-paper

https://www.academia.edu/7411497/Low_power_single_bitline_6T_SRAM_cell_with_high_read_stability?email_work_card=view-paper

http://www.iosrjournals.org/iosr-jvlsi/papers/vol8-issue1/Version1/E0801014346.pdf

https://www.academia.edu/30689972/High_Read_Stability_and_Low_Leakage_Cache_Memory_Cell?email_work_card=view-paper

https://www.academia.edu/13779655/DESIGN_OF_LOW_POWER_SRAM_CELL_WITH_IMPROVED_STABILITY?email_work_card=view-paper