VDF

Assignment 6: DFT

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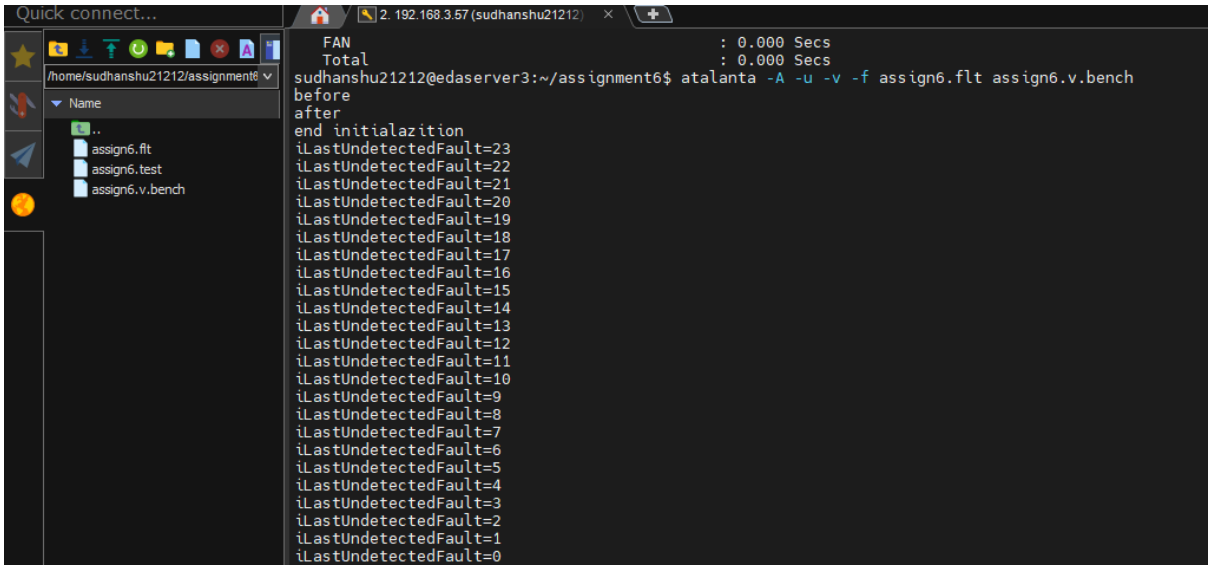
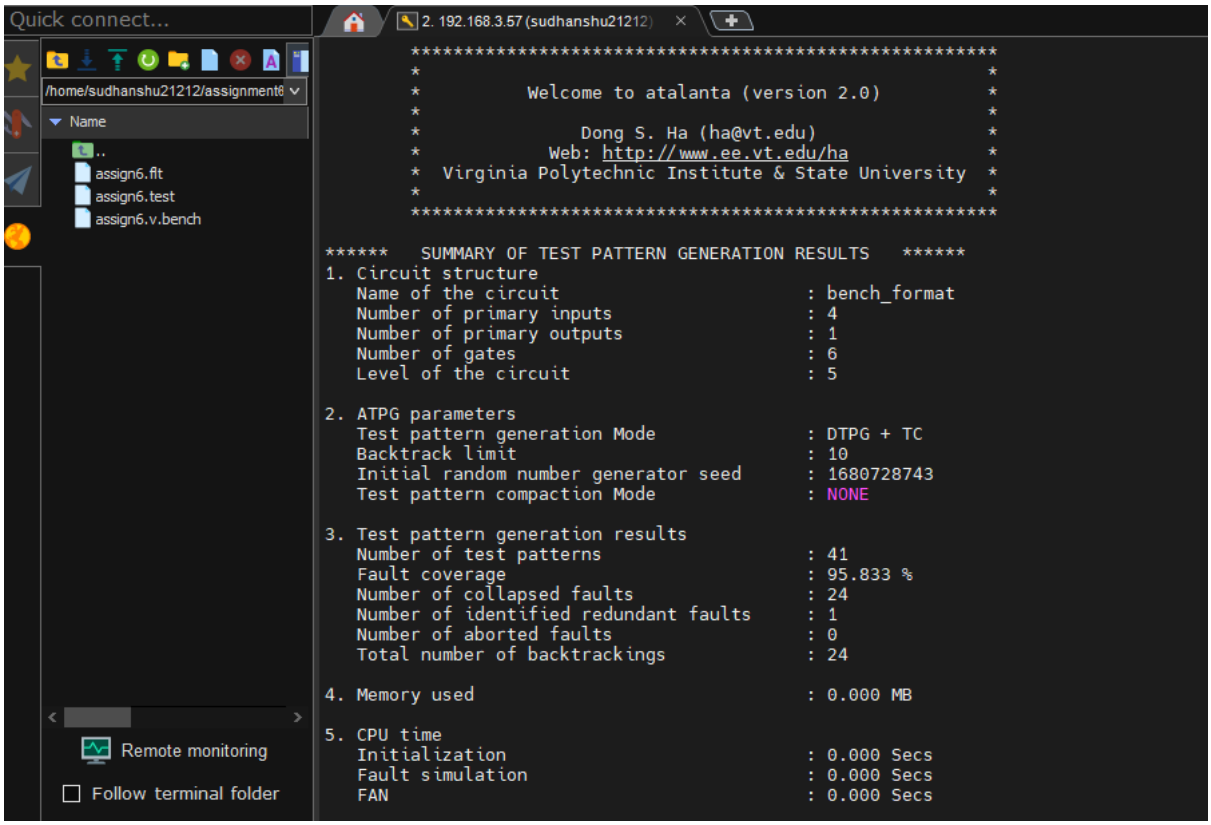
<u>Question1:</u> Show screenshot or snippet of log file to prove that you have indeed run the tool.

Answer: Tool used: Atalanta ATPG

Snippet





Question 2: 2. Run the tool and find the test patterns for the single stuck at faults in the circuit shown in Fig. 1.

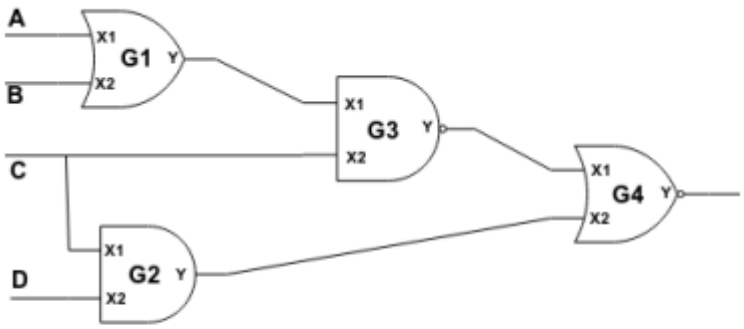


Fig 1

Solution:

```
2. 192.168.3.57 (sudhanshu21212)   3. 192.168.3.57 (sudhanshu21212)
        *          Welcome to atalanta (version 2.0)          *
        *                                                     *
        *               Dong S. Ha (ha@vt.edu)                *
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        *                                                     *
        *******************************************************

******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
1. Circuit structure
   Name of the circuit                      : bench_format
   Number of primary inputs                 : 4
   Number of primary outputs                : 1
   Number of gates                          : 6
   Level of the circuit                     : 5

2. ATPG parameters
   Test pattern generation Mode             : DTPG + TC
   Backtrack limit                          : 10
   Initial random number generator seed     : 1681129443
   Test pattern compaction Mode             : NONE

3. Test pattern generation results
   Number of test patterns                  : 41
   Fault coverage                           : 95.833 %
   Number of collapsed faults               : 24
   Number of identified redundant faults    : 1
   Number of aborted faults                 : 0
   Total number of backtrackings            : 24

4. Memory used                              : 0.000 MB

5. CPU time
   Initialization                           : 0.000 Secs
   Fault simulation                         : 0.000 Secs
   FAN                                      : 0.000 Secs
   Total                                    : 0.000 Secs
sudhanshu21212@edaserver3:~/assignment6$
```

Note: If we don't give manually input location of all fault sites, the tool will operate in normal Diagnostic mode mode and won't generate all possible collapse fault test vectors like here; if we don't set .flt file tool will ignore fault SA1 at A,B and SA0 at D.

I have 1st identified all possible SA0/SA1 faults locations and provide it as an input to my tool, Atalanta ATPG for generating test pattern for its detectability. After performing test pattern generation, we found that total 24 collapse faults possible and tool reported it with 1 redundent fault. Hence fault coverage = (24-23)/24= 0.95833 = 95.83%.

Below is the input files: assign6.v.bench & assign6.flt

Output files: assign6.test & assign6.ufaults

```
#bench format
INPUT(A)
INPUT(B)
INPUT(C)
INPUT(D)

w1= OR(A,B)
w2= AND(w1,C)
w3= NOT(w2)
w4= AND(C,D)
w5= OR(w3,w4)
Z= NOT(w5)
OUTPUT(Z)
```

Assign6.v.bench file

```
A /1
A /0
B /1
B /0
C /1
C /0
D /1
D /0
w1 /1
w1 /0
w2 /1
w2 /0
w3 /1
w3 /0
w4 /1
w4 /0
w5 /1
w5 /0
C→w2 /1
C→w2 /0
C→w4 /1
C→w4 /0
Z /1
Z /0
```

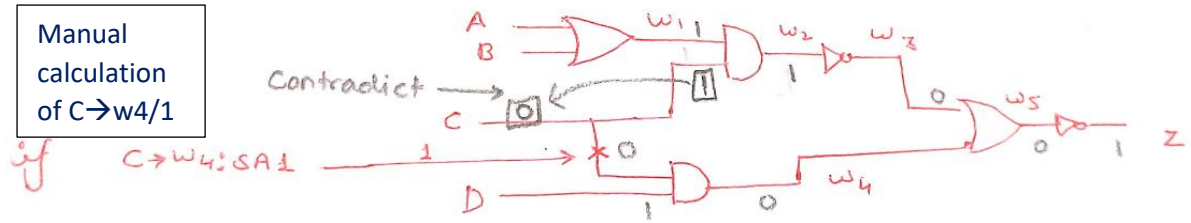
Assign6.flt

Output file:

```
* Name of circuit:  assign6.v.bench
* Primary inputs :
  A B C D

* Primary outputs:
  Z

* Test patterns and fault free responses:

A /1
       1: 0010 0
A /0
       1: 1010 1
B /1
       1: 0010 0
B /0
       1: 0110 1
C /1
       1: 1x00 0
C /0
       1: 1x10 1
D /1
       1: 1x10 1
D /0
       1: 1x11 0
w1 /1
       1: 0010 0
w1 /0
       1: 1x10 1
       2: 0110 1
w2 /1
       1: xx0x 0
       2: 0010 0
w2 /0
       1: 1x10 1
       2: 0110 1
w3 /1
       1: 1x10 1
       2: 0110 1
w3 /0
       1: xx0x 0
       2: 0010 0
w4 /1
       1: 1x10 1
       2: 0110 1
w4 /0
       1: 1x11 0
       2: 0111 0
w5 /1
       1: 1x10 1
       2: 0110 1
w5 /0
       1: xx11 0
       2: xx01 0
       3: xx00 0
       4: 0010 0
C→w2 /1
       1: 1x0x 0
       2: 010x 0
C→w2 /0
       1: 1x10 1
       2: 0110 1
C→w4 /1
C→w4 /0
       1: 1x11 0
       2: 0111 0
Z /1
       1: xx11 0
       2: xx01 0
       3: xx00 0
       4: 0010 0
Z /0
       1: 1x10 1
       2: 0110 1
```

```
C→w4 /1
```

Manual calculation of C→w4/1

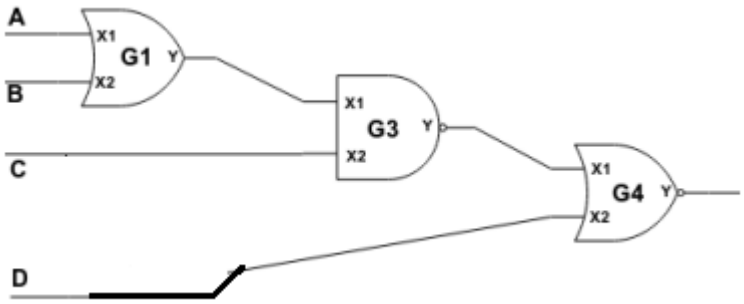


Fault Site and fault type (SA0 or SA1)	Test Pattern reported by Tool	Test Pattern Manually Computed
A /1	0010	0010
A /0	1010	1010
B /1	0010	0010
B /0	0110	0110
C /1	1x00	1100 1000
C /0	1x10	1010 1110
D /1	1x10	1010 1110
D /0	1x11	1x11
w1 /1	0010	0010
w1 /0	1x10 0110	1x10 0110
w2 /1	xx0x 0010	xx0x 0010
w2 /0	1x10 0110	1x10 0110
w3 /1	1x10 0110	1x10 0110
w3 /0	xx0x 0010	xx0x 0010
w4 /1	1x10 0110	1x10 0110
w4 /0	1x11 0111	1x11 0111
w5 /1	1x10 0110	1x10 0110
w5 /0	xx11 xx01 xx00 0010	xx11 xx01 xx00 0010
C->w2 /1	1x0x 010x	1x0x 010x
C->w2 /0	1x10 0110	1x10 0110
C->w4 /1	Redundant fault	Redundant fault
C->w4 /0	1x11 0111	1x11 0111

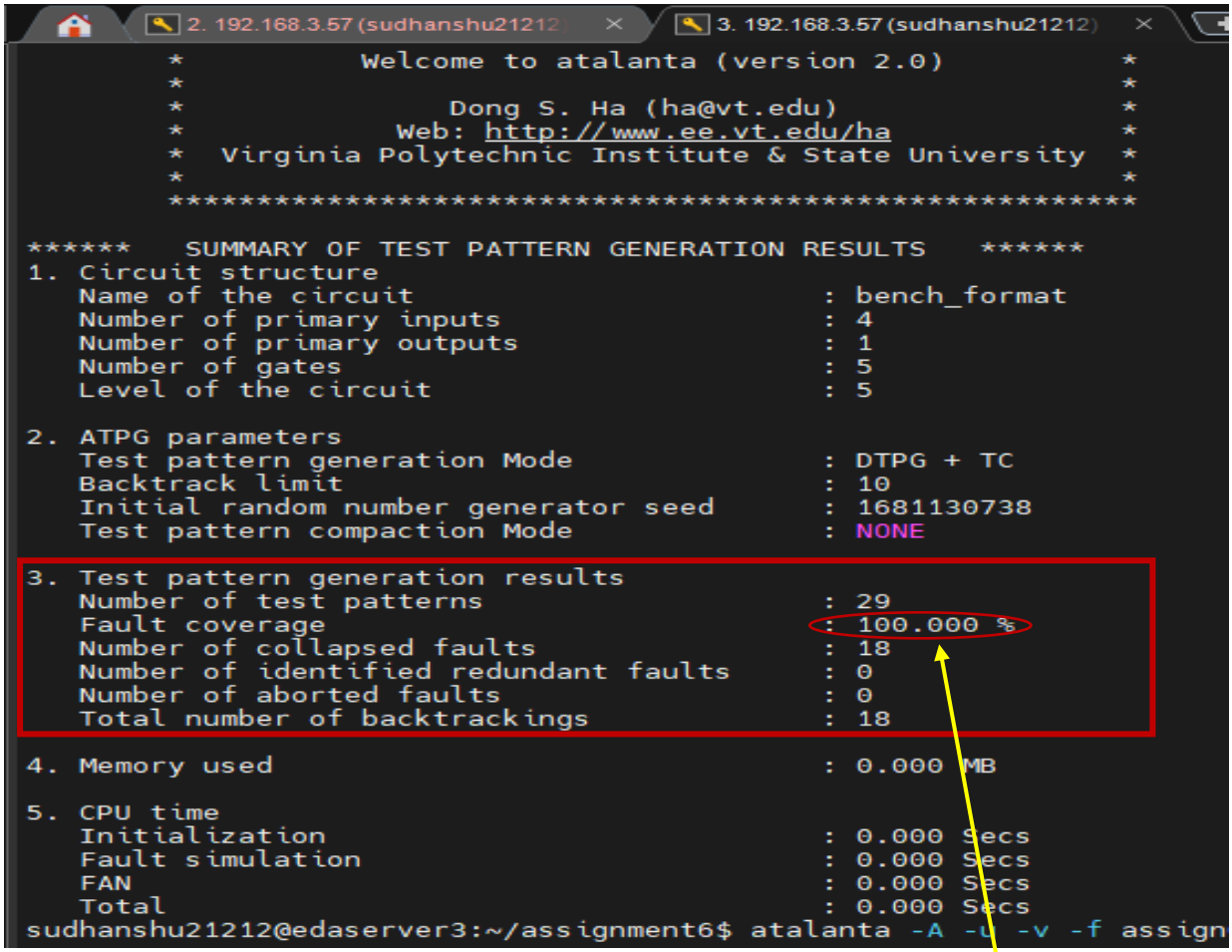
Z /1	xx11 xx01 xx00 0010	xx11 xx01 xx00 0010
Z /0	1x10 0110	1010 1110 0110

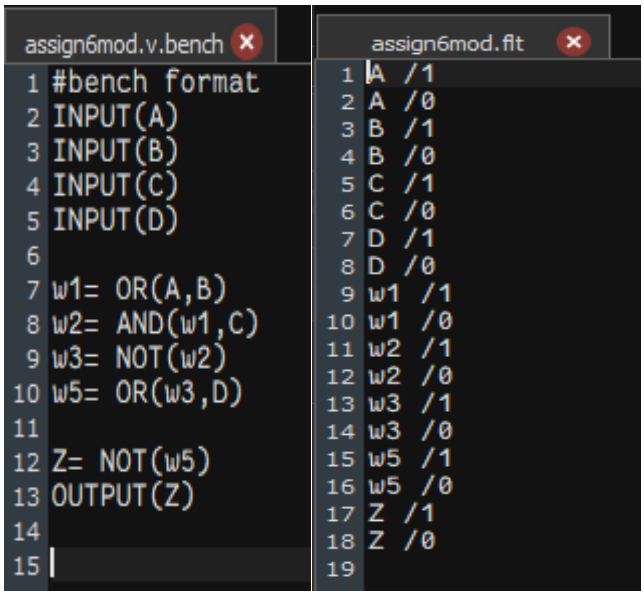
Question3: Modify the circuit to remove redundant fault reported by the ATPG tool preserving the Boolean function implemented by the circuit. Report the modified netlist in the "bench" format and schematic (you can draw by hand and paste the photograph). Run the ATPG tool again on the modified bench file. Report the output of the ATPG tool. Make the above table again for the modified circuit.

Explanation: We know redundant fault can help us to reduce the hardware and with or without redundant, circuit will behave same. By preserving the circuit functionality, we can remove the redundant fault. As earlier it was showing redundant error at C->w4 /1, here when it is stuck at 1 fault, there is no impact of the corresponding AND gate over output, we can remove AND gate from circuit its functionality will not be changed.




```
sudhanshu21212@edaserver3:~/assignment6$ vim assign6mod.flt
sudhanshu21212@edaserver3:~/assignment6$ atalanta -A -u -v -f assign6mod.flt assign6mod.v.bench
before
after
end initialazition
iLastUndetectedFault=17
iLastUndetectedFault=16
iLastUndetectedFault=15
iLastUndetectedFault=14
iLastUndetectedFault=13
iLastUndetectedFault=12
iLastUndetectedFault=11
iLastUndetectedFault=10
iLastUndetectedFault=9
iLastUndetectedFault=8
iLastUndetectedFault=7
iLastUndetectedFault=6
iLastUndetectedFault=5
iLastUndetectedFault=4
iLastUndetectedFault=3
iLastUndetectedFault=2
iLastUndetectedFault=1
iLastUndetectedFault=0
```





Fault coverage is 100%

I have taken “assign6mod.flt” file and “assign6.v.bench” file which contain all the possible stuck-at faults sites and modified circuit bench file. After running the tool we have find that there is no redundant fault present in my circuit and functionality is kept intact.

The below table summarizes all stuck at faults and corresponding generated test vectors.

Fault Site and fault type (SA0 or SA1)	Test Pattern reported by Tool	Test Pattern Manually Computed
A /1	0010	0010
A /0	1010	1010
B/1	0010	0010
B/0	0110	0110
C/1	1x00	1x00
C/0	1x10	1x10
D/1	1x10	1x10
D/0	1x11	1x11
W1 /1	0010	0010
W1 /0	1x10 0110	1x10 0110
W2 /1	xx00 0010	xx00 0010
W2 /0	1x10 0110	1x10 0110
W3 /1	1x10 0110	1010 1110 0110
W3 /0	xx00 0010	xx00 0010
W5 /1	1x10 0110	1010 1110 0110
W5/0	xx11 xx00 0010	xx11 xx00 0010
Z /1	xxx1 xx00 0010	xxx1 xx00 0010
Z /0	1x10 0110	1x10 0110

assign6mod.test

```
* Name of circuit:  assign6mod.v.bench
* Primary inputs :
  A B C D

* Primary outputs:
  Z

* Test patterns and fault free responses:

A /1
      1: 0010 0
A /0
      1: 1010 1
B /1
      1: 0010 0
B /0
      1: 0110 1
C /1
      1: 1x00 0
C /0
      1: 1x10 1
D /1
      1: 1x10 1
D /0
      1: 1x11 0
w1 /1
      1: 0010 0
w1 /0
      1: 1x10 1
      2: 0110 1
w2 /1
      1: xx00 0
      2: 0010 0
w2 /0
      1: 1x10 1
      2: 0110 1
```

```
w3 /1
      1: 1x10 1
      2: 0110 1
w3 /0
      1: xx00 0
      2: 0010 0
w5 /1
      1: 1x10 1
      2: 0110 1
w5 /0
      1: xxx1 0
      2: xx00 0
      3: 0010 0
Z /1
      1: xxx1 0
      2: xx00 0
      3: 0010 0
Z /0
      1: 1x10 1
      2: 0110 1

```

Output file assign6mod.test
note: there is no redundant fault in our circuit hence no ufault file generated