```
  .D(outputreg_R[13]),
  .Q(R[13]),
  .QN(_246_)
);
(* src = "rtl.v:11.1-17.4" *)
DFF_X1 _511_ (
  .CK(clk),
  .D(P[0]),
  .Q(inputreg_P[0]),
  .QN(_247_)
);
(* src = "rtl.v:11.1-17.4" *)
DFF_X1 _512_ (
  .CK(clk),
  .D(P[1]),
  .Q(inputreg_P[1]),
  .QN(_248_)
);
(* src = "rtl.v:11.1-17.4" *)
DFF_X1 _513_ (
  .CK(clk),
  .D(P[2]),
  .Q(inputreg_P[2]),
  .QN(_249_)
);
(* src = "rtl.v:11.1-17.4" *)
DFF_X1 _514_ (
  .CK(clk),
  .D(P[3]),
```

```
  .Q(inputreg_P[3]),
  .QN(_250_)
 );
 (* src = "rtl.v:11.1-17.4" *)
 DFF_X1 _515_ (
  .CK(clk),
  .D(P[4]),
  .Q(inputreg_P[4]),
  .QN(_223_)
 );
endmodule
```

we have designed out RTL code as simple multiplier of A[6:0] and B[6:0] and total instances are generated .

library used : NANGATE45.lib

SDC file :

```
create_clock -name clk -period 8 -waveform {0 4} [get_ports "clk"]
set_clock_transition -rise 0.08 [get_clocks "clk"]
set_clock_transition -fall 0.05  [get_clocks "clk"]
set_clock_uncertainty 0.2  [get_clocks "clk"]
set_clock_latency 0.05 [get_clocks "clk"]
set_input_delay -max 0.8 [get_ports "B"] -clock  [get_clocks "clk"]
set_input_delay -min 0.3 [get_ports "B"] -clock  [get_clocks "clk"]
set_input_delay -max 0.8 [get_ports "A"] -clock  [get_clocks "clk"]
set_input_delay -min 0.4 [get_ports "A"] -clock  [get_clocks "clk"]
```

Question2: Initialize floorplan by assuming some reasonable values of die size and core size. Report the commands you used and the outputs obtained.

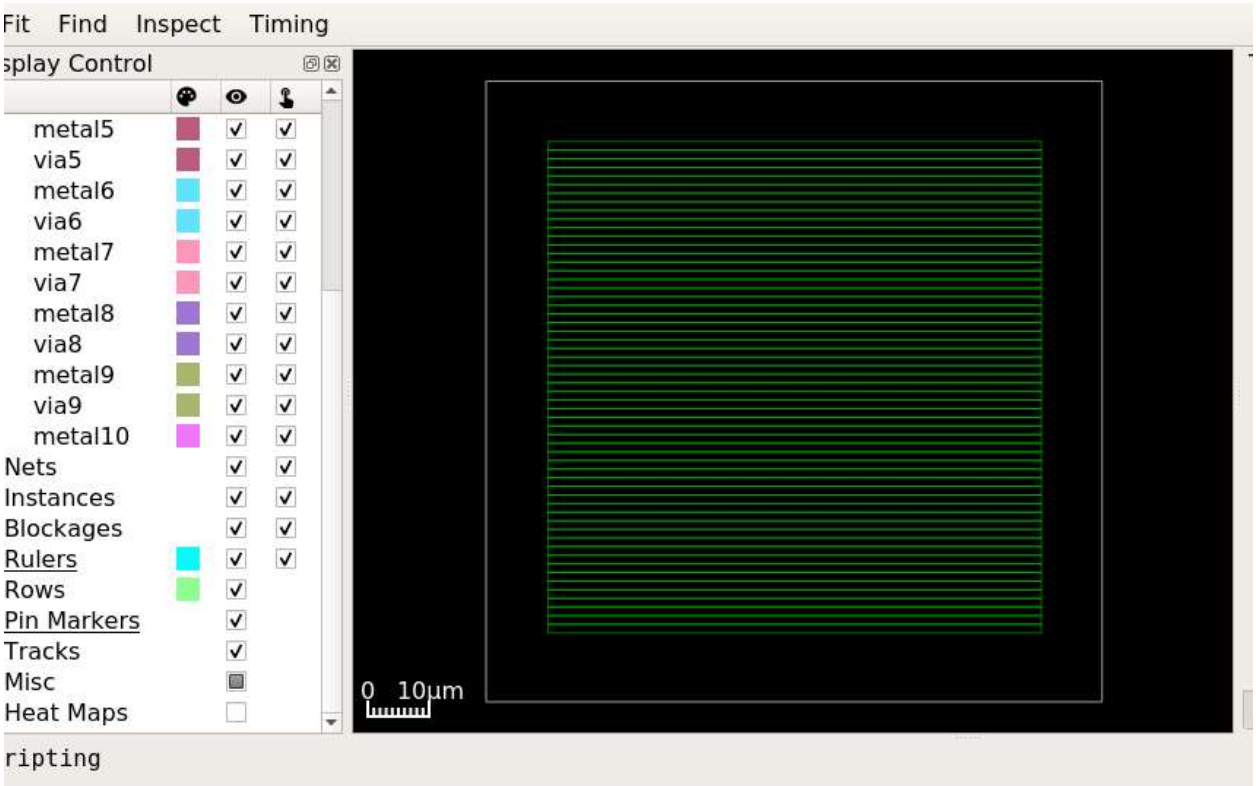
Answer: **Die Area and Core area**

set die_area size {0 0 100.13 100.8}

set core_area size {10.07 11.2 90.25 91}

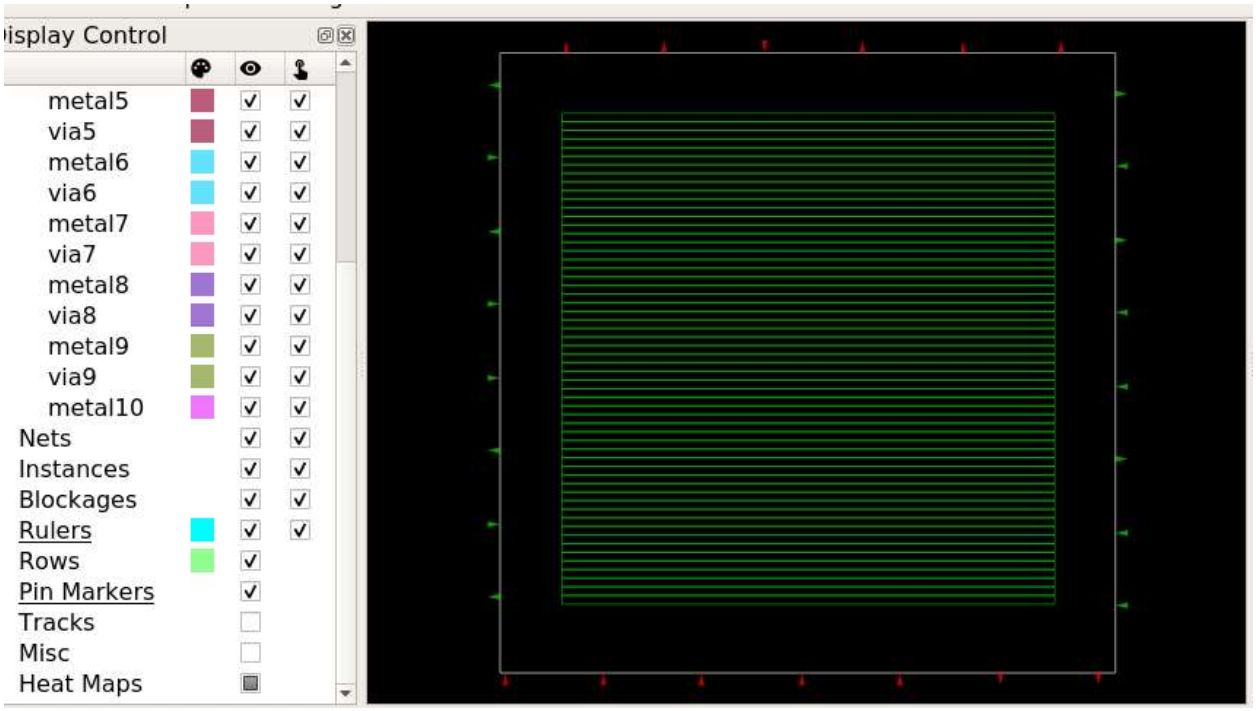
Commands: For floorplanning :

```
################################################################################

# Assumes flow_helpers.tcl has been read.
read_libraries
read_verilog $synth_verilog
link_design $top_module
read_sdc $sdc_file

utl::metric "ord_version" [ord::openroad_git_describe]
# Note that sta::network_instance_count is not valid after tapcells are added.
utl::metric "instance_count" [sta::network_instance_count]

initialize_floorplan -site $site \
  -die_area $die_area \
  -core_area $core_area

source $tracks_file

# remove buffers inserted by synthesis
remove_buffers

################################################################
# IO Placement (random)
```

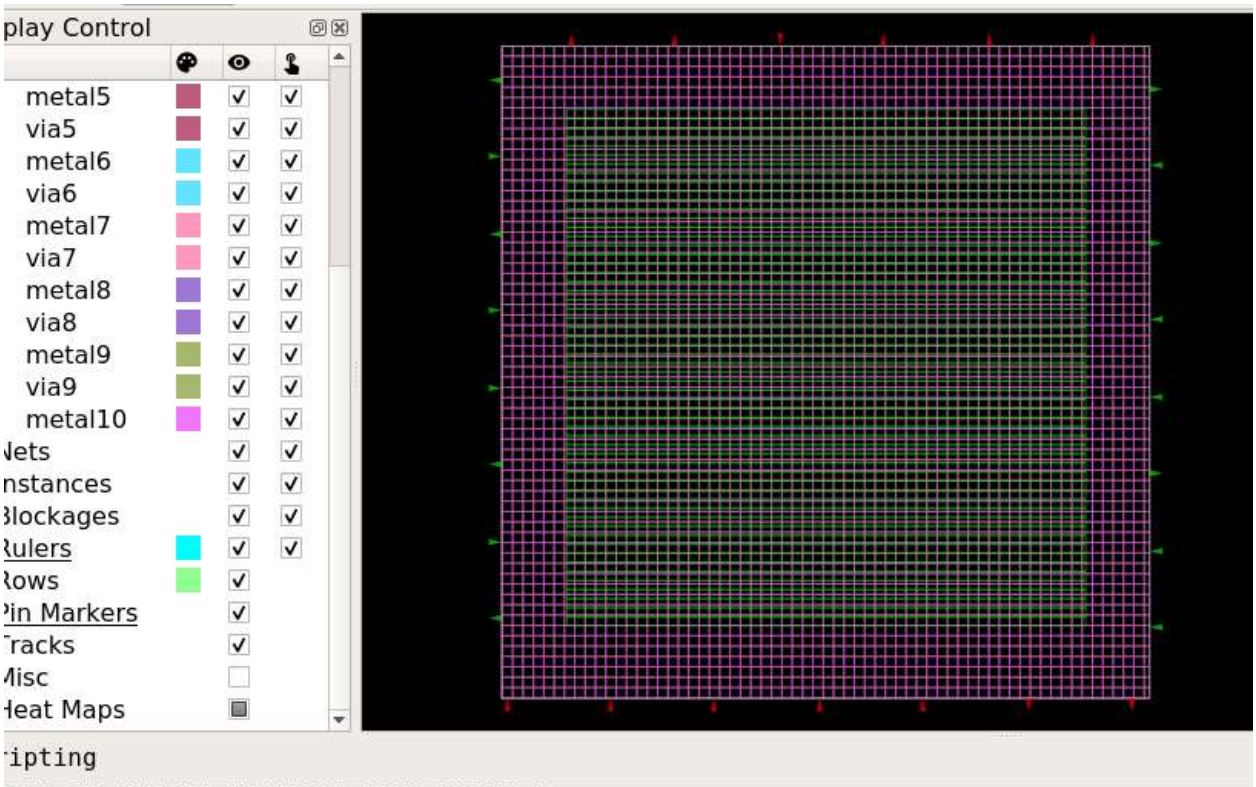



```
INFO RSZ-0026] Removed 0 buffers.
################################################################
```

Question3:



Pin placementwith tracks;

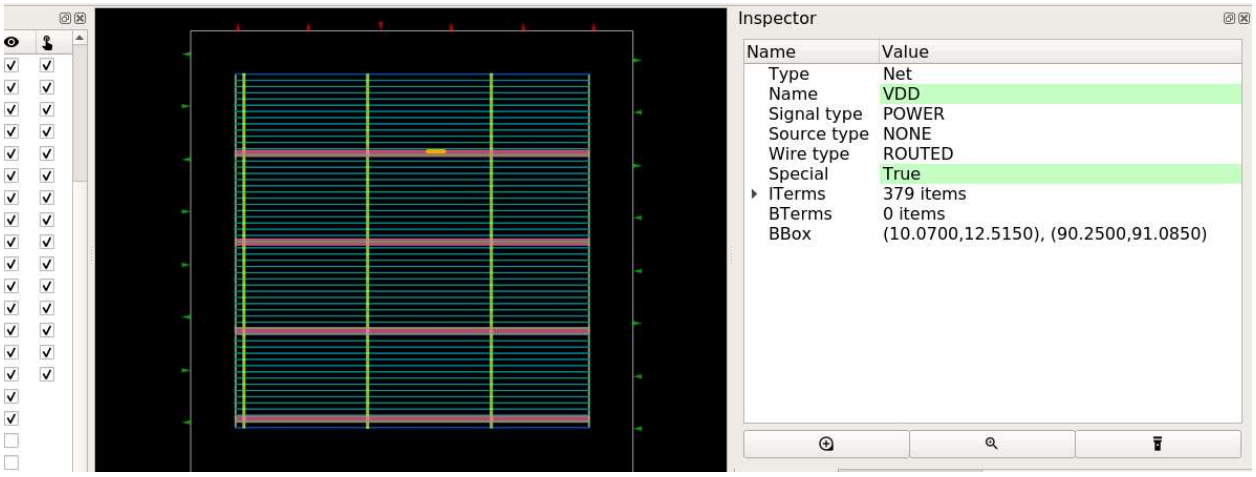


Output at terminal :

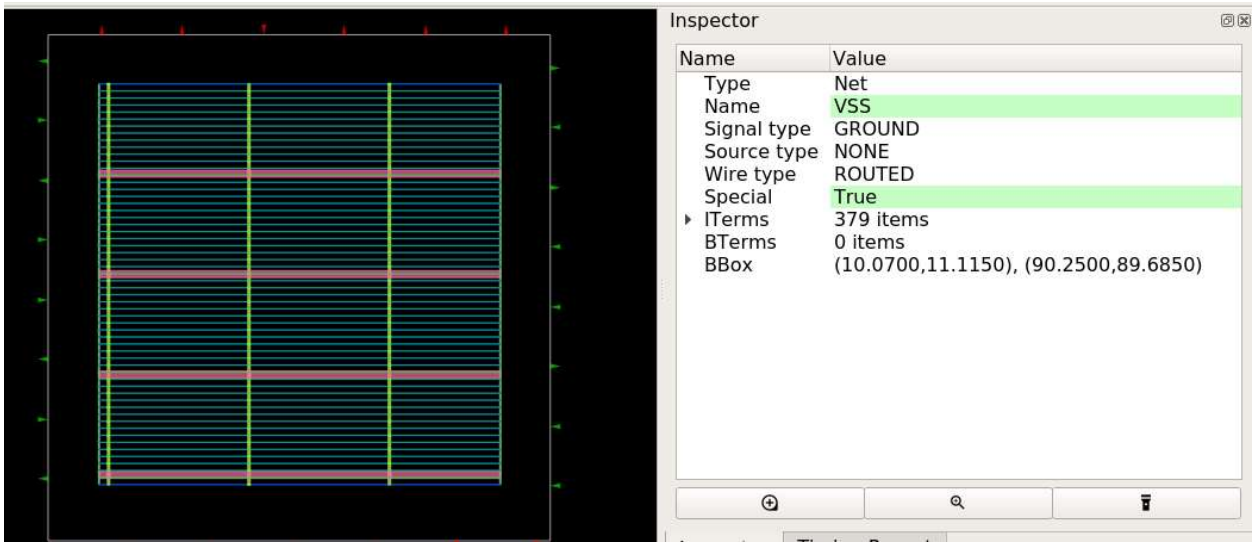
```
###############################################################
# IO Placement (random)
################################################################################
# Assumes flow_helpers.tcl has been read.
read_libraries
[WARNING ODB-0229] Error: library (Nangate45_tech) already exists
[WARNING ODB-0229] Error: library (Nangate45_stdcell) already exists
[WARNING STA-0053] Nangate45/Nangate45_typ.lib line 37, library NangateOpenCellLibrary already exists.
read_verilog $synth_verilog
link_design $top_module
read_sdc $sdc_file
utl::metric "ord_version" [ord::openroad_git_describe]
# Note that sta::network_instance_count is not valid after tapcells are added.
utl::metric "instance_count" [sta::network_instance_count]
initialize_floorplan -site $site \
  -die_area $die_area \
  -core_area $core_area
[INFO IFP-0001] Added 57 rows of 422 sites.
source $tracks_file
# remove buffers inserted by synthesis
remove_buffers
[INFO RSZ-0026] Removed 0 buffers.
###############################################################
# IO Placement (random)
place_pins -random -hor_layers $io_placer_hor_layer -ver_layers $io_placer_ver_layer
Found 0 macro blocks.
```

QUEstion4. Perform Power Planning.

Answer:



RED grid is for vdd

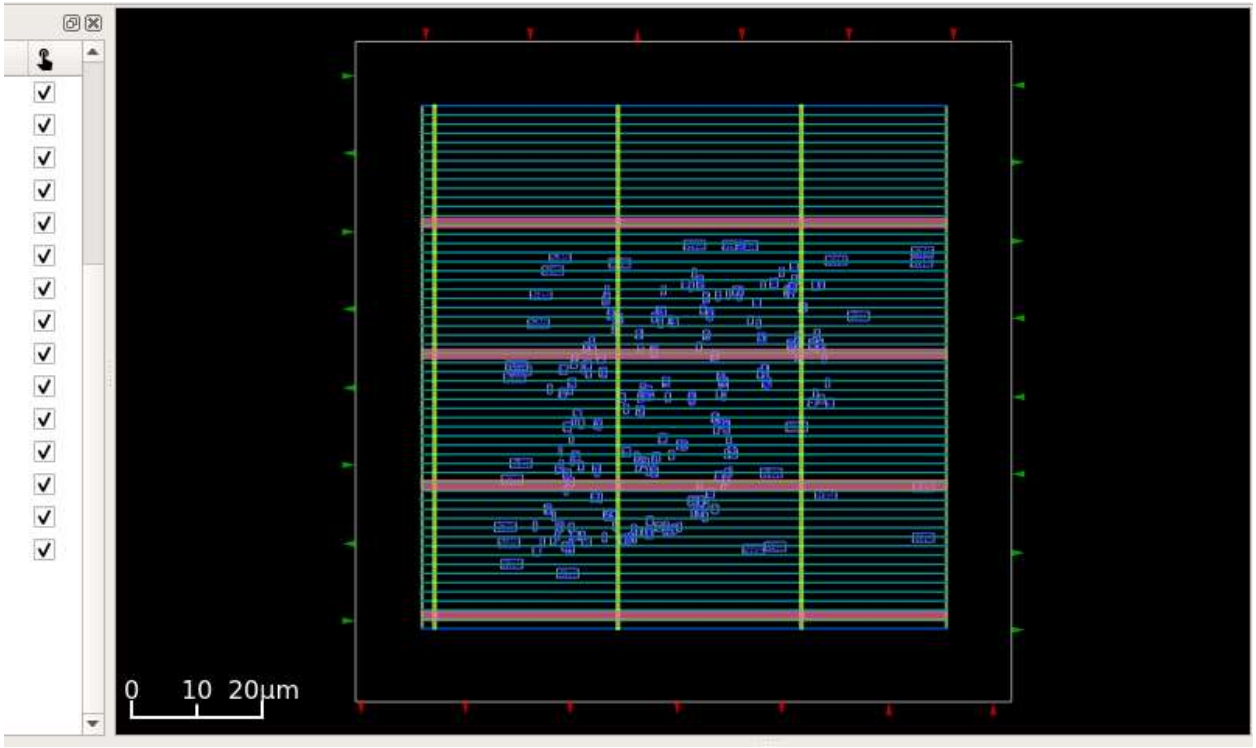


Green columns are vss rails

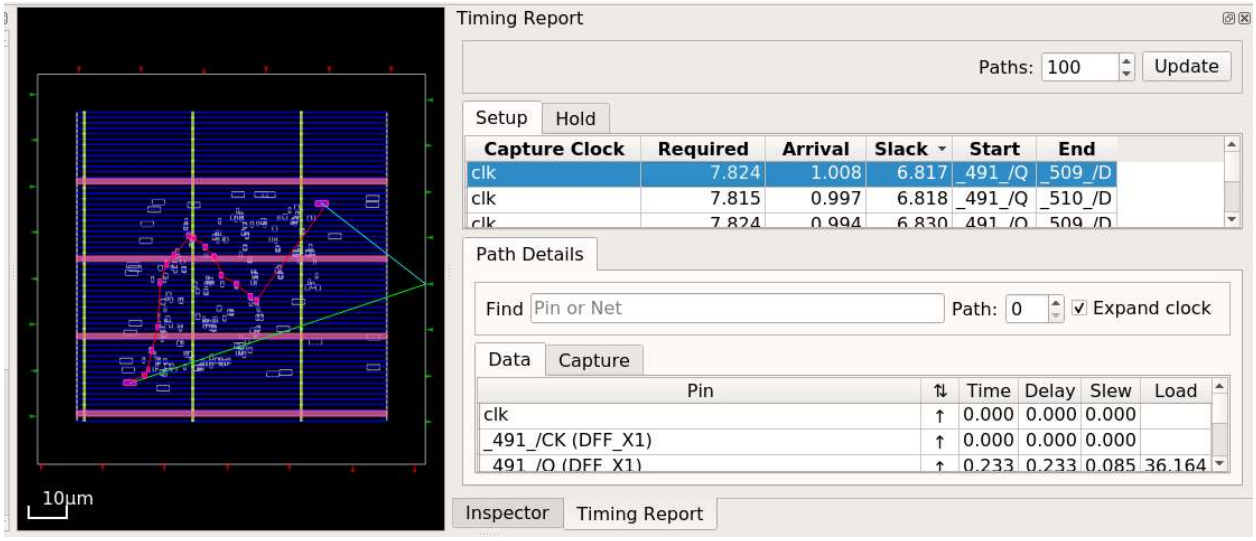
Question5: 5. Perform global placement, legalization, and detailed placement. Perform timing analysis after each step. Report the results of timing analysis.

Answer:

Global placement:

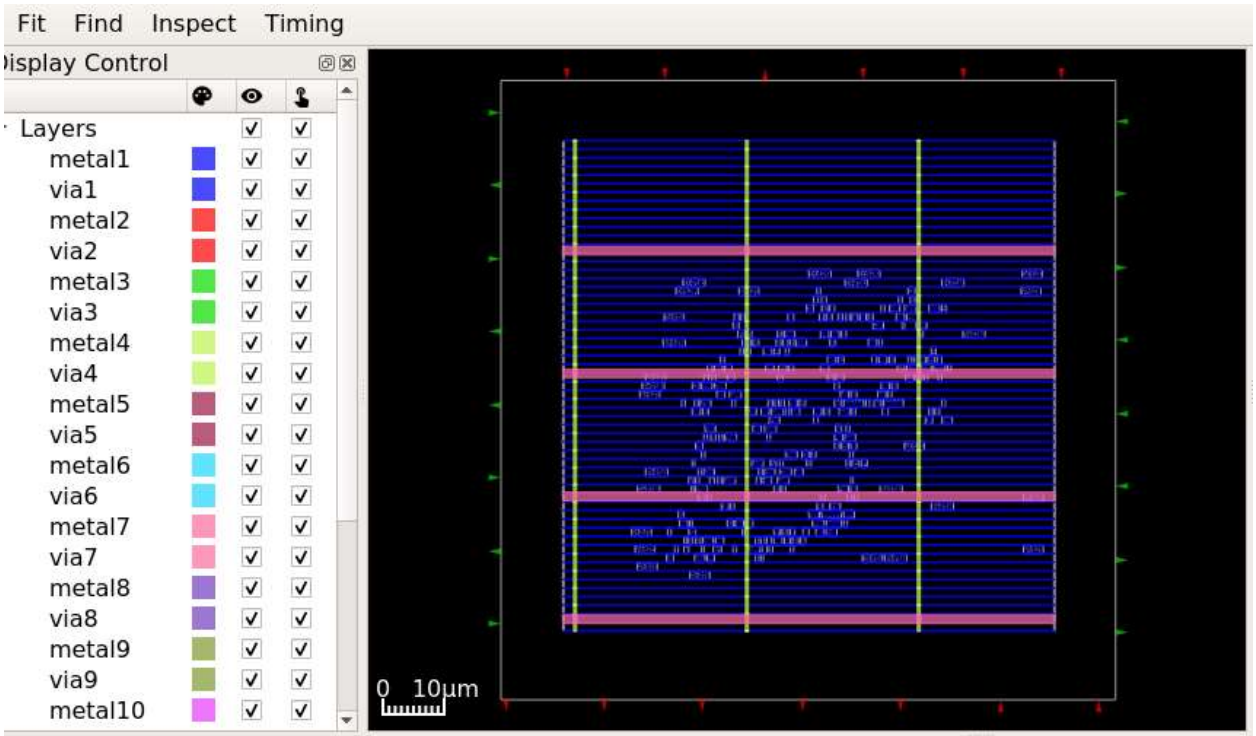


Timing Report:




```
          7.85 ^ _509_/CK (DFF_X1)
  -0.03    7.82   library setup time
           7.82   data required time
-----------------------------------------------------------
           7.82   data required time
          -1.01   data arrival time
-----------------------------------------------------------
           6.82   slack (MET)


Group                                  Slack
-------------------------------------------
clk                                   -0.06
clk                                    6.82

max slew

Pin                                    Limit    Slew   Slack
------------------------------------------------------------
_491_/Q                                 0.20    0.09    0.11 (MET)

max capacitance

Pin                                    Limit     Cap   Slack
------------------------------------------------------------
_287_/ZN                               16.02    1.94   14.09 (MET)

worst slack 6.82
```

Legalization:



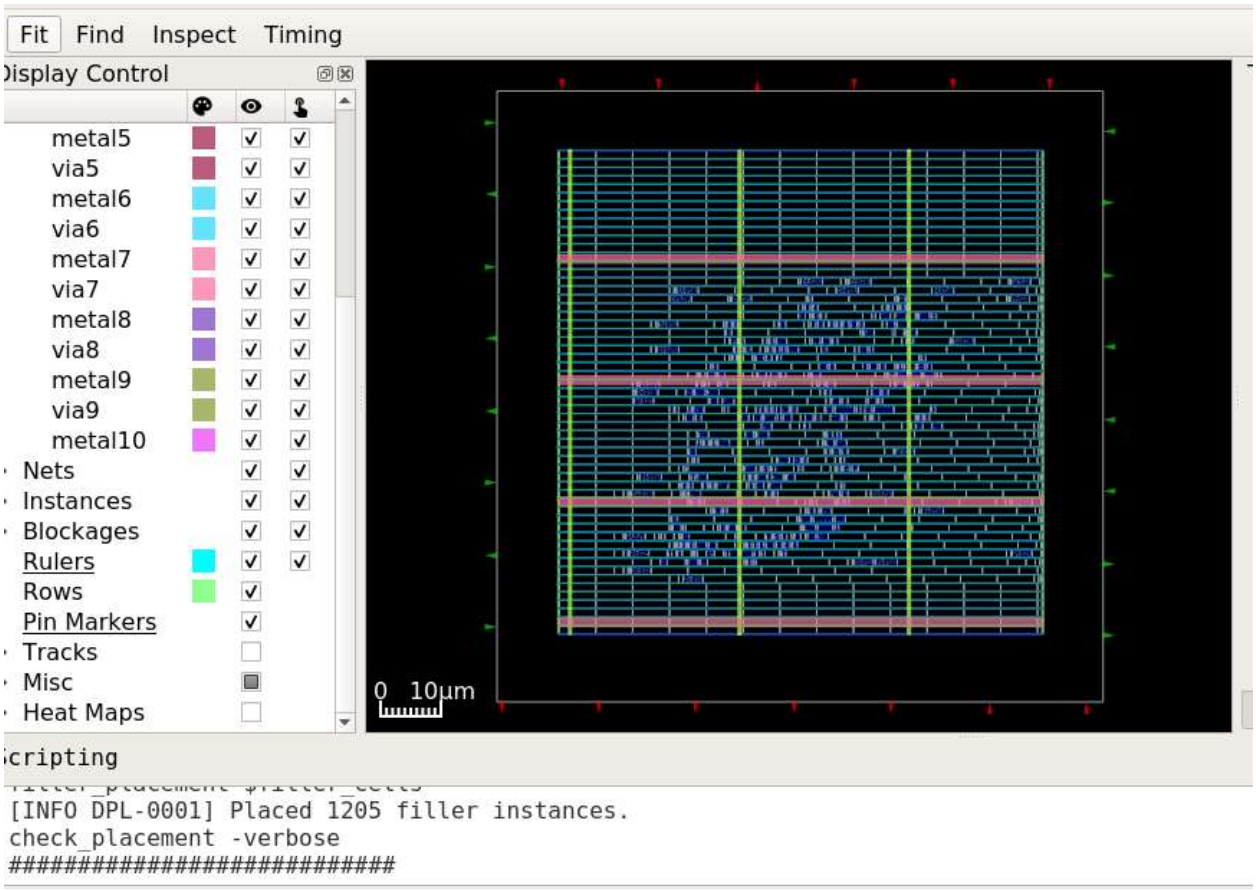
legalized HPWL 3591.1 u
delta HPWL 5 %

Report timing:

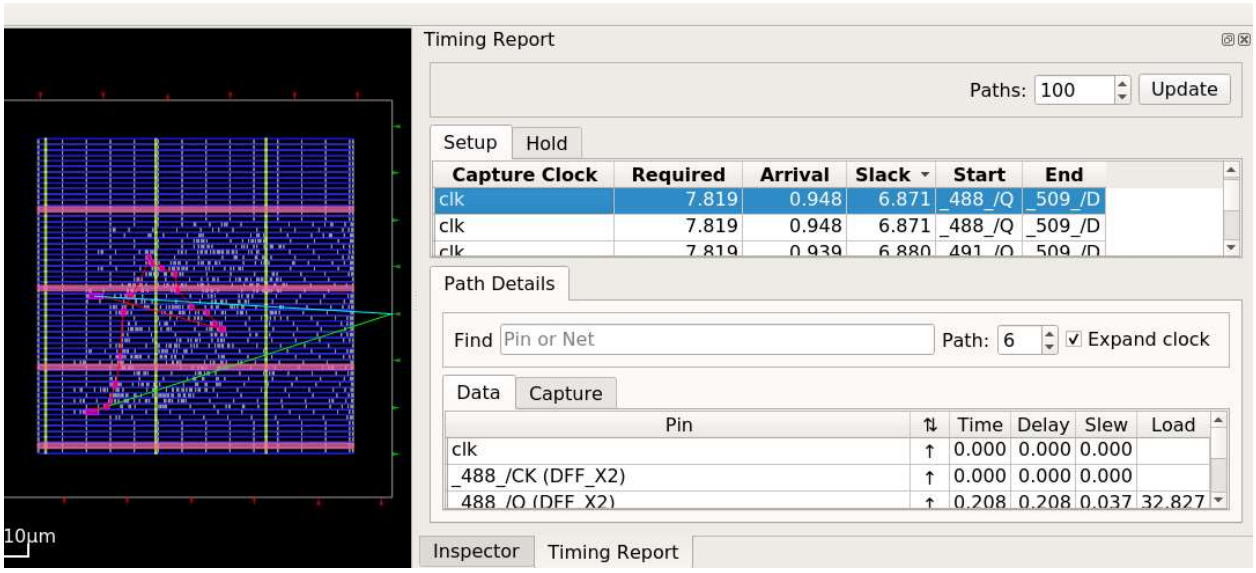
```
  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk (rise edge)
   0.05    0.05   clock network delay (ideal)
   0.00    0.05 ^ _491_/CK (DFF_X2)
   0.17    0.22 ^ _491_/Q (DFF_X2)
   0.04    0.26 v _390_/ZN (AOI22_X2)
   0.10    0.36 v _391_/ZN (OR3_X1)
   0.04    0.40 v _393_/ZN (AND3_X1)
   0.08    0.48 v _402_/ZN (OR3_X1)
   0.04    0.52 v _404_/ZN (AND3_X1)
   0.09    0.61 v _407_/ZN (OR3_X1)
   0.04    0.65 v _409_/ZN (AND3_X1)
   0.08    0.73 v _412_/ZN (OR3_X2)
   0.05    0.77 v _420_/ZN (AND3_X1)
   0.04    0.81 ^ _475_/ZN (OAI211_X2)
   0.02    0.83 v _260_/ZN (AOI21_X2)
   0.04    0.87 ^ _282_/ZN (OAI21_X1)
   0.02    0.89 v _294_/ZN (AOI21_X2)
   0.03    0.93 ^ _297_/ZN (NOR2_X1)
   0.04    0.97 ^ _303_/ZN (XNOR2_X1)
   0.00    0.97 ^ _509_/D (DFF_X1)
           0.97   data arrival time

   8.00    8.00   clock clk (rise edge)
   0.05    8.05   clock network delay (ideal)
  -0.20    7.85   clock uncertainty
   0.00    7.85   clock reconvergence pessimism
           7.85 ^ _509_/CK (DFF_X1)
  -0.03    7.82   library setup time
           7.82   data required time
---------------------------------------------------------
           7.82   data required time
          -0.97   data arrival time
---------------------------------------------------------
           6.85   slack (MET)
```

Slack increases minutely

Detailed placement:

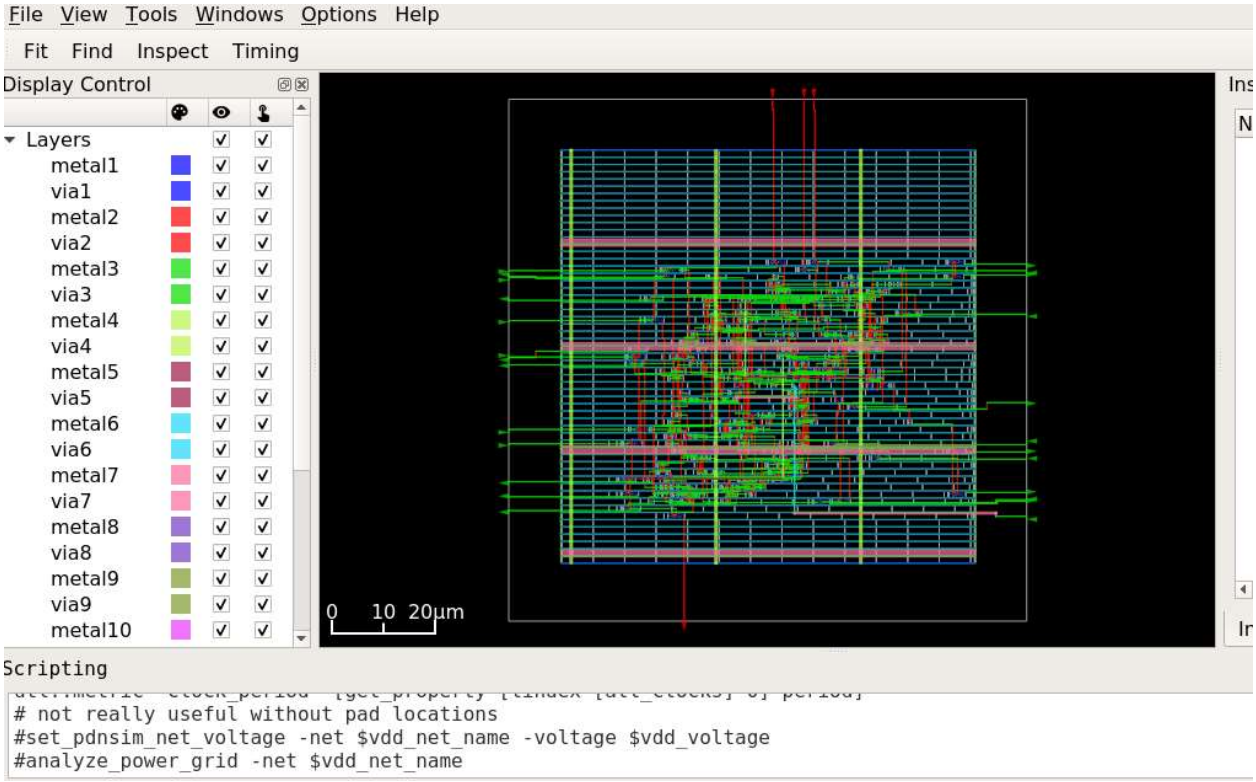


Timing



Question6: Perform Global Routing. Report the results and analyze the QOR of the design.

Answer:



Report power:

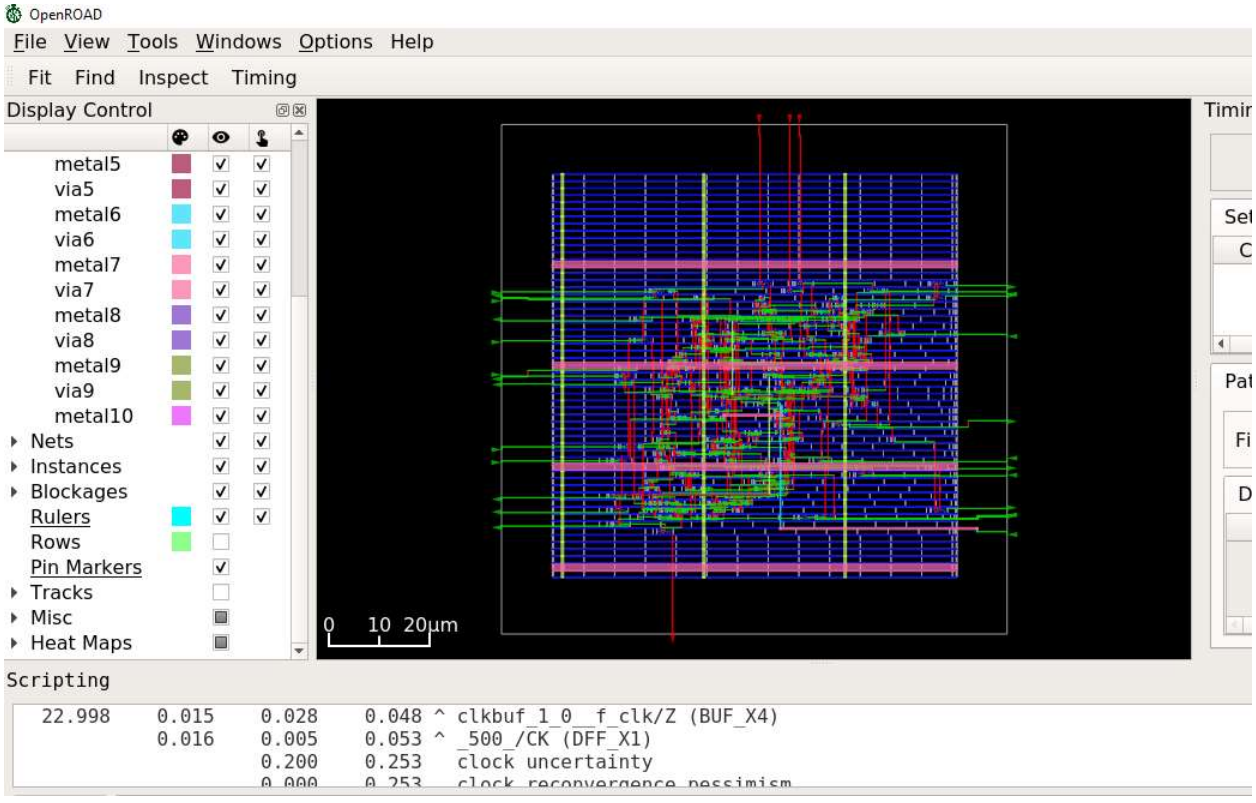
```
report_power -corner $power_corner
Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power
----------------------------------------------------------------
Sequential             1.74e-05   3.11e-06   2.72e-06   2.32e-05  33.6%
Combinational          1.71e-05   1.92e-05   9.52e-06   4.58e-05  66.4%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  3.44e-05   2.23e-05   1.22e-05   6.90e-05 100.0%
                          49.9%      32.4%      17.7%
```

Report time:

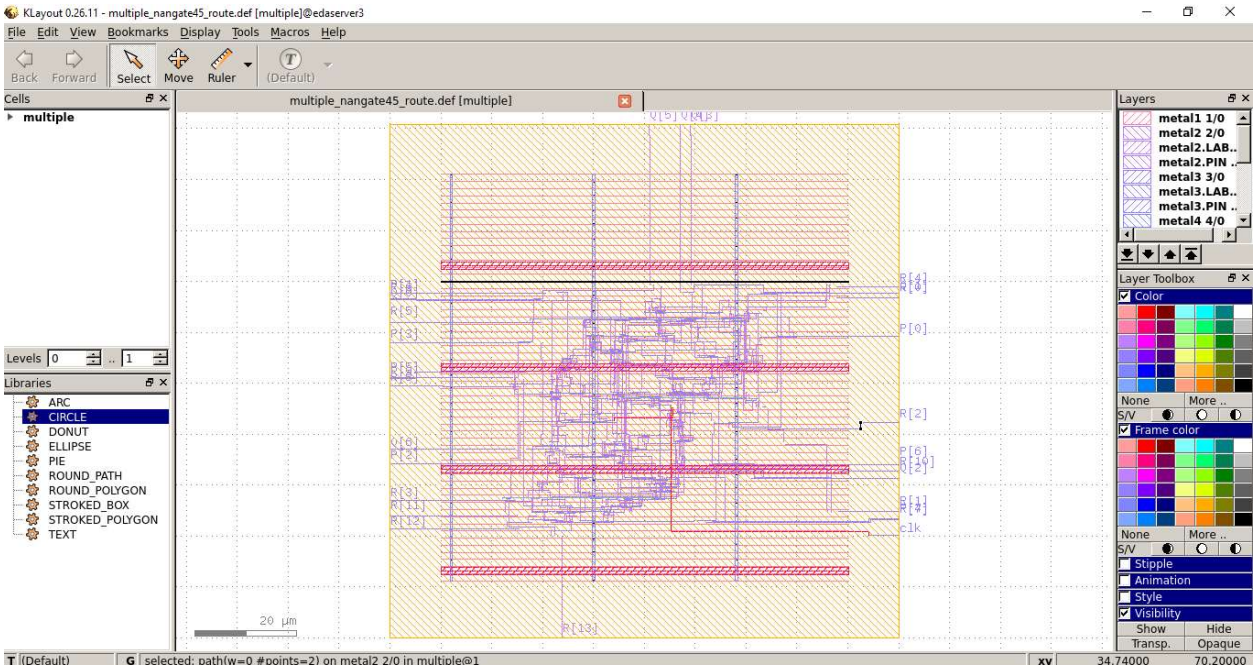
```
                              7.820   data required time
---------------------------------------------------------------------------
                              7.820   data required time
                             -0.984   data arrival time
---------------------------------------------------------------------------
                              6.835   slack (MET)


report_worst_slack -min -digits 3
worst slack 0.000
report_worst_slack -max -digits 3
worst slack 6.835
report_tns -digits 3
tns 0.000
report_check_types -max_slew -max_capacitance -max_fanout -violators -digits 3
report_clock_skew -digits 3
```

Question7: Changing the IO position

Answer : IO location type random



Klayout Report after changing IO location




```
Group                                    Slack
-------------------------------------------------
clk                                       0.00
clk                                       6.84

max slew

Pin                                     Limit    Slew   Slack
-------------------------------------------------------------
_491_/Q                                  0.20    0.05    0.15 (MET)

max capacitance

Pin                                     Limit     Cap   Slack
-------------------------------------------------------------
_287_/ZN                                16.02    3.92   12.11 (MET)
```