

VDF PROJECT REPORT

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LIBRARY USED- slow.lib (90nm)

STEP1: DETAILED SPECIFICATION OF THE PROBLEM

PROBLEM STATEMENT:

If C=8'h00 TO 8'h59, 6-bit down counter

C=8'h69 TO 8'h90, 4-bit Binary to Excess 3 Converter

C=8'hD6 TO 8'hFF, 4-bit odd parity generator

Else, A*B[9:0]

A, B, and C are input ports. A and B are data ports.

C is the control port.

Specifications :

Inputs:

Clock – clock

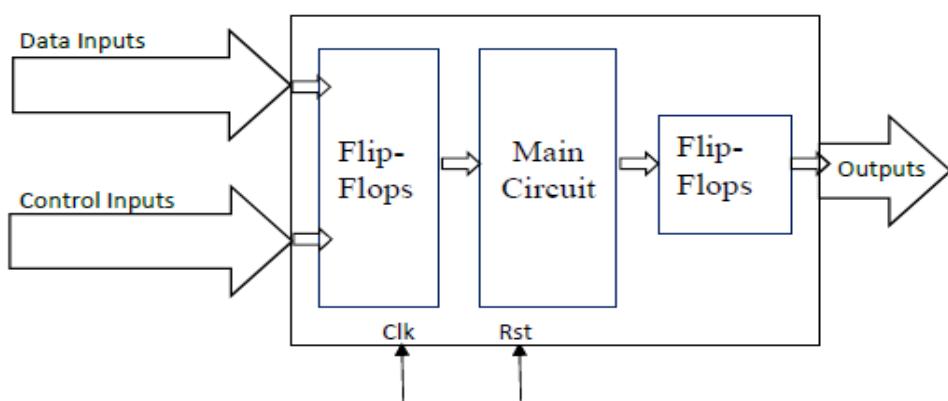
Data Inputs – A[9:0], B[9:0]

Control Input – C[7:0]

Reset – reset

Outputs:

Output – M



Modules:

- 1) **topmodule**
- 2) **controlpath**
- 3) **datapath**
- 4) **downcounter_6**

All the inputs (A, B, C) are first passed through a D flip flop and then passed through the modules. In datapath, modules generate the output in accordance with the control signal. Controlpath generates a 2-bit control signal, which selects the operation in the datapath. From the main circuit, the output is given to a D flip flop. The output of the D flip flop is declared M.

Assumptions:

Different input and output widths are used in the modules and wires are reused for multiple operations, this is done because the input and output bits of each module is different. This is done in order to save the area, that could have been used by the extra wires.

- 1) In datapath, the inputs are reset, clk, 10 bits A, B, and 2-bit control signal. The output is 20 bit M_out. The control pin selects the operation as given in the above problem statement.

Control signal[1:0]	Operation
00	6 bit down counter
01	Binary to excess3
10	4 bit Odd Parity generator
11	10 bit Multiplier

- 2) The output of the counter is given into M[5:0] and all unused bits in M are made 0.
- 3) In Binary to Excess 3, it takes the 4-bit value of A[7:4] and the output is given to M_out[7:3] and other ports are made zero.

- 4) Odd parity generator has a 4-bit input B[7:3] and output is given to M_out[0].
- 5) In the multiplication block, each input A and B is 10-bit, and the output is a 20bit value.
- 6) In the control path, The inputs are 8 bit C, clock, reset, and the output is a 2-bit control signal which is given to the datapath for operation selection.
- 7) In the top module instance datapath and controlpath are created and connected with appropriate wires. The inputs and outputs are passed into a D flipflop. It takes 2 cycles to get the output, in the first cycle the value is moved to the input_side flipflop output, then the output value is computed and in the second cycle, we get the output.

STEP 2: SIMULATION & COVERAGE ANALYSIS

Tool used for simulation: Incisive tool/NCSim

Commands used: nclaunch -new

VERILOG CODE: Top module

```

module topmodule(A,B,C,clock,reset,M);

//port declarations
input [9:0]A,B;
input [7:0]C;
input clock;
input reset;
output reg [19:0]M;
reg [9:0]A_in_side_reg,B_in_side_reg;
reg [7:0]C_in_side_reg;
wire [19:0]M_out_side_reg;

wire [1:0] ctrl_signal;
always@(posedge clock)
begin
//input side flipflop output
A_in_side_reg <= A;
B_in_side_reg <= B;
C_in_side_reg <= C;

//output side flipflop output
end

controlpath instance_controlpath(.C(C_in_side_reg),.reset(reset),.clk(clock),.control_signal(ctrl_signal));

datapath instance_datapath(.A(A_in_side_reg),.B(B_in_side_reg),.control_signal(ctrl_signal),.clk(clock),.reset
(reset),.M_out(M_out_side_reg));

//intermediate wire and reg declarations

//input and output registers
always@(posedge clock)
begin
M<= M_out_side_reg ;
end

endmodule

```

Datapath

```
controlpath.v *datapath.v *Top_module_test.v

module datapath(A,B,control_signal,clk,reset,M_out);

//port declarations
input [9:0]A, B;
input[1:0]control_signal;
input clk, reset;
output reg [19:0]M_out;

//Intermediate net and reg declarations
wire [5:0]out_counter;

|
***** 6bit down counter instantiation *****
downcounter_6 counter(.clk(clk),.reset(reset),.out(out_counter));

always@(*)
begin
    M_out = 20'b0;
    case(control_signal)
        2'b00 : begin // DownCounter6
            M_out[5:0] = out_counter;
        end

        2'b01 : begin // Binary to excess3

            case( A[7:4] )
                4'b0000 : M_out[7:4] = 4'b0011;
                4'b0001 : M_out[7:4] = 4'b0100;
                4'b0010 : M_out[7:4] = 4'b0101;
                4'b0011 : M_out[7:4] = 4'b0110;
                4'b0100 : M_out[7:4] = 4'b0111;
                4'b0101 : M_out[7:4] = 4'b1000;
                default : M_out[7:4] = 4'b0000;
            endcase
        end

        2'b10 : begin //Odd Parity generator
            M_out[0] = ~^B[7:4];
        end

        2'b11 : begin
            M_out      =  A*B;
        end
    endcase
end
endmodule
```

ControlPath

```
//  
//  
  
module controlpath(C,reset,clk,control_signal);  
  
input [7:0]C;  
input reset;  
input clk;  
output reg [1:0]control_signal;  
  
always@(posedge clk)  
begin  
    if(reset)  
        control_signal <= 2'b00;      //reset state  
  
    //6-bit down counter  
    else if (C >= 8'h00 && C <= 8'h59)  
        control_signal <= 2'b00;  
  
    // 4-bit Binary to Excess 3 Converter  
    else if (C >= 8'h69 && C <= 8'h90)  
        control_signal <= 2'b01;  
  
    //4-bit odd parity generator  
    else if (C >= 8'hD6 && C <= 8'hFF)  
        control_signal <= 2'b10;  
    |  
    //A*B operation  
    else  
        control_signal <= 2'b11;  
end  
endmodule
```

TESTBENCH 1:

```
controlpath.v × datapath.v × Top_module_test.v ×
`timescale 1ns / 1ps
module Top_module_test();

//connections
reg [9:0]A_in,B_in;
reg [7:0]C_in;
reg clk;
reg rst;
wire [19:0]M_out;
|
integer i;

//module instantiation
topmodule instance_top(.A(A_in),.B(B_in),.C(C_in),.clock(clk),.reset(rst),.M(M_out));

//initial block
initial
begin

$monitor("Time : %d\tA : %b\tB : %b\tC : %b\tM : %b",$time,A_in,B_in,C_in,M_out);

clk = 0;
rst = 1;
A_in = 10'b0;
B_in = 10'b0;
C_in = 8'b0;

//6-bit down counter test
#10 rst = 0;
#22
for(i=0;i<=89;i=i+1)
begin
#10 C_in = i;

```

```
controlpath.v × datapath.v × Top_module_test.v ×
//6-bit down counter test
#10 rst = 0;
#22
for(i=0;i<=89;i=i+1)
begin
#10 C_in = i;
end

#10 rst = 1;
#10 rst = 0;

// Binary to excess3

#10 C_in = 8'h69; A_in[7:4] = 4'b0000;
#10 C_in = 8'h7A; A_in[7:4] = 4'b0001;
#10 C_in = 8'h73; A_in[7:4] = 4'b0010;
#10 C_in = 8'h77; A_in[7:4] = 4'b0011;
#10 C_in = 8'h81; A_in[7:4] = 4'b0100;
#10 C_in = 8'h80; A_in[7:4] = 4'b0101;
#10 C_in = 8'h88; A_in[7:4] = 4'b0110;
#10 C_in = 8'h72; A_in[7:4] = 4'b0111;
#10 C_in = 8'h71; A_in[7:4] = 4'b1000;
#10 C_in = 8'h86; A_in[7:4] = 4'b1001;
#10 C_in = 8'h85; A_in[7:4] = 4'b1010;
#10 C_in = 8'h74; A_in[7:4] = 4'b1011;
#10 C_in = 8'h79; A_in[7:4] = 4'b1100;
#10 C_in = 8'h8D; A_in[7:4] = 4'b1101;
#10 C_in = 8'h83; A_in[7:4] = 4'b1110;
#10 C_in = 8'h90; A_in[7:4] = 4'b1111;
#10 C_in = 8'h74; A_in[7:4] = 4'b0000;
#10 C_in = 8'h79; A_in[7:4] = 4'b0000;

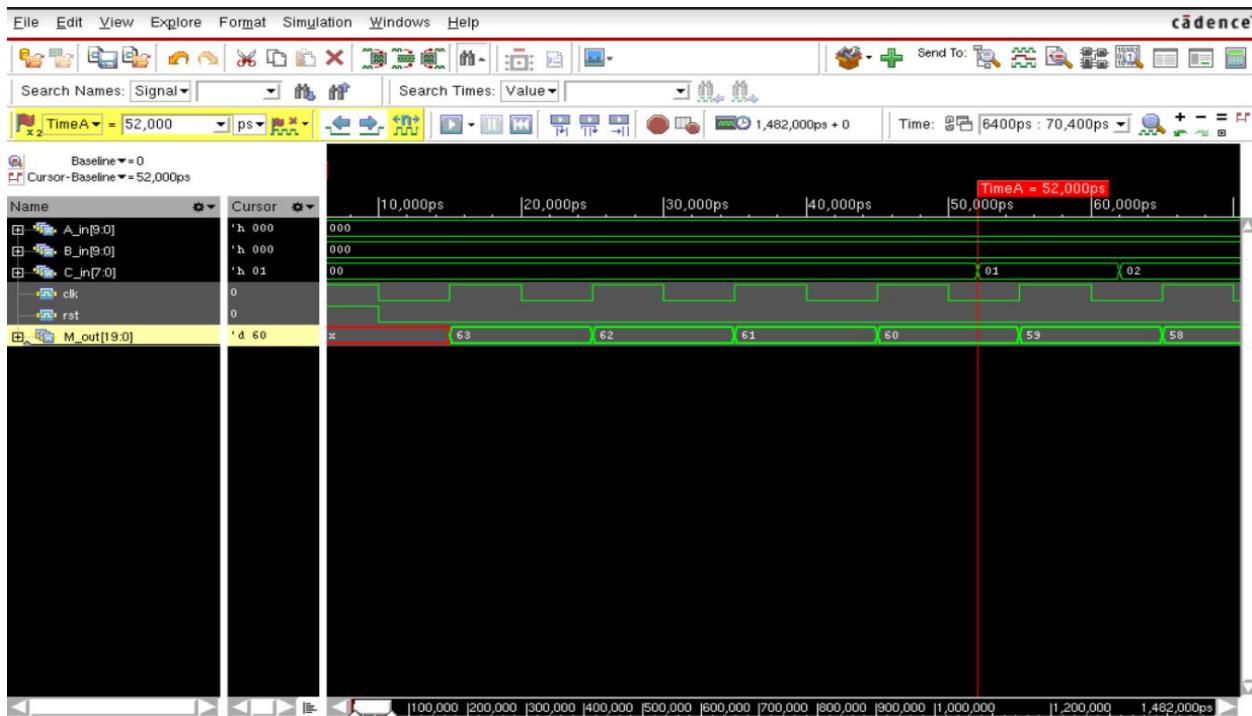
#10 rst = 1;
```

```

controlpath.v  X  datapath.v  X  *Top_module_test.v  X
#10 rst = 1;
#10 rst = 0;
A_in = 10'b0;
B_in = 10'b0;
C_in = 8'b0;
//Mul
#10 C_in = 8'h5A; B_in = 10'd24 ; A_in =10'd39;
#10 C_in = 8'h5E; B_in = 10'd105; A_in =10'd45;
#10 C_in = 8'h60; B_in = 10'd14; A_in =10'd14;
#10 C_in = 8'h62; B_in = 10'd83; A_in =10'd16;
#10 C_in = 8'h65; B_in = 10'd145; A_in =10'd114;
#10 C_in = 8'h67; B_in = 10'd64; A_in =10'd74;
#10 C_in = 8'h91; B_in = 10'd19; A_in =10'd37;
#10 C_in = 8'h93; B_in = 10'd33; A_in =10'd11;
#10 C_in = 8'hA9; B_in = 10'd74; A_in =10'd44;
#10 C_in = 8'hA4; B_in = 10'd5; A_in =10'd189;
#10 C_in = 8'hB2; B_in = 10'd85; A_in =10'd12;
#10 C_in = 8'hB7; B_in = 10'd210; A_in =10'd2;
#10 C_in = 8'hC4; B_in = 10'd345; A_in =10'd3;
#10 C_in = 8'hC3; B_in = 10'd145; A_in =10'd5;
#10 C_in = 8'hD1; B_in = 10'd1021; A_in =10'd1;
#10 C_in = 8'hD5; B_in = 10'd500; A_in =10'd2;
#10 C_in = 8'hB7; B_in = 10'd0; A_in =10'd1023;
#10 C_in = 8'hC4; B_in = 10'd1; A_in =10'd1022;
#10 C_in = 8'hC3; B_in = 10'd1023; A_in =10'd1023;
#10 C_in = 8'hD4; B_in = 10'd1000; A_in =10'd1021;
#10 C_in = 8'hD5; B_in = 10'd500; A_in =10'd265;
#10 C_in = 8'hD2; B_in = 10'd1024; A_in =10'd1023;
#10 C_in = 8'hB7; B_in = 10'd1024; A_in =10'd1043;
#20 $finish;
end
always #5 clk = ~clk; //clock
endmodule

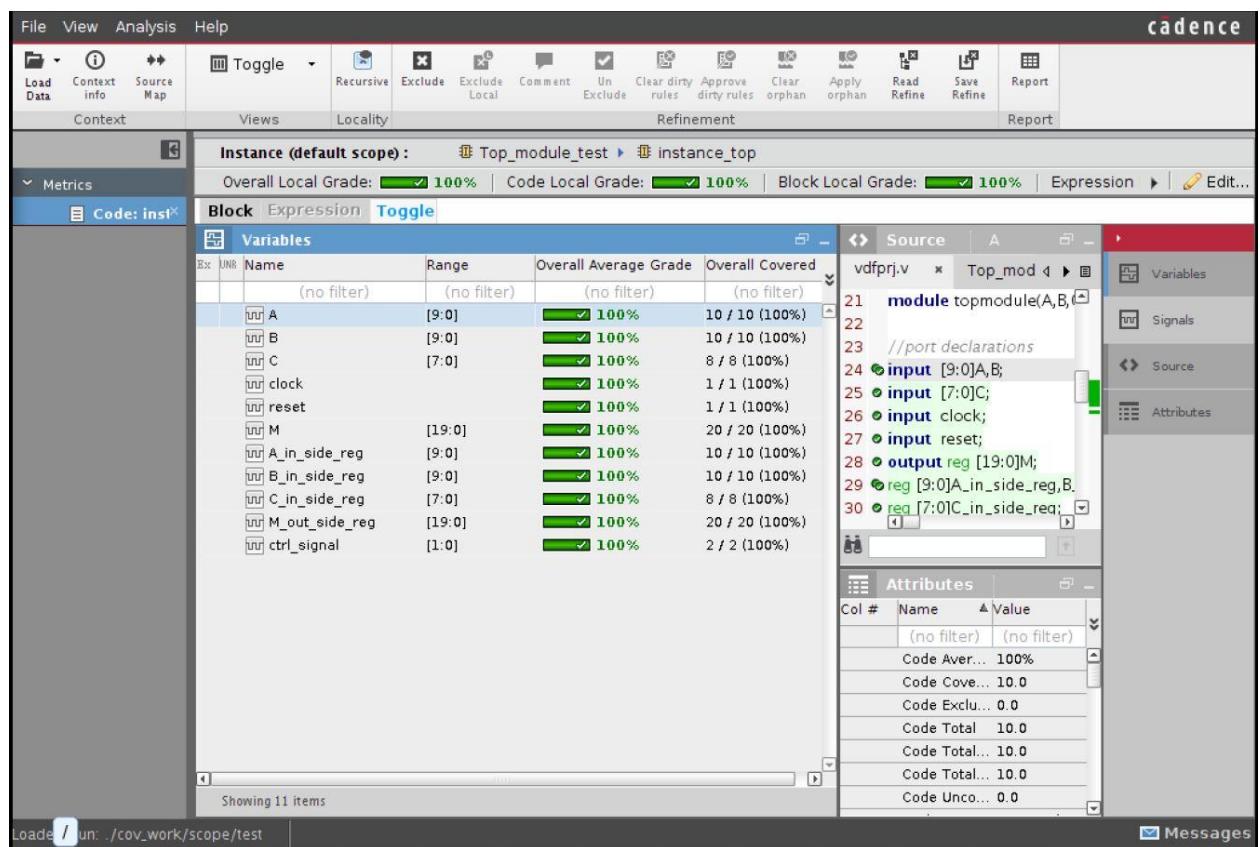
```

SIMULATION WAVEFORM 1:



CODE COVERAGE REPORT 1:

Ex UNB Name	Overall Average Grade	Overall Covered	Assertion Status Grade
Verification Metrics	98.23%	654 / 660 (99.09%)	n/a
Types	97.93%	327 / 330 (99.09%)	n/a
Top_module_test	✓ 100%	120 / 120 (100%)	n/a
topmodule	✓ 100%	102 / 102 (100%)	n/a
controlpath	92.59%	28 / 30 (93.33%)	n/a
datapath	97.06%	66 / 67 (98.51%)	n/a
downcounter_6	✓ 100%	11 / 11 (100%)	n/a
Instances	98.52%	327 / 330 (99.09%)	n/a



Overall code coverage is 99%.

Toggle coverage, in this case, is 100%.

To increase the toggle coverage to 100%, we needed to toggle M[19], M[18], which were not toggling in Testbench2. So we trigger these signals in the multiplication block, By multiplying two bigger numbers so as to trigger the MSB bits of M output.

TESTBENCH 2:

```
Top_module_test.v X
'timescale 1ns / 1ps
module Top_module_test();

//connections
reg [9:0]A_in,B_in;
reg [7:0]C_in;
reg clk;
reg rst;
wire [19:0]M_out;

integer i;

//module instantiation
topmodule instance_top(.A(A_in),.B(B_in),.C(C_in),.clock(clk),.reset(rst),.M(M_out));

//initial block
initial
begin

$monitor("Time : %d\tA : %b\tB : %b\tC : %b\tM : %b",$time,A_in,B_in,C_in,M_out);

clk = 0;
rst = 1;
A_in = 10'b00;
B_in = 10'b00;
C_in = 8'b0;

//6-bit down counter test|
#10 rst = 0;
#22
for(i=0;i<=89;i=i+1)
begin
#10 C_in = i+5;

.
.

end

#10 rst = 1;
#10 rst = 0;

// Binary to excess3

#10 C_in = 8'h69; A_in[7:4] = 4'b0000;
#10 C_in = 8'h7A; A_in[7:4] = 4'b0001;
#10 C_in = 8'h77; A_in[7:4] = 4'b0011;
#10 C_in = 8'h81; A_in[7:4] = 4'b0100;
#10 C_in = 8'h88; A_in[7:4] = 4'b0110;
#10 C_in = 8'h72; A_in[7:4] = 4'b0111;
#10 C_in = 8'h86; A_in[7:4] = 4'b1001;
#10 C_in = 8'h74; A_in[7:4] = 4'b1011;
#10 C_in = 8'h74; A_in[7:4] = 4'b0000;
#10 C_in = 8'h79; A_in[7:4] = 4'b0000;

#10 rst = 1;
#10 rst = 0;

//Odd Parity generator
#10 C_in = 8'hd6; B_in[7:4] = 4'b0000;
#10 C_in = 8'hd8; B_in[7:4] = 4'b0001;
#10 C_in = 8'hda; B_in[7:4] = 4'b0010;
#10 C_in = 8'hd7; B_in[7:4] = 4'b0011;
#10 C_in = 8'he8; B_in[7:4] = 4'b0110;
#10 C_in = 8'he2; B_in[7:4] = 4'b0111;
#10 C_in = 8'hee; B_in[7:4] = 4'b1001;
#10 C_in = 8'he5; B_in[7:4] = 4'b1010;
#10 C_in = 8'hf4; B_in[7:4] = 4'b1011;
#10 C_in = 8'hf9; B_in[7:4] = 4'b1100;
#10 C_in = 8'hf9; B_in[7:4] = 4'b1101;
```

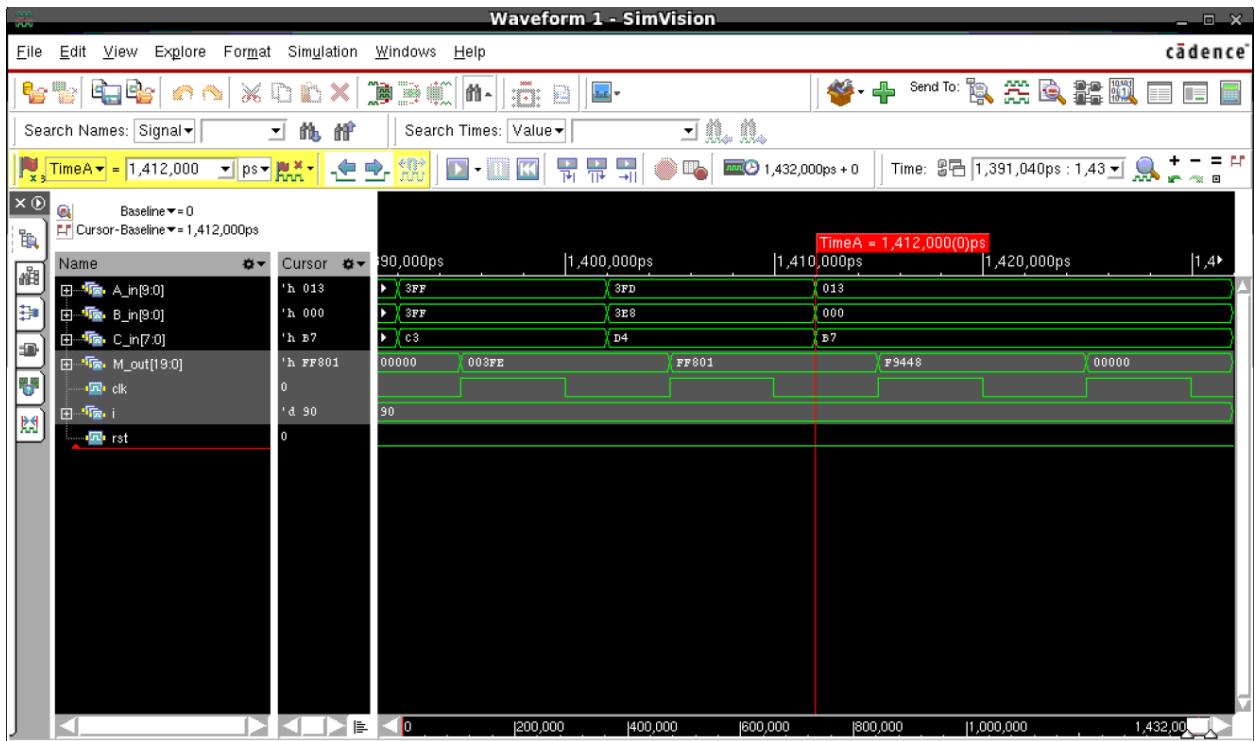
```
A_in = 10'b0;
B_in = 10'b0;
C_in = 8'b0;

//Mul
#10 C_in = 8'h5A; B_in = 10'd24 ; A_in =10'd39;
#10 C_in = 8'h60; B_in = 10'd14; A_in =10'd14;
#10 C_in = 8'h62; B_in = 10'd83; A_in =10'd16;
#10 C_in = 8'h65; B_in = 10'd145; A_in =10'd114;
#10 C_in = 8'h67; B_in = 10'd64; A_in =10'd74;
#10 C_in = 8'h91; B_in = 10'd19; A_in =10'd37;
#10 C_in = 8'h93; B_in = 10'd33; A_in =10'd11;
#10 C_in = 8'hA9; B_in = 10'd74; A_in =10'd44;
#10 C_in = 8'hA4; B_in = 10'd5; A_in =10'd189;
#10 C_in = 8'hB2; B_in = 10'd85; A_in =10'd12;
#10 C_in = 8'hB7; B_in = 10'd210; A_in =10'd2;
#10 C_in = 8'hC3; B_in = 10'd145; A_in =10'd5;
#10 C_in = 8'hD1; B_in = 10'd1021; A_in =10'd1;
#10 C_in = 8'hD5; B_in = 10'd500; A_in =10'd2;
#10 C_in = 8'hB7; B_in = 10'd0; A_in =10'd1023;
#10 C_in = 8'hC4; B_in = 10'd1; A_in =10'd1022;
#10 C_in = 8'hC3; B_in = 10'd1023; A_in =10'd1023;
#10 C_in = 8'hD4; B_in = 10'd1000; A_in =10'd1021;
#10 C_in = 8'hB7; B_in = 10'd1024; A_in =10'd1043;

#20 $finish;
end

//clock
always #5 clk = ~clk;
|  
endmodule
```

SIMULATION WAVEFORM 2:



CODE COVERAGE REPORT 2:

The screenshot displays two windows from the Cadence verification tool. The top window is titled 'Verification Hierarchy' and shows a tree view of verification metrics. The bottom window is titled 'Relative Elements' and shows a list of elements with their coverage details. Both windows use a color-coded scale for coverage percentages.

Ex	UNR	Name	Overall Average Grade	Overall Covered	Assertion Status Grade
		(no filter)	(no filter)	(no filter)	(no filter)
		Verification Metrics	96.98%	618 / 630 (98.1%)	n/a
		Types	96.17%	309 / 315 (98.1%)	n/a
		Instances	97.79%	309 / 315 (98.1%)	n/a
		Top_module_test	97.79%	309 / 315 (98.1%)	n/a
		instance_top	95.57%	204 / 210 (97.14%)	n/a
		instance_controlpath	92.59%	28 / 30 (93.33%)	n/a
		instance_datapath	94.12%	74 / 78 (94.87%)	n/a

Ex	UNR	Name	Overall Average Grade	Overall Covered	Assertion Status Grade
		(no filter)	(no filter)	(no filter)	(no filter)
		Types	96.17%	309 / 315 (98.1%)	n/a
		Instances	97.79%	309 / 315 (98.1%)	n/a

e: 88.24% | Block Local Grade: 76.47% | Expression Local Grade: n/a | Toggle Local Grade: ✓ 100% | Edit...

Block **Expression** **Toggle**

	Range	Overall Average Grade	Overall Covered
filter)	(no filter)	(no filter)	(no filter)
[9:0]	✓ 100%	10 / 10 (...	
[9:0]	✓ 100%	10 / 10 (...	
[1:0]	✓ 100%	2 / 2 (10...	
	✓ 100%	1 / 1 (10...	
	✓ 100%	1 / 1 (10...	
[19:0]	✓ 100%	20 / 20 (...	
[5:0]	✓ 100%	6 / 6 (10...	

Source A

```

controlpath.v * vdfprj.v * datapath.v *
22
23 module datapath(A,B,control_signal,clk,reset,M,
24
25 //port declarations
26 input [9:0]A, B;
27 input[1:0]control_signal;
28 input clk, reset;
29 output reg [19:0]M_out;
30
31

```

Variables **Signals** **Source** **Attributes**

Overall code coverage is 98%. Here in this case the toggle coverage is 100%, This was an improvement from testbench3 where we have 83%. Block coverage is low as some blocks were not triggered in the testbench2.

TESTBENCH 3:

```
tb_topmodule.v
```

```
module tb_topmodule();
reg clk;
reg reset;
reg [9:0] A;
reg [9:0] B;
reg [7:0] C;
wire [19:0] M;

///initialize the design
initial begin
$display($time,"<<STARTING>>");
A=0;
B=0;
C=0;
reset=1;
clk=0;
end

initial begin
#10 reset=0;
#15 A=10'b01001_10010;
B=10'b10110_01101;
C=8'h49;
#350 C=8'h80;
#10 A=10'b01011_10010;
#10 A=10'b01111_10010;
#20 C=8'hEF;
#10 B=10'b1111111111;
#10 C=8'h5B;
#30 A=10'b0000110000;
B=10'b0001100000;
#10 A=10'b1000000001;
#10 reset|=1;

#15 C=8'h71;
A=8'b11111110;
#10 A=10'b1111111111;
#10 A=10'b1100000000;
B=10'b1111111111;
C=8'b00000000;
#10 C=8'hB2;
A=10'b1000110001;
#10 B=10'b1001110011;

end

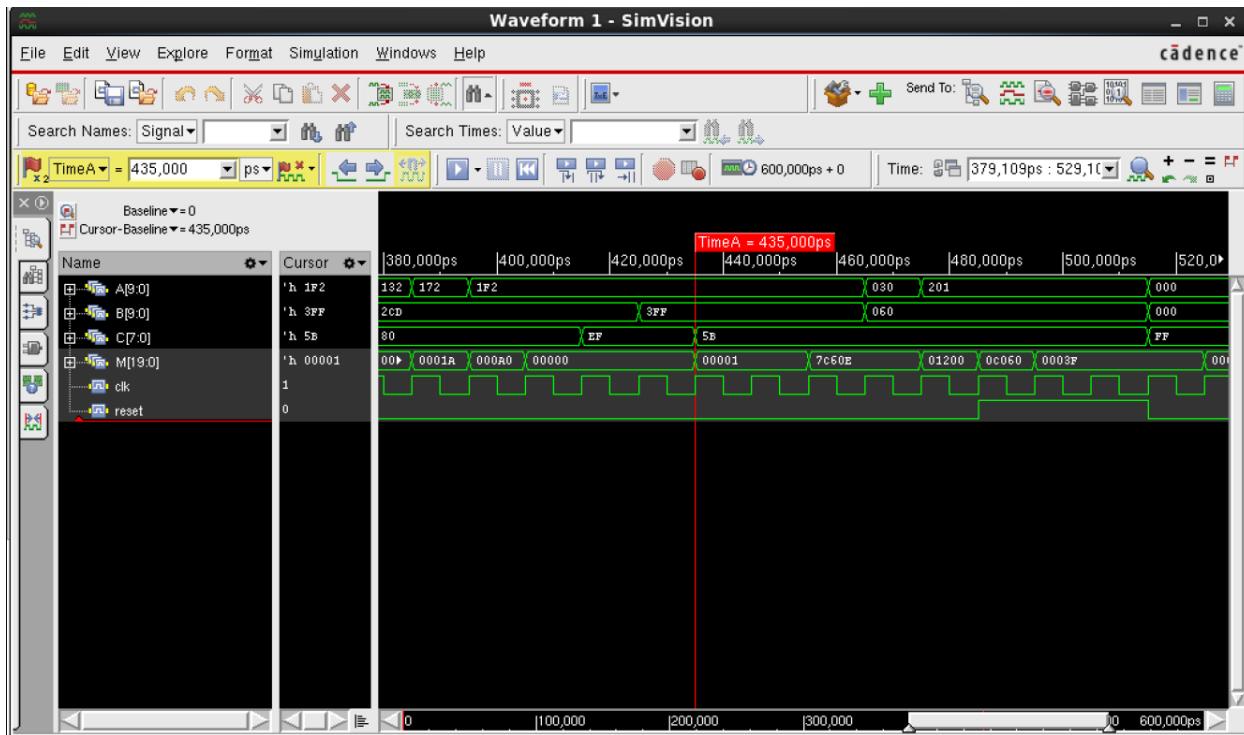
/// generate test signals
always #5 clk=~clk;

///instantiate the DUT
topmodule I1(.A(A),.B(B),.C(C),.M(M),.reset(reset),.clock(clk));

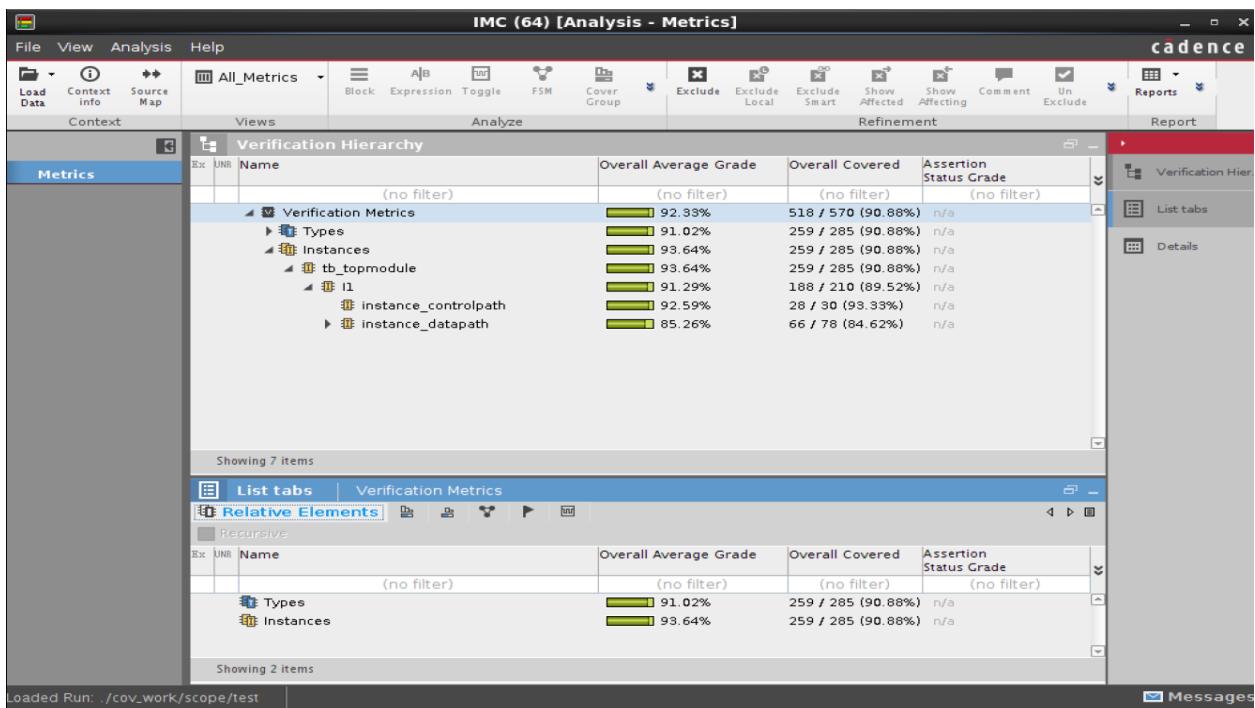
///monitor the signal and save it in a file
initial
begin
$dumpfile ("ckt.vcd");
$dumpvars;
end
initial begin
$monitor("%d,\t%b,\t%b,\t%b,\t%b,\t%b,\t%b", $time,clk,reset,A,B,C,M);
end

////end sim
initial begin
#600 $finish;
end
endmodule
```

SIMULATION WAVEFORM 3:



CODE COVERAGE REPORT 3:



Instance (default scope) : tb_topmodule		Overall Local Grade: 96%		Code Local Grade: 96%		Block Local Grade: 100%		Expression Local Grade: 100%	
		Block		Expression		Toggle			
Variables									
Ex	UNR	Name	Range	Overall	Average Grade	Overall	Covered		
		(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)		
		w clk			✓ 100%	1 / 1 (100%)			
		w reset			✓ 100%	1 / 1 (100%)			
		w A	[9:0]		✓ 100%	10 / 10 (100%)			
		w B	[9:0]		✓ 100%	10 / 10 (100%)			
		w C	[7:0]		✓ 100%	8 / 8 (100%)			
		w M	[19:0]		80%	16 / 20 (80%)			

Overall code coverage is 90.88%.

Block coverage is 100%

Toggle coverage is 83%. Here M[19], M[18], M[17] and M[16] did not toggle,i.e.
Go from 1->0 and 0->1. This was increased in testbench1.

ANALYSIS OF THE RESULTS:

TESTBENCH	TOTAL COVERAGE (%)
Testbench - 3	90.8
Testbench - 2	98
Testbench - 1	99

1. Coverage report measures the quality of test benches and models. One can understand how the RTL source code has been exercised by the testbench So by optimizing the testvectors we achieved a total coverage of 99%.
2. In coverage report analysis we studied the effect of the block, expression, and toggle coverage. Line coverage was made to be 100%.
3. In TEST BENCH 3, 83% toggle coverage was observed. To improve this we had to toggle M[18], M[19], M[17], and M[16] bits of the output. The multiplier was used to assert these bits. This resulted in 100% toggle coverage.
4. In TEST BENCH 2, The block coverage is 76% and toggle coverage is 100%. To improve the block coverage we used multiple test vectors to trigger different blocks(case, if-else) in the code.
5. In TEST BENCH 1, The total coverage is 99%. The block coverage improved in this case. This resulted in improving the coverage report.

STEP3: RTL SYNTHESIS

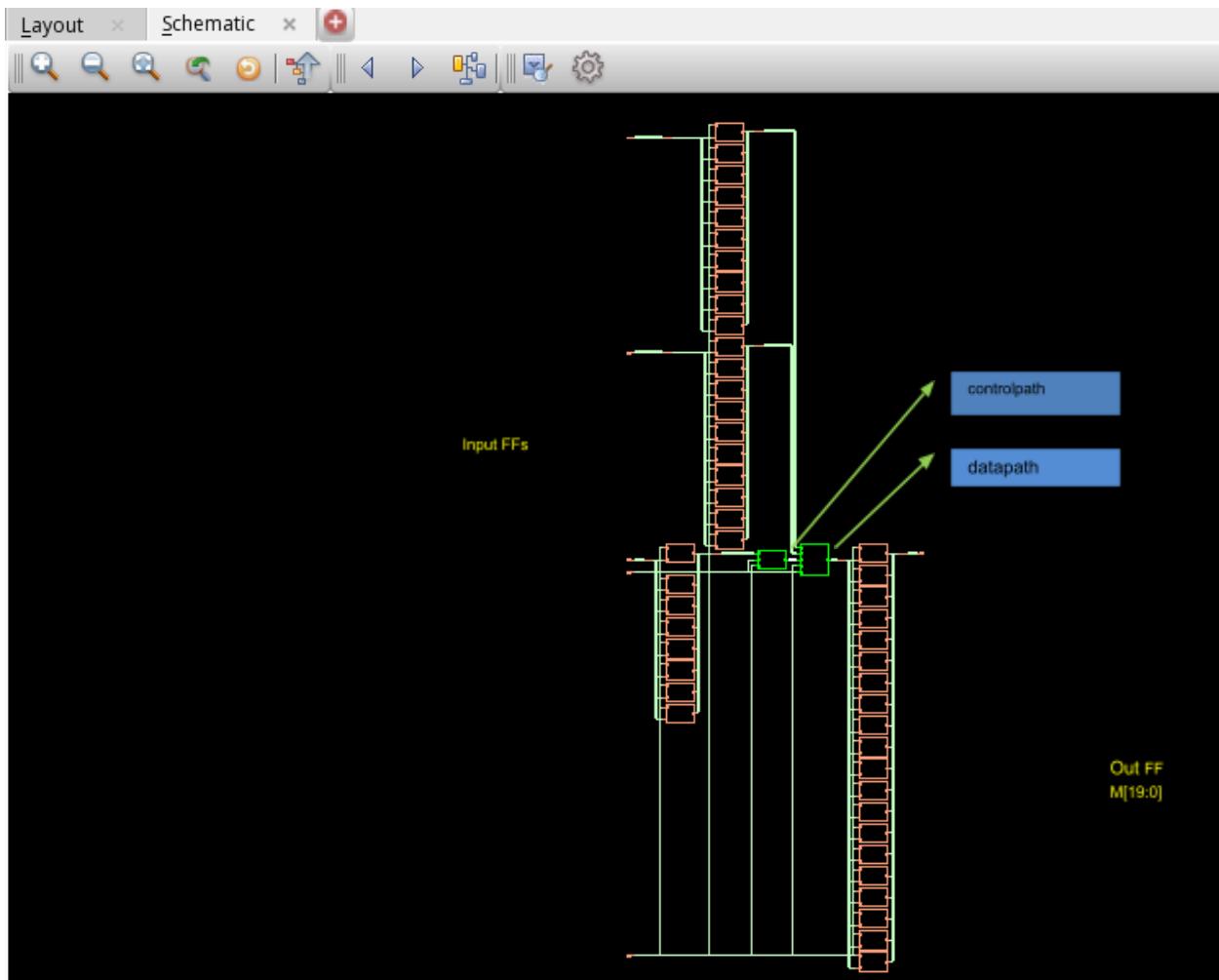
Tool used: Genus

Command: genus –legacy_ui

After synthesis outcomes generated: Cell report, total required area, power, and timing summary, and corresponding netlist.v (considering slow.lib Library, As each library has predefined time and area for particular gates and instances)

A. Synthesize for the minimum area, keeping timing constraints highly relaxed.

Schematic



Constraint: Constraints are given to clock input and output ports. This is done to used to specify the design intent, including timing, power and area constraints for a design.

Here we can see the set_wire_load_model command used to specify the wire load model. As there were no wire load model in 90nm slow.lib library we used the wireload model of the tsmc 180nm library for analysis purpose.

Cell report(considering area)

Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
 Generated on: Apr 07 2022 01:23:54 pm
 Module: topmodule
 Technology library: slow
 Operating conditions: slow (balanced_tree)
 Wireload mode: enclosed
 Area mode: timing library

Tool, topmodule and library information header

Gate	Instances	Area	Library
ADDFX1	19	373.909	slow
ADDFXL	60	1180.764	slow
AND2X1	4	18.166	slow
A021X1	1	6.812	slow
A022XL	3	22.707	slow
AOI211X1	2	10.597	slow
AOI21X1	10	45.414	slow
AOI21XL	2	9.083	slow
AOI221X1	1	7.569	slow
AOI22X1	1	6.055	slow
AOI32X1	1	6.812	slow
CLKINVX1	6	13.624	slow
CLKXR2X1	4	33.304	slow
DFFHQX8	20	499.554	slow
DFFQX1	36	572.216	slow
INVX1	29	65.850	slow
INVXL	4	9.083	slow
MXI2XL	2	12.110	slow
NAND2BX1	1	4.541	slow
NAND2XL	108	326.981	slow
NAND3BX1	1	6.055	slow
NAND3XL	1	4.541	slow

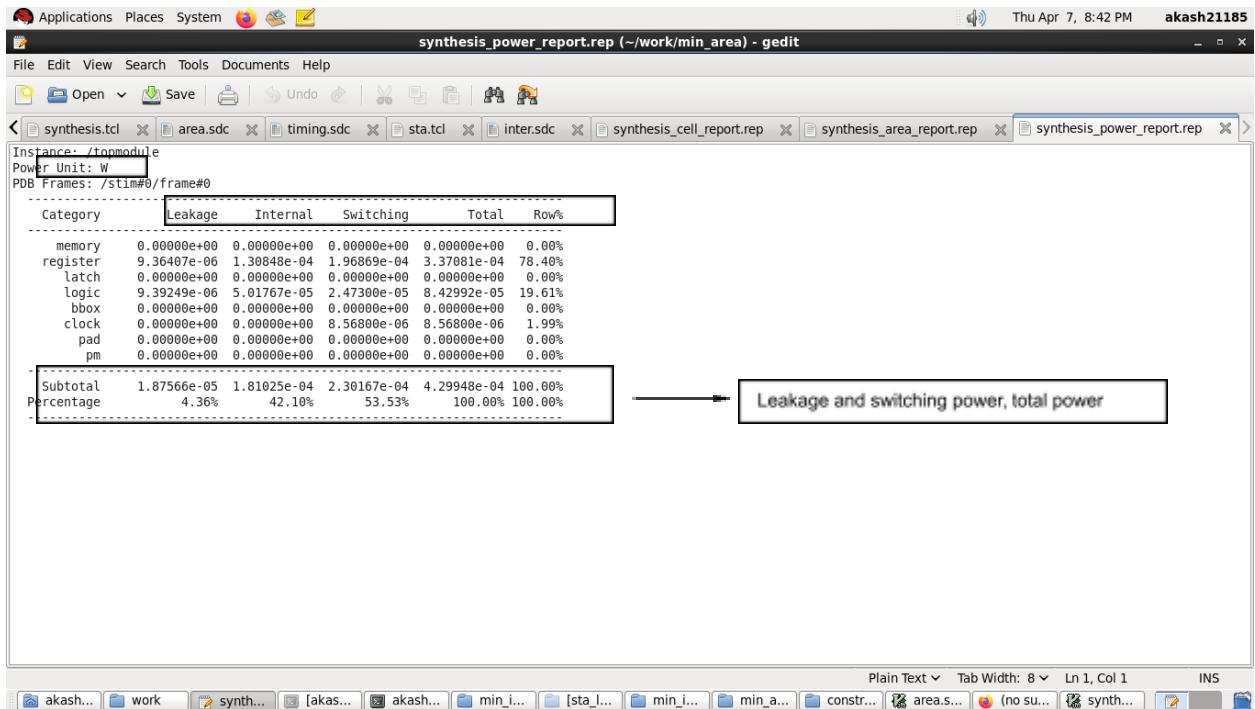
Gates,instances and their area with slow library

Type	Instances	Area	Area %
sequential	56	1071.770	30.7
inverter	39	88.557	2.5
logic	276	2333.523	66.8
physical_cells	0	0.000	0.0
total	371	3493.850	100.0

Combination and sequential area separately

Here we analyzed the area of each of the gates. The complete area for all the cells is added up and the results as shown. And it can also be observed what the no of instances and percentage of sequential circuits are there and what percent of combinational circuits are present.

Power report:



synthesis_power_report.rep (~/work/min_area) - gedit

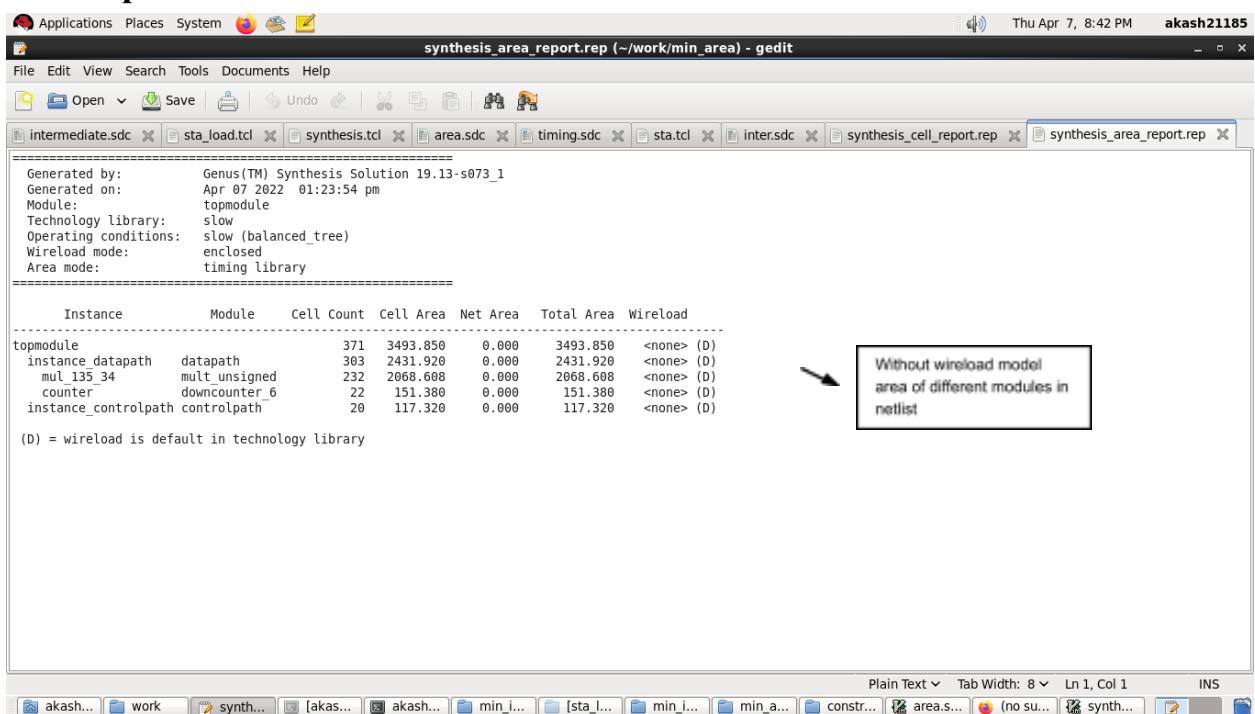
File Edit View Search Tools Documents Help

Instance: /topmodule
Power Unit: W
PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	9.36407e-06	1.30848e-04	1.96869e-04	3.37081e-04	78.40%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	9.39249e-06	5.01767e-05	2.47300e-05	8.42992e-05	19.61%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	8.56800e-06	8.56800e-06	1.99%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	1.87566e-05	1.81025e-04	2.30167e-04	4.29948e-04	100.00%
Percentage	4.36%	42.10%	53.53%	100.00%	100.00%

Leakage and switching power, total power

Area report:



synthesis_area_report.rep (~/work/min_area) - gedit

File Edit View Search Tools Documents Help

Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 07 2022 01:23:54 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library

Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload
topmodule		371	3493.850	0.000	3493.850	<none> (D)
instance datapath	datapath	303	2431.920	0.000	2431.920	<none> (D)
mul_135_34	mult_unsigned	232	2068.608	0.000	2068.608	<none> (D)
counter	downcounter_6	22	151.380	0.000	151.380	<none> (D)
instance controlpath	controlpath	20	117.320	0.000	117.320	<none> (D)

(D) = wireload is default in technology library

Without wireload model
area of different modules in netlist

Timing Reports:

Thu Apr 7, 8:47 PM akash21185

synthesis_timing_report.rep (~/work/min_area) - gedit

File Edit View Search Tools Documents Help

Open Save Undo Redo Cut Copy Paste Find Replace Select All

timing.sdc sta.tcl inter.sdc synthesis_cell_report.rep synthesis_area_report.rep synthesis_power_report.rep synthesis_timing_report.rep

```
=====
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 07 2022 01:23:53 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====
```

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)
(clock clock)	launch latency			+10	10 R	
B_in_side_reg[0]/CK	DFFQX1	10	17.0	157	+343	353 R
instance datapath/B[0]						
mul_135_34/B[0]						
g2481/B	NAND2XL	2	5.2	156	+147	499 F
g2481/Y					+0	499
g2464/B	XNOR2X1	1	4.9	77	+241	740 R
g2464/Y					+0	740
g2447/CI	ADDFXL	1	2.7	88	+314	1054 F
g2447/S					+0	1054
g2429/A	INVX1	1	6.7	72	+79	1134 R
g2429/Y					+0	1134
g2400/A	ADDFX1	1	2.7	76	+213	1347 R
g2400/C0					+0	1347
g2399/A	INVX1	1	4.9	52	+55	1402 F
g2399/Y					+0	1402
g2390/CI	ADDFX1	1	4.9	96	+238	1640 F
g2390/C0					+0	1640

Launching and latency

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akash... work synth... [akas... akash... min_i... sta_i... min_i... min_a... constr... area.s... (no su... synth...]

Thu Apr 7, 8:47 PM akash21185

synthesis_timing_report.rep (~/work/min_area) - gedit

File Edit View Search Tools Documents Help

Open Save Undo Redo Cut Copy Paste Find Replace Select All

timing.sdc sta.tcl inter.sdc synthesis_cell_report.rep synthesis_area_report.rep synthesis_power_report.rep synthesis_timing_report.rep

```
=====
g2362/C0 ADDFX1 1 4.9 96 +250 3389 F
g2366/CI ADDFX1 1 4.9 96 +250 3369 F
g2366/C0 ADDFX1 1 4.9 96 +250 3639 F
g2358/CI ADDFX1 1 4.9 96 +250 3889 F
g2358/C0 ADDFX1 1 4.9 96 +250 3889 F
g2356/CI ADDFX1 1 4.9 96 +250 4139 F
g2354/CI ADDFX1 1 4.9 96 +250 4389 F
g2354/C0 ADDFX1 1 4.9 96 +250 4389 F
g2352/CI ADDFX1 1 4.9 96 +250 4639 F
g2352/C0 ADDFX1 1 4.9 96 +250 4639 F
g2350/CI ADDFX1 1 4.9 96 +250 4889 F
g2350/C0 ADDFX1 1 4.9 96 +250 4889 F
g2348/CI ADDFX1 1 1.6 73 +229 5117 F
g2348/S ADDFXL 1 1.6 73 +229 5117 F
g2346/A ADDFXL 1 1.7 45 +54 5171 R
g2346/Y INVXL 1 1.7 45 +54 5171 R
mul_135_34/Z[18]
g751/AN NOR2BX1 1 2.3 216 +116 5286 R
g751/Y
instance datapath/M_out[18] NOR2BX1 1 2.3 216 +116 5286 R
M_reg[18]/D <<< DFFHQX8 10 +189 5476 R
M_reg[18]/CK setup 10 +189 5476 R
(capture 9000 R
latency 9010 R
uncertainty -20 8990 R
=====
Cost Group : 'clock' (path_group 'clock')
Timing slack : 3514ps
Start-point : B_in_side_reg[0]/CK
End-point : M_reg[18]/D

```

Latency and uncertainty given in area.SDC file where all the measurements are

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akash... work synth... [akas... akash... min_i... sta_i... min_i... min_a... constr... area.s... (no su... synth...]

Analysis of result: Minimum Area

Load = 1 pf			
Time Period	Area (um2)	Slack (ps)	Power
4	3773	0	1.01mW
5	3534	12	766uW
6	3488	539	627uW
7	3490	1514	541uW
8	3492	2540	473uW
9	3493	3514	429uW
10	3493	4514	388uW
15	3493	9514	265uW

After the clock period area gets minimized and no significant change is observed with the increase of the time period of clock.

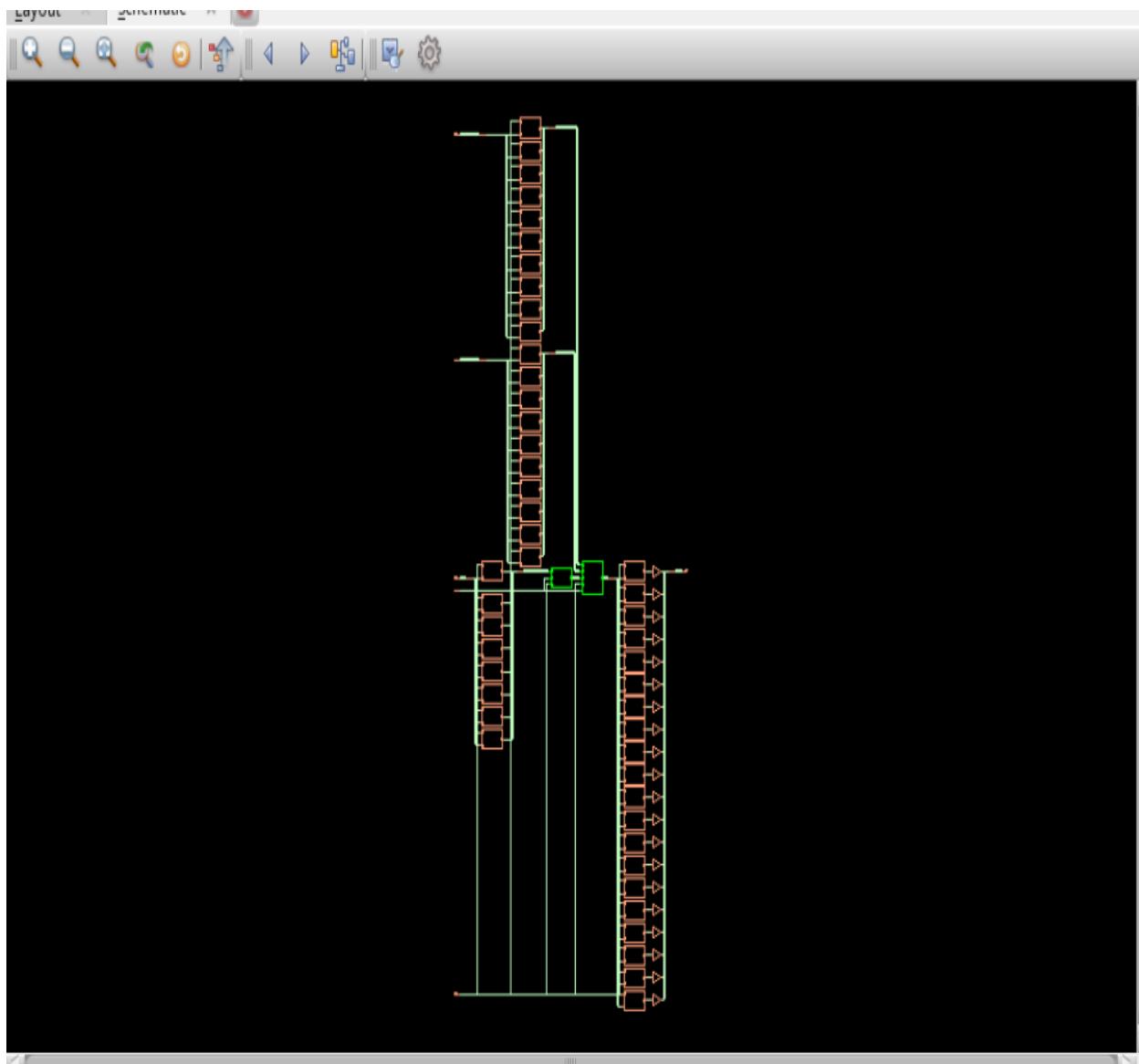
From the above table, we can analyze that as long as we are increasing our time period area reduces significantly but after a certain time period (9ns in our case) further reduction of design area is stopped and it becomes almost constant. Another observation is made that while increasing the clock period power absorption is also diminishing.

Points to ponder:

- a.when we provide sufficient large time period tool is utilizing those instances and gates that have less area irrespective of that's a delay.
- b. With the increment in clock period frequency will be reduced and so of power switching power and leakage power.

B. Keep making the timing constraints tighter unless you observe a negative slack. The timing analysis should show slight negative slack for this constraint.

Schematic



Constraint:

The screenshot shows a Gedit window titled "timing.sdc (~/constraints_2) - gedit". The window contains an SDC script for timing constraints. The script includes commands for creating a clock, setting clock uncertainty, loading models, and specifying input and output delays. It also includes a comment for failed commands.

```
create_clock -name clock -period 3.185 [get_ports "clock"]

set_clock_uncertainty 0.1 [get_clocks "clock"]
#set_wire_load_model -name tsmc18_wl10 -lib slow
set_input_delay -max 0.5 [all_inputs] -clock [get_clocks "clock"]
set_input_delay -min 0.1 [all_inputs] -clock [get_clocks "clock"]
set_clock_transition -rise 0.01 [get_clocks "clock"]
set_clock_transition -fall 0.01 [get_clocks "clock"]
set_load 7.7 [get_ports "M"]
set_input_transition 0.001 [all_inputs]
set_external_delay -clock clock 0.1 [all_inputs]
set_external_delay -clock clock 0.1 [all_outputs]
set_output_delay -clock clock -max 0.5 [all_outputs]
set_output_delay -clock clock -min 0.1 [all_outputs]
# $::dc::sdc_failed_commands
```

Area report:

Applications Places System Thu Apr 7, 9:08 PM akash21185

File Edit View Search Tools Documents Help

Undo

synthesis_area_report.rep (~/work/min_timing) - gedit

synthesis_area_report.rep synthesis_cell_report.rep synthesis_power_report.rep synthesis_timing_report.rep

```
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 07 2022 01:39:08 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
```

Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload
topmodule		615	4542.914	0.000	4542.914	<none> (D)
instance_datapath	datapath	528	3042.738	0.000	3042.738	<none> (D)
mul_135_34	mult_unsigned	460	2680.183	0.000	2680.183	<none> (D)
counter_	downcounter_6	22	151.380	0.000	151.380	<none> (D)
instance_controlpath	controlpath_	19	112.778	0.000	112.778	<none> (D)

(D) = wireload is default in technology library

Cell Report:

```
Applications Places System synthesis_cell_report.rep (~/work/min_timing) - gedit
Thu Apr 7, 9:07 PM akash21185
File Edit View Search Tools Documents Help
Open Save Undo Redo Copy Paste Find Select All
synthesis_area_report.rep synthesis_cell_report.rep synthesis_power_report.rep synthesis_timing_report.rep
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 07 2022 01:39:08 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
WireLoad mode: enclosed
Area mode: timing library
=====
Gate Instances Area Library
-----
ADDFHX1 6 127.159 slow
ADDHXL 4 84.773 slow
ADDFX1 7 137.756 slow
ADDFXL 14 275.512 slow
AND2X1 11 49.955 slow
AND2XL 4 18.166 slow
A021X1 2 13.624 slow
A022XL 3 22.707 slow
A0I211X1 2 10.597 slow
A0I21X1 25 113.535 slow
A0I21X2 1 8.326 slow
A0I21XL 11 49.955 slow
A0I22XL 1 6.055 slow
A0I2BB1X1 12 72.662 slow
A0I2BB1X2 1 8.326 slow
A0I31X2 1 9.840 slow
A0I32X1 2 13.624 slow
A0I33XL 1 7.569 slow
BUFX20 20 514.692 slow
BUFX3 1 6.055 slow
-----
Plain Text Tab Width: 8 Ln 73, Col 40 INS
akas... work [aka... akas... min... [sta... min... const... area... Sent... synt... min... synt... Docu...
synthesis_cell_report.rep (~/work/min_timing) - gedit
Thu Apr 7, 9:08 PM akash21185
File Edit View Search Tools Documents Help
Open Save Undo Redo Copy Paste Find Select All
synthesis_area_report.rep synthesis_cell_report.rep synthesis_power_report.rep synthesis_timing_report.rep
OAI211XL 2 10.597 slow
OAI21X1 11 49.955 slow
OAI21X2 4 33.304 slow
OAI21XL 4 18.166 slow
OAI22X2 1 9.840 slow
OAI2BB1X1 4 21.193 slow
OAI2BB1X2 1 7.569 slow
OAI2BB1XL 6 31.790 slow |
OAI32X1 2 13.624 slow
OR2X1 5 22.707 slow
OR2X4 2 16.652 slow
OR2XL 1 4.541 slow
XNOR2X1 10 83.259 slow
XNOR2X2 1 10.597 slow
XNOR2XL 13 108.237 slow
XNOR3X1 1 22.707 slow
XOR2XL 3 24.978 slow
XOR3X1 4 90.828 slow
-----
total 615 4542.914
-----
Type Instances Area Area %
-----
sequential 56 999.865 22.0
inverter 73 174.844 3.8
buffer 22 535.128 11.8
logic 464 2833.077 62.4
physical_cells 0 0.000 0.0
-----
total 615 4542.914 100.0
Plain Text Tab Width: 8 Ln 73, Col 40 INS
akas... work [aka... akas... min... [sta... min... const... area... Sent... synt... min... synt... Docu...

```

Power Report:

synthesis_power_report.rep (~/work/min_timing) - gedit

Thu Apr 7, 9:07 PM akash21185

File Edit View Search Tools Documents Help

Open Save Undo | Cut Copy Paste Find Replace |

synthesis_area_report.rep synthesis_cell_report.rep synthesis_power_report.rep synthesis_timing_report.rep

Instance: /topmodule
Power Unit: W
PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	7.67281e-06	3.35168e-04	2.14642e-05	3.64304e-04	8.11%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	2.23344e-05	3.24155e-04	3.75975e-03	4.10624e-03	91.38%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	2.32192e-05	2.32192e-05	0.52%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	3.00064e-05	6.59323e-04	3.80443e-03	4.49376e-03	100.01%
Percentage	0.67%	14.67%	84.66%	100.00%	100.00%

Plain Text ▾ Tab Width: 8 ▾ Ln 1, Col 1 INS

akas... work aka... akas... min... sta... min... const... area... Sent... synt... min... synt... Docu... INS

Timing report:

```
=====
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 07 2022 01:39:07 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====
```

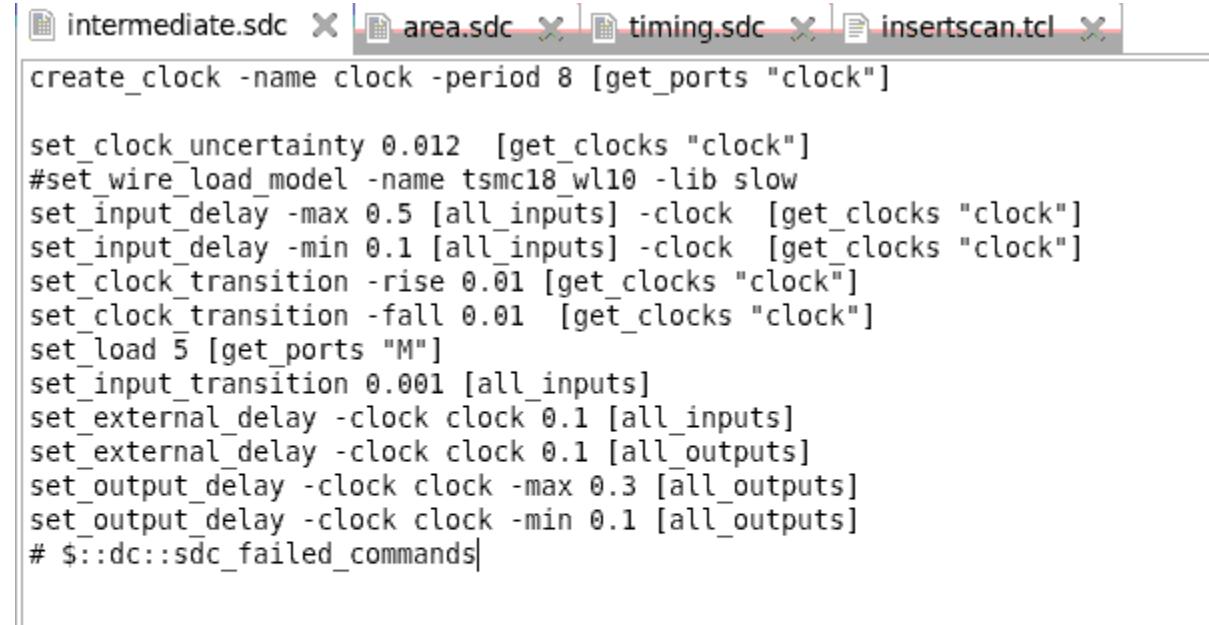
Pin	Type	Fanout	Load	Slew	Delay	Arrival
		(fF)	(ps)	(ps)	(ps)	
(clock clock)	launch					0 R
M_reg[18]/CK				10		0 R
M_reg[18]/Q	DFFQX2	1	13.2	80	+308	308 R
g6/A					+0	308
g6/Y	BUFX20	1	7700.0	3213	+2278	2586 R
M[18]	<< interconnect			3213	+0	2586 R
	out port				+0	2586 R
(timing.sdc_line_13_57_1)	ext delay				+500	3086 R
-----	-----	-----	-----	-----	-----	-----
(clock clock)	capture					3185 R
	uncertainty				-100	3085 R
-----	-----	-----	-----	-----	-----	-----
Cost Group : 'clock' (path_group 'clock')						
Timing slack : -1ps (TIMING VIOLATION)						
Start-point : M_reg[18]/CK						
End point : M[10]						

Cost Group : 'clock' (path_group 'clock')
Timing slack : -1ps (TIMING VIOLATION)
Start-point : M_reg[18]/CK
End point : M[10]

Timing slack slightly negative

C.Synthesize for timing constraints that are between (a) and (b) above.

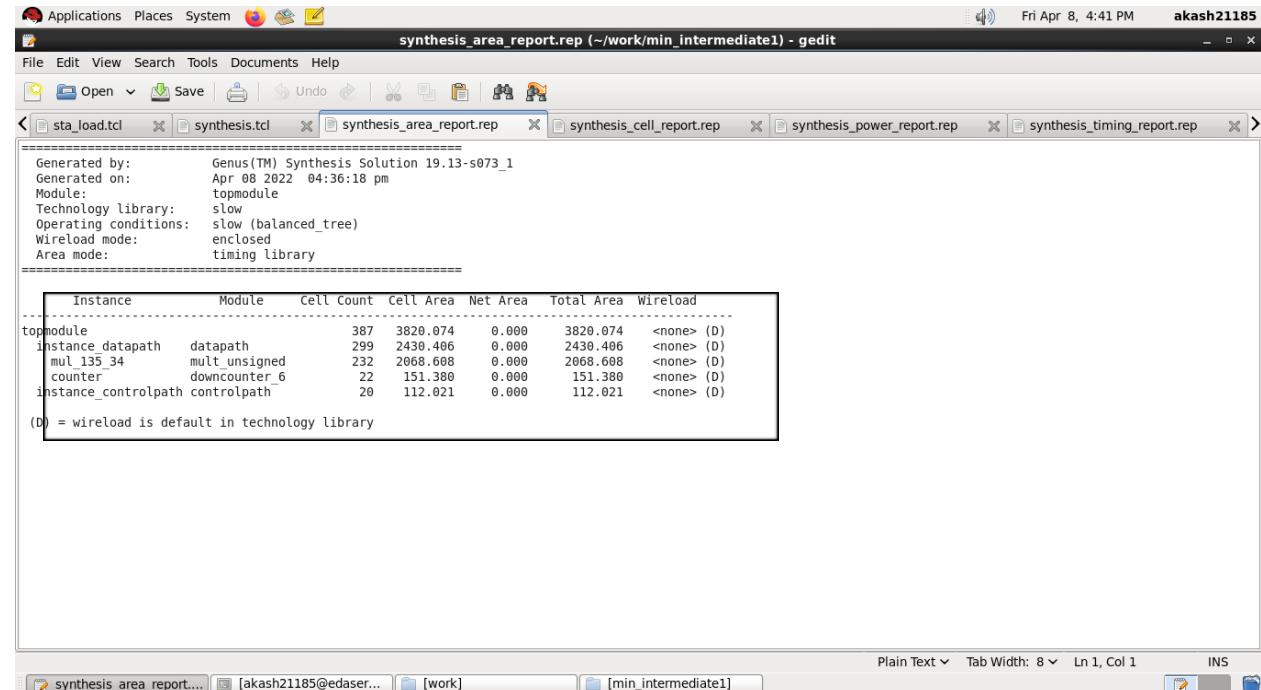
Constraint:



```
intermediate.sdc X | area.sdc X | timing.sdc X | insertscan.tcl X
create_clock -name clock -period 8 [get_ports "clock"]

set_clock_uncertainty 0.012 [get_clocks "clock"]
#set_wire_load_model -name tsmc18_wl10 -lib slow
set_input_delay -max 0.5 [all_inputs] -clock [get_clocks "clock"]
set_input_delay -min 0.1 [all_inputs] -clock [get_clocks "clock"]
set_clock_transition -rise 0.01 [get_clocks "clock"]
set_clock_transition -fall 0.01 [get_clocks "clock"]
set_load 5 [get_ports "M"]
set_input_transition 0.001 [all_inputs]
set_external_delay -clock clock 0.1 [all_inputs]
set_external_delay -clock clock 0.1 [all_outputs]
set_output_delay -clock clock -max 0.3 [all_outputs]
set_output_delay -clock clock -min 0.1 [all_outputs]
# $::dc::sdc_failed_commands
```

Area:



synthesis_area_report.rep (~/work/min_intermediate1) - gedit

Fri Apr 8, 4:41 PM akash21185

Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload
topmodule		387	3820.074	0.000	3820.074	<none> (D)
instance_datapath	datapath	299	2438.406	0.000	2438.406	<none> (D)
mul_135_34	mult_unsigned	232	2068.608	0.000	2068.608	<none> (D)
counter	downcounter_6	22	151.380	0.000	151.380	<none> (D)
instance_controlpath	controlpath	20	112.021	0.000	112.021	<none> (D)

(D) = wireload is default in technology library

Area reports of all modules are calculated and assimilated to a total area of 3312 μm^2 .

Cell Report:

```
Applications Places System synthesis_cell_report.rep (~/work/min_intermediate1) - gedit
Fri Apr 8, 4:42 PM akash21185
File Edit View Search Tools Documents Help
Open Save Undo Redo Cut Copy Paste Find Replace
sta_load.tcl synthesis.tcl synthesis_area_report.rep synthesis_cell_report.rep synthesis_power_report.rep synthesis_timing_report.rep
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 08 2022 04:36:18 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
WireLoad mode: enclosed
Area mode: timing library
=====
Gate Instances Area Library
-----
ADDFX1 19 373.909 slow
ADDFXL 60 1180.764 slow
AND2X1 4 18.166 slow
AND2XL 12 54.497 slow
A021X1 3 20.436 slow
A022XL 3 22.707 slow
A0121X1 2 10.597 slow
A0121X1 7 31.790 slow
A0121XL 3 13.624 slow
A0132X1 2 13.624 slow
A0133XL 1 7.569 slow
BUF2X0 20 514.692 slow
CLKINVX1 6 13.624 slow
CLKXOR2X1 4 33.304 slow
DFFQX1 55 874.220 slow
DFFQXL 1 15.895 slow
INVX1 25 56.768 slow
INVXL 7 15.895 slow
MX2X1 1 6.812 slow
MXI2XL 1 6.055 slow
-----
Plain Text Tab Width: 8 Ln 1, Col 1 INS
synthesis_cell_report.r... [akash21185@edaser... [work] [min_intermediate1]
Applications Places System synthesis_cell_report.rep (~/work/min_intermediate1) - gedit
Fri Apr 8, 4:41 PM akash21185
File Edit View Search Tools Documents Help
Open Save Undo Redo Cut Copy Paste Find Replace
sta_load.tcl synthesis.tcl synthesis_area_report.rep synthesis_cell_report.rep synthesis_power_report.rep synthesis_timing_report.rep
MX2X1 1 6.812 slow
MXI2XL 1 6.055 slow
NAND2BX1 1 4.541 slow
NAND2XL 105 317.898 slow
NAND3BX1 1 6.055 slow
NOR2BX1 3 13.624 slow
NOR2BXL 1 4.541 slow
NOR2XL 15 45.414 slow
NOR3X1 2 9.083 slow
NOR3XL 3 15.895 slow
NOR4XL 1 10.597 slow
NOR4XL 2 9.083 slow
NOR4XL 1 6.055 slow
NOR4XL 1 21.193 slow
NOR4XL 1 6.812 slow
NOR4XL 4 18.166 slow
NOR4XL 1 4.541 slow
NOR4XL 5 41.630 slow
-----
total 387 3820.074
-----
Type Instances Area Area %
-----
sequential 56 890.114 23.3
inverter 38 86.287 2.3
buffer 20 514.692 13.5
logic 273 2328.981 61.0
physical_cells 0 0.000 0.0
-----
total 387 3820.074 100.0
Plain Text Tab Width: 8 Ln 1, Col 1 INS
synthesis_cell_report.r... [akash21185@edaser... [work] [min_intermediate1]
```

Power Report:

```
Applications Places System Fri Apr 8, 4:42 PM akash21185
synthesis_power_report.rep (~/work/min_intermediate1) - gedit
File Edit View Search Tools Documents Help
Open Save Undo Redo Cut Copy Paste Find Replace Select All
sta_load.tcl synthesis.tcl synthesis_area_report.rep synthesis_cell_report.rep synthesis_power_report.rep synthesis_timing_report.rep
Instance: /topmodule
Power Unit: W
PDB Frames: /stim#/frame#0
-----

| Category   | Leakage     | Internal    | Switching   | Total       | Row%    |
|------------|-------------|-------------|-------------|-------------|---------|
| memory     | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00%   |
| register   | 5.53081e-06 | 1.12051e-04 | 7.63970e-06 | 1.25222e-04 | 10.83%  |
| latch      | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00%   |
| logic      | 1.68133e-05 | 8.51731e-05 | 9.18899e-04 | 1.02689e-03 | 88.33%  |
| bbox       | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00%   |
| clock      | 0.00000e+00 | 0.00000e+00 | 9.63990e-06 | 9.63990e-06 | 0.83%   |
| pad        | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00%   |
| pm         | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00%   |
| Subtotal   | 2.23441e-05 | 1.97224e-04 | 9.36178e-04 | 1.15575e-03 | 99.99%  |
| Percentage | 1.93%       | 17.06%      | 81.00%      | 100.00%     | 100.00% |


-----
```

Plain Text Tab Width: 8 Ln 1, Col 1 INS

Timing Report:

```
Applications Places System Fri Apr 8, 4:42 PM akash21185
synthesis_timing_report.rep (~/work/min_intermediate1) - gedit
File Edit View Search Tools Documents Help
Open Save Undo Redo Cut Copy Paste Find Replace Select All
sta_load.tcl synthesis.tcl synthesis_area_report.rep synthesis_cell_report.rep synthesis_power_report.rep synthesis_timing_report.rep
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 08 2022 04:36:18 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
-----


| Pin                     | Type    | Fanout | Load | Slew | Delay | Arrival |
|-------------------------|---------|--------|------|------|-------|---------|
|                         |         | (fF)   | (ps) | (ps) | (ps)  |         |
| (clock clock)           | launch  |        |      |      | 0 R   |         |
| B_in_side_reg_reg[0]/CK |         |        | 10   |      | 0 R   |         |
| B_in_side_reg_reg[0]/Q  | DFFQX1  | 10     | 17.0 | 157  | +343  | 343 R   |
| instance datapath/B[0]  |         |        |      |      |       |         |
| mul_135_34/B[0]         |         |        |      |      |       |         |
| g2481/B                 |         |        |      | +0   | 343   |         |
| g2481/Y                 | NAND2XL | 2      | 5.2  | 156  | +147  | 489 F   |
| g2464/B                 |         |        |      | +0   | 489   |         |
| g2464/Y                 | XNOR2X1 | 1      | 4.9  | 77   | +241  | 730 R   |
| g2447/CI                |         |        |      | +0   | 730   |         |
| g2447/S                 | ADDFXL  | 1      | 2.7  | 88   | +314  | 1044 F  |
| g2429/A                 |         |        |      | +0   | 1044  |         |
| g2429/Y                 | INVX1   | 1      | 6.7  | 72   | +79   | 1124 R  |
| g2400/A                 |         |        |      | +0   | 1124  |         |
| g2400/CO                | ADDFX1  | 1      | 2.7  | 76   | +213  | 1337 R  |
| g2399/A                 |         |        |      | +0   | 1337  |         |
| g2399/Y                 | INVX1   | 1      | 4.9  | 52   | +55   | 1392 F  |
| g2390/CI                |         |        |      | +0   | 1392  |         |
| g2390/CO                | ADDFX1  | 1      | 4.9  | 96   | +238  | 1630 F  |
| g2380/CI                |         |        |      | +0   | 1630  |         |


-----
```

Plain Text Tab Width: 8 Ln 1, Col 1 INS

Applications Places System Firefoxgedit synthesis_timing_report.rep (~~/work/min_intermediate1) - gedit

File Edit View Search Tools Documents Help

Open Save Undo Redo Cut Copy Paste Find Replace

sta_load.tcl synthesis.tcl synthesis_area_report.rep synthesis_cell_report.rep synthesis_power_report.rep synthesis_timing_report.rep

```

g2362/CI          +0    3129
g2362/CO ADDFX1   1 4.9 96 +250 3379 F
g2366/CI          +0    3379
g2366/CO ADDFX1   1 4.9 96 +250 3629 F
g2358/CI          +0    3629
g2358/CO ADDFX1   1 4.9 96 +250 3879 F
g2356/CI          +0    3879
g2356/CO ADDFX1   1 4.9 96 +250 4129 F
g2354/CI          +0    4129
g2354/CO ADDFX1   1 4.9 96 +250 4379 F
g2352/CI          +0    4379
g2352/CO ADDFX1   1 4.9 96 +250 4629 F
g2350/CI          +0    4629
g2350/CO ADDFX1   1 4.9 96 +250 4879 F
g2348/CI          +0    4879
g2348/S ADDFXL   1 1.6 73 +229 5107 F
g2346/A           +0    5107
g2346/Y INVXL    1 1.7 45 +54 5161 R
mul_135_34/Z[18] +0    5161
g733/B
g733/Y AND2XL   1 1.6 67 +111 5272 R
instance_datapath/M_out[18]
M_reg[18]/D      <<< DFFQX1      +0    5272
M_reg[18]/CK     setup        10 +202 5474 R
----- (clock clock)
capture          8000 R
uncertainty       -12 7988 R
-----
Cost Group : 'clock' (path_group 'clock')
Timing slack : 2514ps
Start-point : B_in_side_reg_reg[0]/CK
End-point   : M_reg[18]/D

```

Plain Text Tab Width: 8 Ln 1, Col 1 INS

synthesis_timing_repo... [akash21185@edaser... [work] [min_intermediate1]

Impact of changing the constraints on the QoR:

- When output delay increases slack reduces, area & total power remains the same. The effective time for the combinational circuit reduces, so the slack reduces and area and power does not change.
- When uncertainty increases, slack decreases but total power increases and area remains the same.
- When the latency is increased or decreased, no change in area, slack & total power is observed. This is because, the same amount of change occurs in both RT and AT. This change cancels each other.
- The effect of the input delay on QOR is same as that of the output delay.

UNDERSTANDING HOW RTL CORRESPONDS TO INSTANCES IN NETLIST:

```

module controlpath(C, reset, clk, control_signal);
    input [7:0] C;
    input reset, clk;
    output [1:0] control_signal;
    wire [7:0] C;
    wire reset, clk;
    wire [1:0] control_signal;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
    wire n_16, n_17;
    DFFQX1 control_signal_reg[1] (.CK (clk), .D (n_17), .Q(control_signal[1]));
    DFFQX1 control_signal_reg[0] (.CK (clk), .D (n_16), .Q(control_signal[0]));
    OAI32X1 g462(.A0 (n_1), .A1 (reset), .A2 (n_13), .B0 (n_3), .B1(n_12), .Y (n_17));
    OAI2BB1XL g463(.A0N (C[6]), .A1N (n_14), .B0 (n_15), .Y (n_16));
    OAI21X1 g464(.A0 (n_1), .A1 (n_9), .B0 (n_2), .Y (n_15));
    AOI211X1 g465(.A0 (n_0), .A1 (n_7), .B0 (C[7]), .C0 (reset), .Y(n_14));
    AOI21X1 g466(.A0 (C[5]), .A1 (n_10), .B0 (n_11), .Y (n_13));
    AOI211X1 g467(.A0 (C[4]), .A1 (n_8), .B0 (C[5]), .C0 (C[6]), .Y(n_12));
    NOR2XL g468(.A (C[5]), .B (n_7), .Y (n_11));
    AOI21X1 g469(.A0 (C[3]), .A1 (n_6), .B0 (C[4]), .Y (n_10));
    AOI21X1 g470(.A0 (C[4]), .A1 (n_5), .B0 (C[5]), .Y (n_9));
    OR2XL g471(.A (C[3]), .B (n_6), .Y (n_8));
    NAND3BX1 g472(.AN (n_4), .B (C[4]), .C (C[3]), .Y (n_7));
    NAND2BX1 g473(.AN (C[0]), .B (n_4), .Y (n_6));
    AO21X1 g474(.A0 (C[1]), .A1 (C[2]), .B0 (C[3]), .Y (n_5));
    NOR2XL g475(.A (C[2]), .B (C[1]), .Y (n_4));
    INVXL g476(.A (n_2), .Y (n_3));
    NOR2BX1 g477(.AN (C[7]), .B (reset), .Y (n_2));
    INVXI g478(.A (C[6]), .Y (n_1));
    INVXL g479(.A (C[5]), .Y (n_0));
endmodule

module controlpath(C,reset,clk,control_signal);

    input [7:0]C;
    input reset;
    input clk;
    output reg [1:0]control_signal;

    always@ (posedge clk)
    begin
        if(reset)
            control_signal <= 2'b00;      //reset state

        //6-bit down counter
        else if (C >= 8'h00 && C <= 8'h59)
            control_signal <= 2'b00;

        // 4-bit Binary to Excess 3 Converter
        else if (C >= 8'h69 && C <= 8'h90)
            control_signal <= 2'b01;

        //4-bit odd parity generator
        else if (C >= 8'hD6 && C <= 8'hFF)
            control_signal <= 2'b10;

        //A*B operation
        else
            control_signal <= 2'b11;
    end
endmodule

```

The above netlist and RTL are for Control Path. Input and output ports names and sizes are the same in both, The functionality of the RTL is mapped to the corresponding standard cells in the 90nm slow. lib.

```

module downcounter_6(clk, reset, out);
    input clk, reset;
    output [5:0] out;
    wire clk, reset;
    wire [5:0] out;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
    DFFQX1 out_reg[5] (.CK(clk), .D(n_15), .Q(out[5]));
    OAI211XL g205(.A0 (out[5]), .A1 (n_12), .B0 (n_0), .C0 (n_14), .Y(n_15));
    DFFQX1 out_reg[4] (.CK(clk), .D(n_13), .Q(out[4]));
    NAND2XL g207(.A (out[5]), .B (n_12), .Y (n_14));
    OAI211XL g208(.A0 (n_9), .A1 (n_2), .B0 (n_0), .C0 (n_12), .Y (n_13));
    DFFQX1 out_reg[3] (.CK(clk), .D(n_11), .Q(out[3]));
    NAND2XL g210(.A (n_2), .B (n_9), .Y (n_12));
    NAND2XL g211(.A (n_0), .B (n_10), .Y (n_11));
    DFFQX1 out_reg[2] (.CK(clk), .D(n_8), .Q(out[2]));
    AOI21XL g213(.A0 (out[3]), .A1 (n_7), .B0 (n_9), .Y (n_10));
    NOR2XL g214(.A (out[3]), .B (n_7), .Y (n_9));
    OAI211XL g215(.A0 (n_3), .A1 (n_1), .B0 (n_0), .C0 (n_7), .Y (n_8));
    DFFQX1 out_reg[1] (.CK(clk), .D(n_6), .Q(out[1]));
    NAND2XL g217(.A (n_1), .B (n_3), .Y (n_7));
    NAND2XL g218(.A (n_0), .B (n_5), .Y (n_6));
    DFFQX1 out_reg[0] (.CK(clk), .D(n_4), .Q(out[0]));
    AOI21XL g220(.A0 (out[1]), .A1 (out[0]), .B0 (n_3), .Y (n_5));
    NAND2XL g221(.A (n_0), .B (out[0]), .Y (n_4));
    NOR2XL g222(.A (out[0]), .B (out[1]), .Y (n_3));
    CLKINVX1 g223(.A (out[4]), .Y (n_2));
    CLKINVX1 g225(.A (out[2]), .Y (n_1));
    CLKINVX1 g226(.A (reset), .Y (n_0));
endmodule

module downcounter_6(clk,reset,out);
    input clk,reset;
    output reg [5:0]out;

    always@ (posedge clk)
    begin
        if(reset)
            out <= 6'b111_111;
        else
            out <= out - 6'b000001;
    end
endmodule

```

Here we can see the RTL and synthesized netlist. It has a clock, reset, and 6-bit output.

```

module topmodule(A, B, C, clock, reset, M);
input [9:0] A, B;
input [7:0] C;
input clock, reset;
output [19:0] M;
wire [9:0] A, B;
wire [7:0] C;
wire clock, reset;
wire [19:0] M;
wire [7:0] C_in_side_reg;
wire [1:0] ctrl_signal;
wire [9:0] A_in_side_reg;
wire [9:0] B_in_side_reg;
wire [19:0] M_out_side_reg;
wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
wire n_16, n_17, n_18, n_19;
controlpath instance_controlpath(.C (C_in_side_reg), .reset
    .clk (clock), .control_signal (ctrl_signal));
datapath instance_datapath(.A (A_in_side_reg), .B (B_in_si
    .control_signal (ctrl_signal), .clk (clock), .reset (.
    .M_out (M_out_side_reg));
DFFQX1 \B_in_side_reg_reg[4] (.CK (clock), .D (B[4]), .Q
    (B_in_side_reg[4]));
DFFQX1 \C_in_side_reg_reg[6] (.CK (clock), .D (C[6]), .Q
    (C_in_side_reg[6]));
DFFQX1 \C_in_side_reg_reg[1] (.CK (clock), .D (C[1]), .Q
    (C_in_side_reg[1]));
module topmodule(A,B,C,clock,reset,M);

    //port declarations
    input [9:0]A,B;
    input [7:0]C;
    input clock;
    input reset;
    output [19:0]M;

    datapath     instance_datapath(.A(A
controlpath   instance_controlpath(.

    //intermediate wire and reg declare
    reg [9:0]A_in_side_reg,B_in_side_re
    reg [7:0]C_in_side_reg;
    reg [19:0]M_out_side_reg;

    wire [1:0] ctrl_signal;

    //input and output registers
    always@ (posedge clock)
    begin

```

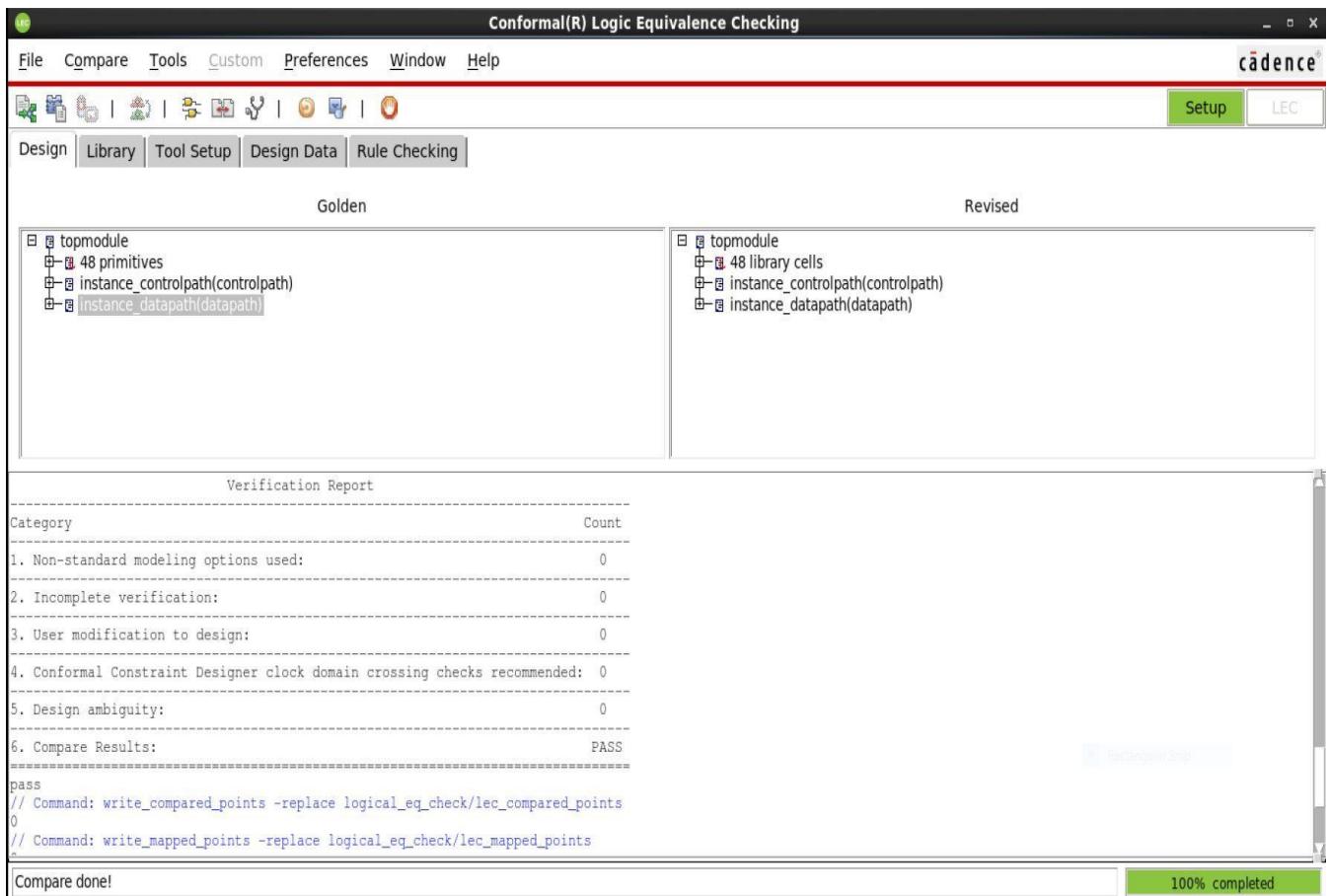
Some part of the topmodule is shown the above, in this apart from the port we can see that the control path and data path are instantiated in both RTL and the synthesized netlist. Similar observations can be made in the other modules in the design.

STEP 4: FORMAL EQUIVALENCE CHECKING

Tool used: Conformal_Low_Power_GXL

Command used: lec -lpgxl -dofile lechecking.tcl

Formal equivalence checking result for minimum area is shown below:-



Formal equivalence checking result for negative slack is shown below:-

The screenshot shows the Cadence Conformal(R) Logic Equivalence Checking software interface. The window title is "Conformal(R) Logic Equivalence Checking". The menu bar includes File, Compare, Tools, Custom, Preferences, Window, and Help. The toolbar contains icons for various functions. The main menu bar has tabs: Design, Library, Tool Setup, Design Data, and Rule Checking. The "Design" tab is currently selected.

The interface displays two columns: "Golden" and "Revised". Under "Golden", the tree view shows:

- topmodule
 - 48 primitives
 - instance_controlpath(controlpath)
 - instance_datapath(datapath)

Under "Revised", the tree view shows:

- topmodule
 - 138 library cells
 - instance_datapath_mul_135_34(mult_unsigned)

Below the tree views is a "Verification Report" section:

```
// Command: report_verification
=====
Verification Report
=====
Category                                     Count
1. Non-standard modeling options used:      0
2. Incomplete verification:                 0
3. User modification to design:            0
4. Conformal Constraint Designer clock domain crossing checks recommended: 0
5. Design ambiguity:                      0
6. Compare Results:                         PASS
=====
pass
// Command: write_compared_points -replace logical_eq_check/lec_compared_points
0
// Command: write_compared_points -replace logical_eq_check/lec_compared_points
0
```

The status bar at the bottom left says "Compare done!" and the bottom right says "100% completed".

Formal equivalence checking result of in between timing is shown below:-

The screenshot shows the Cadence Formal Equivalence Checking (LEC) interface. At the top, there's a menu bar with File, Compare, Tools, Custom, Preferences, Window, and Help. On the right, there are buttons for Setup and LEC. Below the menu is a toolbar with various icons. The main window has tabs for Design, Library, Tool Setup, Design Data, and Rule Checking, with Rule Checking selected. The interface is divided into two main sections: 'Golden' and 'Revised'. Both sections show a hierarchical tree view of design components. In the 'Golden' section, under 'topmodule', there are 48 primitives, one 'instance_controlpath(controlpath)', and one 'instance_datapath(datapath)' highlighted with a red border. In the 'Revised' section, there are 68 library cells, one 'instance_controlpath(controlpath)', and one 'instance_datapath(datapath)'. Below these sections is a large text area containing a verification report. The report starts with a header: '0 // Command: report_verification ===== Verification Report ====='. It then lists categories and their counts: 1. Non-standard modeling options used: 0; 2. Incomplete verification: 0; 3. User modification to design: 0; 4. Conformal Constraint Designer clock domain crossing checks recommended: 0; 5. Design ambiguity: 0; 6. Compare Results: PASS. The report concludes with 'pass' and 'Compare done!' at the bottom. A progress bar at the bottom right indicates '100% completed'.

```
0
// Command: report_verification
=====
Verification Report
=====
Category Count
-----
1. Non-standard modeling options used: 0
2. Incomplete verification: 0
3. User modification to design: 0
4. Conformal Constraint Designer clock domain crossing checks recommended: 0
5. Design ambiguity: 0
6. Compare Results: PASS
=====
pass
Compare done!
100% completed
```

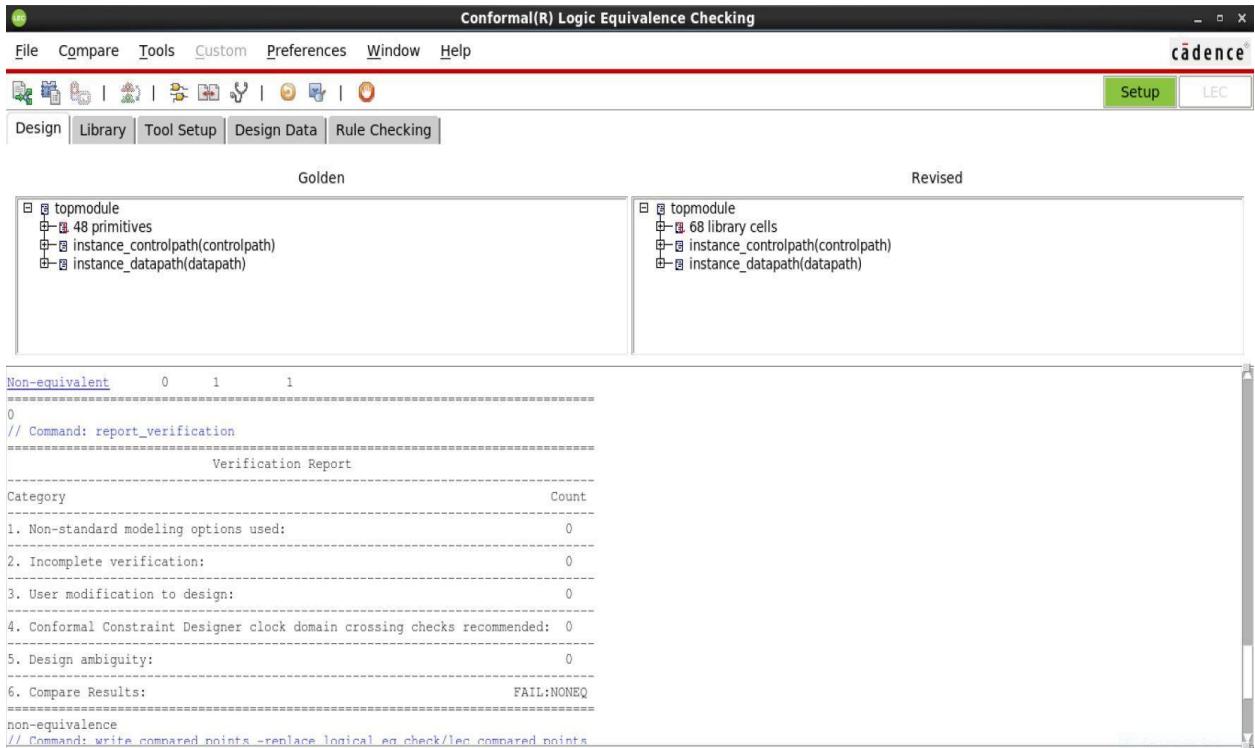
The Conformal Equivalence Checking for all the above mentioned three cases using their respective netlists gave the comparison results to be 'PASS'. Thus, it can be inferred that the Verilog RTL file and the corresponding Netlist generated after synthesis part are functionally equivalent irrespective of the input vectors. Formal verification is a complete way of verification as all the cases are implicitly covered. Also it does not use test vectors as in simulation based verification. This method is more accurate as it does not depend on the efficiency of the test bench.

BAD NETLIST 1: For the 1st case, a small change is made in the synthesised_netlist of the minimum area report. Inside the netlist, AND2XL instance is commented in the decoder module as shown in the below figure:-

```
lecheking.tcl x setup_script_demo.tcl x intermediate_timing.sdc x synthesised_netlist.v x
.C0 (n_16), .Y (n_22));
AOI32XL g692(.A0 (A[4]), .A1 (n_1), .A2 (n_9), .B0 (n_8), .B1 (n_15),
.Y (n_21));
AOI33XL g693(.A0 (n_12), .A1 (A[6]), .A2 (n_8), .B0 (A[7]), .B1
(n_1), .B2 (n_9), .Y (n_20));
OAI21XL g694(.A0 (B[7]), .A1 (n_13), .B0 (n_18), .Y (n_19));
NAND2XL g695(.A (B[7]), .B (n_13), .Y (n_18));
OAI21XL g696(.A0 (A[4]), .A1 (n_7), .B0 (n_14), .Y (n_17));
OAI21XL g697(.A0 (n_6), .A1 (n_7), .B0 (n_14), .Y (n_16));
MXI2XL g698(.A (n_1), .B (n_12), .S0 (A[6]), .Y (n_15));
NAND2XL g699(.A (n_5), .B (n_9), .Y (n_14));
A0I21XL g700(.A0 (B[4]), .A1 (n_10), .B0 (n_11), .Y (n_13));
CLKINVX1 g701(.A (n_5), .Y (n_12));
NOR2XL g702(.A (B[4]), .B (n_10), .Y (n_11));
A022XL g703(.A0 (n_3), .A1 (out_counter[3]), .B0 (n_0), .B1 (n_48),
.Y (M_out[3]));
A022XL g704(.A0 (n_3), .A1 (out_counter[2]), .B0 (n_0), .B1 (n_47),
.Y (M_out[2]));
A022XL g705(.A0 (n_3), .A1 (out_counter[1]), .B0 (n_0), .B1 (n_46),
.Y (M_out[1]));
//AND2XL g706(.A (n_0), .B (n_56), .Y (M_out[11]));
AND2XL g707(.A (n_0), .B (n_62), .Y (M_out[17]));
AND2XL g708(.A (n_0), .B (n_57), .Y (M_out[12]));
AND2XL g709(.A (n_0), .B (n_61), .Y (M_out[16]));
AND2XL g710(.A (n_0), .B (n_58), .Y (M_out[13]));
AND2XL g711(.A (n_0), .B (n_55), .Y (M_out[10]));
AND2XL g712(.A (n_0), .B (n_60), .Y (M_out[15]));
AND2XL g713(.A (n_0), .B (n_54), .Y (M_out[9]));
INVX1 g714(.A (n_8), .Y (n_7));
AOI21XL g715(.A0 (A[4]), .A1 (A[5]), .B0 (n_5), .Y (n_6));
AND2XL g716(.A (n_0), .B (n_64), .Y (M_out[19]));
AND2XL g717(.A (n_0), .B (n_59), .Y (M_out[14]));
CLKAND2X2 g718(.A (n_0), .B (n_63), .Y (M_out[18]));

```

VERIFICATION REPORT:-



Conformal(R) Logic Equivalence Checking

File Compare Tools Custom Preferences Window Help

Setup LEC

Design Library Tool Setup Design Data Rule Checking

Golden Revised

Non-equivalent 0 1 1

```
=====
0 // Command: report_verification
=====

Verification Report
```

Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification:	0
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity:	0
6. Compare Results:	FAIL:NONEQ

```
non-equivalence
// Command: write_compared_points -replace logical_eq_check/lec_compared_points
```

Conformal(R) Logic Equivalence Checking

File Compare Tools Custom Preferences Window Help

Setup LEC

Design Library Tool Setup Design Data Rule Checking

Golden Revised

Non-equivalent 0 1 1

```
=====
0 // Command: report_verification
=====

Verification Report
```

Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification:	0
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity:	0
6. Compare Results:	FAIL:NONEQ

```
non-equivalence
// Command: write_compared_points -replace logical_eq_check/lec_compared_points
```

BAD NETLIST 2: For the 2nd case, synthesised _netlist of the minimum timing report is considered. In this, A[7] is changed to D[7].

```
lechecking.tcl  X  synthesised_netlist.v  X
NAND2XL g2536(.A (A[9]), .B (B[1]), .Y (n_101));
NAND2XL g2537(.A (B[6]), .B (A[1]), .Y (n_89));
NAND2XL g2538(.A (A[8]), .B (B[1]), .Y (n_100));
NAND2XL g2539(.A (A[4]), .B (B[1]), .Y (n_99));
NAND2XL g2540(.A (B[7]), .B (A[0]), .Y (n_88));
NAND2XL g2541(.A (A[6]), .B (B[1]), .Y (n_98));
NAND2XL g2542(.A (B[7]), .B (A[6]), .Y (n_87));
NAND2XL g2543(.A (A[4]), .B (B[5]), .Y (n_86));
NAND2XL g2544(.A (B[7]), .B (A[9]), .Y (n_85));
NAND2XL g2545(.A (A[7]), .B (B[7]), .Y (n_84));
NAND2XL g2546(.A (B[8]), .B (A[2]), .Y (n_83));
NAND2XL g2547(.A (A[5]), .B (B[3]), .Y (n_82));
NAND2XL g2548(.A (A[7]), .B (B[2]), .Y (n_81));
NAND2XL g2549(.A (A[3]), .B (B[4]), .Y (n_80));
NAND2XL g2550(.A (D[7]), .B (B[8]), .Y (n_79)); // A[7] --> D[7]
NAND2XL g2551(.A (A[8]), .B (B[9]), .Y (n_78));
NAND2XL g2552(.A (B[9]), .B (A[3]), .Y (n_77));
NAND2XL g2553(.A (A[9]), .B (B[4]), .Y (n_76));
NAND2XL g2554(.A (B[7]), .B (A[4]), .Y (n_75));
NAND2X1 g2555(.A (B[3]), .B (A[0]), .Y (n_97));
NAND2XL g2556(.A (A[7]), .B (B[3]), .Y (n_74));
NAND2XL g2557(.A (A[9]), .B (B[3]), .Y (n_73));
NAND2XL g2558(.A (B[7]), .B (A[1]), .Y (n_72));
NAND2XL g2559(.A (A[2]), .B (B[5]), .Y (n_71));
NAND2XL g2560(.A (A[5]), .B (B[5]), .Y (n_70));
NAND2XL g2561(.A (A[5]), .B (B[8]), .Y (n_69));
NAND2XL g2562(.A (B[6]), .B (A[3]), .Y (n_68));
NAND2XL g2563(.A (A[6]), .B (B[4]), .Y (n_67));
NAND2X1 g2564(.A (A[3]), .B (B[3]), .Y (n_66));
NAND2XL g2565(.A (B[6]), .B (A[9]), .Y (n_65));
NAND2XL g2566(.A (A[8]), .B (B[4]), .Y (n_64));
NAND2X1 g2567(.A (B[2]), .B (A[1]), .Y (n_95));
NAND2XL g2568(.A (A[8]), .B (B[8]), .Y (n_63));
NAND2XL g2569(.A (B[1]), .B (B[7]), .Y (n_62));
NAND2XL g2570(.A (A[2]), .B (B[6]), .Y (n_61));
NAND2XL g2571(.A (B[5]), .B (B[5]), .Y (n_60));
NAND2XL g2572(.A (A[4]), .B (B[4]), .Y (n_59));
NAND2XL g2573(.A (B[3]), .B (B[3]), .Y (n_58));
NAND2XL g2574(.A (A[6]), .B (B[2]), .Y (n_57));
NAND2XL g2575(.A (B[2]), .B (B[2]), .Y (n_56));
NAND2XL g2576(.A (A[7]), .B (B[1]), .Y (n_55));
NAND2XL g2577(.A (B[1]), .B (B[1]), .Y (n_54));
NAND2XL g2578(.A (A[9]), .B (B[0]), .Y (n_53));
NAND2XL g2579(.A (B[0]), .B (B[0]), .Y (n_52));
NAND2XL g2580(.A (A[1]), .B (B[9]), .Y (n_51));
NAND2XL g2581(.A (B[9]), .B (A[8]), .Y (n_50));
NAND2XL g2582(.A (A[8]), .B (B[8]), .Y (n_49));
NAND2XL g2583(.A (B[8]), .B (A[7]), .Y (n_48));
NAND2XL g2584(.A (A[7]), .B (B[7]), .Y (n_47));
NAND2XL g2585(.A (B[7]), .B (A[6]), .Y (n_46));
NAND2XL g2586(.A (A[6]), .B (B[6]), .Y (n_45));
NAND2XL g2587(.A (B[6]), .B (A[5]), .Y (n_44));
NAND2XL g2588(.A (A[5]), .B (B[5]), .Y (n_43));
NAND2XL g2589(.A (B[5]), .B (A[4]), .Y (n_42));
NAND2XL g2590(.A (A[4]), .B (B[4]), .Y (n_41));
NAND2XL g2591(.A (B[4]), .B (A[3]), .Y (n_40));
NAND2XL g2592(.A (A[3]), .B (B[3]), .Y (n_39));
NAND2XL g2593(.A (B[3]), .B (A[2]), .Y (n_38));
NAND2XL g2594(.A (A[2]), .B (B[2]), .Y (n_37));
NAND2XL g2595(.A (B[2]), .B (A[1]), .Y (n_36));
NAND2XL g2596(.A (A[1]), .B (B[1]), .Y (n_35));
NAND2XL g2597(.A (B[1]), .B (B[0]), .Y (n_34));
NAND2XL g2598(.A (A[0]), .B (B[0]), .Y (n_33));
NAND2XL g2599(.A (B[0]), .B (B[1]), .Y (n_32));
NAND2XL g2600(.A (A[1]), .B (B[0]), .Y (n_31));
NAND2XL g2601(.A (B[0]), .B (B[2]), .Y (n_30));
NAND2XL g2602(.A (A[2]), .B (B[1]), .Y (n_29));
NAND2XL g2603(.A (B[1]), .B (B[0]), .Y (n_28));
NAND2XL g2604(.A (A[0]), .B (B[1]), .Y (n_27));
NAND2XL g2605(.A (B[1]), .B (B[0]), .Y (n_26));
NAND2XL g2606(.A (A[1]), .B (B[0]), .Y (n_25));
NAND2XL g2607(.A (B[0]), .B (B[1]), .Y (n_24));
NAND2XL g2608(.A (A[2]), .B (B[0]), .Y (n_23));
NAND2XL g2609(.A (B[0]), .B (B[2]), .Y (n_22));
NAND2XL g2610(.A (A[3]), .B (B[0]), .Y (n_21));
NAND2XL g2611(.A (B[0]), .B (B[3]), .Y (n_20));
NAND2XL g2612(.A (A[4]), .B (B[0]), .Y (n_19));
NAND2XL g2613(.A (B[0]), .B (B[4]), .Y (n_18));
NAND2XL g2614(.A (A[5]), .B (B[0]), .Y (n_17));
NAND2XL g2615(.A (B[0]), .B (B[5]), .Y (n_16));
NAND2XL g2616(.A (A[6]), .B (B[0]), .Y (n_15));
NAND2XL g2617(.A (B[0]), .B (B[6]), .Y (n_14));
NAND2XL g2618(.A (A[7]), .B (B[0]), .Y (n_13));
NAND2XL g2619(.A (B[0]), .B (B[7]), .Y (n_12));
NAND2XL g2620(.A (A[8]), .B (B[0]), .Y (n_11));
NAND2XL g2621(.A (B[0]), .B (B[8]), .Y (n_10));
NAND2XL g2622(.A (A[9]), .B (B[0]), .Y (n_9));
NAND2XL g2623(.A (B[0]), .B (B[9]), .Y (n_8));
NAND2XL g2624(.A (A[10]), .B (B[0]), .Y (n_7));
NAND2XL g2625(.A (B[0]), .B (B[10]), .Y (n_6));
NAND2XL g2626(.A (A[11]), .B (B[0]), .Y (n_5));
NAND2XL g2627(.A (B[0]), .B (B[11]), .Y (n_4));
NAND2XL g2628(.A (A[12]), .B (B[0]), .Y (n_3));
NAND2XL g2629(.A (B[0]), .B (B[12]), .Y (n_2));
NAND2XL g2630(.A (A[13]), .B (B[0]), .Y (n_1));
NAND2XL g2631(.A (B[0]), .B (B[13]), .Y (n_0));
NAND2XL g2632(.A (A[14]), .B (B[0]), .Y (n_15));
NAND2XL g2633(.A (B[0]), .B (B[14]), .Y (n_14));
NAND2XL g2634(.A (A[15]), .B (B[0]), .Y (n_13));
NAND2XL g2635(.A (B[0]), .B (B[15]), .Y (n_12));
NAND2XL g2636(.A (A[16]), .B (B[0]), .Y (n_11));
NAND2XL g2637(.A (B[0]), .B (B[16]), .Y (n_10));
NAND2XL g2638(.A (A[17]), .B (B[0]), .Y (n_9));
NAND2XL g2639(.A (B[0]), .B (B[17]), .Y (n_8));
NAND2XL g2640(.A (A[18]), .B (B[0]), .Y (n_7));
NAND2XL g2641(.A (B[0]), .B (B[18]), .Y (n_6));
NAND2XL g2642(.A (A[19]), .B (B[0]), .Y (n_5));
NAND2XL g2643(.A (B[0]), .B (B[19]), .Y (n_4));
NAND2XL g2644(.A (A[20]), .B (B[0]), .Y (n_3));
NAND2XL g2645(.A (B[0]), .B (B[20]), .Y (n_2));
NAND2XL g2646(.A (A[21]), .B (B[0]), .Y (n_1));
NAND2XL g2647(.A (B[0]), .B (B[21]), .Y (n_0));
NAND2XL g2648(.A (A[22]), .B (B[0]), .Y (n_16));
NAND2XL g2649(.A (B[0]), .B (B[22]), .Y (n_15));
NAND2XL g2650(.A (A[23]), .B (B[0]), .Y (n_14));
NAND2XL g2651(.A (B[0]), .B (B[23]), .Y (n_13));
NAND2XL g2652(.A (A[24]), .B (B[0]), .Y (n_12));
NAND2XL g2653(.A (B[0]), .B (B[24]), .Y (n_11));
NAND2XL g2654(.A (A[25]), .B (B[0]), .Y (n_10));
NAND2XL g2655(.A (B[0]), .B (B[25]), .Y (n_9));
NAND2XL g2656(.A (A[26]), .B (B[0]), .Y (n_8));
NAND2XL g2657(.A (B[0]), .B (B[26]), .Y (n_7));
NAND2XL g2658(.A (A[27]), .B (B[0]), .Y (n_6));
NAND2XL g2659(.A (B[0]), .B (B[27]), .Y (n_5));
NAND2XL g2660(.A (A[28]), .B (B[0]), .Y (n_4));
NAND2XL g2661(.A (B[0]), .B (B[28]), .Y (n_3));
NAND2XL g2662(.A (A[29]), .B (B[0]), .Y (n_2));
NAND2XL g2663(.A (B[0]), .B (B[29]), .Y (n_1));
NAND2XL g2664(.A (A[30]), .B (B[0]), .Y (n_0));
NAND2XL g2665(.A (B[0]), .B (B[30]), .Y (n_15));
NAND2XL g2666(.A (A[31]), .B (B[0]), .Y (n_14));
NAND2XL g2667(.A (B[0]), .B (B[31]), .Y (n_13));
NAND2XL g2668(.A (A[32]), .B (B[0]), .Y (n_12));
NAND2XL g2669(.A (B[0]), .B (B[32]), .Y (n_11));
NAND2XL g2670(.A (A[33]), .B (B[0]), .Y (n_10));
NAND2XL g2671(.A (B[0]), .B (B[33]), .Y (n_9));
NAND2XL g2672(.A (A[34]), .B (B[0]), .Y (n_8));
NAND2XL g2673(.A (B[0]), .B (B[34]), .Y (n_7));
NAND2XL g2674(.A (A[35]), .B (B[0]), .Y (n_6));
NAND2XL g2675(.A (B[0]), .B (B[35]), .Y (n_5));
NAND2XL g2676(.A (A[36]), .B (B[0]), .Y (n_4));
NAND2XL g2677(.A (B[0]), .B (B[36]), .Y (n_3));
NAND2XL g2678(.A (A[37]), .B (B[0]), .Y (n_2));
NAND2XL g2679(.A (B[0]), .B (B[37]), .Y (n_1));
NAND2XL g2680(.A (A[38]), .B (B[0]), .Y (n_0));
NAND2XL g2681(.A (B[0]), .B (B[38]), .Y (n_15));
NAND2XL g2682(.A (A[39]), .B (B[0]), .Y (n_14));
NAND2XL g2683(.A (B[0]), .B (B[39]), .Y (n_13));
NAND2XL g2684(.A (A[40]), .B (B[0]), .Y (n_12));
NAND2XL g2685(.A (B[0]), .B (B[40]), .Y (n_11));
NAND2XL g2686(.A (A[41]), .B (B[0]), .Y (n_10));
NAND2XL g2687(.A (B[0]), .B (B[41]), .Y (n_9));
NAND2XL g2688(.A (A[42]), .B (B[0]), .Y (n_8));
NAND2XL g2689(.A (B[0]), .B (B[42]), .Y (n_7));
NAND2XL g2690(.A (A[43]), .B (B[0]), .Y (n_6));
NAND2XL g2691(.A (B[0]), .B (B[43]), .Y (n_5));
NAND2XL g2692(.A (A[44]), .B (B[0]), .Y (n_4));
NAND2XL g2693(.A (B[0]), .B (B[44]), .Y (n_3));
NAND2XL g2694(.A (A[45]), .B (B[0]), .Y (n_2));
NAND2XL g2695(.A (B[0]), .B (B[45]), .Y (n_1));
NAND2XL g2696(.A (A[46]), .B (B[0]), .Y (n_0));
NAND2XL g2697(.A (B[0]), .B (B[46]), .Y (n_15));
NAND2XL g2698(.A (A[47]), .B (B[0]), .Y (n_14));
NAND2XL g2699(.A (B[0]), .B (B[47]), .Y (n_13));
NAND2XL g2700(.A (A[48]), .B (B[0]), .Y (n_12));
NAND2XL g2701(.A (B[0]), .B (B[48]), .Y (n_11));
NAND2XL g2702(.A (A[49]), .B (B[0]), .Y (n_10));
NAND2XL g2703(.A (B[0]), .B (B[49]), .Y (n_9));
NAND2XL g2704(.A (A[50]), .B (B[0]), .Y (n_8));
NAND2XL g2705(.A (B[0]), .B (B[50]), .Y (n_7));
NAND2XL g2706(.A (A[51]), .B (B[0]), .Y (n_6));
NAND2XL g2707(.A (B[0]), .B (B[51]), .Y (n_5));
NAND2XL g2708(.A (A[52]), .B (B[0]), .Y (n_4));
NAND2XL g2709(.A (B[0]), .B (B[52]), .Y (n_3));
NAND2XL g2710(.A (A[53]), .B (B[0]), .Y (n_2));
NAND2XL g2711(.A (B[0]), .B (B[53]), .Y (n_1));
NAND2XL g2712(.A (A[54]), .B (B[0]), .Y (n_0));
NAND2XL g2713(.A (B[0]), .B (B[54]), .Y (n_15));
NAND2XL g2714(.A (A[55]), .B (B[0]), .Y (n_14));
NAND2XL g2715(.A (B[0]), .B (B[55]), .Y (n_13));
NAND2XL g2716(.A (A[56]), .B (B[0]), .Y (n_12));
NAND2XL g2717(.A (B[0]), .B (B[56]), .Y (n_11));
NAND2XL g2718(.A (A[57]), .B (B[0]), .Y (n_10));
NAND2XL g2719(.A (B[0]), .B (B[57]), .Y (n_9));
NAND2XL g2720(.A (A[58]), .B (B[0]), .Y (n_8));
NAND2XL g2721(.A (B[0]), .B (B[58]), .Y (n_7));
NAND2XL g2722(.A (A[59]), .B (B[0]), .Y (n_6));
NAND2XL g2723(.A (B[0]), .B (B[59]), .Y (n_5));
NAND2XL g2724(.A (A[60]), .B (B[0]), .Y (n_4));
NAND2XL g2725(.A (B[0]), .B (B[60]), .Y (n_3));
NAND2XL g2726(.A (A[61]), .B (B[0]), .Y (n_2));
NAND2XL g2727(.A (B[0]), .B (B[61]), .Y (n_1));
NAND2XL g2728(.A (A[62]), .B (B[0]), .Y (n_0));
NAND2XL g2729(.A (B[0]), .B (B[62]), .Y (n_15));
NAND2XL g2730(.A (A[63]), .B (B[0]), .Y (n_14));
NAND2XL g2731(.A (B[0]), .B (B[63]), .Y (n_13));
NAND2XL g2732(.A (A[64]), .B (B[0]), .Y (n_12));
NAND2XL g2733(.A (B[0]), .B (B[64]), .Y (n_11));
NAND2XL g2734(.A (A[65]), .B (B[0]), .Y (n_10));
NAND2XL g2735(.A (B[0]), .B (B[65]), .Y (n_9));
NAND2XL g2736(.A (A[66]), .B (B[0]), .Y (n_8));
NAND2XL g2737(.A (B[0]), .B (B[66]), .Y (n_7));
NAND2XL g2738(.A (A[67]), .B (B[0]), .Y (n_6));
NAND2XL g2739(.A (B[0]), .B (B[67]), .Y (n_5));
NAND2XL g2740(.A (A[68]), .B (B[0]), .Y (n_4));
NAND2XL g2741(.A (B[0]), .B (B[68]), .Y (n_3));
NAND2XL g2742(.A (A[69]), .B (B[0]), .Y (n_2));
NAND2XL g2743(.A (B[0]), .B (B[69]), .Y (n_1));
NAND2XL g2744(.A (A[70]), .B (B[0]), .Y (n_0));
NAND2XL g2745(.A (B[0]), .B (B[70]), .Y (n_15));
NAND2XL g2746(.A (A[71]), .B (B[0]), .Y (n_14));
NAND2XL g2747(.A (B[0]), .B (B[71]), .Y (n_13));
NAND2XL g2748(.A (A[72]), .B (B[0]), .Y (n_12));
NAND2XL g2749(.A (B[0]), .B (B[72]), .Y (n_11));
NAND2XL g2750(.A (A[73]), .B (B[0]), .Y (n_10));
NAND2XL g2751(.A (B[0]), .B (B[73]), .Y (n_9));
NAND2XL g2752(.A (A[74]), .B (B[0]), .Y (n_8));
NAND2XL g2753(.A (B[0]), .B (B[74]), .Y (n_7));
NAND2XL g2754(.A (A[75]), .B (B[0]), .Y (n_6));
NAND2XL g2755(.A (B[0]), .B (B[75]), .Y (n_5));
NAND2XL g2756(.A (A[76]), .B (B[0]), .Y (n_4));
NAND2XL g2757(.A (B[0]), .B (B[76]), .Y (n_3));
NAND2XL g2758(.A (A[77]), .B (B[0]), .Y (n_2));
NAND2XL g2759(.A (B[0]), .B (B[77]), .Y (n_1));
NAND2XL g2760(.A (A[78]), .B (B[0]), .Y (n_0));
NAND2XL g2761(.A (B[0]), .B (B[78]), .Y (n_15));
NAND2XL g2762(.A (A[79]), .B (B[0]), .Y (n_14));
NAND2XL g2763(.A (B[0]), .B (B[79]), .Y (n_13));
NAND2XL g2764(.A (A[80]), .B (B[0]), .Y (n_12));
NAND2XL g2765(.A (B[0]), .B (B[80]), .Y (n_11));
NAND2XL g2766(.A (A[81]), .B (B[0]), .Y (n_10));
NAND2XL g2767(.A (B[0]), .B (B[81]), .Y (n_9));
NAND2XL g2768(.A (A[82]), .B (B[0]), .Y (n_8));
NAND2XL g2769(.A (B[0]), .B (B[82]), .Y (n_7));
NAND2XL g2770(.A (A[83]), .B (B[0]), .Y (n_6));
NAND2XL g2771(.A (B[0]), .B (B[83]), .Y (n_5));
NAND2XL g2772(.A (A[84]), .B (B[0]), .Y (n_4));
NAND2XL g2773(.A (B[0]), .B (B[84]), .Y (n_3));
NAND2XL g2774(.A (A[85]), .B (B[0]), .Y (n_2));
NAND2XL g2775(.A (B[0]), .B (B[85]), .Y (n_1));
NAND2XL g2776(.A (A[86]), .B (B[0]), .Y (n_0));
NAND2XL g2777(.A (B[0]), .B (B[86]), .Y (n_15));
NAND2XL g2778(.A (A[87]), .B (B[0]), .Y (n_14));
NAND2XL g2779(.A (B[0]), .B (B[87]), .Y (n_13));
NAND2XL g2780(.A (A[88]), .B (B[0]), .Y (n_12));
NAND2XL g2781(.A (B[0]), .B (B[88]), .Y (n_11));
NAND2XL g2782(.A (A[89]), .B (B[0]), .Y (n_10));
NAND2XL g2783(.A (B[0]), .B (B[89]), .Y (n_9));
NAND2XL g2784(.A (A[90]), .B (B[0]), .Y (n_8));
NAND2XL g2785(.A (B[0]), .B (B[90]), .Y (n_7));
NAND2XL g2786(.A (A[91]), .B (B[0]), .Y (n_6));
NAND2XL g2787(.A (B[0]), .B (B[91]), .Y (n_5));
NAND2XL g2788(.A (A[92]), .B (B[0]), .Y (n_4));
NAND2XL g2789(.A (B[0]), .B (B[92]), .Y (n_3));
NAND2XL g2790(.A (A[93]), .B (B[0]), .Y (n_2));
NAND2XL g2791(.A (B[0]), .B (B[93]), .Y (n_1));
NAND2XL g2792(.A (A[94]), .B (B[0]), .Y (n_0));
NAND2XL g2793(.A (B[0]), .B (B[94]), .Y (n_15));
NAND2XL g2794(.A (A[95]), .B (B[0]), .Y (n_14));
NAND2XL g2795(.A (B[0]), .B (B[95]), .Y (n_13));
NAND2XL g2796(.A (A[96]), .B (B[0]), .Y (n_12));
NAND2XL g2797(.A (B[0]), .B (B[97]), .Y (n_11));
NAND2XL g2798(.A (A[98]), .B (B[0]), .Y (n_10));
NAND2XL g2799(.A (B[0]), .B (B[99]), .Y (n_9));
NAND2XL g2800(.A (A[100]), .B (B[0]), .Y (n_8));
NAND2XL g2801(.A (B[0]), .B (B[101]), .Y (n_7));
NAND2XL g2802(.A (A[102]), .B (B[0]), .Y (n_6));
NAND2XL g2803(.A (B[0]), .B (B[103]), .Y (n_5));
NAND2XL g2804(.A (A[104]), .B (B[0]), .Y (n_4));
NAND2XL g2805(.A (B[0]), .B (B[105]), .Y (n_3));
NAND2XL g2806(.A (A[106]), .B (B[0]), .Y (n_2));
NAND2XL g2807(.A (B[0]), .B (B[107]), .Y (n_1));
NAND2XL g2808(.A (A[108]), .B (B[0]), .Y (n_0));
NAND2XL g2809(.A (B[0]), .B (B[109]), .Y (n_15));
NAND2XL g2810(.A (A[110]), .B (B[0]), .Y (n_14));
NAND2XL g2811(.A (B[0]), .B (B[111]), .Y (n_13));
NAND2XL g2812(.A (A[112]), .B (B[0]), .Y (n_12));
NAND2XL g2813(.A (B[0]), .B (B[113]), .Y (n_11));
NAND2XL g2814(.A (A[114]), .B (B[0]), .Y (n_10));
NAND2XL g2815(.A (B[0]), .B (B[115]), .Y (n_9));
NAND2XL g2816(.A (A[116]), .B (B[0]), .Y (n_8));
NAND2XL g2817(.A (B[0]), .B (B[117]), .Y (n_7));
NAND2XL g2818(.A (A[118]), .B (B[0]), .Y (n_6));
NAND2XL g2819(.A (B[0]), .B (B[119]), .Y (n_5));
NAND2XL g2820(.A (A[120]), .B (B[0]), .Y (n_4));
NAND2XL g2821(.A (B[0]), .B (B[121]), .Y (n_3));
NAND2XL g2822(.A (A[122]), .B (B[0]), .Y (n_2));
NAND2XL g2823(.A (B[0]), .B (B[123]), .Y (n_1));
NAND2XL g2824(.A (A[124]), .B (B[0]), .Y (n_0));
NAND2XL g2825(.A (B[0]), .B (B[125]), .Y (n_15));
NAND2XL g2826(.A (A[126]), .B (B[0]), .Y (n_14));
NAND2XL g2827(.A (B[0]), .B (B[127]), .Y (n_13));
NAND2XL g2828(.A (A[128]), .B (B[0]), .Y (n_12));
NAND2XL g2829(.A (B[0]), .B (B[129]), .Y (n_11));
NAND2XL g2830(.A (A[130]), .B (B[0]), .Y (n_10));
NAND2XL g2831(.A (B[0]), .B (B[131]), .Y (n_9));
NAND2XL g2832(.A (A[132]), .B (B[0]), .Y (n_8));
NAND2XL g2833(.A (B[0]), .B (B[133]), .Y (n_7));
NAND2XL g2834(.A (A[134]), .B (B[0]), .Y (n_6));
NAND2XL g2835(.A (B[0]), .B (B[135]), .Y (n_5));
NAND2XL g2836(.A (A[136]), .B (B[0]), .Y (n_4));
NAND2XL g2837(.A (B[0]), .B (B[137]), .Y (n_3));
NAND2XL g2838(.A (A[138]), .B (B[0]), .Y (n_2));
NAND2XL g2839(.A (B[0]), .B (B[139]), .Y (n_1));
NAND2XL g2840(.A (A[140]), .B (B[0]), .Y (n_0));
NAND2XL g2841(.A (B[0]), .B (B[141]), .Y (n_15));
NAND2XL g2842(.A (A[142]), .B (B[0]), .Y (n_14));
NAND2XL g2843(.A (B[0]), .B (B[143]), .Y (n_13));
NAND2XL g2844(.A (A[144]), .B (B[0]), .Y (n_12));
NAND2XL g2845(.A (B[0]), .B (B[145]), .Y (n_11));
NAND2XL g2846(.A (A[146]), .B (B[0]), .Y (n_10));
NAND2XL g2847(.A (B[0]), .B (B[147]), .Y (n_9));
NAND2XL g2848(.A (A[148]), .B (B[0]), .Y (n_8));
NAND2XL g2849(.A (B[0]), .B (B[149]), .Y (n_7));
NAND2XL g2850(.A (A[150]), .B (B[0]), .Y (n_6));
NAND2XL g2851(.A (B[0]), .B (B[151]), .Y (n_5));
NAND2XL g2852(.A (A[152]), .B (B[0]), .Y (n_4));
NAND2XL g2853(.A (B[0]), .B (B[153]), .Y (n_3));
NAND2XL g2854(.A (A[154]), .B (B[0]), .Y (n_2));
NAND2XL g2855(.A (B[0]), .B (B[155]), .Y (n_1));
NAND2XL g2856(.A (A[156]), .B (B[0]), .Y (n_0));
NAND2XL g2857(.A (B[0]), .B (B[157]), .Y (n_15));
NAND2XL g2858(.A (A[158]), .B (B[0]), .Y (n_14));
NAND2XL g2859(.A (B[0]), .B (B[159]), .Y (n_13));
NAND2XL g2860(.A (A[160]), .B (B[0]), .Y (n_12));
NAND2XL g2861(.A (B[0]), .B (B[161]), .Y (n_11));
NAND2XL g2862(.A (A[162]), .B (B[0]), .Y (n_10));
NAND2XL g2863(.A (B[0]), .B (B[163]), .Y (n_9));
NAND2XL g2864(.A (A[164]), .B (B[0]), .Y (n_8));
NAND2XL g2865(.A (B[0]), .B (B[165]), .Y (n_7));
NAND2XL g2866(.A (A[166]), .B (B[0]), .Y (n_6));
NAND2XL g2867(.A (B[0]), .B (B[167]), .Y (n_5));
NAND2XL g2868(.A (A[168]), .B (B[0]), .Y (n_4));
NAND2XL g2869(.A (B[0]), .B (B[169]), .Y (n_3));
NAND2XL g2870(.A (A[170]), .B (B[0]), .Y (n_2));
NAND2XL g2871(.A (B[0]), .B (B[171]), .Y (n_1));
NAND2XL g2872(.A (A[172]), .B (B[0]), .Y (n_0));
NAND2XL g2873(.A (B[0]), .B (B[173]), .Y (n_15));
NAND2XL g2874(.A (A[174]), .B (B[0]), .Y (n_14));
NAND2XL g2875(.A (B[0]), .B (B[175]), .Y (n_13));
NAND2XL g2876(.A (A[176]), .B (B[0]), .Y (n_12));
NAND2XL g2877(.A (B[0]), .B (B[177]), .Y (n_11));
NAND2XL g2878(.A (A[178]), .B (B[0]), .Y (n_10));
NAND2XL g2879(.A (B[0]), .B (B[179]), .Y (n_9));
NAND2XL g2880(.A (A[180]), .B (B[0]), .Y (n_8));
NAND2XL g2881(.A (B[0]), .B (B[181]), .Y (n_7));
NAND2XL g2882(.A (A[182]), .B (B[0]), .Y (n_6));
NAND2XL g2883(.A (B[0]), .B (B[183]), .Y (n_5));
NAND2XL g2884(.A (A[184]), .B (B[0]), .Y (n_4));
NAND2XL g2885(.A (B[0]), .B (B[185]), .Y (n_3));
NAND2XL g2886(.A (A[186]), .B (B[0]), .Y (n_2));
NAND2XL g2887(.A (B[0]), .B (B[187]), .Y (n_1));
NAND2XL g2888(.A (A[188]), .B (B[0]), .Y (n_0));
NAND2XL g2889(.A (B[0]), .B (B[189]), .Y (n_15));
NAND2XL g2890(.A (A[190]), .B (B[0]), .Y (n_14));
NAND2XL g2891(.A (B[0]), .B (B[191]), .Y (n_13));
NAND2XL g2892(.A (A[192]), .B (B[0]), .Y
```

```

Conformal(R) Logic Equivalence Checking
File Compare Tools Custom Preferences Window Help
cadence®
Setup LEC
Design Library Tool Setup Design Data Rule Checking
Golden Revised
topmodule
  48 primitives
  instance_controlpath(controlpath)
  instance_datapath(datapath)

// Warning: (RTL14) Signal has input but it has no output (occurrence:196)
// Warning: (RTL14.1) Fanout load of the signal is removed (occurrence:84)
// Warning: (VLG5.2) Primitive input port has multiple bits. Ignore all but LSB bit (occurrence:2)
// Warning: (DIR6.1) Ignored compiler directive is detected (occurrence:480)
// Warning: (DIR6.2) Supported compiler directive is detected (occurrence:960)
// Warning: (HRC1.4) Module/entity is empty (blackboxed) (occurrence:1)
// Warning: (HRC3.10b) An input port is declared, but it is not used. Module is empty (occurrence:1)
// Note: Read VERILOG library successfully
0
CPU time      : 0.72    seconds
Elapse time   : 1       seconds
Memory usage  : 289.23  M bytes
// Command: read_design ../../rtl/Top.v -verilog -golden
// Parsing file ../../rtl/Top.v ...
// Golden root module is set to 'topmodule'
// Warning: (RTL1.5b) Potential loss of RHS msb or carry-out bit (occurrence:1)
// Note: Read VERILOG design successfully
0
// Command: read_design ../../script/synth_report_intermediate_timing/synthesised_netlist.v -verilog -revised
// Parsing file ../../script/synth_report_intermediate_timing/synthesised_netlist.v ...
// Error: PARSE_ERROR: Parsing syntax error
// Identifier 'D' not declared near token ')'
// on line 368 in file '../../script/synth_report_intermediate_timing/synthesised_netlist.v'
1
// 'dofile /home/akash21185/logical_eq_check
/lechecking.tcl' is aborted at line 5

```

Reading VERILOG design failed! 0%

Analysis of the result obtained:-

1. PARSE_ERROR message is generated on the window, therefore resulting in parsing syntax error.
2. The Identifier D is not declared. As a result the comparison is not performed further.

BAD NETLIST 3: For the 3rd case, synthesised_netlist of the intermediate timing report is considered. In this, the name of the instance is changed from NOR2XL to NOR2PL.

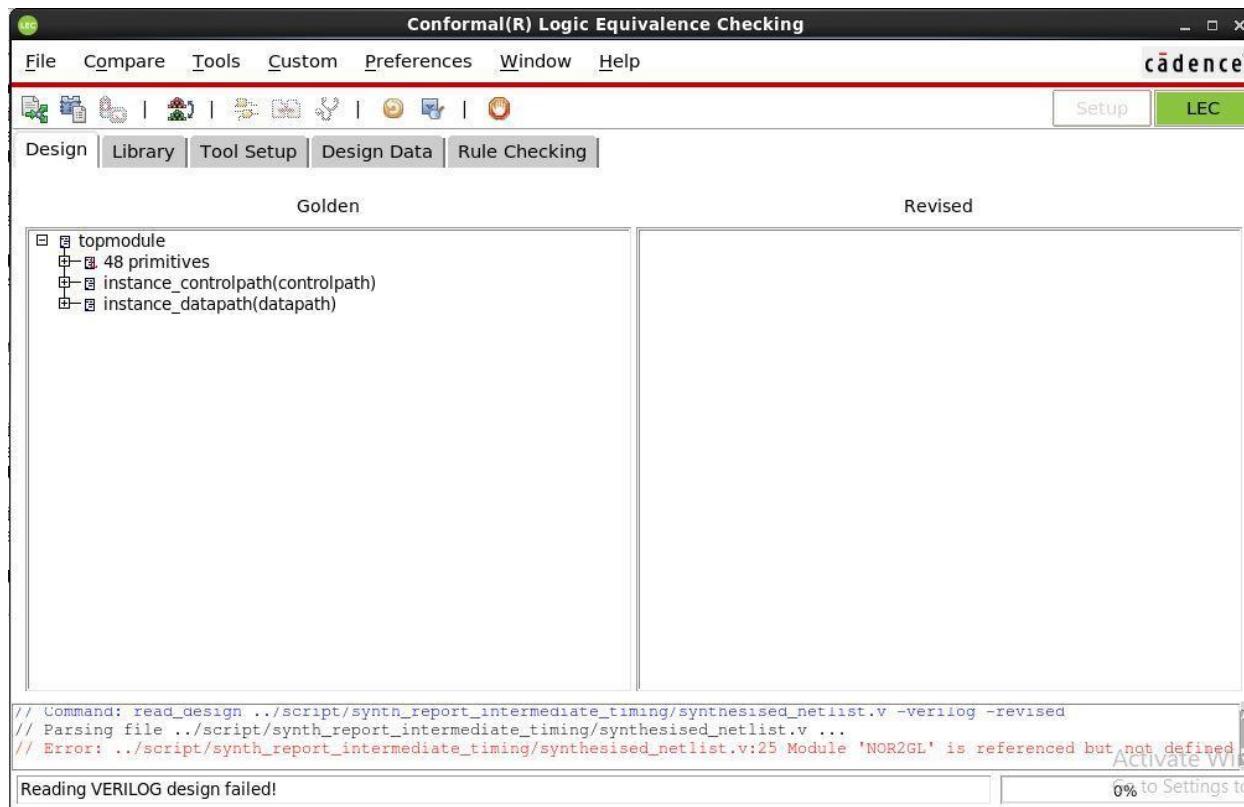
```

// Verification Directory fv/topmodule

module controlpath(C, reset, clk, control_signal);
    input [7:0] C;
    input reset, clk;
    output [1:0] control_signal;
    wire [7:0] C;
    wire reset, clk;
    wire [1:0] control_signal;
    wire n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
    wire n_16;
    DFFQX1 `control_signal_reg[1] (.CK (clk), .D (n_16), .Q
        (control_signal[1]));
    DFFQX1 `control_signal_reg[0] (.CK (clk), .D (n_15), .Q
        (control_signal[0]));
    OAI32X1 g482(.A0 (n_1), .A1 (reset), .A2 (n_13), .B0 (n_3), .B1
        (n_12), .Y (n_16));
    OAI32X1 g483(.A0 (n_2), .A1 (reset), .A2 (n_8), .B0 (n_3), .B1
        (n_14), .Y (n_15));
    NOR2GL g484(.A (n_1), .B (n_11), .Y (n_14)); //NOR2XL --> NOR2GL
    AOI2BB1X1 g485(.A0N (C[5]), .A1N (n_6), .B0 (n_10), .Y (n_13));
    AOI211X1 g486(.A0 (C[4]), .A1 (n_9), .B0 (C[6]), .C0 (C[5]), .Y
        (n_12));
    AOI211X1 g487(.A0 (C[4]), .A1 (n_5), .B0 (C[5]), .Y (n_11));
    AOI211X1 g488(.A0 (C[3]), .A1 (n_7), .B0 (C[4]), .C0 (n_0), .Y
        (n_10));
    OR2XL g489(.A (C[3]), .B (n_7), .Y (n_9));
    AND2X1 g490(.A (n_0), .B (n_6), .Y (n_8));
    NAND2BX1 g491(.AN (C[0]), .B (n_4), .Y (n_7));
    A021X1 g492(.A0 (C[1]), .A1 (C[2]), .B0 (C[3]), .Y (n_5));
    NAND2BX1 g493(.AN (n_4), .B (C[4]), .C (C[3]), .Y (n_6));
    NOR2XL g494(.A (C[2]), .B (C[1]), .Y (n_4));

```

Activate Windows



Analysis of the result obtained:

1. Error is generated while running the tcl script.
2. The error states that the module NOR2GL is not defined. This is because such a module is not defined in the slow.lib library.

BAD NETLIST 4: For the 4th case, a single change is considered in the synthesised_netlist of the intermediate timing report. Inside it, for the instance of DFFQX1, the CK pin is connected to ‘clock’ instead of ‘clk’ port of downcounter module.

```

lechecking.tcl  synthesised_netlist.v
NOR2XL g494(.A (C[2]), .B (C[1]), .Y (n_4));
NAND2BX1 g495(.AN (C[7]), .B (C[6]), .Y (n_2));
NAND2BX1 g496(.AN (reset), .B (C[7]), .Y (n_3));
CLKINVX1 g497(.A (C[6]), .Y (n_1));
INVX1 g498(.A (C[5]), .Y (n_0));
endmodule

module downcounter_6(clk, reset, out);
    input clk, reset;
    output [5:0] out;
    wire clk, reset;
    wire [5:0] out;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
    DFFQX1 \out_reg[5] (.CK (clock), .D (n_15), .Q (out[5])); //clk --> clock
    OAI211X1 g205(.A0 (out[5]), .A1 (n_12), .B0 (n_0), .C0 (n_14), .Y (n_15));
    DFFQX1 \out_reg[4] (.CK (clk), .D (n_13), .Q (out[4]));
    NAND2XL g207(.A (out[5]), .B (n_12), .Y (n_14));
    OAI211XL g208(.A0 (n_9), .A1 (n_2), .B0 (n_0), .C0 (n_12), .Y (n_13));
    DFFQX1 \out_reg[3] (.CK (clk), .D (n_11), .Q (out[3]));
    NAND2XL g210(.A (n_2), .B (n_9), .Y (n_12));
    NAND2XL g211(.A (n_0), .B (n_10), .Y (n_11));
    DFFQX1 \out_reg[2] (.CK (clk), .D (n_8), .Q (out[2]));
    AOI21XL g213(.A0 (out[3]), .A1 (n_7), .B0 (n_9), .Y (n_10));
    NOR2XL g214(.A (out[3]), .B (n_7), .Y (n_9));
    OAI211XL g215(.A0 (n_3), .A1 (n_1), .B0 (n_0), .C0 (n_7), .Y (n_8));
    DFFQX1 \out_reg[1] (.CK (clk), .D (n_6), .Q (out[1]));
    NAND2XL g217(.A (n_1), .B (n_3), .Y (n_7));
    NAND2XL g218(.A (n_0), .B (n_5), .Y (n_6));
    DFFQX1 \out_reg[0] (.CK (clk), .D (n_4), .Q (out[0]));
    AOI21XL g220(.A0 (out[1]), .A1 (out[0]), .B0 (n_3), .Y (n_5));
    NAND2XL g221(.A (n_0), .B (out[0]), .Y (n_4));
    NOR2XL g222(.A (out[0]), .B (out[1]), .Y (n_2));

```

The screenshot shows the Cadence LE (Logic Equivalence Checking) interface. The main window displays two columns: 'Golden' and 'Revised'. Both columns show a tree view of the topmodule structure, which includes 48 primitives and instances for controlpath and datapath. Below the tree, detailed timing reports are provided for each column.

Golden Column:

- CPU time : 41.21 seconds
- Elapse time : 42 seconds
- Memory usage : 405.70 M bytes
- // Command: report_messages -compare -verb 0
- // Command: report_compare_data -noneq
- Compared points are: Non-equivalent
 - (G) + 101 DFF /instance_datapath/counter/out_reg[5]
 - (R) + 53 DFF /instance_datapath/counter/out_reg[5]/U\$1/U\$1
- Due to these Non-equivalent points:
 - [CLOCK]
 - (G) + 29 PI /clock
 - (R) + 107 Z /instance_datapath/counter/clock
- 1 Non-equivalent point(s) reported
- 1 compared point(s) reported

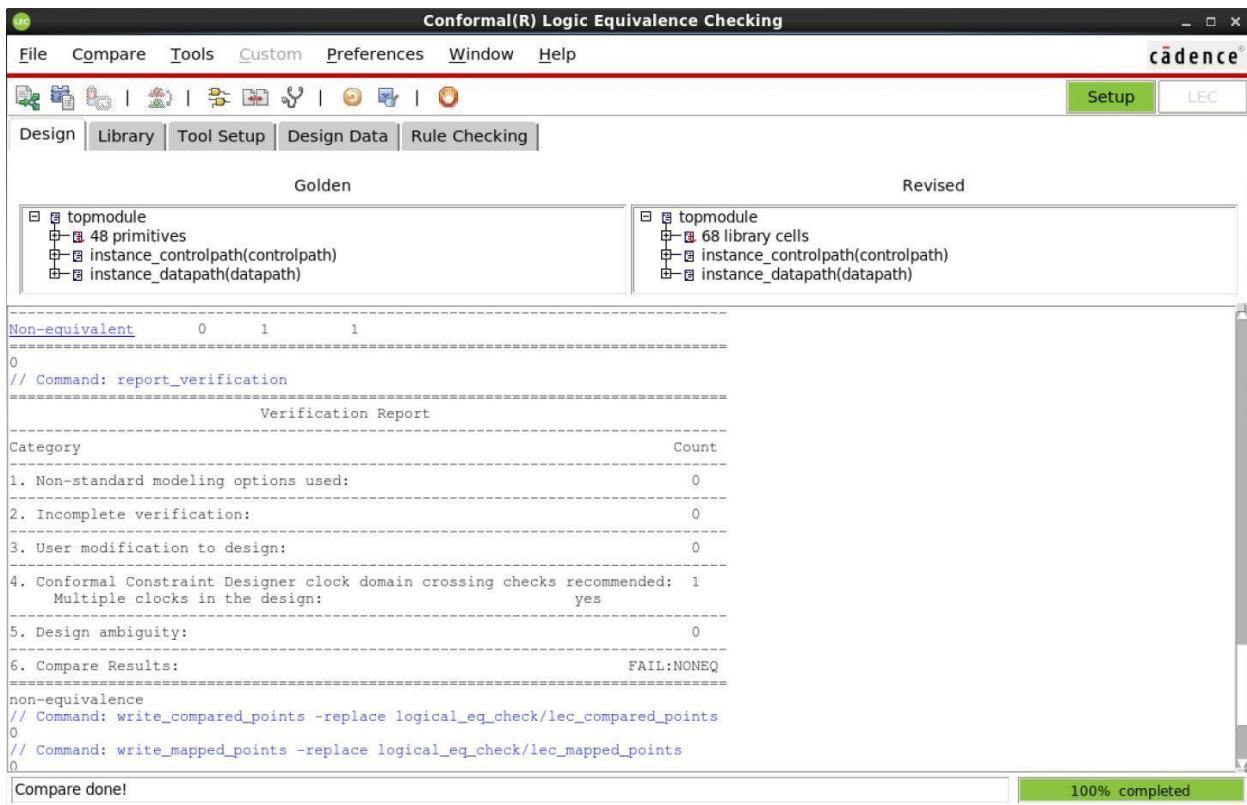
Compared points	PO	DFF	Total
Equivalent	20	55	75
Non-equivalent	0	1	1

// Command: report_verification

Verification Report

Compare done!

Conformal(R) Logic Equivalence Checking



Analysis of the result obtained:

1. The comparison results came out to be ‘Non-Equivalent’ as the report suggests that there are multiple clocks in the design.
2. This is because we connected the D-Flipflop cell clock pin to a different clock not defined in the design.

BAD NETLIST 5: For this case, a single change was done in the synthesized_netlist of the intermediate timing report. Inside it, the name of ‘downcounter’ module was changed to ‘upcounter’.

```

lechecking.tcl  X | synthesised_netlist.v  X
-----
A0I21X1 g487(.A0 (C[4]), .A1 (n_5), .B0 (C[5]), .Y (n_11));
A0I211X1 g488(.A0 (C[3]), .A1 (n_7), .B0 (C[4]), .C0 (n_0), .Y
(n_10));
OR2XL g489(.A (C[3]), .B (n_7), .Y (n_9));
AND2X1 g490(.A (n_0), .B (n_6), .Y (n_8));
NAND2BX1 g491(.AN (C[0]), .B (n_4), .Y (n_7));
A021X1 g492(.A0 (C[1]), .A1 (C[2]), .B0 (C[3]), .Y (n_5));
NAND3BX1 g493(.AN (n_4), .B (C[4]), .C (C[3]), .Y (n_6));
NOR2XL g494(.A (C[2]), .B (C[1]), .Y (n_4));
NAND2BX1 g495(.AN (C[7]), .B (C[6]), .Y (n_2));
NAND2BX1 g496(.AN (reset), .B (C[7]), .Y (n_3));
CLKINVX1 g497(.A (C[6]), .Y (n_1));
INVX1 g498(.A (C[5]), .Y (n_0));
endmodule

module upcounter_6(clk, reset, out);      //downcounter ---> upcounter
  input clk, reset;
  output [5:0] out;
  wire clk, reset;
  wire [5:0] out;
  wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
  wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
  DFFQX1 \out_reg[5] (.CK (clk), .D (n_15), .Q (out[5]));
  OAI211X1 g205(.A0 (out[5]), .A1 (n_12), .B0 (n_0), .C0 (n_14), .Y
(n_15));
  DFFQX1 \out_reg[4] (.CK (clk), .D (n_13), .Q (out[4]));
  NAND2XL g207(.A (out[5]), .B (n_12), .Y (n_14));
  OAI211XL g208(.A0 (n_9), .A1 (n_2), .B0 (n_0), .C0 (n_12), .Y (n_13));
  DFFQX1 \out_reg[3] (.CK (clk), .D (n_11), .Q (out[3]));
  NAND2XL g210(.A (n_2), .B (n_9), .Y (n_12));
  NAND2XL g211(.A (n_0), .B (n_10), .Y (n_11));
  DFFQX1 \out_reg[2] (.CK (clk), .D (n_8), .Q (out[2]));
  A0I21XL g213(.A0 (out[3]), .A1 (n_7), .B0 (n_9), .Y (n_10));
  NOR2XL g214(.A (out[2]), .B (n_7), .Y (n_0));

```

Conformal(R) Logic Equivalence Checking

File Compare Tools Custom Preferences Window Help

Setup LEC

Design Library Tool Setup Design Data Rule Checking

Golden Revised

0 Compared point(s) reported

Compared points	DFF	Total
<u>Non-equivalent</u>	6	6

0 // Command: report_verification

===== Verification Report =====

Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification: All primary outputs are mapped:	1 no
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity:	0
6. Compare Results:	FAIL:NONEQ

non-equivalence
// Command: write_compared_points -replace_logical_eq_check/lec_compared_points

Compare done! 100% completed

Analysis of the result obtained:

1. Here we observe that changing the name of the downcounter module did not incur any error.
2. The tool generates a message, FAIL: INCOMPLETE. That is the INCOMPLETE VERIFICATION has been encountered.
3. Also, it is clearly visible in the snapshot that all the primary output ports are not mapped as the module name has changed.
4. Therefore verification could not be performed between the golden netlist and the revised netlist.

STEP5: STA ANALYSIS

Tool used : Tempus –nowin

Command : source sta_load.tcl

Outcomes : Violation report , setup time report , Hold time report, delay.sdf , and clock reports.

Library slow_load.lib we have made small changes in library to include wireload model



```
/* wire-loads */
wire_load("tsmc18_wl10") {
    resistance : 8.5e-8;
    capacitance : 1.5e-4;
    area : 0.7;
    slope : 66.667;
    fanout_length (1,66.667);
}
```

Above changes are made in slow.lib file to include wire load model

Part 1. Normal STA analysis with corresponding SDC file

Timing reports of STA analysis:

a. Minimum area: QoR

timing_report_setup.rpt (~/work/sta_load/wire_area) - gedit

```

File Edit View Search Tools Documents Help
Open Save Undo Redo Cut Copy Paste Find Replace Select All
area.sdc timing.sdc intermediate.sdc sta_load.tcl synthesis.tcl timing_report_setup.rpt timing_report_hold.rpt
= Slack Time 1.846
Clock Rise Edge 0.000
+ Clock Network Latency (Ideal) 0.010
= Beginpoint Arrival Time 0.010
Instance Arc Cell Delay Arrival Required Time
# in side_reg_reg[0]
CK ^ - - 0.010 1.856
CK ^ -> Y - AND2X1 0.336 1.206 2.326
instance datapath/mul_135_34/g4261 B ^ -> Y A AND2X1 0.267 1.546 2.593
instance datapath/mul_135_34/g2427 A ^ -> S ^ ADDHX1 0.451 1.997 3.843
instance datapath/mul_135_34/g2305 CE v -> CO v ADDFX1 0.348 2.345 3.392
instance datapath/mul_135_34/g2374 CE v -> CO v ADDFX1 0.339 2.684 3.738
instance datapath/mul_135_34/g2365 CE v -> CO v ADDFX1 0.339 3.023 4.069
instance datapath/mul_135_34/g2363 CE v -> CO v ADDFX1 0.339 3.364 4.403
instance datapath/mul_135_34/g2358 CE v -> CO v ADDFX1 0.339 4.378 5.424
instance datapath/mul_135_34/g2354 CE v -> CO v ADDFX1 0.339 4.717 5.763
instance datapath/mul_135_34/g2351 CE v -> CO v ADDFX1 0.339 5.056 6.102
instance datapath/mul_135_34/g2352 CE v -> CO v ADDFX1 0.339 5.394 6.441
instance datapath/mul_135_34/g2351 CE v -> CO v ADDFX1 0.339 5.733 6.788
instance datapath/mul_135_34/g2358 CE v -> CO v ADDFX1 0.339 6.072 7.118
instance datapath/mul_135_34/g2349 CE v -> CO v ADDFX1 0.339 6.411 7.457
instance datapath/mul_135_34/g2348 CE v -> CO v ADDFX1 0.339 6.758 7.796
instance datapath/mul_135_34/g2347 CE v -> CO v ADDFX1 0.339 7.888 8.135
instance datapath/mul_135_34/g2346 CE v -> S ^ ADDFX1 0.471 7.568 8.086
instance datapath/g714 B ^ -> Y ^ AND2X1 0.220 7.779 8.026
M_req[18]
Slack = 1.046 [MET]

```

Header which include start point ,endpoint and path group

Time period

Plain Text Tab Width: 8 Ln 20, Col 38 INS

timing_report_setup.rpt akash21185@edaserv... work [Inbox (4) - vdfproject...] sta_load wire_area

timing_report_hold.rpt (~/work/sta_load/wire_area) - gedit

```

File Edit View Search Tools Documents Help
Open Save Undo Redo Cut Copy Paste Find Replace Select All
area.sdc timing.sdc intermediate.sdc sta_load.tcl synthesis.tcl timing_report_setup.rpt timing_report_hold.rpt
#####
# Generated by: Cadence Tempus 20.10-p003 1
# OS: Linux x86_64 (Host ID edaserver4)
# Generated on: Fri Apr 8 17:08:50 2022
# Design: topmodule
# Command: report timing -early > $report_dir/timing_report_hold.rpt
#####
Path 1: MET Hold Check with Pin A in side_reg_reg[0]/CK
Endpoint: A in side_reg_reg[0]/D (v) checked with leading edge of 'clock'
Beginpoint: A[0] (v) triggered by leading edge of 'clock'
Path Groups: {clock}
Other End Arrival Time 0.010
+ Hold 0.000
+ Phase Shift 0.000
+ Uncertainty 0.020
= Required Time 0.110
Arrival Time 0.110
Slack Time 0.000
Clock Rise Edge 0.000
+ Input Delay 0.000
+ Network Insertion Delay 0.010
= Beginpoint Arrival Time 0.110
Instance Arc Cell Delay Arrival Required Time
A[0] v - - 0.110 0.110
A_in_side_reg_reg[0] D v DFQFX1 0.000 0.110 0.110

```

NO Hold violation happens

Plain Text Tab Width: 8 Ln 1, Col 1 INS

timing_report_hold.rpt akash21185@edaserv... work [Inbox (4) - vdfproject...] sta_load wire_area

Report Analysis:

Above setup report snapshot of path 1 is attached. There are a total of 46 paths reported by the tempus while performing STA . In path 1, for M_reg[18]/ck rising. The Real Time analysis is taking into account the data path slew and uncertainty of 0.020 ns setup threshold of 0.164. End point: M_reg[18]/D checked with leading edge of ‘clock’. And Begin point is B_in_side_reg_reg[0]/Q triggered by leading edge of clock.

Flow path path is beginning with B_in_side_reg_reg[0] with positive triggering edge of clock at time 0 and initial uncertainty is defined as 0.010. After this signal is launched by DFFQX1 having delay of 0.919 ns , after this if we trace the path signal is propagated through instance_datapath and multiply mult/instances.similarly all the delays of instance are added up and resulted into arrived time. Now at end point capture flipflop will have next clock edge greater than its arriaved time inorder to met positive slack. No timing violation is happened for minimum area STA analysis.We can see in all violation reports.

Considering HOLD report no violation occurs

Slack = Required time – arrived time

= 9.00- 7.954

= 1.046

a. Minimum time (slightly negative slack):

STA QoR analysis :

```

Applications Places System Firefox Gedit
timing_report_setup.rpt (~/work/sta_load/wire_timing) - gedit
Fri Apr 8, 5:15 PM akash21185
File Edit View Search Tools Documents Help
Open Save Undo Redo Cut Copy Paste Find Replace
area.sdc timing.sdc intermediate.sdc sta_load.tcl synthesis.tcl timing_report_setup.rpt timing_report_hold.rpt
#####
# Generated by: Cadence Tempus 20.10-p003.1
# OS: Linux x86_64 (Host ID edaserver4)
# Generated on: Fri Apr 8 17:13:29 2022
# Design: topmodule
# Command: report_timing -late > $report_dir/timing_report_setup.rpt
#####
Path 1: VIOLATED Setup Check with Pin M_reg[18]/CK
Endpoint: M_reg[18]/D (^) checked with leading edge of 'clock'
Beginpoint: A_in_side_reg_reg[4]/0 (v) triggered by leading edge of 'clock'
Path Groups: {clock}
Other End Arrival Time 0.000
+ Setup 0.151
+ Phase Shift 3.185
- Uncertainty 0.100
Required Time 2.934
- Arrival Time 3.141
= Slack Time -0.207
Clock Rise Edge 0.000
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time 0.000
-----
Instance Arc Cell Delay Arrival Required
Time Time
-----
A_in_side_reg_reg[4] CK ^ - - 0.000 -0.207
A_in_side_reg_reg[4] CK ^ -> Q v DFFH0X8 0.419 0.419 0.212
instance_datapath/mul_135_34/g9659 A v -> Y v BUFX20 0.160 0.578 0.372
instance_datapath/mul_135_34/g5860_dup A v -> Y ^ CLKINVX20 0.070 0.649 0.442
instance_datapath/mul_135_34/g9666 A ^ -> Y v CLKINVX20 0.057 0.705 0.499
instance_datapath/mul_135_34/g7453 A v -> Y ^ CLKINVX16 0.060 0.765 0.559
instance_datapath/mul_135_34/g833 B ^ -> Y v NOR2X8 0.039 0.805 0.598
instance_datapath/mul_135_34/g838 A1 v -> Y ^ OA121X4 0.113 0.918 0.711
instance_datapath/mul_135_34/g8449 A1 v -> Y ^ CLKAND2X12 0.178 1.096 0.889
instance_datapath/mul_135_34/g8398 A ^ -> Y v CLKINVX12 0.058 1.154 0.948
instance_datapath/mul_135_34/f0pt5933 A ^ -> Y v NAND2X8 0.071 1.225 1.019
instance_datapath/mul_135_34/g6726 B v -> Y ^ NAND2X8 0.112 1.388 1.181
instance_datapath/mul_135_34/g8763 C ^ -> Y v NAND3X8 0.163 1.388 1.181
instance_datapath/mul_135_34/g8762 A v -> Y ^ NAND2X8 0.137 1.525 1.318
instance_datapath/mul_135_34/g7849 A ^ -> Y v CLKINVX12 0.075 1.600 1.393
instance_datapath/mul_135_34/g7158_dup B v -> Y ^ NAND2X8 0.063 1.662 1.456
instance_datapath/mul_135_34/g7853 B ^ -> Y v NAND2X8 0.081 1.743 1.537
instance_datapath/mul_135_34/g9728 B v -> Y ^ NAND2X8 0.072 1.815 1.608
instance_datapath/mul_135_34/f0pt9727 A ^ -> Y v CLKINVX12 0.049 1.864 1.658
instance_datapath/mul_135_34/g7939 B v -> Y ^ NOR2X4 0.112 1.976 1.769
instance_datapath/mul_135_34/g92 C ^ -> Y v NOR3X6 0.074 2.050 1.843
instance_datapath/mul_135_34/g91 A v -> Y ^ NOR2X8 0.119 2.169 1.962
instance_datapath/mul_135_34/g10817 B ^ -> Y v NOR2X8 0.069 2.238 2.031
instance_datapath/mul_135_34/g6229 B v -> Y ^ NOR2X8 0.073 2.311 2.105
instance_datapath/mul_135_34/g10934 B0 ^ -> Y v OA121X4 0.099 2.410 2.204
instance_datapath/mul_135_34/g10932 B v -> Y v CLKAND2X12 0.181 2.591 2.385
instance_datapath/mul_135_34/g9863 B v -> Y ^ NAND2X8 0.065 2.656 2.450
instance_datapath/mul_135_34/g9862 B ^ -> Y v NAND2X8 0.095 2.751 2.545
instance_datapath/mul_135_34/g20 A v -> Y ^ INVX16 0.092 2.844 2.637
instance_datapath/mul_135_34/g17 B ^ -> Y v NAND2X4 0.117 2.960 2.754
instance_datapath/mul_135_34/g10668 B v -> Y ^ NAND3X8 0.073 3.034 2.827
instance_datapath/g741 B ^ -> Y ^ CLKAND2X6 0.107 3.141 2.934
M_reg[18] D ^ DFFX4 0.000 3.141 2.934
-----
```

```

Plain Text Tab Width: 8 Ln 1, Col 1 INS
timing_report_setup.rpt akash21185@edaserv... work [Inbox (4) - vdfproject...] sta_load wire_timing
area.sdc timing.sdc intermediate.sdc sta_load.tcl synthesis.tcl timing_report_setup.rpt timing_report_hold.rpt
A in side reg reg[4] CK ^ - - 0.000 -0.207
A in side reg reg[4] CK ^ -> Q v DFFH0X8 0.419 0.419 0.212
instance_datapath/mul_135_34/g9659 A v -> Y v BUFX20 0.160 0.578 0.372
instance_datapath/mul_135_34/g5860_dup A v -> Y ^ CLKINVX20 0.070 0.649 0.442
instance_datapath/mul_135_34/g9666 A ^ -> Y v CLKINVX20 0.057 0.705 0.499
instance_datapath/mul_135_34/g7453 A v -> Y ^ CLKINVX16 0.060 0.765 0.559
instance_datapath/mul_135_34/g833 B ^ -> Y v NOR2X8 0.039 0.805 0.598
instance_datapath/mul_135_34/g838 A1 v -> Y ^ OA121X4 0.113 0.918 0.711
instance_datapath/mul_135_34/g8449 A1 v -> Y ^ CLKAND2X12 0.178 1.096 0.889
instance_datapath/mul_135_34/g8398 A ^ -> Y v CLKINVX12 0.058 1.154 0.948
instance_datapath/mul_135_34/f0pt5933 A ^ -> Y v NAND2X8 0.071 1.225 1.019
instance_datapath/mul_135_34/g6726 B v -> Y ^ NAND2X8 0.112 1.388 1.181
instance_datapath/mul_135_34/g8763 C ^ -> Y v NAND3X8 0.163 1.388 1.181
instance_datapath/mul_135_34/g8762 A v -> Y ^ NAND2X8 0.137 1.525 1.318
instance_datapath/mul_135_34/g7849 A ^ -> Y v CLKINVX12 0.075 1.600 1.393
instance_datapath/mul_135_34/g7158_dup B v -> Y ^ NAND2X8 0.063 1.662 1.456
instance_datapath/mul_135_34/g7853 B ^ -> Y v NAND2X8 0.081 1.743 1.537
instance_datapath/mul_135_34/g9728 B v -> Y ^ NAND2X8 0.072 1.815 1.608
instance_datapath/mul_135_34/f0pt9727 A ^ -> Y v CLKINVX12 0.049 1.864 1.658
instance_datapath/mul_135_34/g7939 B v -> Y ^ NOR2X4 0.112 1.976 1.769
instance_datapath/mul_135_34/g92 C ^ -> Y v NOR3X6 0.074 2.050 1.843
instance_datapath/mul_135_34/g91 A v -> Y ^ NOR2X8 0.119 2.169 1.962
instance_datapath/mul_135_34/g10817 B ^ -> Y v NOR2X8 0.069 2.238 2.031
instance_datapath/mul_135_34/g6229 B v -> Y ^ NOR2X8 0.073 2.311 2.105
instance_datapath/mul_135_34/g10934 B0 ^ -> Y v OA121X4 0.099 2.410 2.204
instance_datapath/mul_135_34/g10932 B v -> Y v CLKAND2X12 0.181 2.591 2.385
instance_datapath/mul_135_34/g9863 B v -> Y ^ NAND2X8 0.065 2.656 2.450
instance_datapath/mul_135_34/g9862 B ^ -> Y v NAND2X8 0.095 2.751 2.545
instance_datapath/mul_135_34/g20 A v -> Y ^ INVX16 0.092 2.844 2.637
instance_datapath/mul_135_34/g17 B ^ -> Y v NAND2X4 0.117 2.960 2.754
instance_datapath/mul_135_34/g10668 B v -> Y ^ NAND3X8 0.073 3.034 2.827
instance_datapath/g741 B ^ -> Y ^ CLKAND2X6 0.107 3.141 2.934
M_reg[18] D ^ DFFX4 0.000 3.141 2.934
-----
```

```

Plain Text Tab Width: 8 Ln 1, Col 1 INS
timing_report_setup.rpt akash21185@edaserv... work [Inbox (4) - vdfproject...] sta_load wire_timing
area.sdc timing.sdc intermediate.sdc sta_load.tcl synthesis.tcl timing_report_setup.rpt timing_report_hold.rpt

```

```

#####
# Generated by: Cadence Tempus 20.10-p003_1
# Host: Linux-006-64(Host ID edaserver4)
# Generated on: Fri Apr  8 17:13:29 2022
# Design: topmodule
# Command: report timing -early > $report dir/timing_report_hold.rpt
#####
Path 1: VIOLATED Hold Check with Pin B_in_side_reg_reg[4]/CK
Endpoint: B_in_side_reg_reg[4]/D (v) checked with leading edge of 'clock'
Beginpoint: B[4] (v) triggered by leading edge of 'clock'
Path Groups: {clock}
Other_End_Arrival_Time 0.000
+ Hold 0.080
+ Phase_Shift 0.000
+ Uncertainty 0.100
= Required_Time 0.100
= Arrival_Time 0.100
Slack_Time -0.080
Clock_Rise_Edge 0.060
+ Input_Delay 0.160
= Beginpoint_Arrival_Time 0.100
-----
Instance Arc Cell Delay Arrival Required Time Time
----- -
B[4] v - 0.100 0.180
B_in_side_reg_reg[4] D v DFFHQX8 0.000 0.100 0.180

```

Hold report

Report Analysis: While analysis setup report we observed that setup check is violated as during synthesis we have already taken path 1 snapshot is attached with path group <clock>.

Beginpoint : A_in_side_reg_reg[4]/Q triggered by leading edge of clock.

Slack calculation : required time – arrived time

$$= 2.934 - 3.141$$

$$= -0.207 \text{ ps (setup violation)}$$

STA QoR analysis :

C. Intermediate conditions with positive slack and optimized area Timing reports:

The screenshot shows a Gedit window displaying a STA timing report. The window title is "timing_report_setup.rpt (~/work/sta_load_intermediate/wire_area) - gedit". The status bar indicates "Fri Apr 8, 5:20 PM akash21185". The menu bar includes File, Edit, View, Search, Tools, Documents, Help. The toolbar includes Open, Save, Undo, Redo, Cut, Copy, Paste, Find, Replace, Select All, and Find Next.

The report content starts with header information:

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edaserver4)
# Generated on: Fri Apr 8 17:19:29 2022
# Design: topmodule
# Command: report timing -late > $report_dir/timing_report_setup.rpt
#####
Path 1: MET Setup Check with Pin M_reg[18]/CK
```

It details a specific path from an endpoint to a beginpoint, including arrival times and slack times for various stages of the clock network.

```
Endpoint: M_reg[18]/D (^) checked with leading edge of 'clock'
Beginpoint: B_in_side_reg_reg[0]/0 (^) triggered by leading edge of 'clock'
Path Groups: {clock}
Other End Arrival Time      0.000
- Setup                      0.164
+ Phase Shift                8.000
- Uncertainty                 0.012
= Required Time               7.824
- Arrival Time                7.769
= Slack Time                  0.054
  Clock Rise Edge            0.000
  + Clock Network Latency (Ideal) 0.000
  = Beginpoint Arrival Time    0.000
-----
Instance          Arc           Cell       Delay   Arrival Required
                    Time          Time
-----
```

Instance	Arc	Cell	Delay	Arrival Time	Required Time
B_in_side_reg_reg[0]	CK ^	-	-	0.000	0.054
B_in_side_reg_reg[0]	CK ^ -> Q ^	DFFOX1	0.919	0.919	0.974
instance_datapath/mul_135_34/g2489	B ^ -> Y ^	AND2X1	0.350	1.270	1.324
instance_datapath/mul_135_34/g2427	A ^ -> S ^	ADDHX1	0.267	1.536	1.591
instance_datapath/mul_135_34/g2419	CI ^ -> S v	ADDFX1	0.451	1.987	2.041
instance_datapath/mul_135_34/g2381	A v -> CO v	ADDFX1	0.348	2.335	2.390
instance_datapath/mul_135_34/g2374	CI v -> CO v	ADDFX1	0.339	2.674	2.728
instance_datapath/mul_135_34/g2365	CI v -> CO v	ADDFX1	0.339	3.013	3.067

At the bottom, there are tabs for "timing_report_setup.rpt", "akash21185@edaserv...", "work", "[Inbox (4) - vdfproject...", "sta_load_intermediate", and "wire_area". The status bar also shows "Plain Text", "Tab Width: 8", "Ln 1, Col 1", and "INS".

Fri Apr 8, 5:20 PM akash21185

timing_report_setup.rpt (~/work/sta_load_intermediate/wire_area) - gedit

```

Slack Time          0.054
Clock Rise Edge    0.000
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time 0.000
-----
Instance           Arc      Cell     Delay   Arrival Required
                           Time     Time
-----
```

Instance	Arc	Cell	Delay	Arrival Time	Required Time
B_in_side_reg_reg[0]	CK ^	-	-	0.000	0.054
B_in_side_reg_reg[0]	CK ^ -> Q ^	DFFQX1	0.919	0.919	0.974
instance_datapath/mul_135_34/g2489	B ^ -> Y ^	AND2X1	0.350	1.270	1.324
instance_datapath/mul_135_34/g2427	A ^ -> S ^	ADDHX1	0.267	1.536	1.591
instance_datapath/mul_135_34/g2419	C1 ^ -> S v	ADDFX1	0.451	1.987	2.041
instance_datapath/mul_135_34/g2381	A v -> CO v	ADDFX1	0.348	2.335	2.390
instance_datapath/mul_135_34/g2374	C1 v -> CO v	ADDFX1	0.339	2.674	2.728
instance_datapath/mul_135_34/g2365	C1 v -> CO v	ADDFX1	0.339	3.013	3.067
instance_datapath/mul_135_34/g2363	C1 v -> CO v	ADDFX1	0.339	3.352	3.406
instance_datapath/mul_135_34/g2357	C1 v -> CO v	ADDFX1	0.339	3.690	3.745
instance_datapath/mul_135_34/g2356	C1 v -> CO v	ADDFX1	0.339	4.029	4.084
instance_datapath/mul_135_34/g2355	C1 v -> CO v	ADDFX1	0.339	4.368	4.422
instance_datapath/mul_135_34/g2354	C1 v -> CO v	ADDFX1	0.339	4.707	4.761
instance_datapath/mul_135_34/g2353	C1 v -> CO v	ADDFX1	0.339	5.046	5.100
instance_datapath/mul_135_34/g2352	C1 v -> CO v	ADDFX1	0.339	5.384	5.439
instance_datapath/mul_135_34/g2351	C1 v -> CO v	ADDFX1	0.339	5.723	5.778
instance_datapath/mul_135_34/g2350	C1 v -> CO v	ADDFX1	0.339	6.062	6.116
instance_datapath/mul_135_34/g2349	CI v -> CO v	ADDFX1	0.339	6.401	6.455
instance_datapath/mul_135_34/g2348	CI v -> CO v	ADDFX1	0.339	6.740	6.794
instance_datapath/mul_135_34/g2347	CI v -> CO v	ADDFX1	0.339	7.078	7.133
instance_datapath/mul_135_34/g2346	CI v -> S ^	ADDFX1	0.471	7.550	7.604
instance_datapath/g714	B ^ -> Y ^	AND2X1	0.220	7.769	7.824
M_reg[18]	D ^	DFFHQX8	0.000	7.769	7.824

Plain Text ▾ Tab Width: 8 ▾ Ln 1, Col 1 INS

timing_report_hold.rpt (~/work/sta_load_intermediate/wire_area) - gedit

```

Fri Apr 8, 5:20 PM akash21185

#####
# Generated by: Cadence Tempus 20.10-p003.1
# OS: Linux x86_64(Host ID: edaserver4)
# Generated on: Fri Apr 8 17:19:29 2022
# Design: topmodule
# Command: report timing -early > $report_dir/timing_report_hold.rpt
#####

Path 1: MET Hold Check with Pin A_in_side_reg_reg[0]/D (v) checked with v leading edge of 'clock'
Endpoint: A_in_side_reg_reg[0]/D (v) checked with v leading edge of 'clock'
Beginpoint: A[0] (v) triggered by v leading edge of 'clock'
Path Groups: {clock}
Other End Arrival Time 0.000
+ Hold 0.080
+ Phase Shift 0.000
+ Uncertainty 0.012
= Required Time 0.092
Arrival Time 0.100
Slack Time 0.008
Clock Rise Edge 0.000
+ Input Delay 0.100
= Beginpoint Arrival Time 0.100
-----
Instance           Arc      Cell     Delay   Arrival Required
                           Time     Time
-----
```

Instance	Arc	Cell	Delay	Arrival Time	Required Time
A_in_side_reg_reg[0]	A[0] v -	-	0.100	0.092	
A_in_side_reg_reg[0]	D v	DFFQX1	0.000	0.100	0.092

Plain Text ▾ Tab Width: 8 ▾ Ln 1, Col 1 INS

Slack calculation : required time – arrived time
 $= 2.934 - 3.141$
 $= -0.207 \text{ ps (setup violation)}$

Report Analysis:

STA analysis of minimum area (a)with wire load model while considering SDC constraints of intermediate condition :

```
# Generated by: Cadence Tempus 20.10-p083.1
# OS: Linux x86_64 (Host ID edaserver4)
# Generated on: Fri Apr 8 17:19:29 2022
# Design: topmodule
# Command: report timing -late > $report_dir/timing_report_setup.rpt
#####
Path 1: MET Setup Check with Pin M_Reg[18]/CK
Endpoint: M_Reg[18]/D (^) checked with leading edge of 'clock'
Beginpoint: B_in_side_reg_reg[0]/0 (^) triggered by leading edge of 'clock'
Path Groups: {clock}
Other End Arrival Time      0.000
- Setup                      0.164
+ Phase Shift                8.000
- Uncertainty                 0.012
= Required Time              7.824
- Arrival Time                7.769
= Slack Time                  0.054
Clock Rise Edge              0.000
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time    0.000
-----
Instance          Arc        Cell       Delay   Arrival  Required
                           Time     Time
-----
```

Instance	Arc	Cell	Delay	Arrival Time	Required Time
B_in_side_reg_reg[0]	CK ^	-	-	0.000	0.054
B_in_side_reg_reg[0]	CK ^ -> Q ^	DFFQX1	0.919	0.919	0.974
instance_datapath/mul_135_34/g2489	B ^ -> Y ^	AND2X1	0.358	1.270	1.324
instance_datapath/mul_135_34/g2427	A ^ -> S ^	ADDHX1	0.267	1.536	1.591
instance_datapath/mul_135_34/g2419	C1 ^ -> S v	ADDFX1	0.451	1.987	2.041
instance_datapath/mul_135_34/g2381	A v -> C0 v	ADDFX1	0.348	2.335	2.390
instance_datapath/mul_135_34/g2374	C1 v -> C0 v	ADDFX1	0.339	2.674	2.728
instance_datapath/mul_135_34/g2365	C1 v -> C0 v	ADDFX1	0.339	3.013	3.067

Setup slack is 0.054 (positive value).

From above STA reports having wire load model with intermediate sdc constraints we get the setup slack and hold slack conditions are met.

Slack calculation

Slack calculation : required time – arrived time

$$= 7.824 - 7.769$$

$$= 0.054 \text{ ps (setup slack MET)}$$

0% violation signifies that no violations have occurred. Beginpoint: B_in_side_reg_reg[0]/0 triggering by positive leading edge and endpoint M_Reg[18]/CK checked with leading edge of clock .

Uncertainty = 0.012ps ,

Hold slack = required time – arrived time

$$0.100 - 0.092$$

$$= 0.008$$

Fri Apr 8, 5:20 PM akash21185

timing_report_setup.rpt (~/work/sta_load_intermediate/wire_area) - gedit

File Edit View Search Tools Documents Help

Open Save Undo Redo Cut Copy Paste Find Replace Select All

area.sdc timing.sdc intermediate.sdc sta_load.tcl synthesis.tcl timing_report_setup.rpt timing_report_hold.rpt

```

= Slack Time          0.054
Clock Rise Edge      0.000
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time 0.000
-----
Instance           Arc   Cell    Delay  Arrival Required
                           Time   Time
-----
B_in_side_reg_reg[0] CK ^   -     -     0.000  0.054
B_in_side_reg[0]    CK ^ -> Q ^  DFFQX1  0.919  0.919  0.974
instance_datapath/mul_135_34/g2489 B ^ -> Y ^  AND2X1  0.350  1.270  1.324
instance_datapath/mul_135_34/g2427 A ^ -> S ^  ADDHX1  0.267  1.536  1.591
instance_datapath/mul_135_34/g2419 CI ^ -> S v  ADDFX1  0.451  1.987  2.041
instance_datapath/mul_135_34/g2381 A v -> CO v ADDFX1  0.348  2.335  2.390
instance_datapath/mul_135_34/g2374 CI v -> CO v ADDFX1  0.339  2.674  2.728
instance_datapath/mul_135_34/g2365 CI v -> CO v ADDFX1  0.339  3.013  3.067
instance_datapath/mul_135_34/g2363 CI v -> CO v ADDFX1  0.339  3.352  3.406
instance_datapath/mul_135_34/g2357 CI v -> CO v ADDFX1  0.339  3.690  3.745
instance_datapath/mul_135_34/g2356 CI v -> CO v ADDFX1  0.339  4.029  4.084
instance_datapath/mul_135_34/g2355 CI v -> CO v ADDFX1  0.339  4.368  4.422
instance_datapath/mul_135_34/g2354 CI v -> CO v ADDFX1  0.339  4.707  4.761
instance_datapath/mul_135_34/g2353 CI v -> CO v ADDFX1  0.339  5.046  5.100
instance_datapath/mul_135_34/g2352 CI v -> CO v ADDFX1  0.339  5.384  5.439
instance_datapath/mul_135_34/g2351 CI v -> CO v ADDFX1  0.339  5.723  5.778
instance_datapath/mul_135_34/g2350 CI v -> CO v ADDFX1  0.339  6.062  6.116
instance_datapath/mul_135_34/g2349 CI v -> CO v ADDFX1  0.339  6.401  6.455
instance_datapath/mul_135_34/g2348 CI v -> CO v ADDFX1  0.339  6.740  6.794
instance_datapath/mul_135_34/g2347 CI v -> S ^  ADDFX1  0.339  7.078  7.133
instance_datapath/mul_135_34/g2346 CI v -> S ^  ADDFX1  0.471  7.550  7.604
instance_datapath/mul_135_34/g714 B ^ -> Y ^  AND2X1  0.220  7.769  7.824
M_reg[18]           D ^             DFFHQX8  0.000  7.769  7.824
-----
```

Plain Text Tab Width: 8 Ln 1, Col 1 INS

timing_report_hold.rpt (~/work/sta_load_intermediate/wire_area) - gedit

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Open Save Undo Redo Cut Copy Paste Find Replace Select All

area.sdc timing.sdc intermediate.sdc sta_load.tcl synthesis.tcl timing_report_setup.rpt timing_report_hold.rpt

```

#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64 (Host ID edaserver4)
# Generated on: Fri Apr 8 17:19:29 2022
# Design: topmodule
# Command: report timing -early > $report_dir/timing_report_hold.rpt
#####

Path 1: MET Hold Check with Pin A_in_side_reg_reg[0]/CK
Endpoint: A_in_side_reg_reg[0]/D (v) checked with leading edge of 'clock'
Beginpoint: A[0]
(v) triggered by leading edge of 'clock'
Path Groups: {clock}
Other End Arrival Time 0.000
+ Hold 0.000
+ Phase Shift 0.000
+ Uncertainty 0.012
= Required Time 0.092
Arrival Time 0.100
Slack Time 0.008
Clock Rise Edge 0.000
+ Input Delay 0.100
= Beginpoint Arrival Time 0.100
-----
Instance           Arc   Cell    Delay  Arrival Required
                           Time   Time
-----
- A[0] v - - 0.100  0.092
A_in_side_reg_reg[0] D v  DFFQX1  0.000  0.100  0.092
-----
```

Plain Text Tab Width: 8 Ln 1, Col 1 INS

Report Analysis:

STA analysis of minimum timing (b)with wire load model while considering SDC constraints of intermediate condition :

timing_report_setup.rpt (~/work/sta_load_intermediate/wire_timing) - gedit

```

#####
# Generated by: Cadence Tempus 20.10-p003.1
# OS: Linux x86_64(Host ID edaserver4)
# Generated on: Fri Apr 8 17:26:00 2022
# Design: topmodule
# Command: report timing -late > $report_dir/timing_report_setup.rpt
#####

Path 1: MET Setup Check with Pin M_reg[18]/CK
Endpoint: M_reg[18]/D          ('') checked with leading edge of 'clock'
Beginpoint: A_in_side_reg[4]/0 (v) triggered by leading edge of 'clock'
Path Groups: {clock}
Other End Arrival Time      0.000
- Setup                      0.151
+ Phase Shift                8.000
- Uncertainty                 0.012
= Required Time              7.837
- Arrival Time               3.141
= Slack Time                 4.696
    Clock Rise Edge           0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time   0.000
-----
Instance                     Arc       Cell     Delay   Arrival Required
                           Time      Time     Time
-----
A_in_side_reg[4]            CK ^      -        0.000  4.696
A_in_side_reg[4]            CK ^ -> Q v  DFHFHQX8  0.419  0.418  5.115
instance_datapath/mul_135_34/g99659 A v -> Y v  BUFX20  0.160  0.578  5.275
instance_datapath/mul_135_34/g5860_dup A v -> Y ^  CLKINVX20 0.070  0.649  5.345
instance_datapath/mul_135_34/g9666_ A ^ -> Y v  CLKINVX20 0.057  0.705  5.402
instance_datapath/mul_135_34/g7453 A v -> Y ^  CLKINVX16 0.060  0.765  5.462
instance_datapath/mul_135_34/g83     B ^ -> Y v  NOR2X8  0.039  0.805  5.501
instance_datapath/mul_135_34/g8449 A1 v -> Y ^  OAII2X4  0.113  0.918  5.614
-----
```

timing_report_setup.rpt (~/work/sta_load_intermediate/wire_timing) - gedit

```

#####
# Generated by: Cadence Tempus 20.10-p003.1
# OS: Linux x86_64(Host ID edaserver4)
# Generated on: Fri Apr 8 17:26:00 2022
# Design: topmodule
# Command: report timing -late > $report_dir/timing_report_setup.rpt
#####

Path 1: MET Setup Check with Pin M_reg[18]/CK
Endpoint: M_reg[18]/D          ('') checked with leading edge of 'clock'
Beginpoint: A_in_side_reg[4]/0 (v) triggered by leading edge of 'clock'
Path Groups: {clock}
Other End Arrival Time      0.000
- Setup                      0.151
+ Phase Shift                8.000
- Uncertainty                 0.012
= Required Time              7.837
- Arrival Time               3.141
= Slack Time                 4.696
    Clock Rise Edge           0.000
    + Clock Network Latency (Ideal) 0.000
    = Beginpoint Arrival Time   0.000
-----
Instance                     Arc       Cell     Delay   Arrival Required
                           Time      Time     Time
-----
A_in_side_reg[4]            CK ^      -        0.000  4.696
A_in_side_reg[4]            CK ^ -> Q v  DFHFHQX8  0.419  0.418  5.115
instance_datapath/mul_135_34/g99659 A v -> Y v  BUFX20  0.160  0.578  5.275
instance_datapath/mul_135_34/g5860_dup A v -> Y ^  CLKINVX20 0.070  0.649  5.345
instance_datapath/mul_135_34/g9666_ A ^ -> Y v  CLKINVX20 0.057  0.705  5.402
instance_datapath/mul_135_34/g7453 A v -> Y ^  CLKINVX16 0.060  0.765  5.462
instance_datapath/mul_135_34/g83     B ^ -> Y v  NOR2X8  0.039  0.805  5.501
instance_datapath/mul_135_34/g8449 A1 v -> Y ^  OAII2X4  0.113  0.918  5.614
-----
```

timing_report_setup.rpt (~/work/sta_load_intermediate/wire_area) - gedit

```

Slack Time          0.054
Clock Rise Edge    0.000
+ Clock Network Latency (Ideal) 0.000
= Beginpoint Arrival Time 0.000
-----
Instance           Arc      Cell     Delay   Arrival  Required
                           Cell    Delay   Time     Time
-----
```

Instance	Arc	Cell	Delay	Arrival Time	Required Time
B_in_side_req_reg[8]	CK ^ -> Q ^	DFFOX1	0.919	0.919	0.974
B_in_side_req_reg[8]	CK ^ -> Y ^	AND2X1	0.350	1.270	1.324
instance_datapath/mul_135_34/g2489	A ^ -> S ^	ADDHX1	0.267	1.536	1.591
instance_datapath/mul_135_34/g2427	A v -> C0 v	ADDFX1	0.451	1.987	2.041
instance_datapath/mul_135_34/g2419	C1 ^ -> S v	ADDFX1	0.348	2.335	2.390
instance_datapath/mul_135_34/g2381	A v -> C0 v	ADDFX1	0.339	2.674	2.728
instance_datapath/mul_135_34/g2374	C1 v -> C0 v	ADDFX1	0.339	3.013	3.067
instance_datapath/mul_135_34/g2365	C1 v -> C0 v	ADDFX1	0.339	3.352	3.406
instance_datapath/mul_135_34/g2363	CI v -> C0 v	ADDFX1	0.339	3.690	3.745
instance_datapath/mul_135_34/g2357	CI v -> C0 v	ADDFX1	0.339	4.029	4.084
instance_datapath/mul_135_34/g2356	CI v -> C0 v	ADDFX1	0.339	4.368	4.422
instance_datapath/mul_135_34/g2355	CI v -> C0 v	ADDFX1	0.339	4.707	4.761
instance_datapath/mul_135_34/g2354	CI v -> C0 v	ADDFX1	0.339	5.046	5.100
instance_datapath/mul_135_34/g2353	CI v -> C0 v	ADDFX1	0.339	5.384	5.439
instance_datapath/mul_135_34/g2351	CI v -> C0 v	ADDFX1	0.339	5.723	5.778
instance_datapath/mul_135_34/g2350	CI v -> C0 v	ADDFX1	0.339	6.062	6.116
instance_datapath/mul_135_34/g2349	CI v -> C0 v	ADDFX1	0.339	6.401	6.455
instance_datapath/mul_135_34/g2348	CI v -> C0 v	ADDFX1	0.339	6.740	6.794
instance_datapath/mul_135_34/g2347	CI v -> C0 v	ADDFX1	0.339	7.078	7.133
instance_datapath/mul_135_34/g2346	C1 v -> S ^	ADDFX1	0.471	7.550	7.664
instance_datapath/g714	B ^ -> Y ^	AND2X1	0.220	7.769	7.824
M_reg[18]	D ^	DFFHQX8	0.000	7.769	7.824

Plain Text ▾ Tab Width: 8 ▾ Ln 1, Col 1 INS

timing_report_hold.rpt (~/work/sta_load_intermediate/wire_timing) - gedit

```

Generated by: Cadence Tempus 20.10-p003_1
OS: Linux x86_64(Host ID edaserver4)
Generated on: Fri Apr 8 17:26:00 2022
Design: topmodule
Command: report timing -early > $report_dir/timing_report_hold.rpt
#####
Path 1: MET Hold Check with Pin B_in_side_req_reg[4]/CK
Endpoint: B_in_side_req_reg[4]/D (v) checked with leading edge of 'clock'
Beginpoint: B[4] (v) triggered by leading edge of 'clock'
Path Groups: {clock}
Other End Arrival Time 0.000
+ Hold 0.080
+ Phase Shift 0.000
+ Uncertainty 0.012
= Required Time 0.092
Arrival Time 0.100
Slack Time 0.008
  Clock Rise Edge 0.000
  + Input Delay 0.100
  = Beginpoint Arrival Time 0.100
-----
Instance           Arc      Cell     Delay   Arrival  Required
                           Cell    Delay   Time     Time
-----
```

Instance	Arc	Cell	Delay	Arrival Time	Required Time
-	B[4] v -	-	0.100	0.092	
B_in_side_req_reg[4]	D v	DFFHQX8	0.000	0.100	0.092

Plain Text ▾ Tab Width: 8 ▾ Ln 1, Col 1 INS

There is a decrease in slack in the wire load model. Due to resistance and capacitance on each fanout path, the load on each path is increased. As there is increase in load because we are considering the wire delays (WLM model) also thus the delay on each path increases, and as a result slack decreases.

STEP 6: DESIGN FOR TESTABILITY (DFT)

Tool : genus

Command for invoking tool :- `genus --legacy_ui`

Sequential circuits testing is quite complex with comparison to combinational circuits, for this we have few methods for testability. By using scan chain design it would be more observable and controllable.

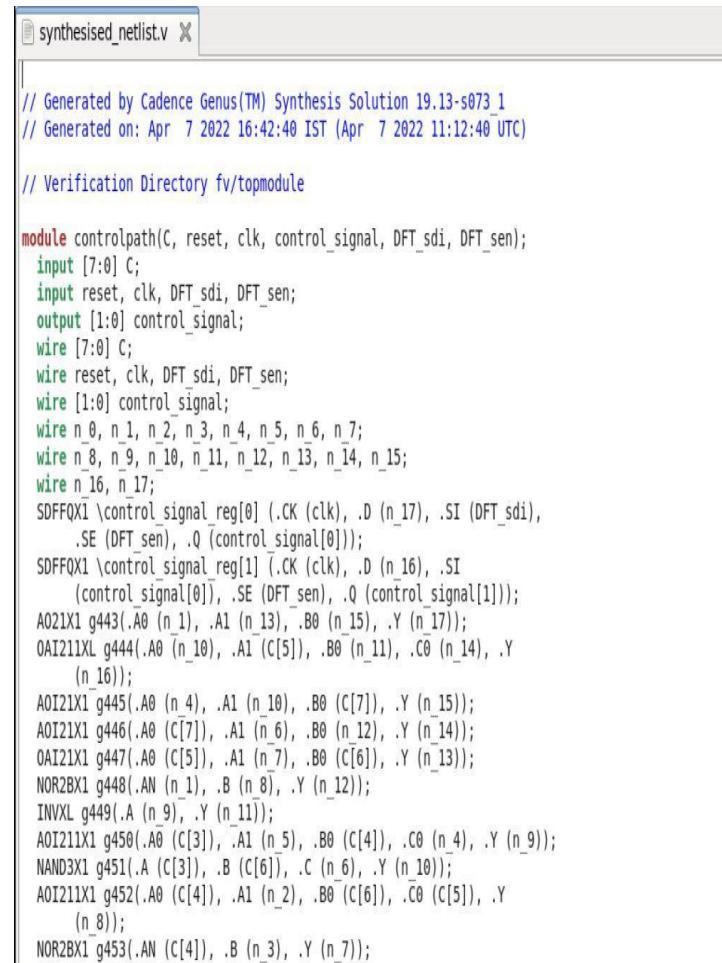
Method used for testing : **scan-cell inserted**

Synthesized Netlist without and with test insertion:

```
module controlpath(C, reset, clk, control_signal);
    input [7:0] C;
    input reset, clk;
    output [1:0] control_signal;
    wire [7:0] C;
    wire reset, clk;
    wire [1:0] control_signal;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
    wire n_16, n_17;

    DFFQX1 \control_signal_reg[1] (.CK (clk), .D (n_17), .Q
        (control_signal[1]));
    DFFQX1 \control_signal_reg[0] (.CK (clk), .D (n_16), .Q
        (control_signal[0]));

    OAII32X1 g462(.A0 (n_1), .A1 (reset), .A2 (n_13), .B0 (n_3), .B1
        (n_12), .Y (n_17));
    OAII2BB1XL g463(.A0N (C[6]), .A1N (n_14), .B0 (n_15), .Y (n_16));
    OAII21X1 g464(.A0 (n_1), .A1 (n_9), .B0 (n_2), .Y (n_15));
    OAII211X1 g465(.A0 (n_0), .A1 (n_7), .B0 (C[7]), .C0 (reset), .Y
        (n_14));
    OAII21X1 g466(.A0 (C[5]), .A1 (n_10), .B0 (n_11), .Y (n_13));
    OAII211X1 g467(.A0 (C[4]), .A1 (n_8), .B0 (C[5]), .C0 (C[6]), .Y
        (n_12));
    NOR2XL g468(.A (C[5]), .B (n_7), .Y (n_11));
    AOII21X1 g469(.A0 (C[3]), .A1 (n_6), .B0 (C[4]), .Y (n_10));
    AOII21X1 g470(.A0 (C[4]), .A1 (n_5), .B0 (C[5]), .Y (n_9));
    OR2XL g471(.A (C[3]), .B (n_6), .Y (n_8));
    NAND3BX1 g472(.A (n_4), .B (C[4]), .C (C[3]), .Y (n_7));
    NAND2BX1 g473(.A (C[0]), .B (n_4), .Y (n_6));
    AO21X1 g474(.A0 (C[1]), .A1 (C[2]), .B0 (C[3]), .Y (n_5));
    NOR2XL g475(.A (C[2]), .B (C[1]), .Y (n_4));
```



The screenshot shows a window titled "synthesised_netlist.v" containing Verilog code. The code is identical to the one above, but includes additional DFT-related components. Specifically, it adds DFFQX1 cells for test signal storage and AOII2BB1XL cells for test signal generation. The code is annotated with comments indicating the generation by Cadence Genus and the synthesis date/time.

```
// Generated by Cadence Genus(TM) Synthesis Solution 19.13-s073_1
// Generated on: Apr 7 2022 16:42:40 IST (Apr 7 2022 11:12:40 UTC)

// Verification Directory fv/topmodule

module controlpath(C, reset, clk, control_signal, DFT_sdi, DFT_sen);
    input [7:0] C;
    input reset, clk, DFT_sdi, DFT_sen;
    output [1:0] control_signal;
    wire [7:0] C;
    wire reset, clk, DFT_sdi, DFT_sen;
    wire [1:0] control_signal;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
    wire n_16, n_17;

    DFFQX1 \control_signal_reg[1] (.CK (clk), .D (n_17), .SI (DFT_sdi),
        .SE (DFT_sen), .Q (control_signal[1]));
    DFFQX1 \control_signal_reg[0] (.CK (clk), .D (n_16), .SI
        (control_signal[0]), .SE (DFT_sen), .Q (control_signal[0]));
    AOII2BB1XL g443(.A0 (n_1), .A1 (n_13), .B0 (n_15), .Y (n_17));
    OAII21X1 g444(.A0 (n_10), .A1 (C[5]), .B0 (n_11), .C0 (n_14), .Y
        (n_16));
    OAII21X1 g445(.A0 (n_4), .A1 (n_10), .B0 (C[7]), .Y (n_15));
    OAII21X1 g446(.A0 (C[7]), .A1 (n_6), .B0 (n_12), .Y (n_14));
    OAII21X1 g447(.A0 (C[5]), .A1 (n_7), .B0 (C[6]), .Y (n_13));
    NOR2XL g448(.A (n_1), .B (n_8), .Y (n_12));
    INVXL g449(.A (n_9), .B (n_11));
    AOII211X1 g450(.A0 (C[3]), .A1 (n_5), .B0 (C[4]), .C0 (n_4), .Y (n_9));
    NAND3XI g451(.A (C[3]), .B (C[6]), .C (n_6), .Y (n_10));
    AOII211X1 g452(.A0 (C[4]), .A1 (n_2), .B0 (C[6]), .C0 (C[5]), .Y
        (n_8));
    NOR2BX1 g453(.A (C[4]), .B (n_3), .Y (n_7));
```

Applications Places System

synthesised_netlist.v (~/work/min_interme)

File Edit View Search Tools Documents Help

Open Save Undo Cut Copy Paste Find Replace

synthesis.tcl synthesis_area_report.rep synthesis_cell_report.rep synthesis synthesis

```

AND2X1 g2588(.A (A[1]), .B (B[1]), .Y (n_1));
NOR2BXL g2589(.AN (B[0]), .B (n_5), .Y (Z[0]));
endmodule

module datapath(A, B, control_signal, clk, reset, M_out);
    input [9:0] A, B;
    input [1:0] control_signal;
    input clk, reset;
    output [19:0] M_out;
    wire [9:0] A, B;
    wire [1:0] control_signal;
    wire clk, reset;
    wire [19:0] M_out;
    wire [5:0] out_counter;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
    wire n_16, n_17, n_18, n_19, n_20, n_21, n_22, n_23;
    wire n_24, n_45, n_46, n_47, n_48, n_49, n_50, n_51;
    wire n_52, n_53, n_54, n_55, n_56, n_57, n_58, n_59;
    wire n_60, n_61, n_62, n_63, n_64;
    downcounter_6 counter(.clk (clk), .reset (reset), .out (out_counter));
    mult_unsigned mul_135_34(.A (A), .B (B), .Z ({n_64, n_63, n_62, n_61,
        n_60, n_59, n_58, n_57, n_56, n_55, n_54, n_53, n_52, n_51,
        n_50, n_49, n_48, n_47, n_46, n_45}));
    OAI2BBB1XL g701(.A0N (n_3), .A1N (out_counter[0]), .B0 (n_24), .Y
        (M_out[0]));
    AOI32X1 g702(.A0 (control_signal[1]), .A1 (n_2), .A2 (n_21), .B0
        (n_45), .B1 (n_0), .Y (n_24));
    OAI2BBB1XL g703(.A0N (n_0), .A1N (n_51), .B0 (n_23), .Y (M_out[6]));
    AO21X1 g704(.A0 (n_3), .A1 (out_counter[5]), .B0 (n_22), .Y
        (M_out[5]));
    AOI32X1 g705(.A0 (A[4]), .A1 (n_1), .A2 (n_10), .B0 (n_9), .B1
        (n_17), .Y (n_23));

```

synthesised_netlist.v ... [akash21185@edaser...]

[work] min_interme

synthesised_netlist.v X

```

endmodule

module datapath(A, B, control_signal, clk, reset, M_out, DFT_sen,
    DFT_sdo);
    input [9:0] A, B;
    input [1:0] control_signal;
    input clk, reset, DFT_sen;
    output [19:0] M_out;
    output DFT_sdo;
    wire [9:0] A, B;
    wire [1:0] control_signal;
    wire clk, reset, DFT_sen;
    wire [19:0] M_out;
    wire DFT_sdo;
    wire [5:0] out_counter;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
    wire n_16, n_17, n_18, n_19, n_20, n_21, n_22, n_23;
    wire n_24, n_25, n_26, n_27, n_28, n_49, n_50, n_51;
    wire n_52, n_53, n_54, n_55, n_56, n_57, n_58, n_59;
    wire n_60, n_61, n_62, n_63, n_64, n_65, n_66, n_67;
    wire n_68;
    downcounter_6 counter(.clk (clk), .reset (reset), .out ({DFT_sdo,
        out_counter[4:0]}), .DFT_sdi (control_signal[1]), .DFT_sen
        (DFT_sen));
    mult_unsigned mul_135_34(.A (A), .B (B), .Z ({n_68, n_67, n_66, n_65,
        n_64, n_63, n_62, n_61, n_60, n_59, n_58, n_57, n_56, n_55,
        n_54, n_53, n_52, n_51, n_50, n_49}));
    OAI31X1 g717(.A0 (control_signal[0]), .A1 (n_1), .A2 (n_28), .B0
        (n_14), .Y (M_out[0]));
    OAI222XL g718(.A0 (n_10), .A1 (n_23), .B0 (A[5]), .B1 (n_17), .C0
        (n_2), .C1 (n_3), .Y (M_out[6]));
    NAND2XL g719(.A (n_20), .B (n_27), .Y (M_out[5]));

```

Changes observed in the above netlist from the original netlist:

- a. From above we can vividly observe that the D flipflop of the min area netlist of without scan chain inserted is converted to SD flip flop in min area netlist of scan chain inserted. That is DFFQX1 is changed to SDFFQX1. S-referred to scanned.
- b. Apart from sequential elements all other gates and instances remain same in both the netlists original as well as insert scanned netlist.
- c. We can observe from above that scanned netlist has some additional ports in input and output side, like input side has additional inputs DFT_sdi1 ,DFT_sdi0 and DFT_sen and at output DFT_sdo. Ports are TM - Test mode, SE - Scan enable, SI - Scan In, SO - Scan Out

The new entities that are appeared inside netlist and their interpretation are as given below

Entities	Interpretations
SI port	It facilitates scanned input insertion
SO port	The output of the scan chain design is moving through the SO port and it is compared with the golden result.
SE	Scan enable is used for enabling and also with test mode it provides which design to be selected

Modes :

When SE =0 & TM =0 Normal

When SE =0 & TM =1 Capture

When SE =1 & TM =1 Shift (Scan enable is set to 1. Then inputs the pattern through the scan input, shifts the pattern through the scan flops and loads all the flops with the test pattern.)

REPORTS COMPARISON AFTER SCAN INSERTION:

Normal synthesis and after test insertions.

1. QoR Comparison of Minimum Area :: Cell Report:-

The screenshot shows two terminal windows side-by-side. The left window displays the contents of `synthesis_cell_report.rep`, and the right window displays the contents of `synthesis_area_report.rep`. Both reports show cell usage statistics and area calculations.

synthesis_cell_report.rep (~/work/min_area) - GVIM2

Type	Instances	Area	Area %
sequential	56	1871.770	30.7
inverter	39	88.557	2.5
logic	276	2333.523	66.8
physical_cells	0	0.000	0.0
total	371	3493.850	100.0

synthesis_area_report.rep

Type	Instances	Area	Area %
NAND2XL	107	323.953	slow
NAND3BX1	1	6.055	slow
NAND3X1	1	4.541	slow
NOR2BX1	4	18.166	slow
NOR2BXL	1	4.541	slow
NOR2XL	16	48.442	slow
NOR3BX1	1	6.055	slow
NOR3X1	2	9.083	slow
OAI211X1	2	10.597	slow
OAI211XL	3	15.895	slow
OAI21X1	2	9.083	slow
OAI222XL	1	8.326	slow
OAI22X1	1	6.055	slow
OAI31X1	1	6.055	slow
OR2X1	4	18.166	slow
OR2XL	1	4.541	slow
XNOR2X1	5	41.630	slow
total	371	3778.445	

Type	Instances	Area	Area %
sequential	56	1356.365	35.9
inverter	39	88.557	2.3
logic	276	2333.523	61.8
physical_cells	0	0.000	0.0
total	371	3778.445	100.0

From above we can observe that the area of sequential components increased, which is certain because additional components MUX with DFF(Muxed scan flip flop). Earlier the percentage area of sequential ckts were 30.7% and now it increases to 35.9%. There is no significant change in other combinations logic areas.

From above we can analyze the area of each of the gates present in design. After insertion the total area for all the cells are added up and reported as shown. Also it can be observed what percentage of sequential circuits are there and what percent of combinational circuits are present.

Timing Report:

Applications Places System Thu Apr 7, 8:42 PM akash21185

synthesis_area_report.rep (~/work/min_area) - gedit

File Edit View Search Tools Documents Help

Open Save Undo | Cut Copy Paste | Find Replace | Select All

intermediate.sdc sta_load.tcl synthesis.tcl area.sdc timing.sdc sta.tcl inter.sdc synthesis_cell_report.rep synthesis_area_report.rep

```
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 07 2022 01:23:54 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====
Instance Module Cell Count Cell Area Net Area Total Area Wireload
-----
topmodule 371 3493.850 0.000 3493.850 <none> (D)
instance_datapath datapath 303 2431.920 0.000 2431.920 <none> (D)
mul_135_34 mult_unsigned 232 2068.608 0.000 2068.608 <none> (D)
counter downcounter_6 22 151.380 0.000 151.380 <none> (D)
instance_controlpath controlpath 20 117.320 0.000 117.320 <none> (D)

(D) = wireload is default in technology library
```

Plain Text Tab Width: 8 Ln 1, Col 1 INS

akash... work synth... [akash... min_i... [sta_l... min_i... min_a... constr... area.s... (no su... synth...

synthesis_cell_report.rep synthesis_area_report.rep

```
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 07 2022 04:42:41 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====
Instance Module Cell Count Cell Area Net Area Total Area Wireload
-----
topmodule 371 3778.445 0.000 3778.445 <none> (D)
instance_datapath datapath 303 2459.168 0.000 2459.168 <none> (D)
mul_135_34 mult_unsigned 232 2068.608 0.000 2068.608 <none> (D)
counter downcounter_6 22 178.628 0.000 178.628 <none> (D)
instance_controlpath controlpath 20 126.402 0.000 126.402 <none> (D)

(D) = wireload is default in technology library
```

Power Report:

```

synthesis_cell_report.rep synthesis_area_report.rep synthesis_timing_report.rep synthesis_power_report.rep
Instance: /topmodule
Power Unit: W
PDB Frames: /stim#0/frame#0

Category      Leakage    Internal   Switching     Total     Row%
-----
memory        0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
register     1.16773e-05  1.39486e-04  1.97982e-04  3.49145e-04  78.97%
latch         0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
logic          9.49567e-06  5.00657e-05  2.47478e-05  8.43092e-05  19.07%
bbox           0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
clock          0.00000e+00  0.00000e+00  8.65800e-06  8.65800e-06  1.96%
pad            0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
pm             0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
-----
Subtotal      2.11730e-05  1.89552e-04  2.31388e-04  4.42112e-04  100.00%
Percentage   4.79%       42.87%      52.34%      100.00%   100.00%
-----
```

Thu Apr 7, 8:42 PM akash21185

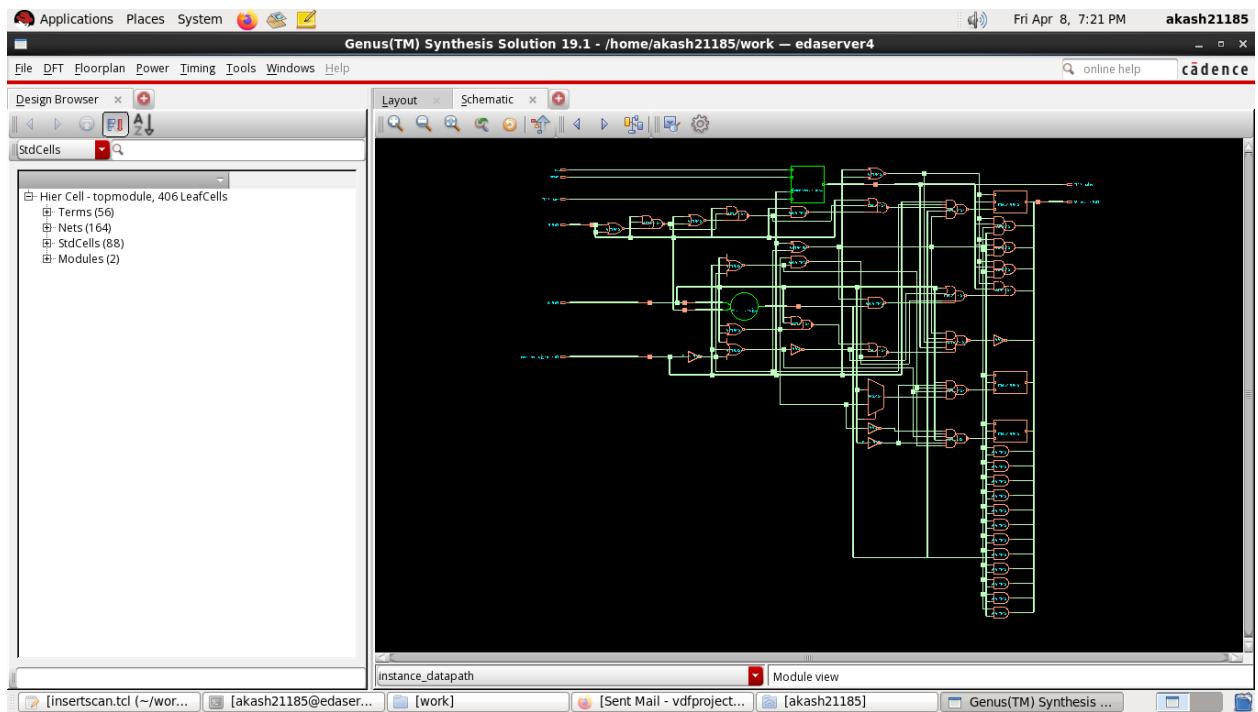
```

Applications Places System Firefox Gedit
synthesis_power_report.rep (~/work/min_area) - gedit
File Edit View Search Tools Documents Help
Open Save Undo Redo Find Replace Minimize Maximize Close
synthesis.tcl area.sdc timing.sdc sta.tcl inter.sdc synthesis_cell_report.rep synthesis_area_report.rep synthesis_power_report.rep
Instance: /topmodule
Power Unit: W
PDB Frames: /stim#0/frame#0

Category      Leakage    Internal   Switching     Total     Row%
-----
memory        0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
register     9.36407e-06  1.38848e-04  1.96869e-04  3.37081e-04  78.40%
latch         0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
logic          9.39249e-06  5.01767e-05  2.47300e-05  8.42992e-05  19.61%
bbox           0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
clock          0.00000e+00  0.00000e+00  8.56800e-06  8.56800e-06  1.99%
pad            0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
pm             0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
-----
Subtotal      1.87566e-05  1.81025e-04  2.30167e-04  4.29948e-04  100.00%
Percentage   4.36%       42.10%      53.53%      100.00%   100.00%
-----
```

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akash... work synth... [akas... akash... min_i... sta_i... min_i... min_a... constr... area.s... (no su... synth...)



From above we can observe that there is a minute increment in power after scan chain insertion. Earlier the power was 429 microwatt and now it increases to 442 microwatts.

Timing report comparisons:

synthesis_cell_report.rep synthesis_area_report.rep synthesis_timing_report.rep

g2362/C0	ADDFX1	1	4.9	96	+250	3397	F
g2360/CI					+0	3397	
g2360/C0	ADDFX1	1	4.9	96	+250	3647	F
g2358/CI					+0	3647	
g2358/C0	ADDFX1	1	4.9	96	+250	3897	F
g2356/CI					+0	3897	
g2356/C0	ADDFX1	1	4.9	96	+250	4147	F
g2354/CI					+0	4147	
g2354/C0	ADDFX1	1	4.9	96	+250	4397	F
g2352/CI					+0	4397	
g2352/C0	ADDFX1	1	4.9	96	+250	4647	F
g2350/CI					+0	4647	
g2350/C0	ADDFX1	1	4.9	96	+250	4897	F
g2348/CI					+0	4897	
g2348/S	ADDFXL	1	1.6	73	+229	5125	F
g2346/A					+0	5125	
g2346/Y	INVXL	1	1.7	45	+54	5179	R
mul_135_34/Z[18]					+0	5179	
g751/B					+0	5179	
g751/Y	AND2X1	1	2.9	92	+129	5308	R
instance_datapath/M_out[18]					+0	5308	
M_reg[18]/D	<<<	SDFFHQX8			+0	5308	
M_reg[18]/CK		setup			10	+232	5540 R
(clock clock)					capture		9000 R
					latency		+10 9010 R
					uncertainty		-20 8990 R

```

Cost Group : 'clock' (path_group 'clock')
Timing slack : 3450ps
Start-point : B_in_side_reg_reg[0]/CK
End-point   : M_reg[18]/D

```


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timing.sdc sta.tcl inter.sdc synthesis_cell_report.rep synthesis_area_report.rep synthesis_power_report.rep synthesis_timing_report.rep

g2362/C0	ADDFX1	1	4.9	96	+250	3389	F
g2366/CI					+0	3389	
g2366/C0	ADDFX1	1	4.9	96	+250	3639	F
g2358/CI					+0	3639	
g2358/C0	ADDFX1	1	4.9	96	+250	3889	F
g2356/CI					+0	3889	
g2356/C0	ADDFX1	1	4.9	96	+250	4139	F
g2354/CI					+0	4139	
g2354/C0	ADDFX1	1	4.9	96	+250	4389	F
g2352/CI					+0	4389	
g2352/C0	ADDFX1	1	4.9	96	+250	4639	F
g2356/CI					+0	4639	
g2356/C0	ADDFX1	1	4.9	96	+250	4889	F
g2348/CI					+0	4889	
g2348/S	ADDFXL	1	1.6	73	+229	5117	F
g2346/A					+0	5117	
g2346/Y	INVXL	1	1.7	45	+54	5171	R
mul_135_34/Z[18]					+0	5171	
g751/AN					+0	5171	
g751/Y	NOR2BX1	1	2.3	216	+116	5286	R
instance_datapath/M_out[18]					+0	5286	
M_reg[18]/D	<<<	DFFHQX8			+0	5286	
M_reg[18]/CK		setup			10	+189	5476 R
(clock clock)					capture		9000 R
					latency		+10 9010 R
					uncertainty		-20 8990 R

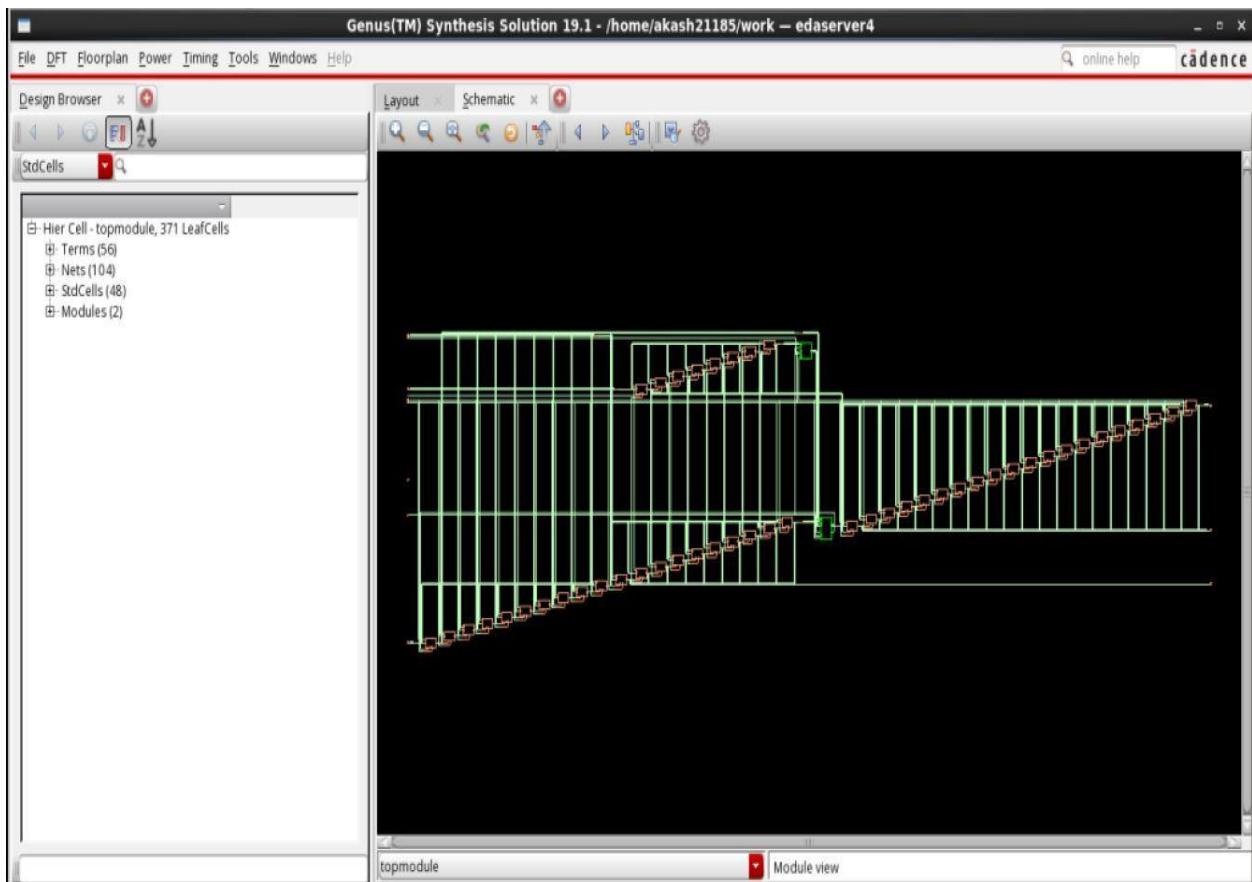
```

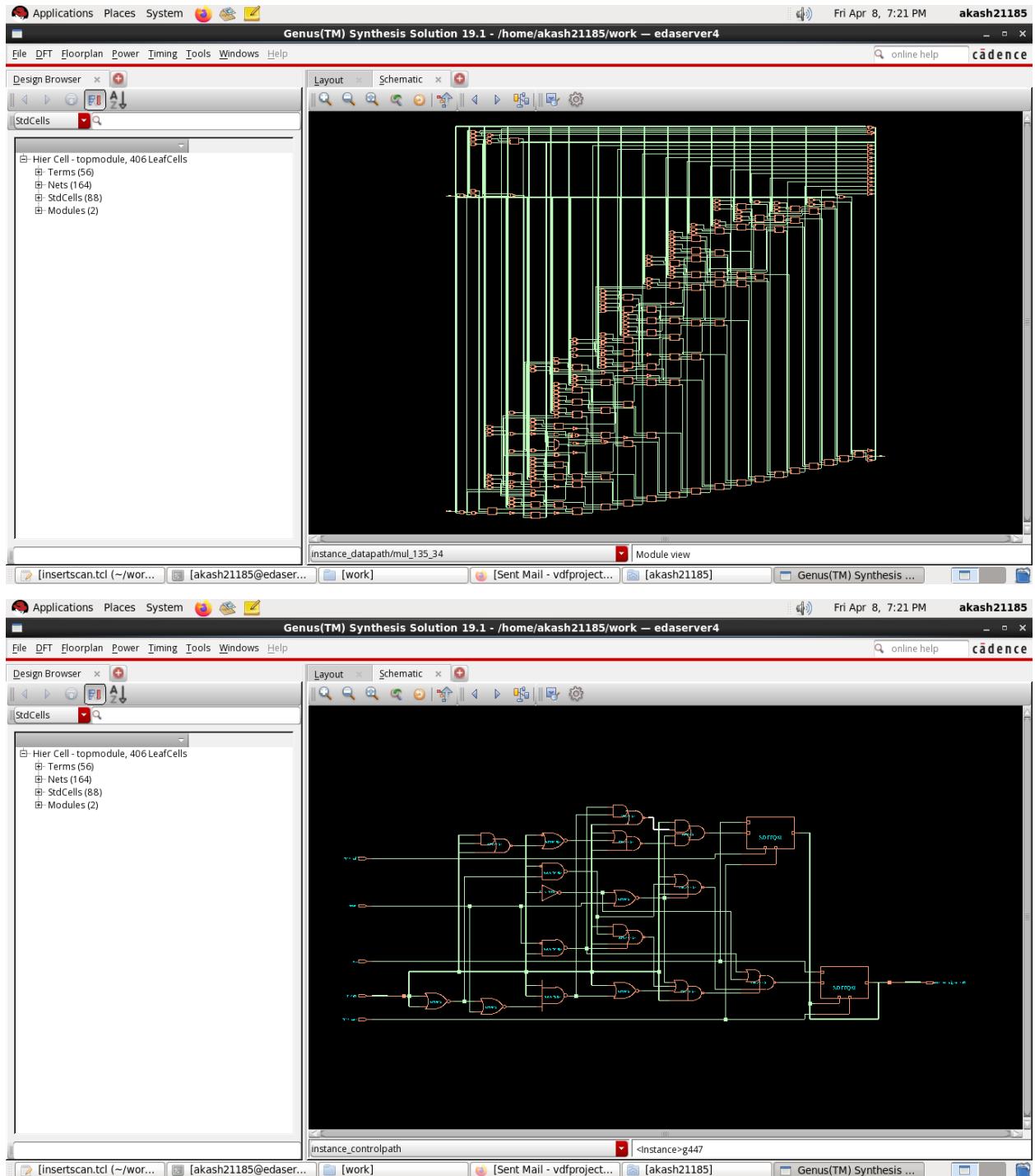
Cost Group : 'clock' (path_group 'clock')
Timing slack : 3514ps
Start-point : B_in_side_reg_reg[0]/CK
End-point   : M_reg[18]/D

```

Slack increases after the insertion after the insertion of the scan flip flop.

Schematics: After insert scan and before insertion

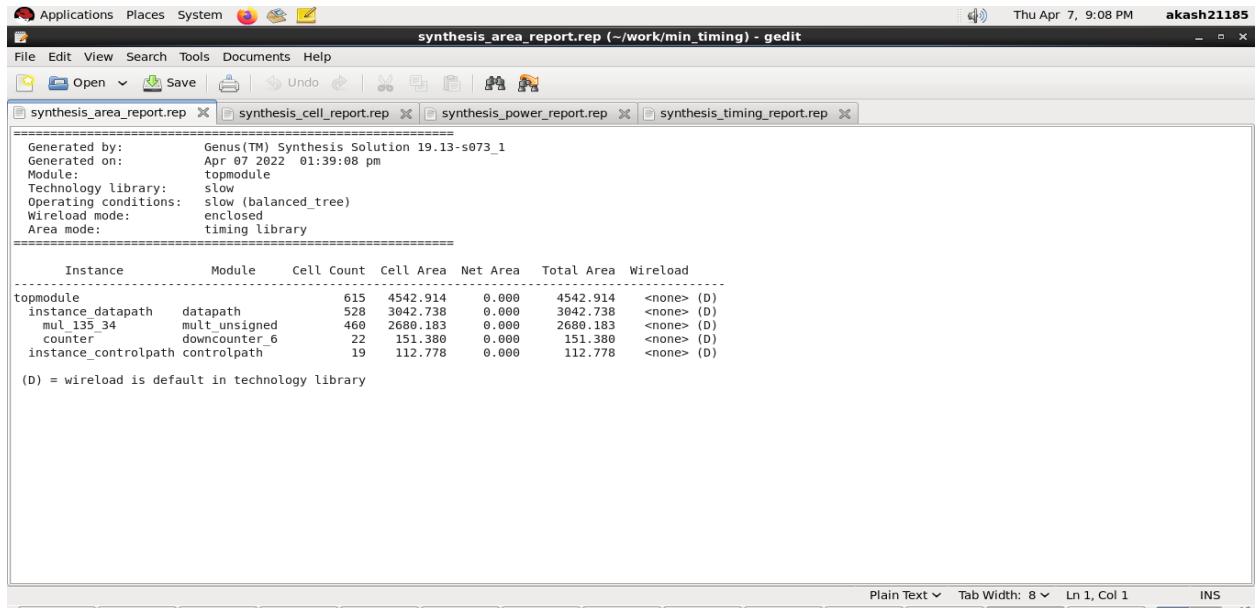




Above three schematics are corresponding to the top module, datapath and control path respectively.

2. QoR comparison of minimum timing(slightly negative) report:

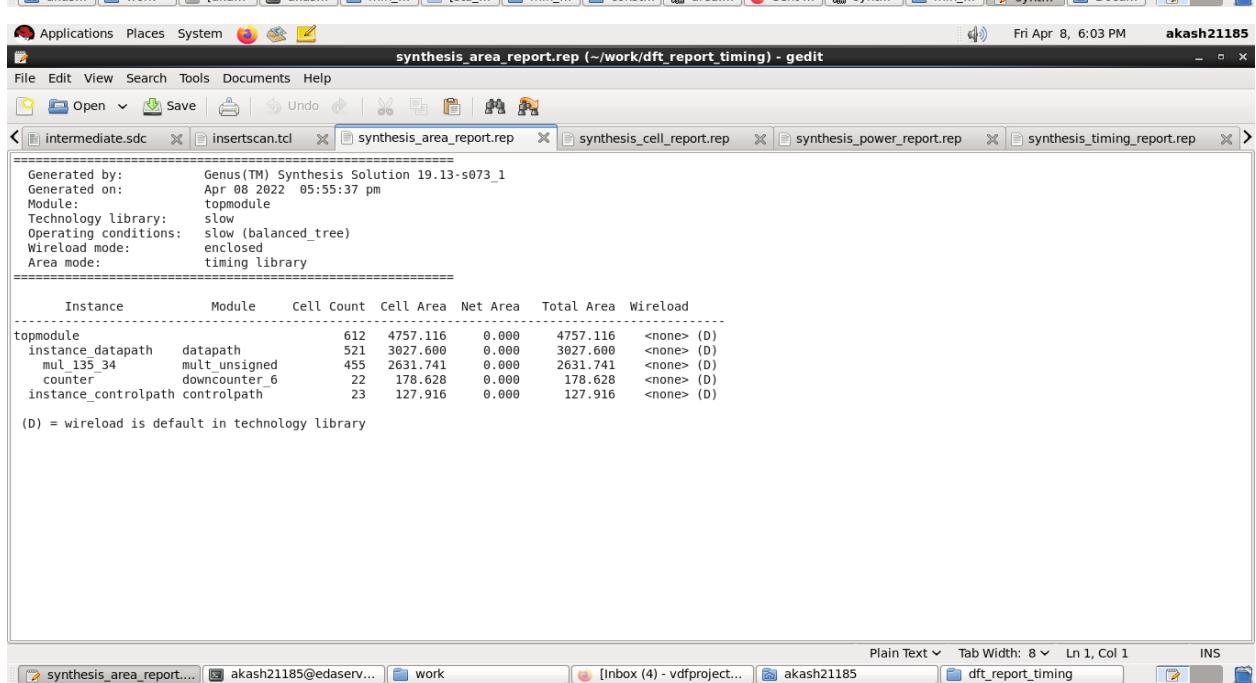
Area report comparison-



synthesis_area_report.rep (~/work/min_timing) - gedit

```
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 07 2022 01:39:08 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====
Instance Module Cell Count Cell Area Net Area Total Area Wireload
-----
topmodule 615 4542.914 0.000 4542.914 <none> (D)
instance_datapath datapath 528 3042.738 0.000 3042.738 <none> (D)
mul_135_34 mult_unsigned 460 2680.183 0.000 2680.183 <none> (D)
counter downcounter_6 22 151.380 0.000 151.380 <none> (D)
instance_controlpath controlpath 19 112.778 0.000 112.778 <none> (D)
(D) = wireload is default in technology library
```

Plain Text Tab Width: 8 Ln 1, Col 1 INS



synthesis_area_report.rep (~/work/dft_report_timing) - gedit

```
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 08 2022 05:55:37 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====
Instance Module Cell Count Cell Area Net Area Total Area Wireload
-----
topmodule 612 4757.116 0.000 4757.116 <none> (D)
instance_datapath datapath 521 3027.600 0.000 3027.600 <none> (D)
mul_135_34 mult_unsigned 455 2631.741 0.000 2631.741 <none> (D)
counter downcounter_6 22 178.628 0.000 178.628 <none> (D)
instance_controlpath controlpath 23 127.916 0.000 127.916 <none> (D)
(D) = wireload is default in technology library
```

Plain Text Tab Width: 8 Ln 1, Col 1 INS

It can be observed here that the Area of top module has increased after scan chain insertion which was initially anticipated. Although the cell count decreased, the cell area increased in the latter part. The wireload is kept to be default in both the cases.

Timing report comparison-

```

Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 07 2022 01:39:07 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====

Pin Type Fanout Load Slew Delay Arrival
          (fF) (ps) (ps) (ps)

(clock clock) launch 0 R
M_reg[18]/CK 10 0 R
M_reg[18]/Q DFFX2 1 13.2 80 +308 308 R
g6/A          +0 308
g6/Y          BUFX20 1 7700.0 3213 +2278 2586 R
M[18]         <<< interconnect 3213 +0 2586 R
                  out port +0 2586 R
(timing.sdc_line_13_57_1) ext delay +500 3086 R
- - - - -
(clock clock) capture 3185 R
uncertainty   -100 3085 R
- - - - -
Cost Group : 'clock' (path_group 'clock')
Timing slack : -1ps (TIMING VIOLATION)
Start-point : M_reg[18]/CK
End-point   : M[18]

-----
```

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synthesis_timing_report.rep (~/work/dft_report_timing) - gedit

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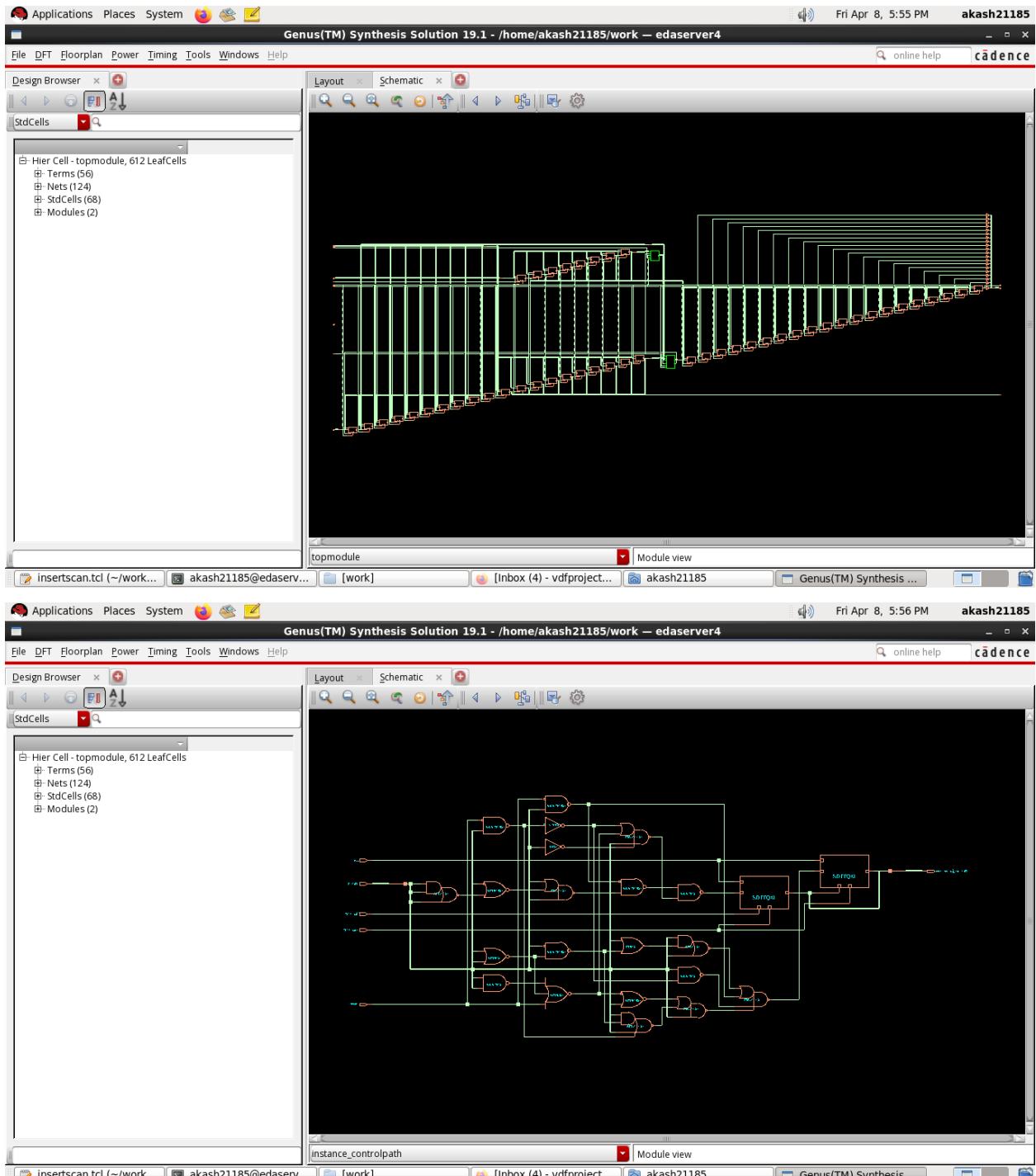
intermediate.sdc insertscan.tcl synthesis_area_report.rep synthesis_cell_report.rep synthesis_power_report.rep synthesis_timing_report.rep

```

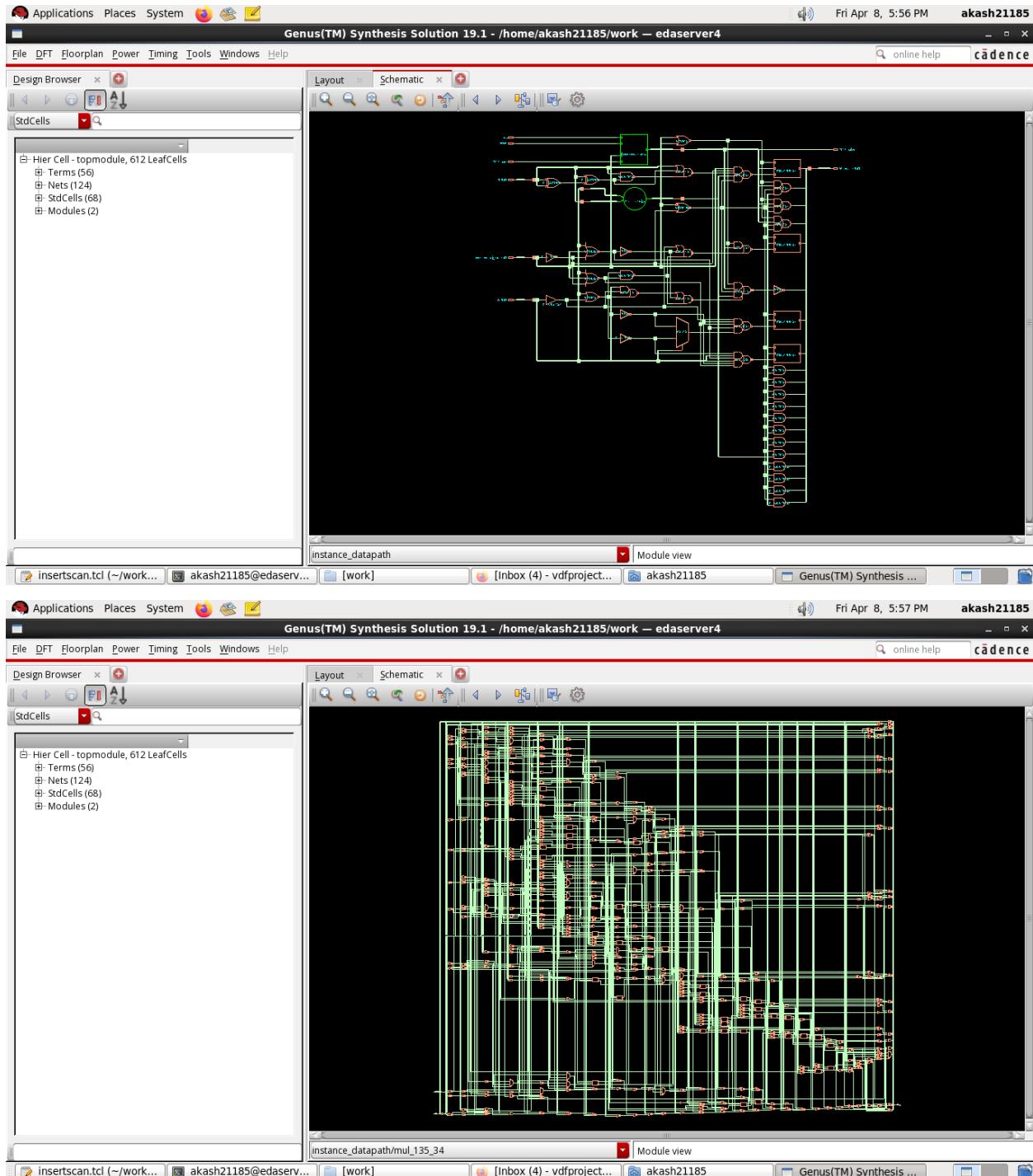
g4828/A1      +0 2043
g4828/Y      A0I21X2 2 7.0 96 +108 2151 R
g4825/A1      +0 2151
g4825/Y      OAI21X2 2 6.9 82 +83 2234 F
g4821/B      +0 2234
g4821/Y      NAND2X2 1 5.4 79 +56 2289 R
g4819/B      +0 2289
g4819/Y      NAND2BX2 2 7.1 80 +74 2364 F
g4816/B      +0 2364
g4816/Y      NAND2X2 1 5.4 79 +55 2418 R
g4814/B      +0 2418
g4814/Y      NAND2BX2 3 6.2 74 +70 2488 F
g4812/B      +0 2488
g4812/Y      NAND2BX1 1 2.8 50 +55 2544 R
g4809/B      +0 2544
g4809/Y      NAND2X1 3 5.9 104 +89 2633 F
g4805/A1      +0 2633
g4805/Y      OAI21X1 1 2.2 87 +94 2727 R
mul_135_34/Z[18]
q2/B          +0 2727
q2/Y          CLKAND2X2 1 2.9 61 +112 2839 R
instance datapath/M_out[18]
M_reg[18]/D    <<< SDFFHQX2 10 +0 2839
M_reg[18]/CK    setup +247 3086 R
- - - - -
(clock clock) capture 3185 R
uncertainty   -100 3085 R
- - - - -
Cost Group : 'clock' (path_group 'clock')
Timing slack : -0ps (TIMING VIOLATION)
Start-point : B_in_side_reg_reg[8]/CK
End-point   : M_reg[18]/D
```

Slack before the scan insertion was -1ps and after insertion the scan insertion the slack became 0 ps.

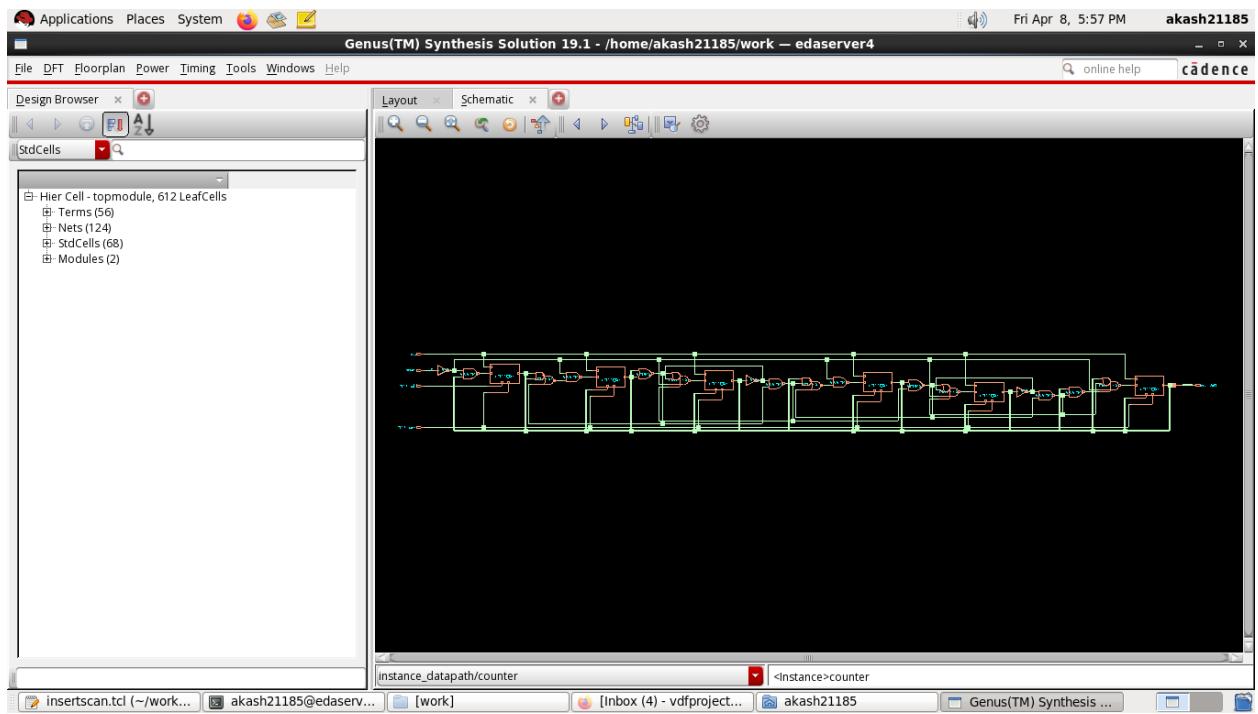
Schematic after Scan Chain Insertion:-



Scan Flip Flop can be seen.



Above is the schematic of the multiplier.



The above screenshot depicts the scan inserted for the best timing case.

3. QoR comparison of intermediate timing(between a and b) report:

Area report comparison-

The screenshot displays two terminal windows side-by-side, both titled "synthesis_area_report.rep (~/work/min_intermediate1) - gedit".

Top Window (Initial Report):

```
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 08 2022 04:36:18 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library

=====

Instance      Module      Cell Count  Cell Area  Net Area  Total Area  Wireload
-----
```

Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload
topmodule		387	3820.074	0.000	3820.074	<none> (D)
instance_datapath	datapath	299	2430.406	0.000	2430.406	<none> (D)
mul_135_34	mult_unsigned	232	2068.608	0.000	2068.608	<none> (D)
counter_	downcounter_6	22	151.380	0.000	151.380	<none> (D)
instance_controlpath	controlpath	20	112.021	0.000	112.021	<none> (D)

(D) = wireload is default in technology library

Bottom Window (Report after Scan Insertion):

```
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 08 2022 07:20:37 pm
Module: topmodule
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library

=====

Instance      Module      Cell Count  Cell Area  Net Area  Total Area  Wireload
-----
```

Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload
topmodule		406	4220.474	0.000	4220.474	<none> (D)
instance_datapath	datapath	299	2456.897	0.000	2456.897	<none> (D)
mul_135_34	mult_unsigned	232	2068.608	0.000	2068.608	<none> (D)
counter_	downcounter_6	22	178.628	0.000	178.628	<none> (D)
instance_controlpath	controlpath	19	116.563	0.000	116.563	<none> (D)

(D) = wireload is default in technology library

Area after scan insertion increases from 3820 to 4220.

Timing Report Comparison:

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synthesis_timing_report.rep (~/work/min_intermediate1) - gedit

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sta_load.tcl synthesis.tcl synthesis_area_report.rep synthesis_cell_report.rep synthesis_power_report.rep synthesis_timing_report.rep

```

g2362/CI          +0    3129
g2362/CO ADDFX1   1  4.9  96 +250  3379 F
g2366/CI          +0    3379
g2366/CO ADDFX1   1  4.9  96 +250  3629 F
g2358/CI          +0    3629
g2358/CO ADDFX1   1  4.9  96 +250  3879 F
g2356/CI          +0    3879
g2356/CO ADDFX1   1  4.9  96 +250  4129 F
g2354/CI          +0    4129
g2354/CO ADDFX1   1  4.9  96 +250  4379 F
g2352/CI          +0    4379
g2352/CO ADDFX1   1  4.9  96 +250  4629 F
g2350/CI          +0    4629
g2350/CO ADDFX1   1  4.9  96 +250  4879 F
g2348/CI          +0    4879
g2348/S ADDFXL   1  1.6  73 +229  5107 F
g2346/A           +0    5107
g2346/Y INVXL    1  1.7  45 +54   5161 R
mul_135_34/Z[18]
g733/B           +0    5161
g733/Y AND2XL   1  1.6  67 +111  5272 R
instance datapath/M_out[18]
M_reg[18]/D      <<< DFFQX1  +0    5272
M_reg[18]/CK      setup   10 +202  5474 R
----- (clock clock)
capture          8000 R
uncertainty      -12   7988 R
-----
Cost Group : 'clock' (path_group 'clock')
Timing slack : 2514ps
Start-point : B_in_side_reg_reg[0]/CK
End-point   : M_reg[18]/D

```

Plain Text Tab Width: 8 Ln 1, Col 1 INS

synthesis_timing_repo... [akash21185@edaser... [work] [min_intermediate1]

Applications Places System Fri Apr 8, 10:18 PM akash21185

synthesis_timing_report (1).rep (~/Downloads) - gedit

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synthesis_timing_report (1).rep

```

g2362/CI          +0    3137
g2362/CO ADDFX1   1  4.9  96 +250  3387 F
g2366/CI          +0    3387
g2366/CO ADDFX1   1  4.9  96 +250  3637 F
g2358/CI          +0    3637
g2358/CO ADDFX1   1  4.9  96 +250  3887 F
g2356/CI          +0    3887
g2356/CO ADDFX1   1  4.9  96 +250  4137 F
g2354/CI          +0    4137
g2354/CO ADDFX1   1  4.9  96 +250  4387 F
g2352/CI          +0    4387
g2352/CO ADDFX1   1  4.9  96 +250  4637 F
g2350/CI          +0    4637
g2350/CO ADDFX1   1  4.9  96 +250  4887 F
g2348/CI          +0    4887
g2348/S ADDFXL   1  1.6  73 +229  5115 F
g2346/A           +0    5115
g2346/Y INVXL    1  1.7  45 +54   5169 R
mul_135_34/Z[18]
g718/B           +0    5169
g718/Y AND2X1   1  2.9  74 +129  5298 R
instance datapath/M_out[18]
M_reg[18]/D      <<< SDFHQX8  +0    5298
M_reg[18]/CK      setup   10 +236  5534 R
----- (clock clock)
capture          6000 R
uncertainty      -200  5800 R
-----
Cost Group : 'clock' (path_group 'clock')
Timing slack : 266ps
Start-point : B_in_side_reg_reg[0]/CK
End-point   : M_reg[18]/D

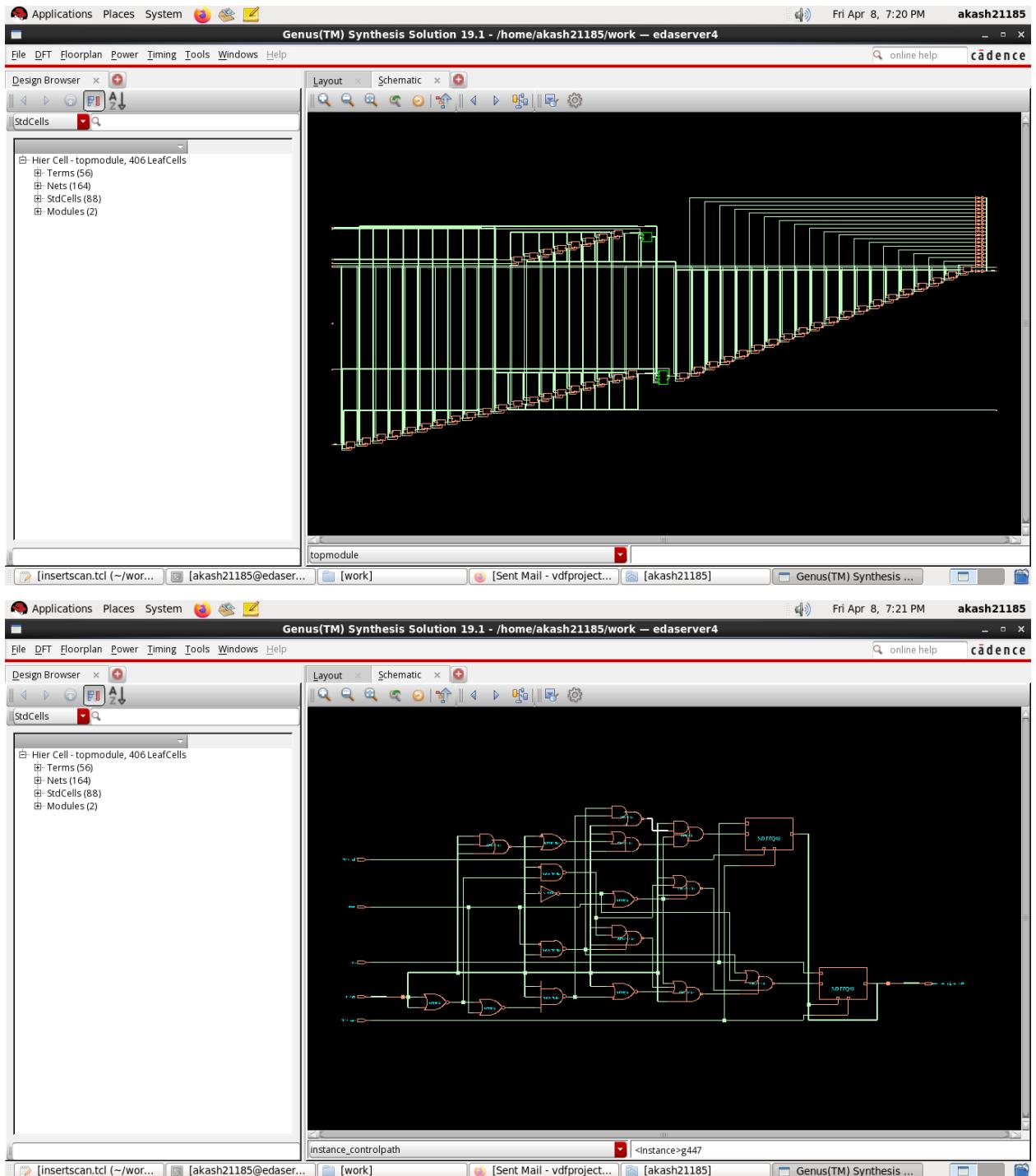
```

Plain Text Tab Width: 8 Ln 74, Col 19 INS

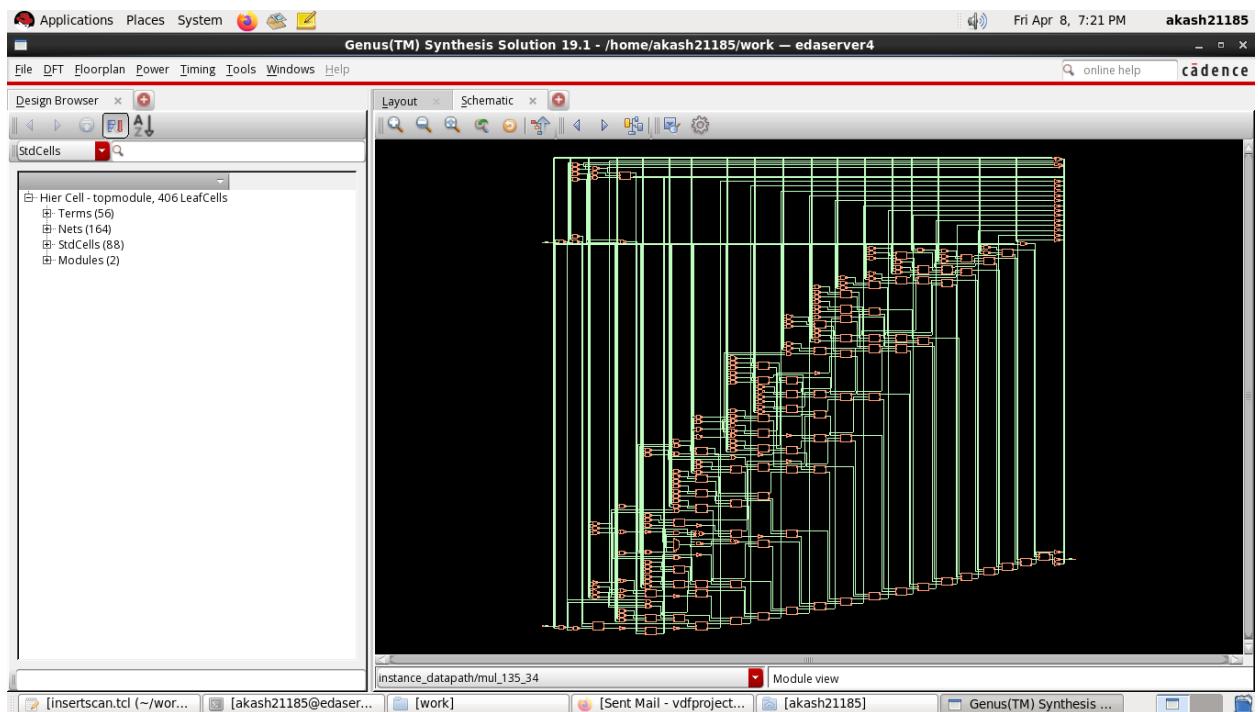
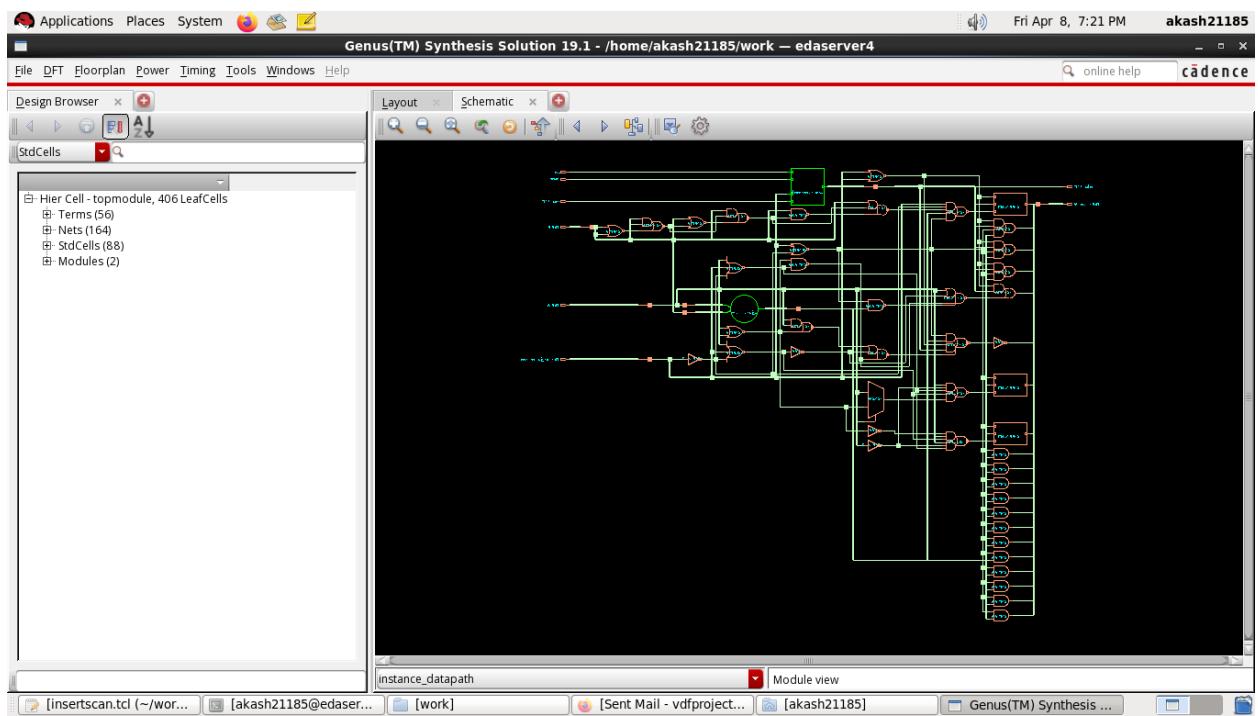
(no subject) - akash21185 work min_timing min_intermediate1 Downloads synthesis_timing_r...

Slack before the scan insertion was 2514ps and after insertion the scan insertion the slack became 266ps. After scan chain insertion the slack reduced which was anticipated.

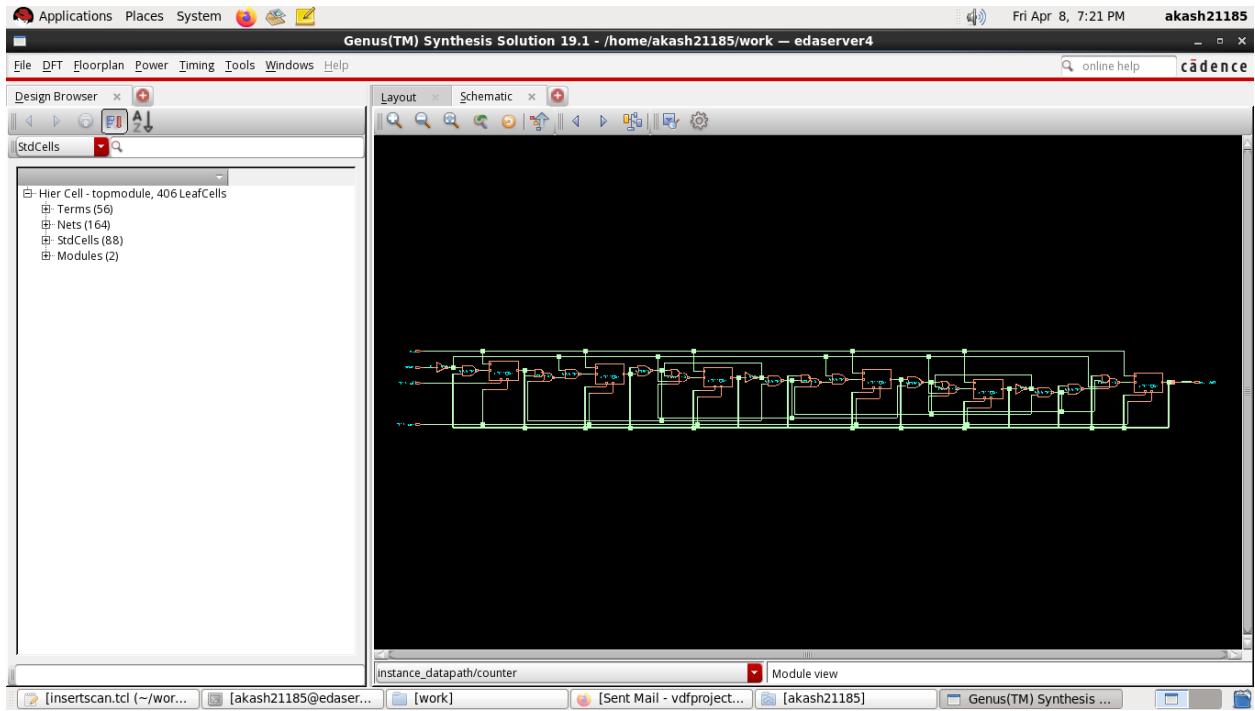
Schematic after scan chain insertion:-



In the schematic above, after insertion of scan chain Scan Flip Flop can be seen.



The above schematic is of the multiplier module for the intermediate timing report.



Reason for difference in QoR for Area:

- 1) It can be observed from the slow.lib file that the size of a DFF is 25% lesser than that of the Scan flip flop.
MUXED SCAN DFF – 21.95
DFF – 15.89
- 2) This is because the scan flip flop has an additional mux in it for the additional testability features it provides. Apart from this at the design level scan insertion takes additional routing resources for implementation of the scan chain.
- 3) There is an additional power overhead for the DFT implementation. But still it is used because of the testability features and ease of testing.

Reason for difference in QoR for Timing:

- 1) From the timing reports of all the three cases it can be easily observed that the setup time, AT, and RT differ. Rest of the values remain the same.
- 2) The slack has reduced when scan chains are introduced in the system. Due to the increase in capacitance and resistance, the delay of the system increases.

- 3) Therefore, the performance degradation leads to increase in delay due to which the slack reduces. Also, in the analysis where scan chains are included it is observed that DFF are now replaced SDFF.

***** END *****