Conventional Latch Type Sense Amplifier(Mux16 configuration)

ECE-611 (Memory Design and Test)

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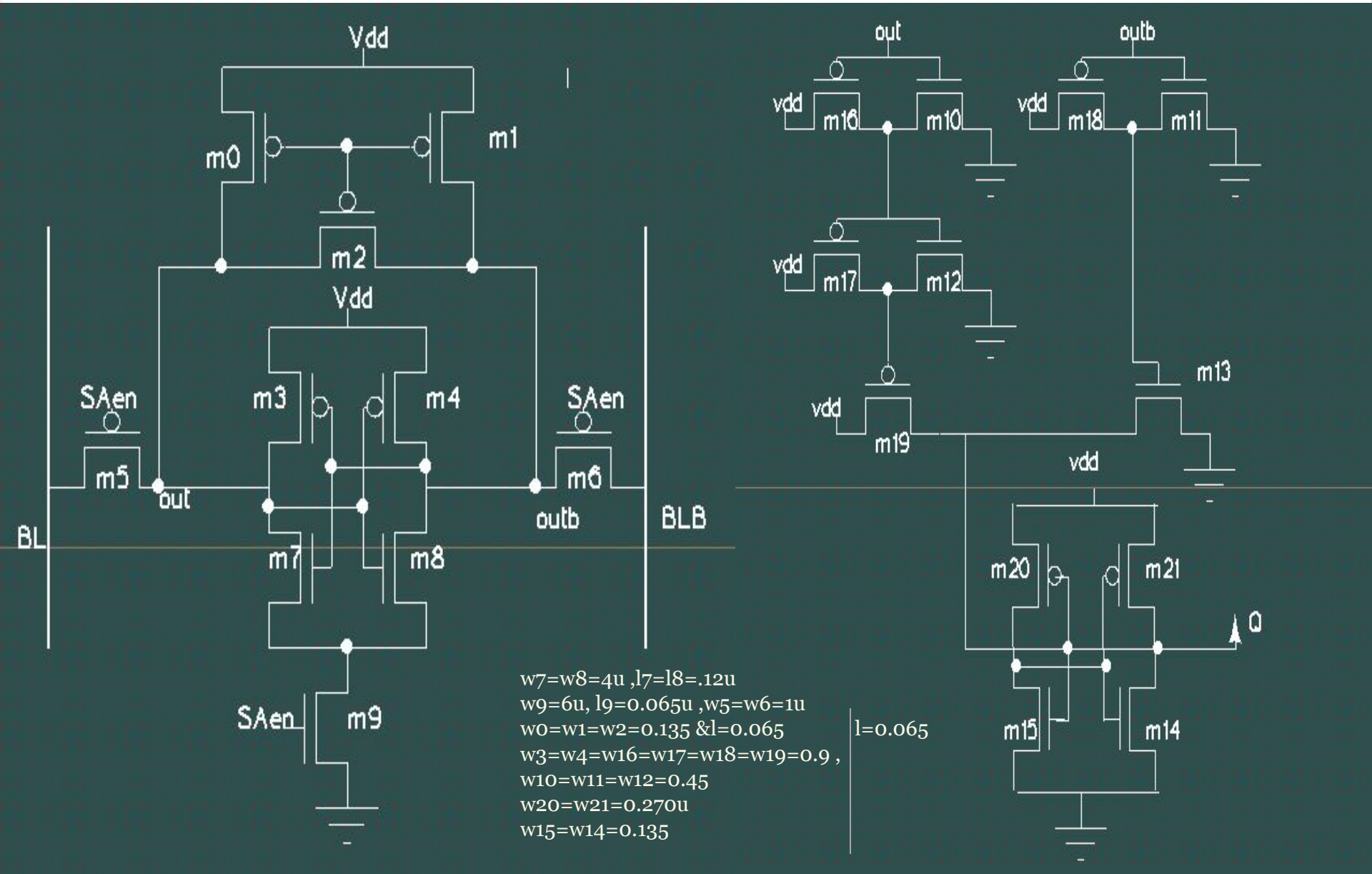
Problem Statement

Design of Conventional latch-type sense amplifier (for MUX-16 configuration) with the following conditions:

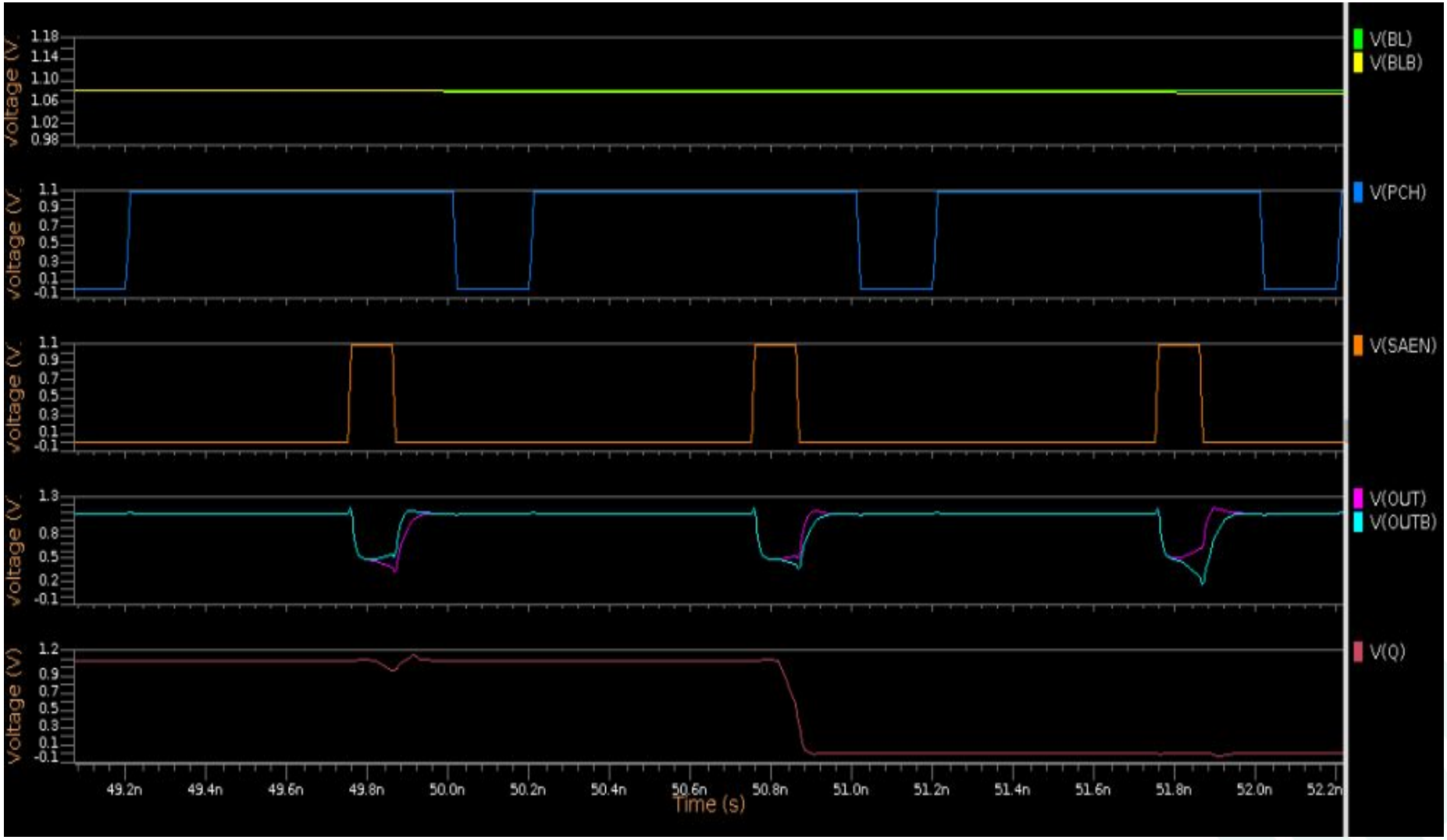
- ✦ Voffset at 3-sigma = 25mV (after layout extraction) @wc, 1.08V
- ✦ SA-enable to Qlatch delay = 200ps @wc, 1.08V
- ✦ SA-enable pulse width = 100ps @wc, 1.08V
- ✦ Study incremental benefit of Common Centroid Layout
- ✦ Study incremental benefit of Structural Matching

In this, we have to design a latch-type sense amplifier circuit with a pre-charge circuit and latch circuit, where the two inputs to the sense amplifier are BL and BLB from the memory cell.We have to minimize offset voltage below 25 mv(After layout extraction).For this design, we will be using the common centroid layout in order to have a common Vt for pull-down devices in the circuit.

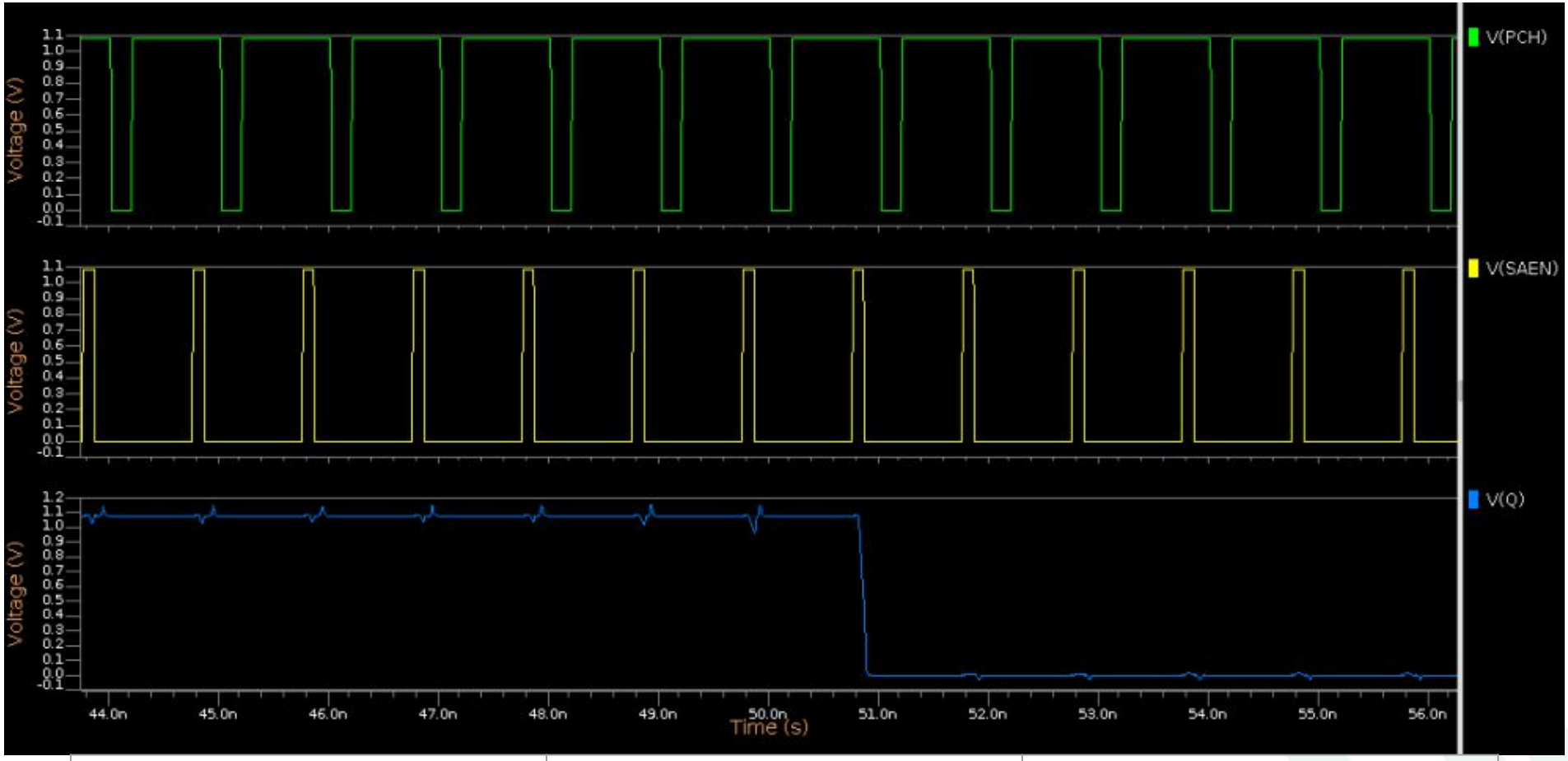
Design Schematic



Read-0 (Functionality)

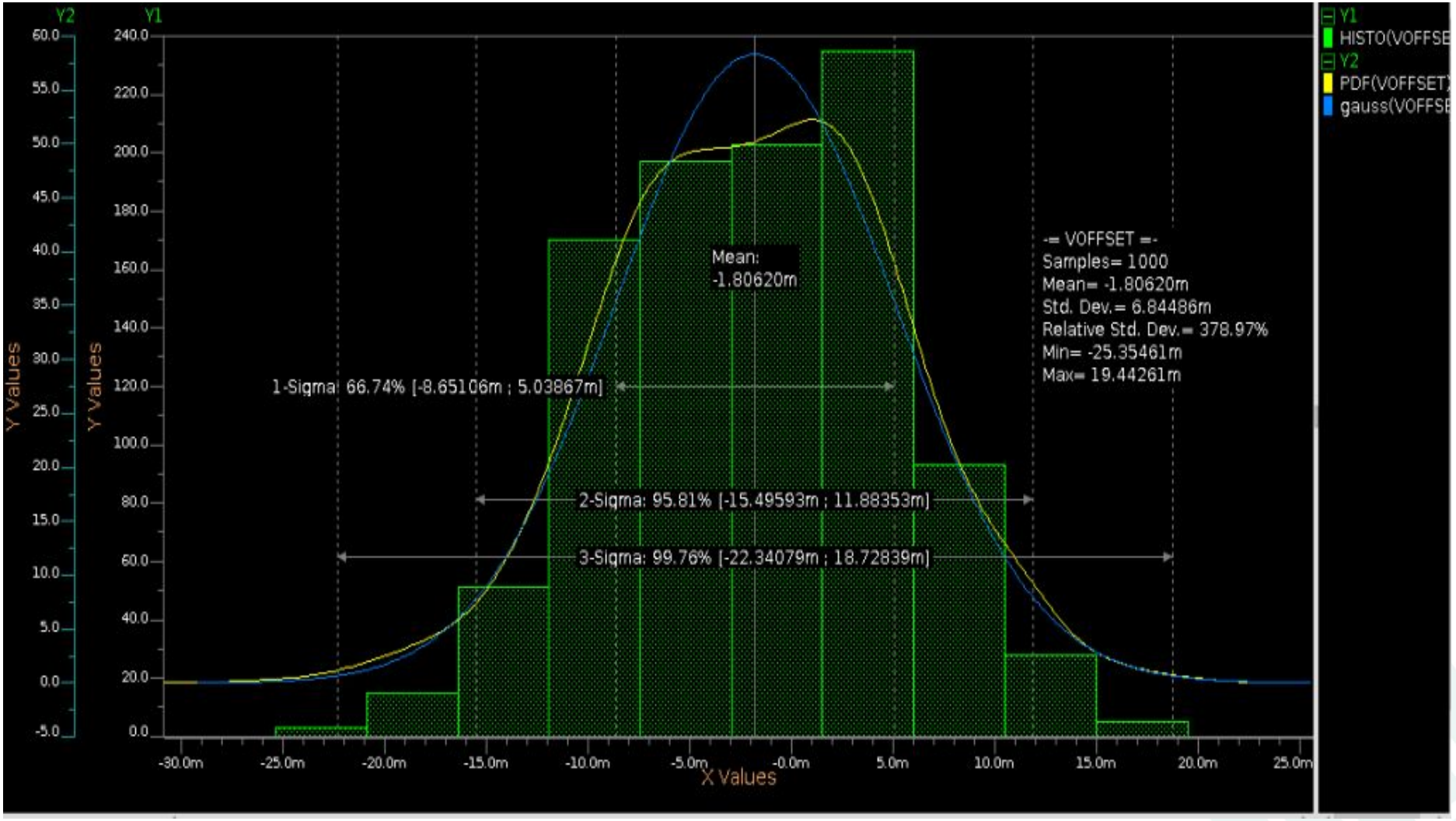


Read-0 (Delay)



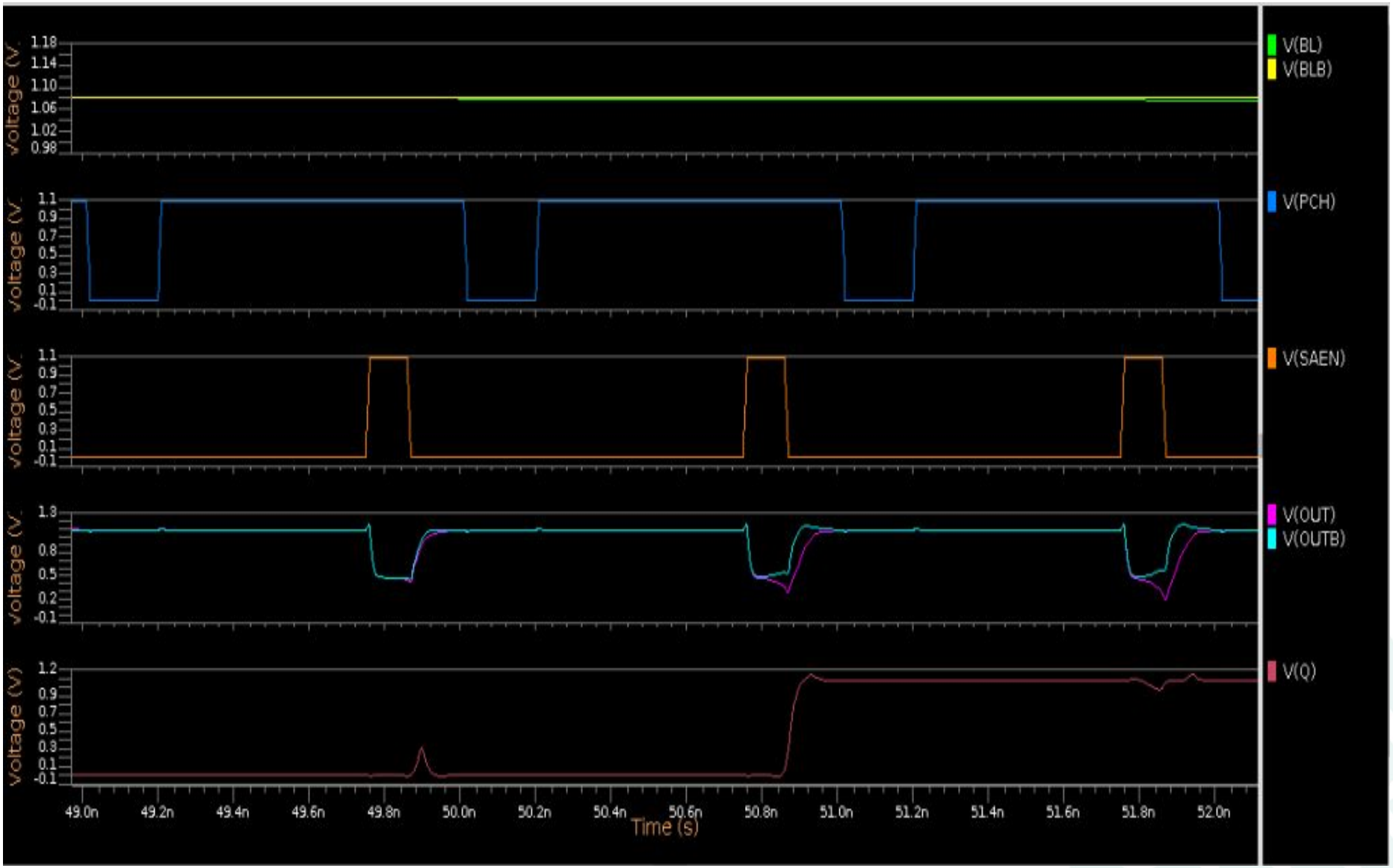
CASE	PVT	DELAY
Worst Case	SS, -40	104.29 ps
Best Case	FF, -40	52.86 ps

Read-0 (Offset)

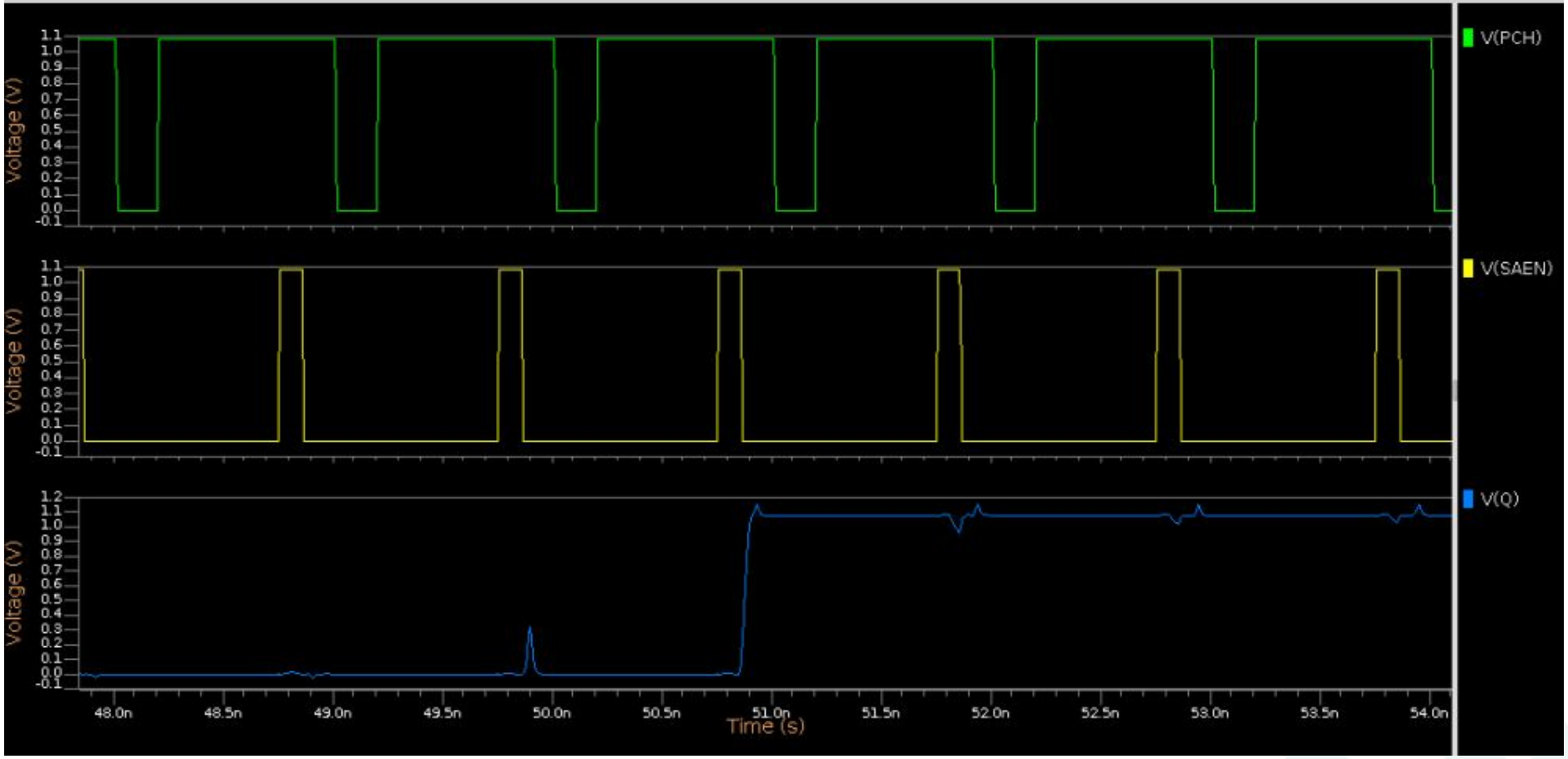


Voffset = 18.72 mV (at worst PVT → FF, -40)

Read-1 (Functionality)

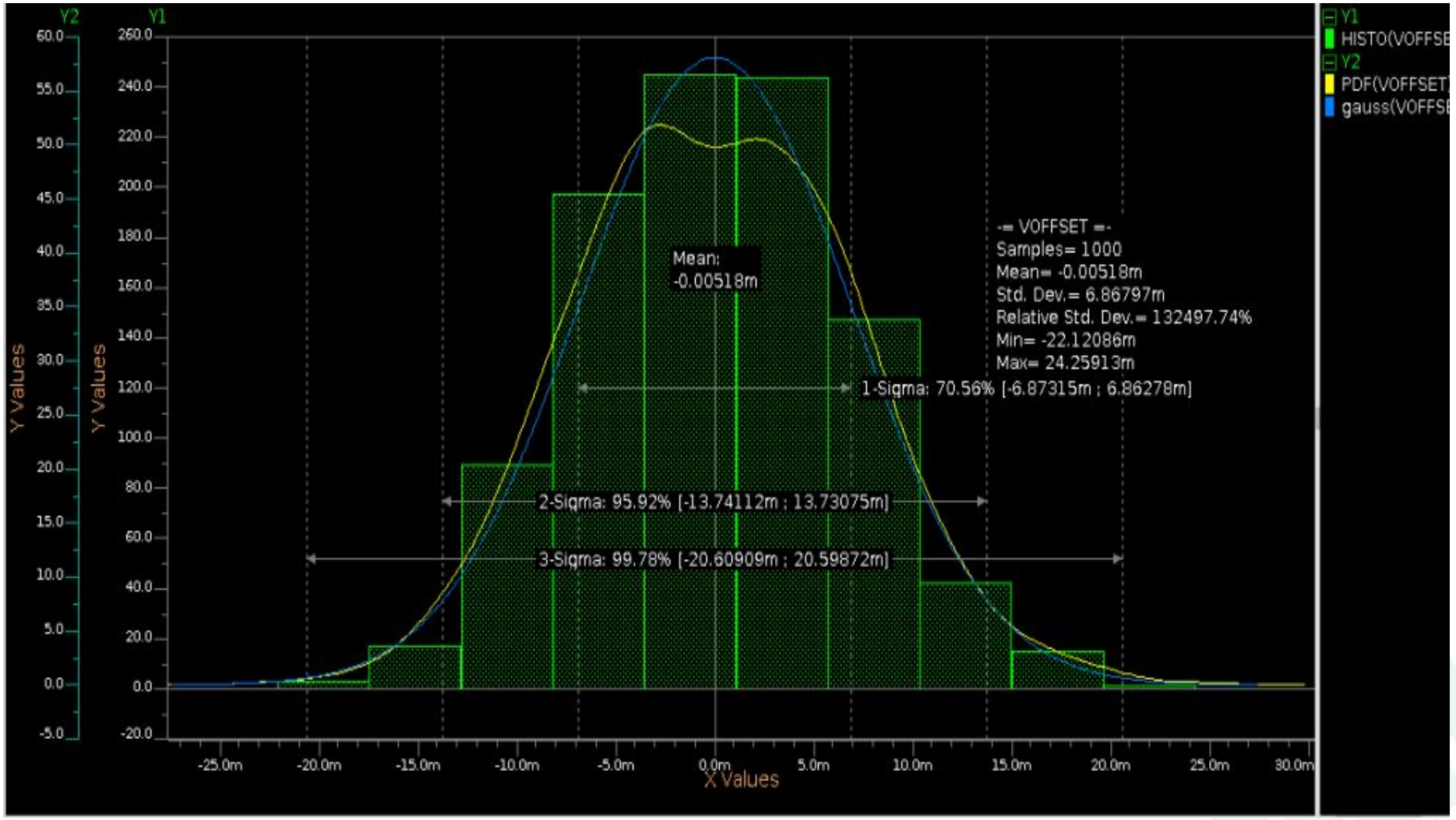


Read-1 (Delay)



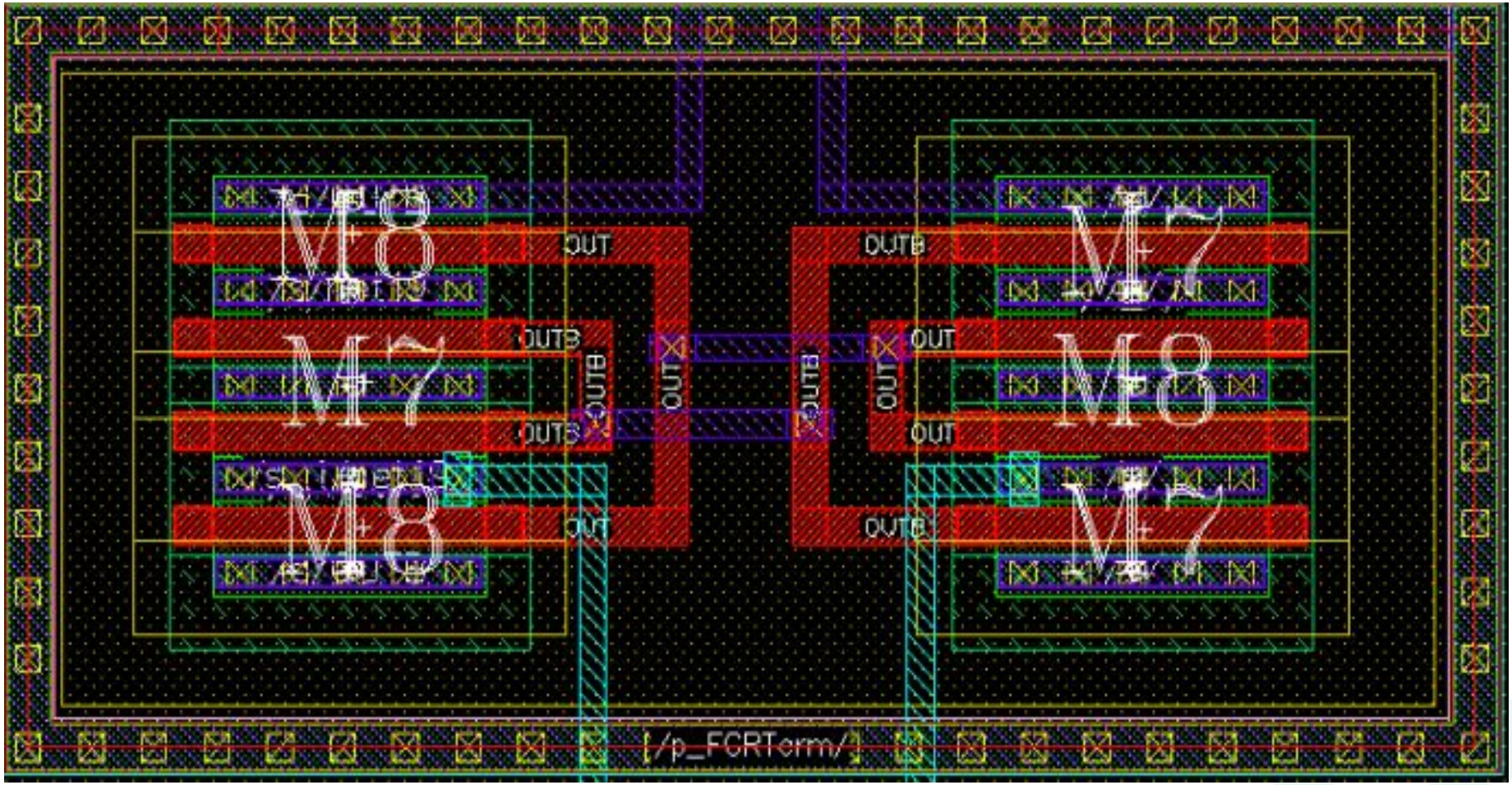
CASE	PVT	DELAY
Worst Case	SS, -40	121.31 ps
Best Case	FF, -40	67.95 ps

Read-1 (Offset)



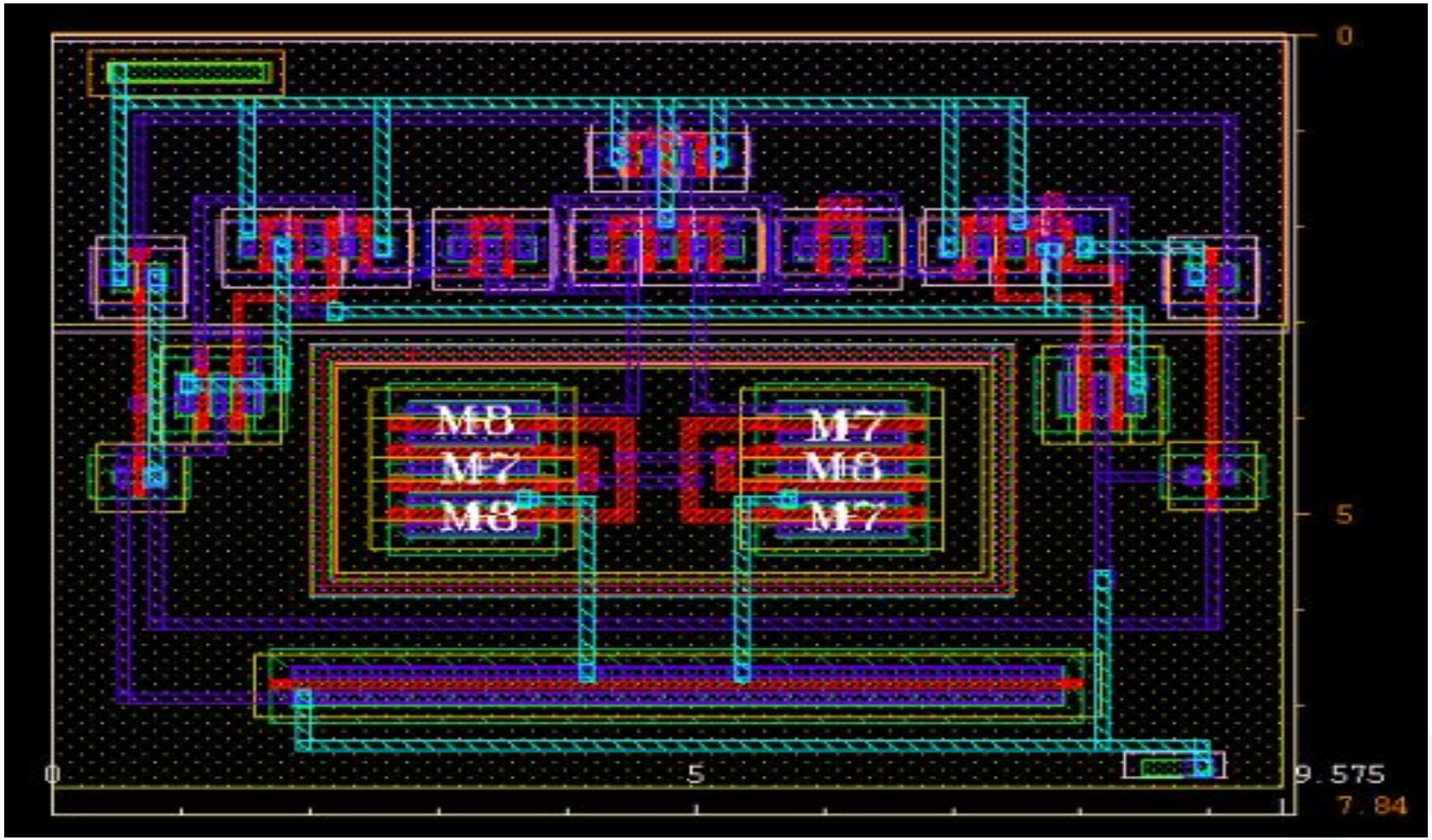
Voffset = 20.59 mV (at worst PVT → FF, -40)

Layout (Common Centroid part)



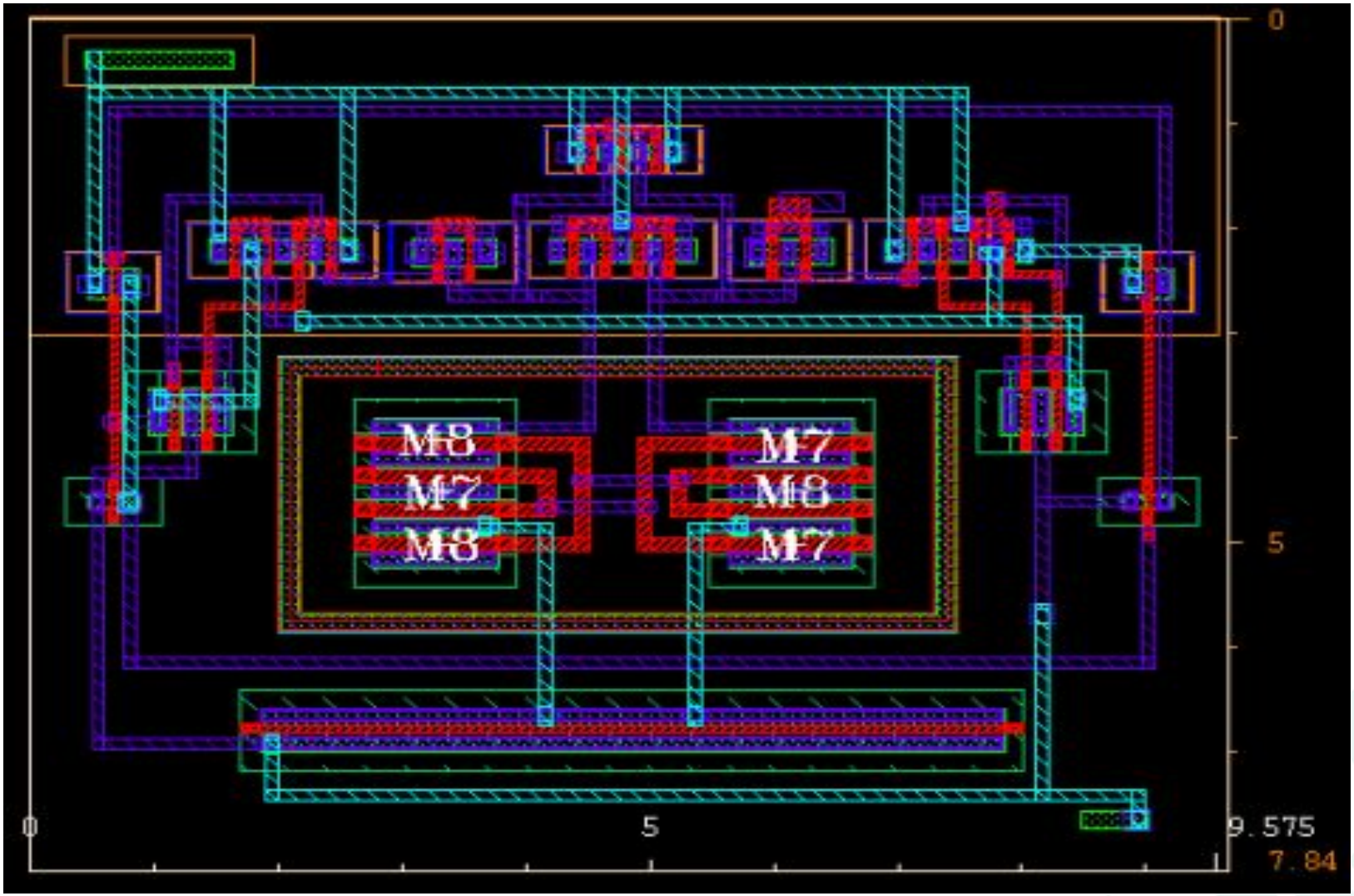
Here we have used common centroid layout for the 2 differential pull down nMOSs (M7 and M8), as we want very least Vt variations in those 2 devices due to Process variations.)

Layout (With PP – NP layers)



Width → 9.575 um, **Height → 7.84 um,** **Total Area → 75.06 um2**

Layout (Without NP-PP layers)



Challenges

- Challenges are there to minimize Voffset
- Finding the Footer and pull down size to maintain 3sigma offset
- And reducing SAen to Qlatch delay below 200 ps, with proper sizing
- Proper matching of pull down devices , it was mitigated with common centroid approach in layout
- Utilizing area while layout making

Conclusions and Future Plans

- Technical Conclusions
  - What worked?

    We have designed the layout with common centroid technique and maintained symmetricity in layout
  - What did not work?

    Layout can be more compact with utilization of available area

- Emphasise on learning from the project
  - Common centroid layout , collaboration with others teams and their design
  - Better understanding of topics

- Future plans
  - We will also try to generate the Pre-charge signal from the clock instead of directly using it as separate signal.
  - We will try to extend and design complete I/O circuitary by ourself.

References

Some references that we have followed

- A High Speed Low Voltage Latch Type Sense
- Comparative analysis of Sense Amplifiers for SRAM in 65nm CMOS technology
- MDT and DVD classroom lectures.