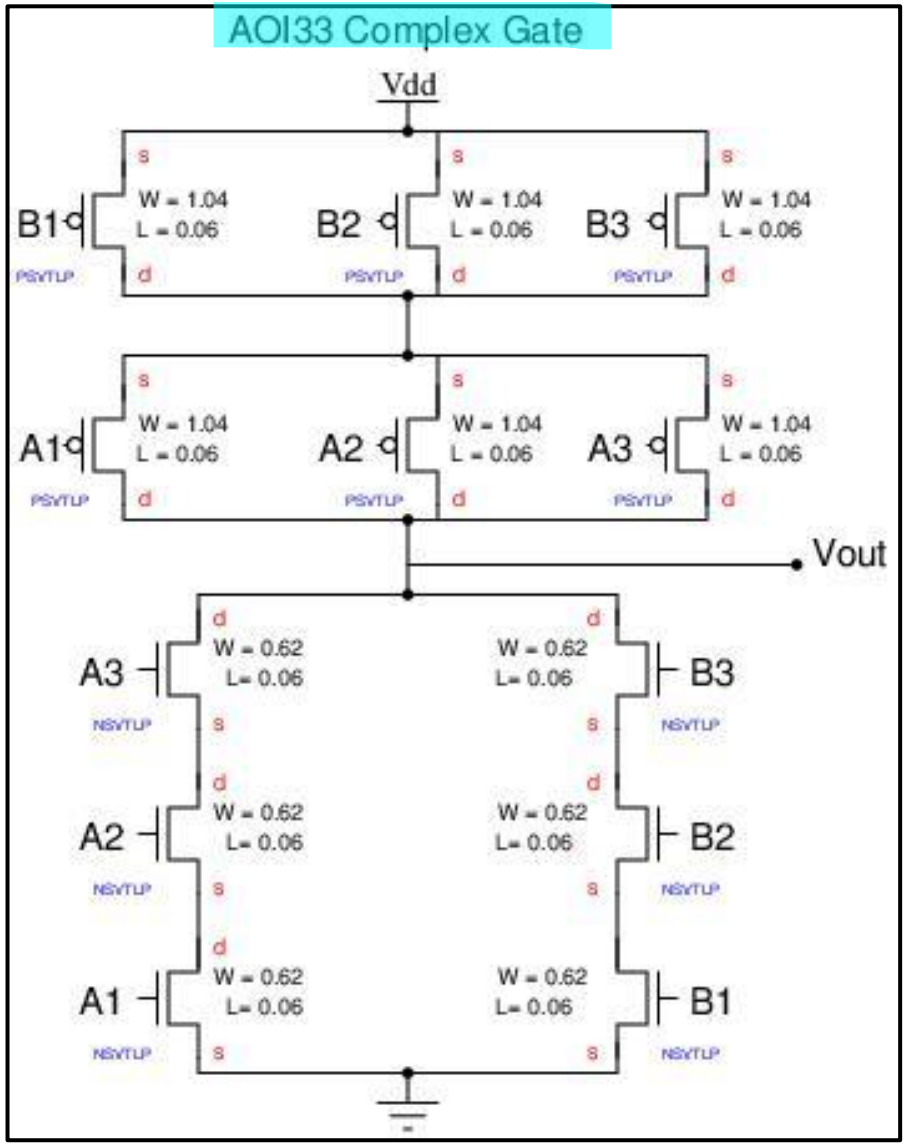
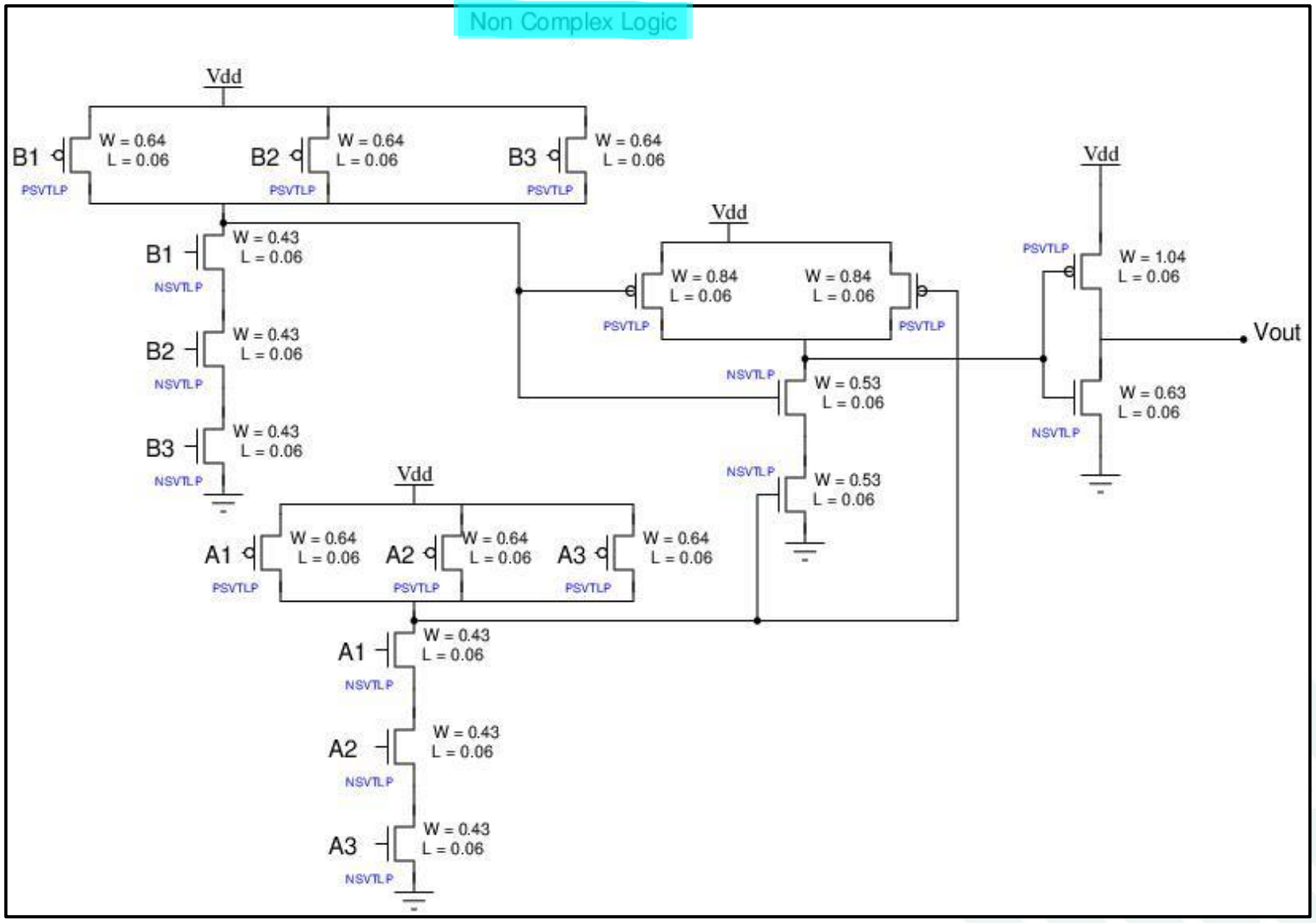
Schematics (Out = $\overline{A1.A2.A3 + B1.B2.B3}$)

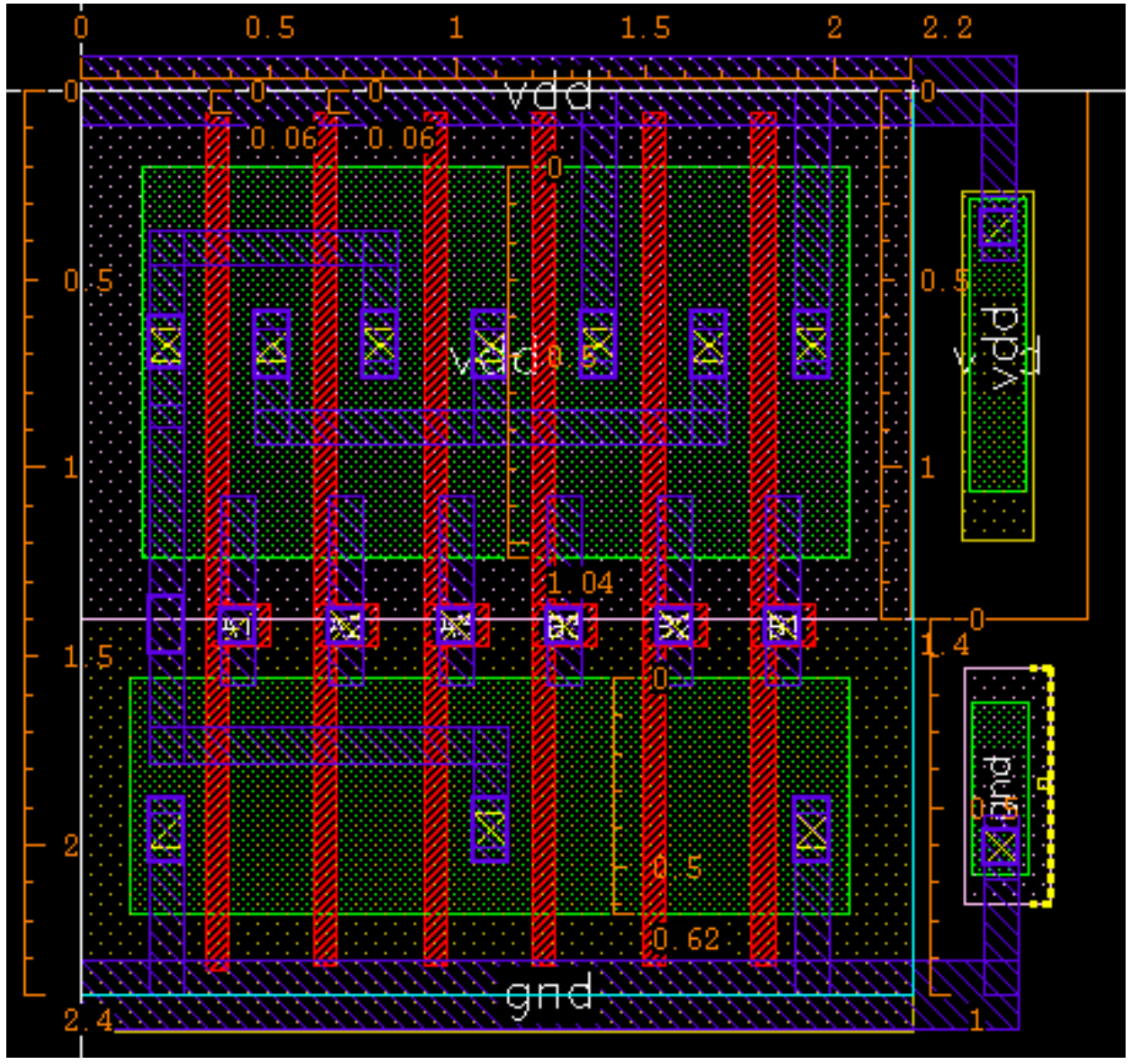




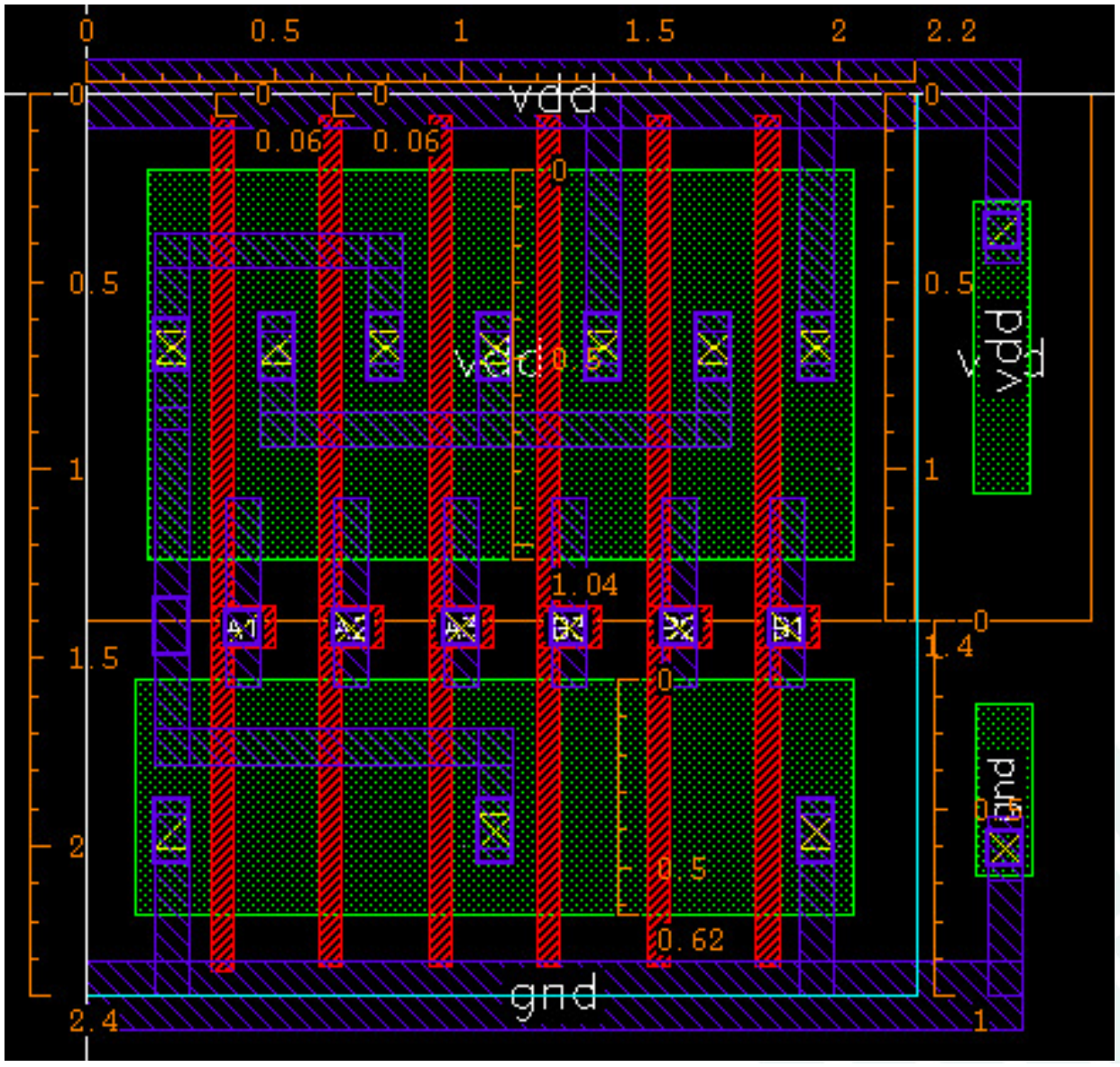
Complex logic Layout

Area ➡ 2.4um x 2.2um ➡ $5.28um^2$

With All Layers



Without NP & PP Layers



Non-Complex Logic Layout with all layers

AREA

2.4um

X

4.4um

10.56 um^2

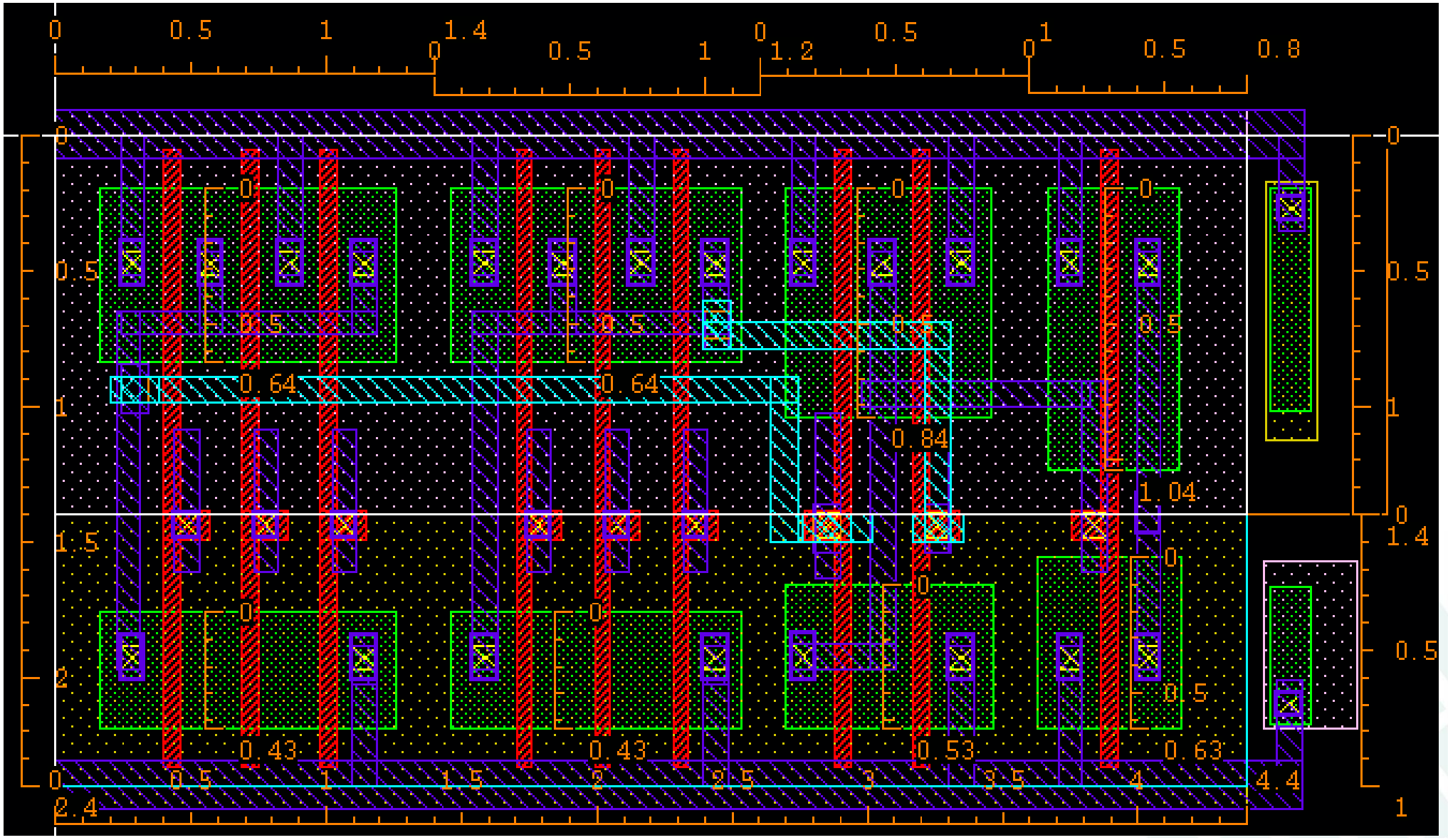
TOTAL HEIGHT

1.4um(7T)

+

1um(5T)

2.4um(12T)



Non-Complex Logic Layout without NP & PP layers

AREA

2.4um

X

4.4um

10.56 um^2

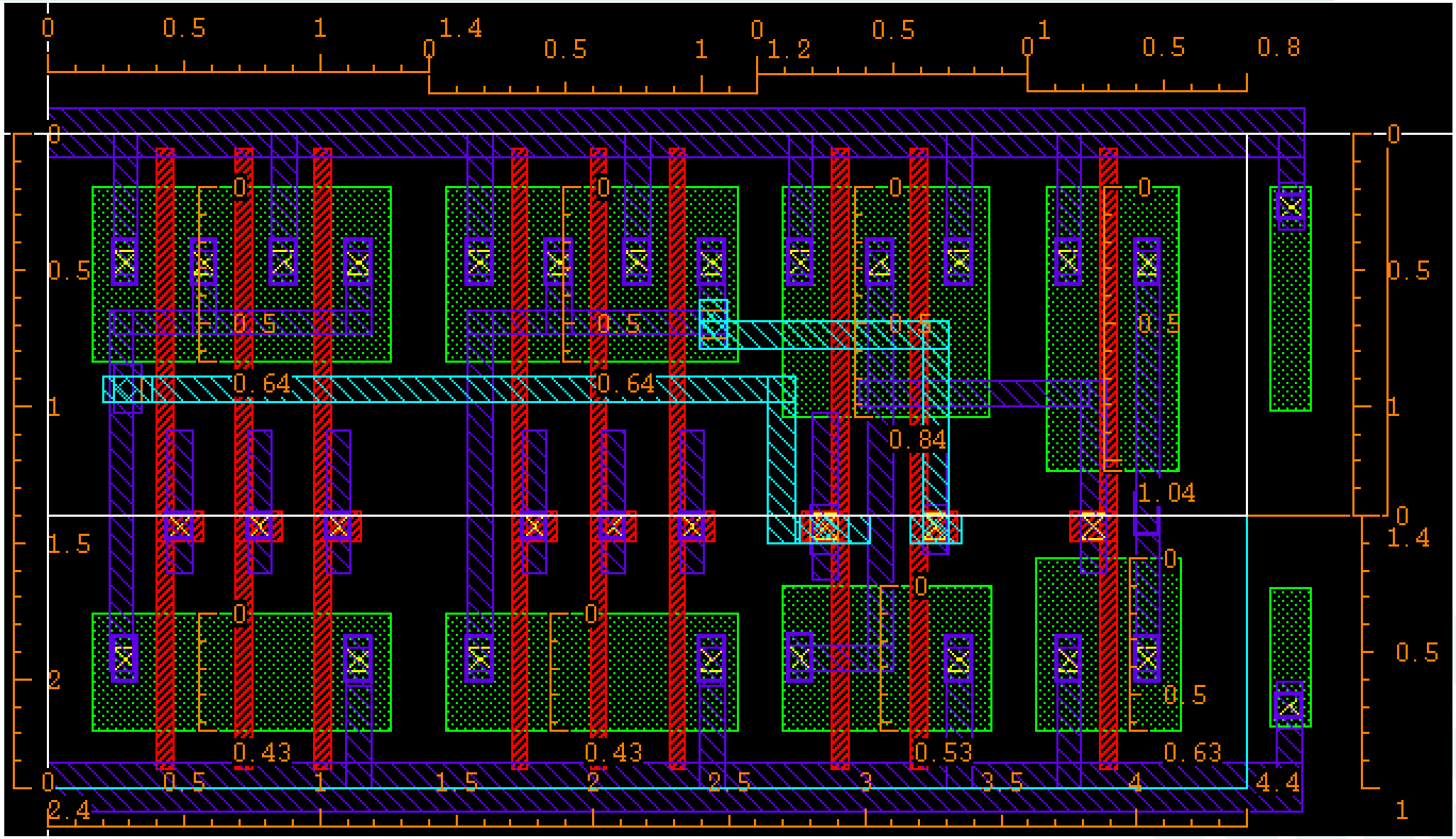
TOTAL HEIGHT

1.4um(7T)

+

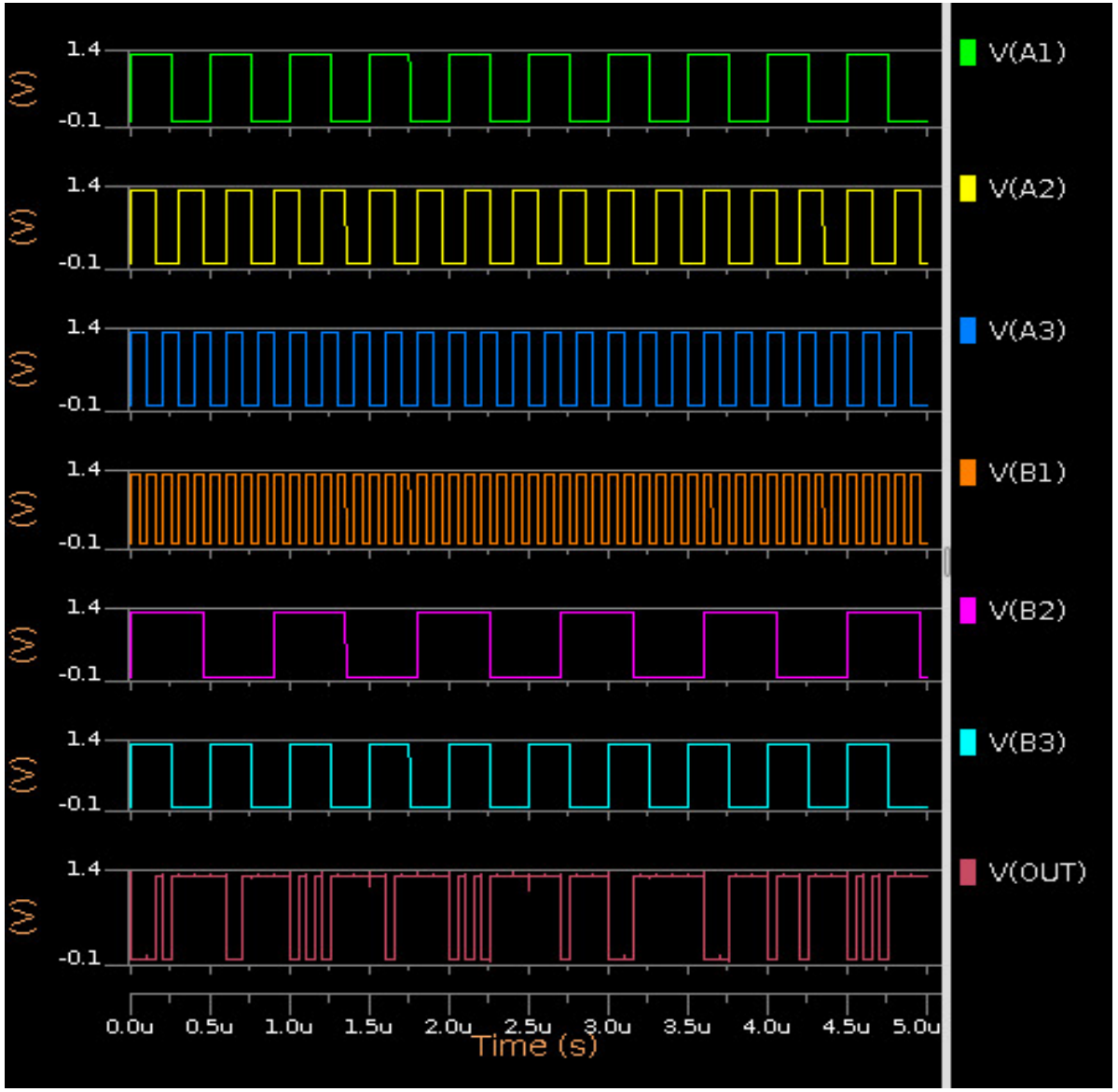
1um(5T)

2.4um(12T)

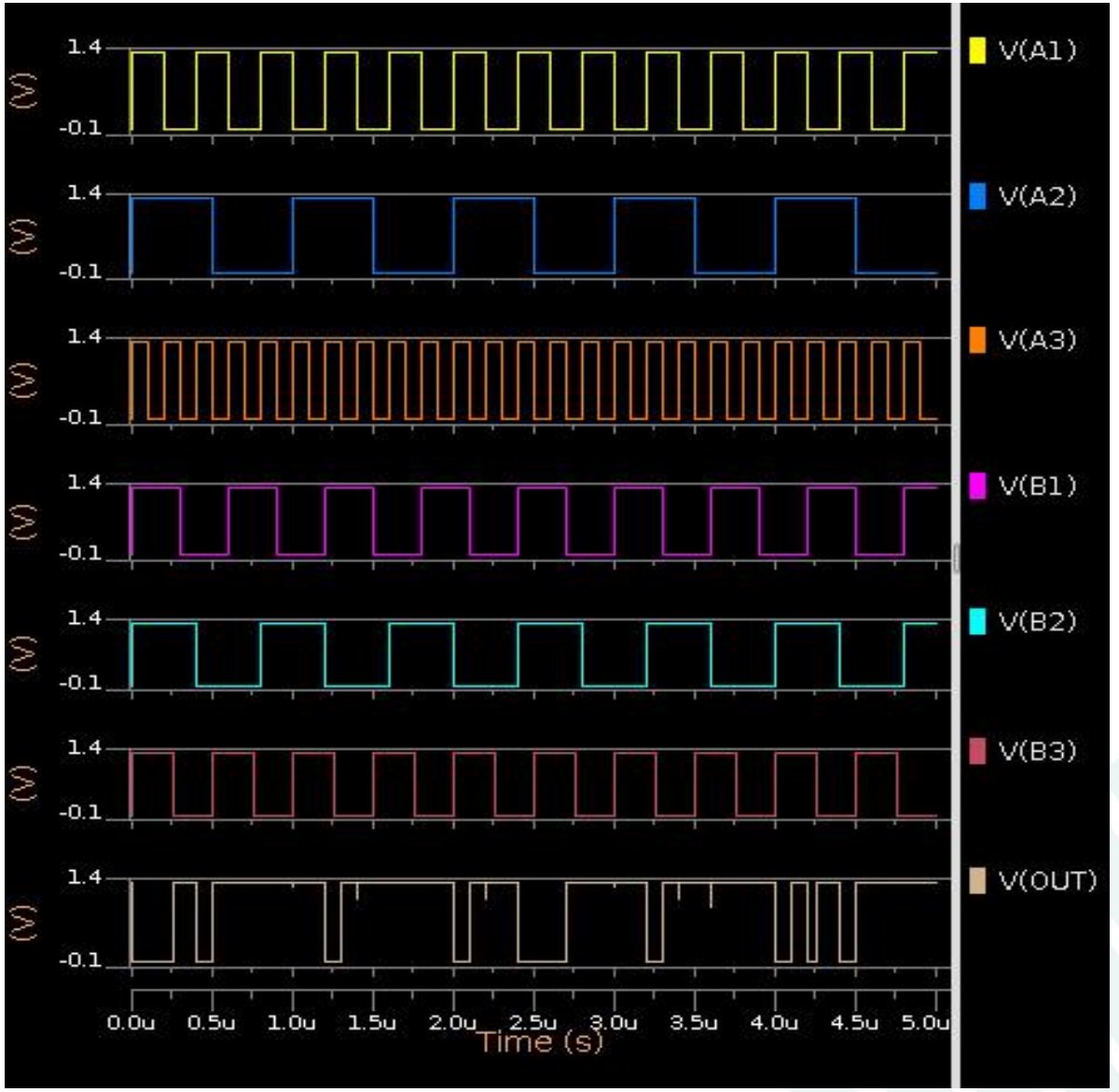


Simulation Waveforms (Ezwave)

Complex logic

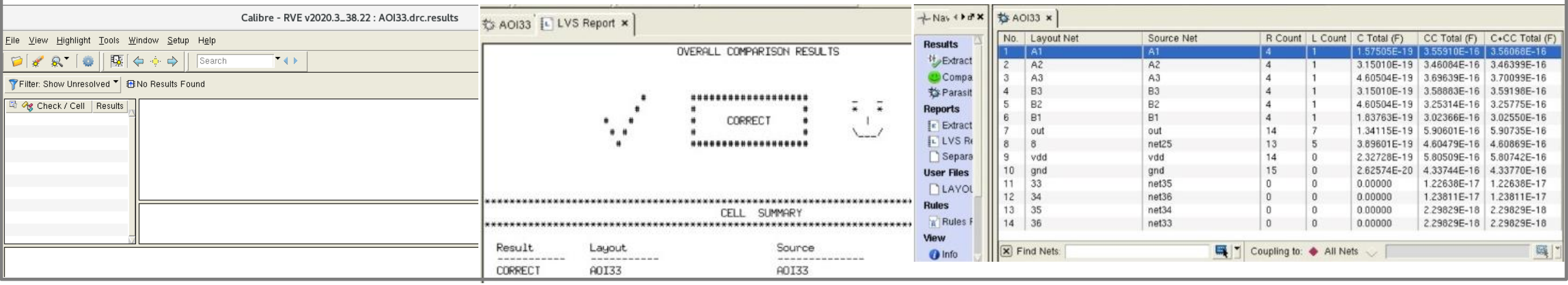


Non Complex logic

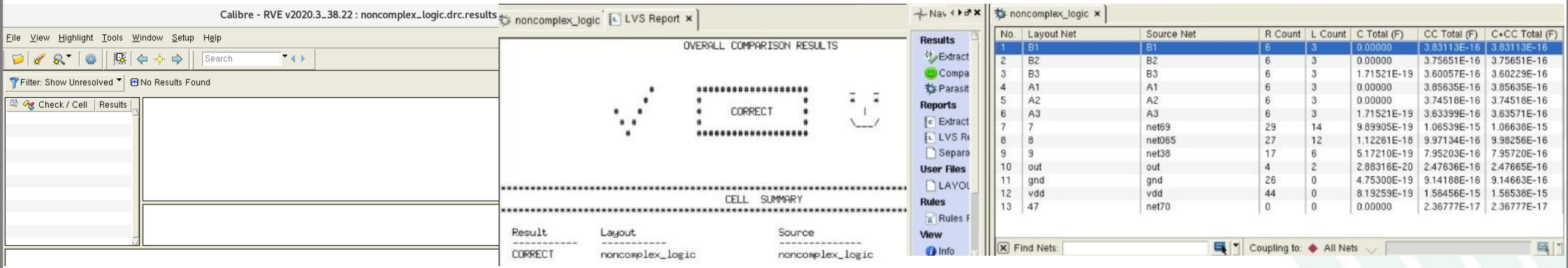


DRC, LVS and PEX Results

Complex Logic



Non Complex Logic



Simulation Results and Comparison

PARAMETERS	PVT CONDITION (Worst Case)	COMPLEX LOGIC		NON COMPLEX LOGIC	
		PRELAYOUT	POSTLAYOUT	PRELAYOUT	POSTLAYOUT
TPDR	SS, 125℃, 1.08V	151ps	203ps	206ps	200ps
TPDF	SS, 125℃, 1.08V	360ps	292ps	232ps	222ps
TCDR	FF, -40℃, 1.32V	37.3ps	38.2ps	71.3ps	72.2ps
TCDF	FF, -40℃, 1.32V	48.6ps	45.4ps	76.9ps	76.9ps
TRISE	SS, 125℃, 1.08V	273ps	259ps	130ps	132ps
TFALL	SS, 125℃, 1.08V	408ps	329ps	113ps	110ps
ILEAK	FF, 125℃, 1.32V	60.2nA	63.3nA	101nA	157nA
PDYN	TT, 25℃, 1.2V	50.1nW	48.2nW	62.2nW	90.4nW
PSTATIC	TT, 25℃, 1.2V	443pW	568pW	644pW	709pW

PARAMETER	COMPLEX LOGIC	NON COMPLEX LOGIC
AREA	**5.28 um^2**	**10.56 um^2**

PPA, Comparison and Conclusion

POWER – Power of Non Complex logic is observed to be more than Complex logic. Power of Post layout simulation is more than Pre layout simulation in both the logics.

PERFORMANCE – For both pre and post layout simulations, the delays for the Complex logic are slightly less than the Non Complex logic. The analysis has been performed under the worst case of PVT condition, so our proposed circuit will work well under all other PVT conditions.

AREA – Area of Complex logic($5.28 um^2$) is half of the area of Non Complex logic($10.56\ um^2$).

LEARNINGS

1. Making layout from scratch (without generating from source).
2. About pc_ct pins (to restrict short circuiting).
3. Sizing beyond theoretical calculation (logical effort).
4. The circuits will be fast for high voltage and low temp. Slow for low voltage and high temperature.
5. Learning about standard cells (DRC's like Poly head to head DRC)
6. Use of M2 for routing.
7. Tradeoff between delays and leakage.
8. Better layouts may lead to reduced delays after PEX.
9. Area is *Gold!!*