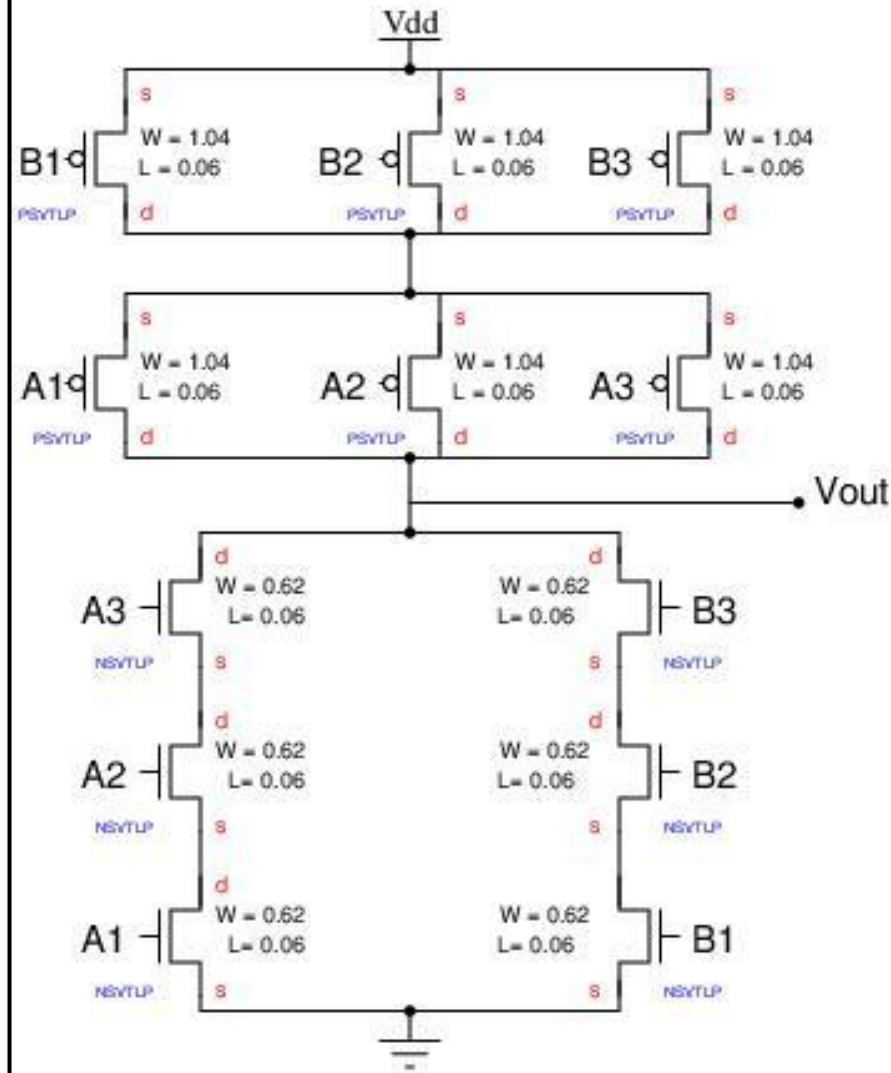


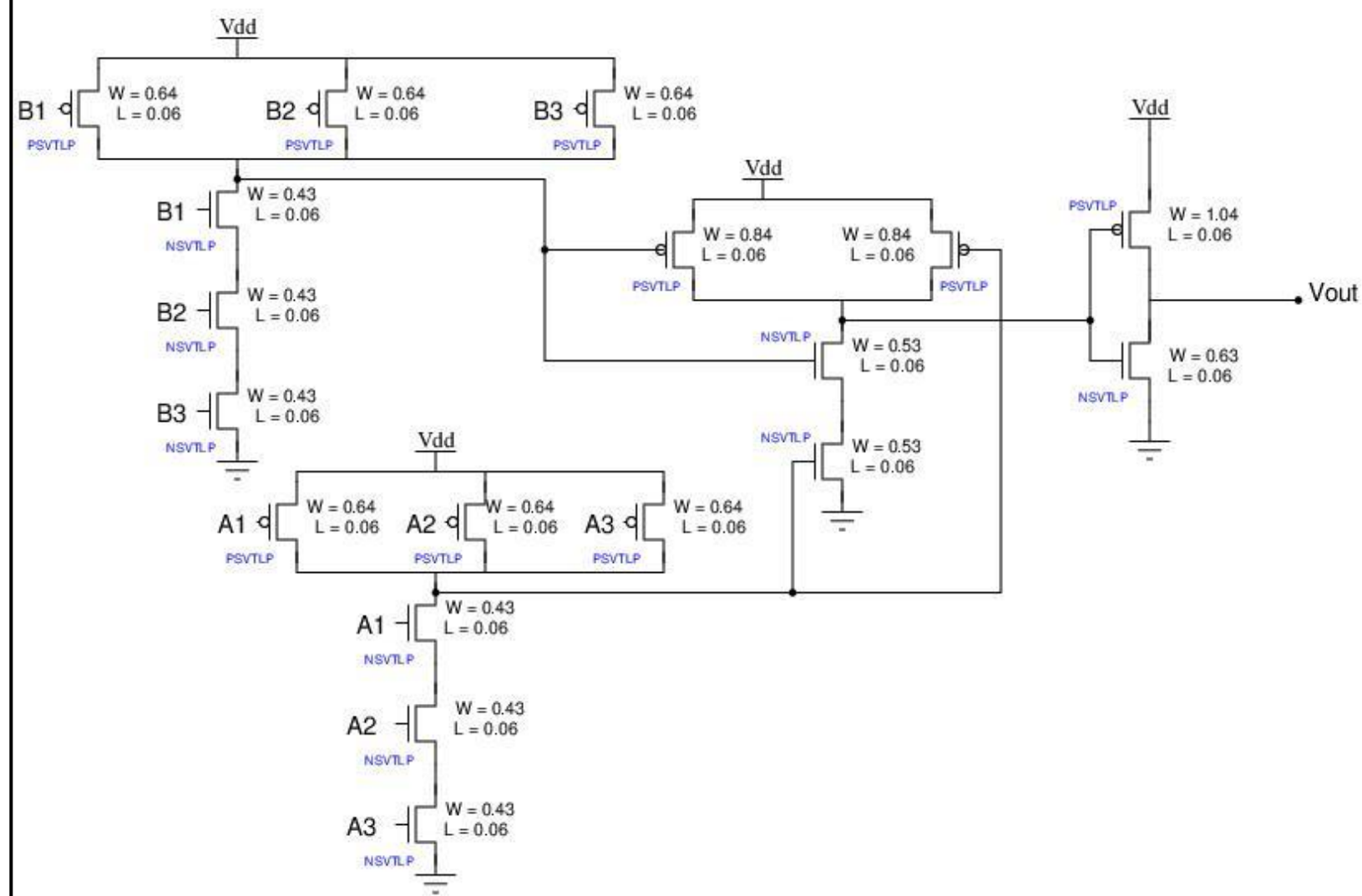
Schematics (Out = A1.A2.A3 + B1.B2.B3)



AOI33 Complex Gate



Non Complex Logic

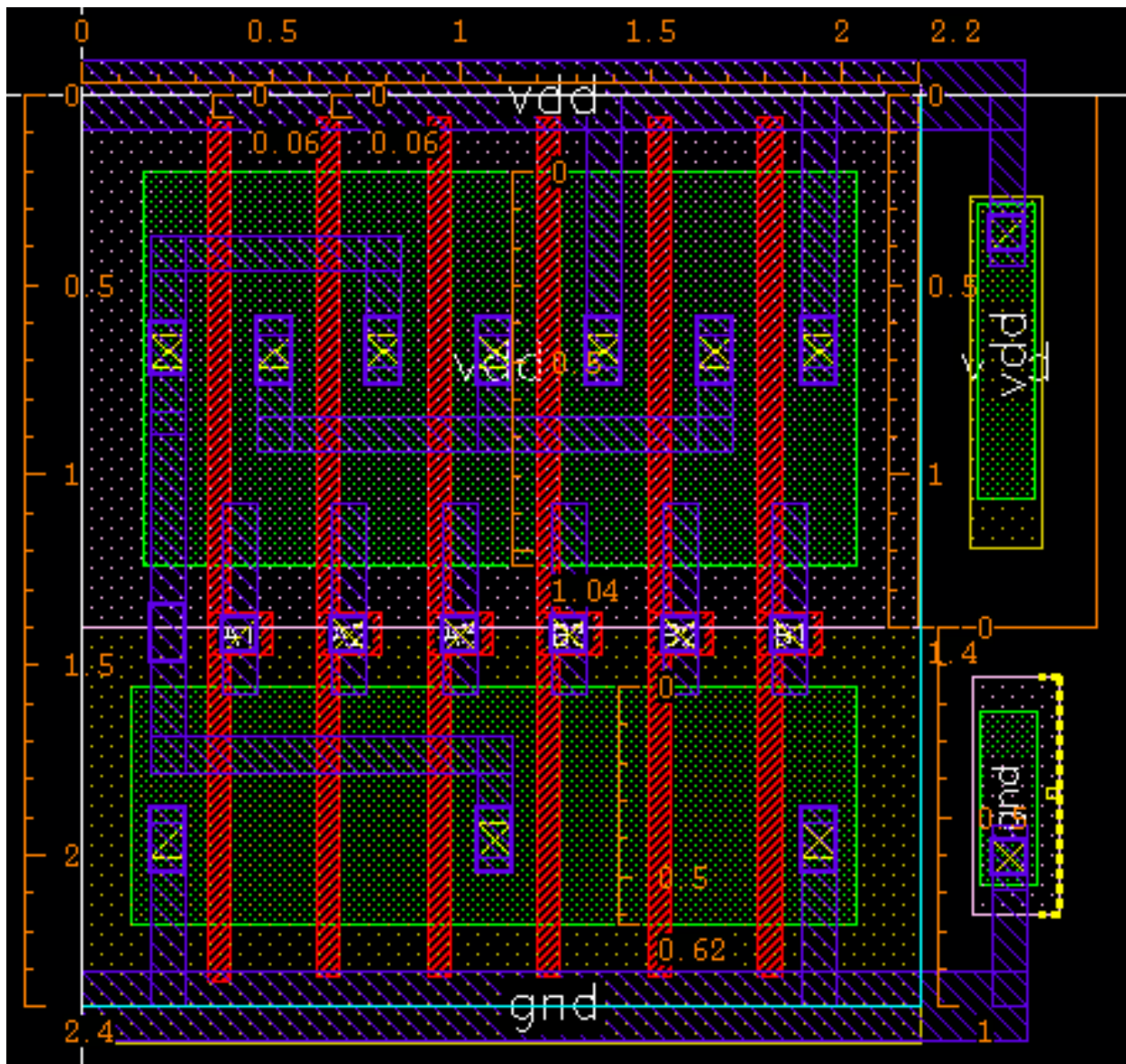


Complex logic Layout

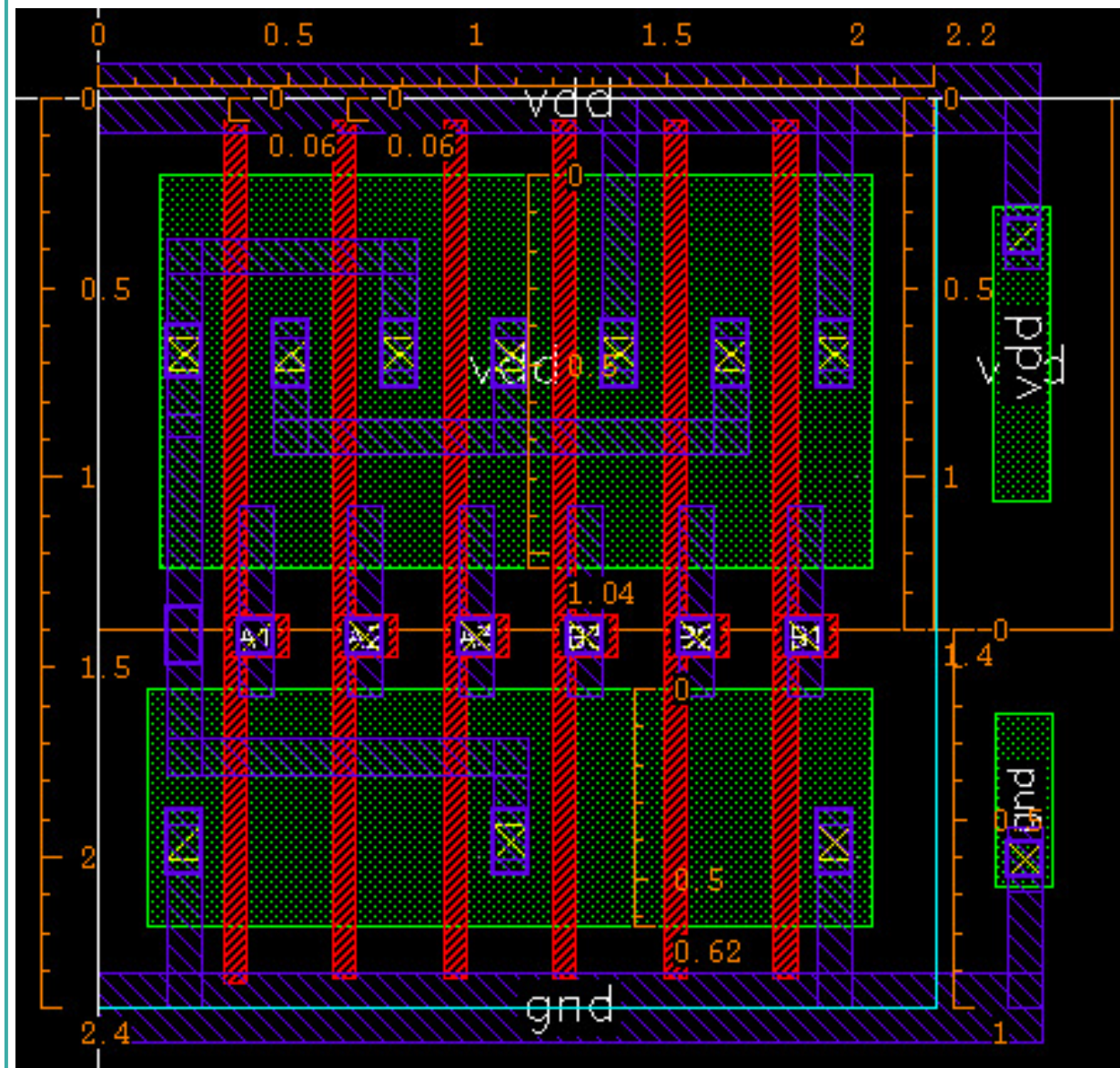
Area $\Rightarrow 2.4\mu\text{m} \times 2.2\mu\text{m} \Rightarrow 5.28\mu\text{m}^2$



With All Layers



Without NP & PP Layers



Non-Complex Logic Layout with all layers



AREA



2.4 μm

X

4.4 μm



10.56 μm^2

TOTAL HEIGHT



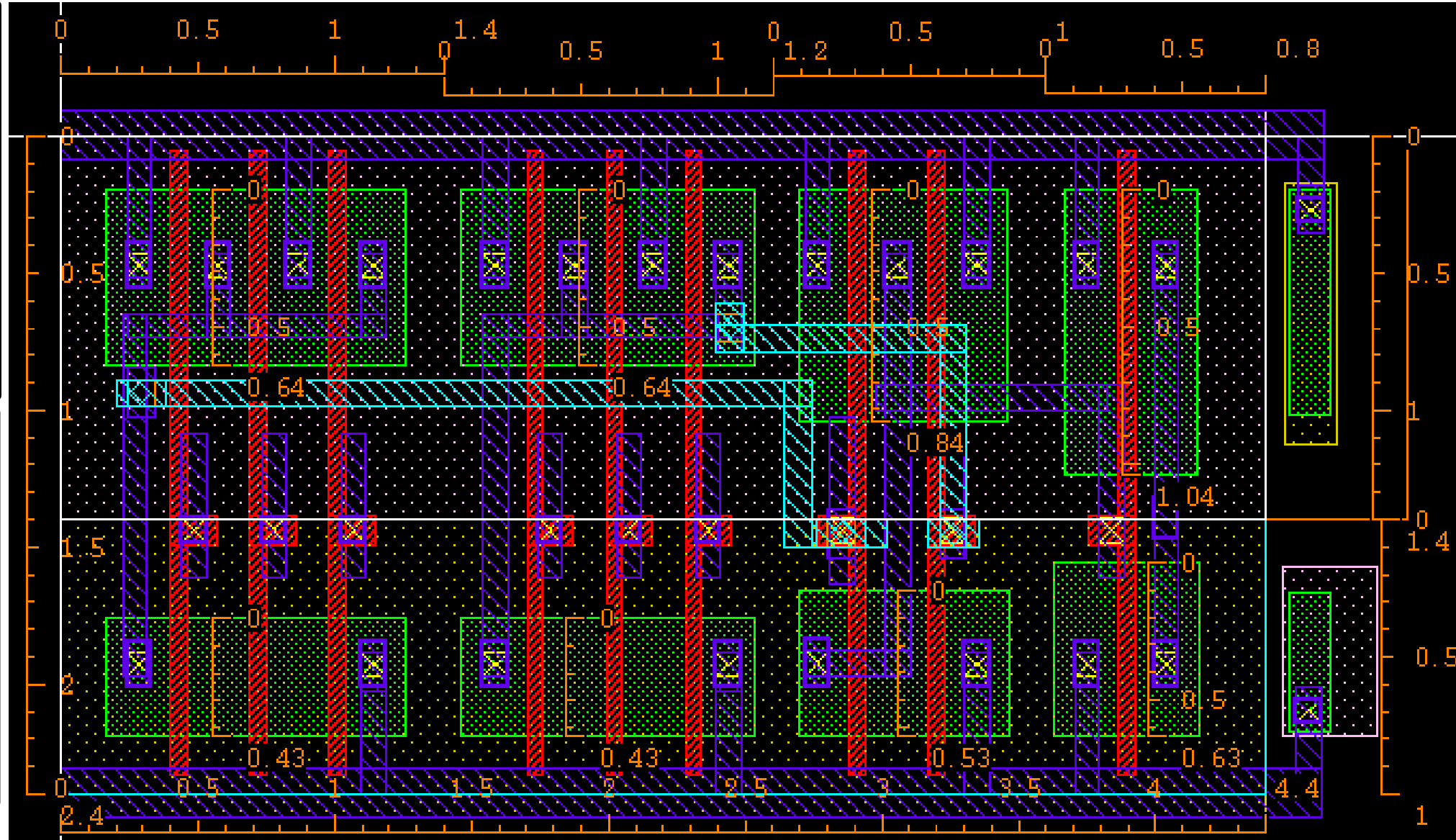
1.4 μm (7T)

+

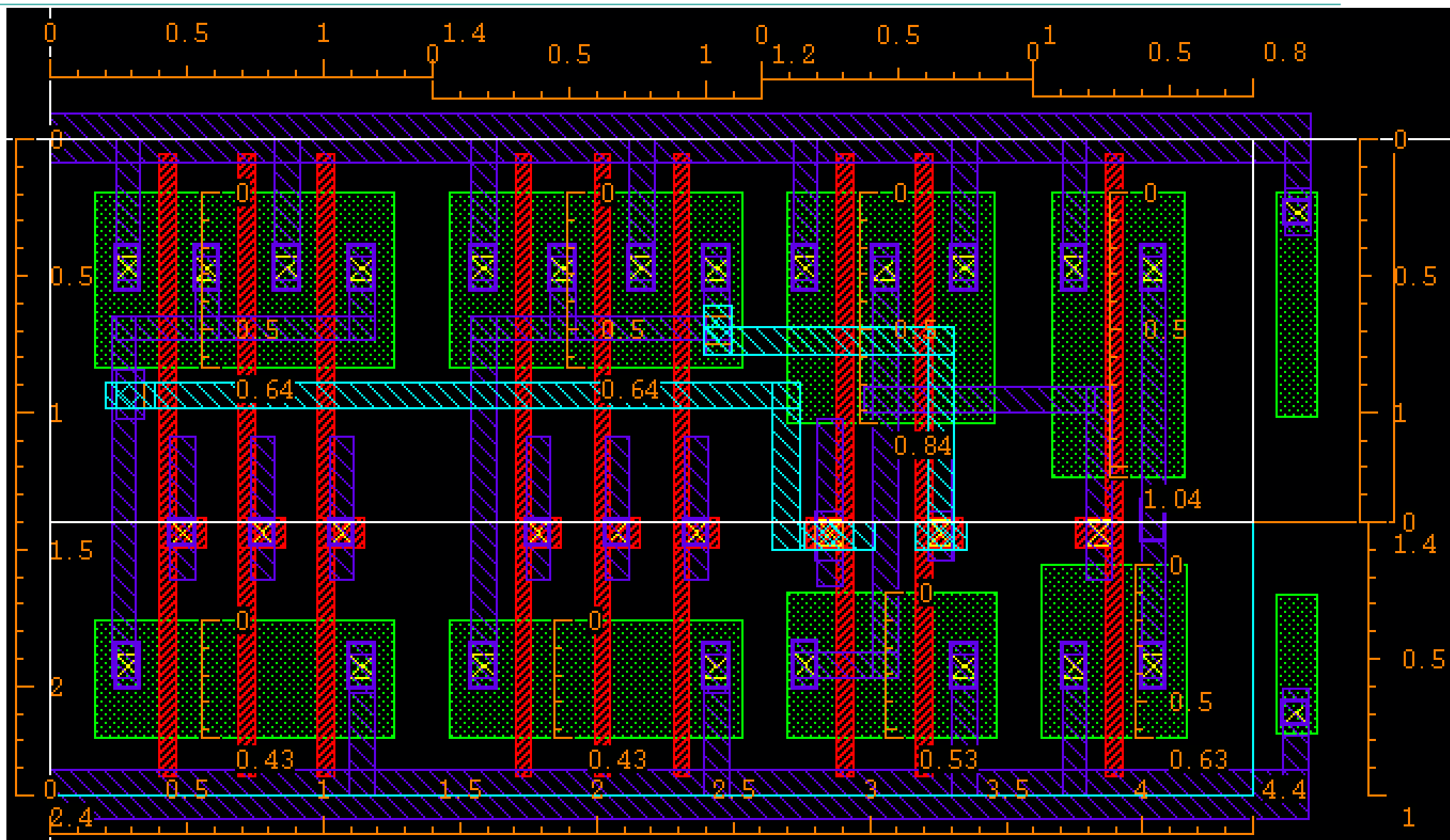
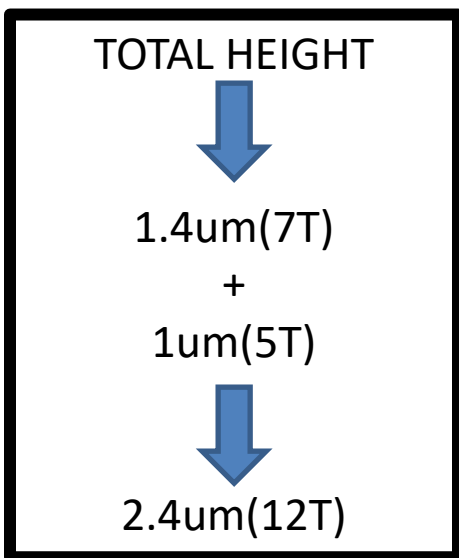
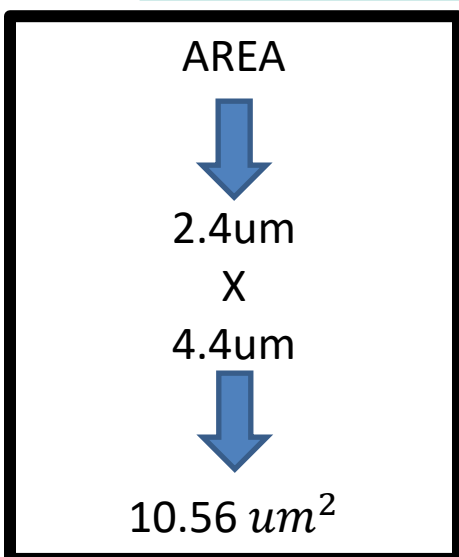
1 μm (5T)



2.4 μm (12T)



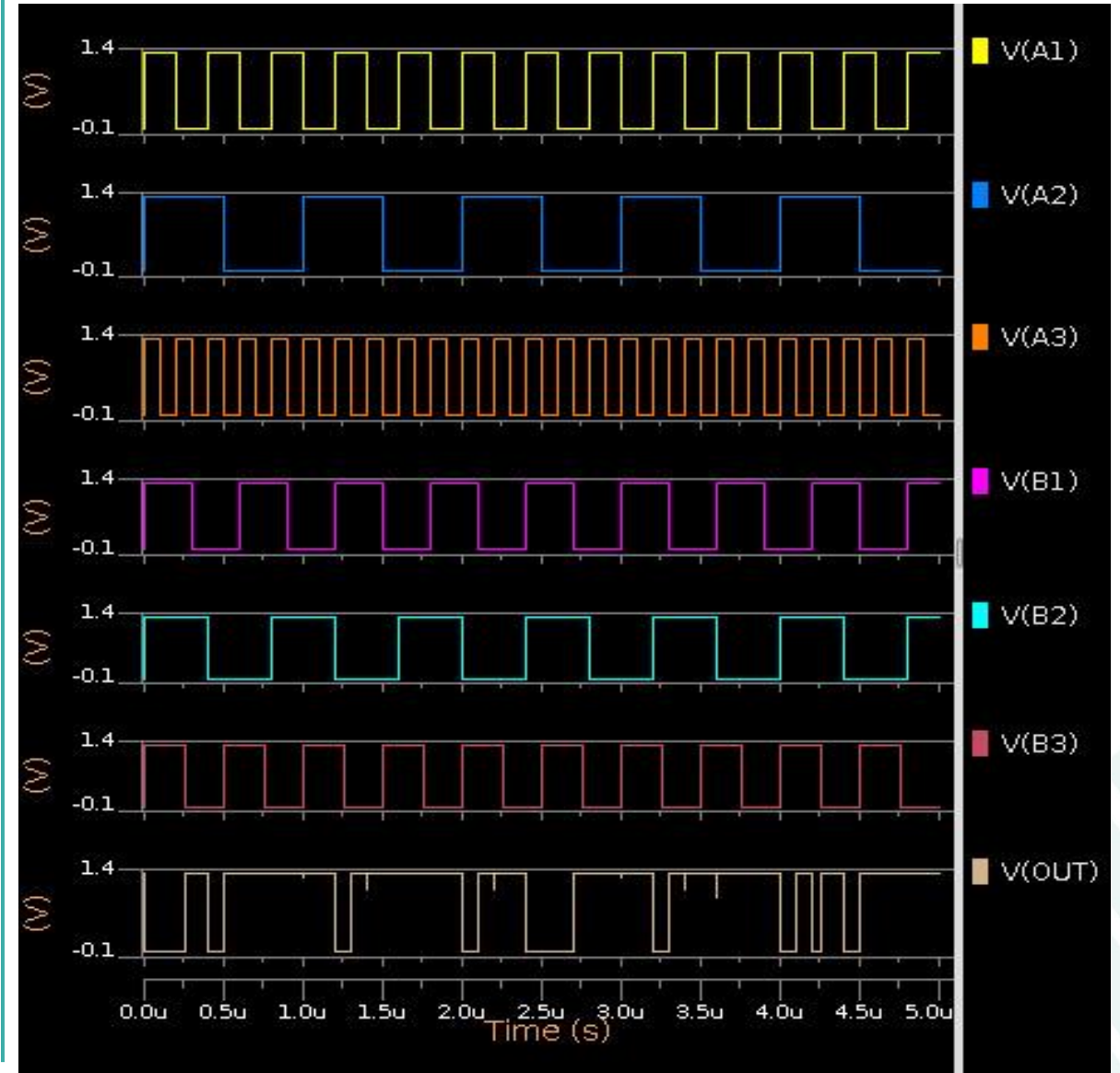
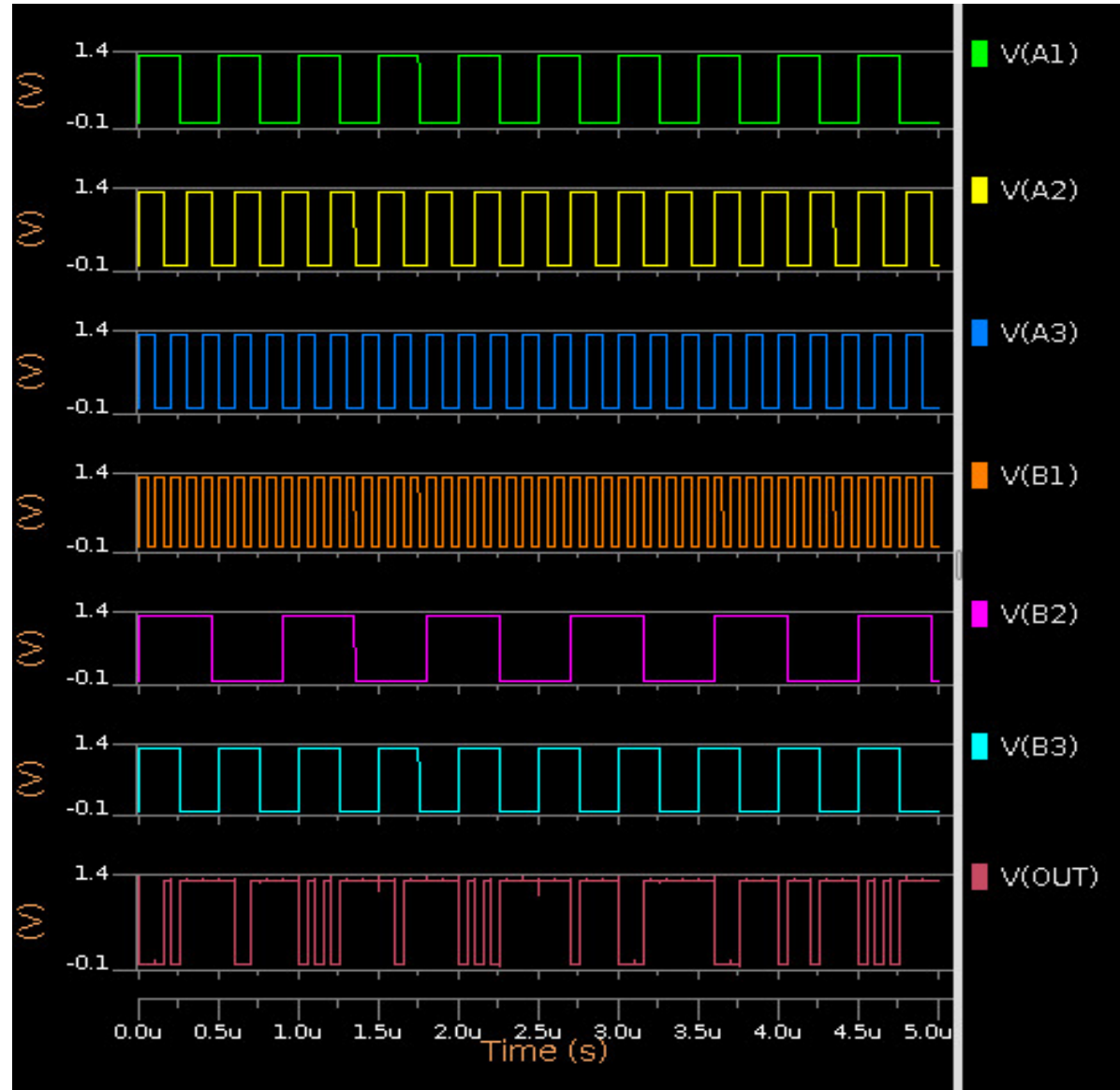
Non-Complex Logic Layout without NP & PP layers



Simulation Waveforms (Ezwave)

Complex logic

Non Complex logic



DRC, LVS and PEX Results



Complex Logic

Calibre - RVE v2020.3_38.22 : AOI33.drc.results

File View Highlight Tools Window Setup Help

Filter: Show Unresolved No Results Found

Check / Cell Results

AOI33 LVS Report

OVERALL COMPARISON RESULTS

CORRECT

CELL SUMMARY

Result	Layout	Source
CORRECT	AOI33	AOI33

Results

- Extract
- Compa
- Parasit

Reports

- Extract
- LVS R
- Separa

User Files

- LAYOU

Rules

- Rules F

View

- Info

No.	Layout Net	Source Net	R Count	L Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	A1	A1	4	1	1.57505E-19	3.55910E-16	3.56068E-16
2	A2	A2	4	1	3.15010E-19	3.46004E-16	3.46399E-16
3	A3	A3	4	1	4.60504E-19	3.69639E-16	3.70099E-16
4	B3	B3	4	1	3.15010E-19	3.58883E-16	3.59198E-16
5	B2	B2	4	1	4.60504E-19	3.25314E-16	3.25775E-16
6	B1	B1	4	1	1.83763E-19	3.02366E-16	3.02550E-16
7	out	out	14	7	1.34115E-19	5.90601E-16	5.90735E-16
8	8	net25	13	5	3.89601E-19	4.60479E-16	4.60869E-16
9	vdd	vdd	14	0	2.32728E-19	5.80509E-16	5.80742E-16
10	gnd	gnd	15	0	2.62574E-20	4.33744E-16	4.33770E-16
11	33	net35	0	0	0.00000	1.22638E-17	1.22638E-17
12	34	net36	0	0	0.00000	1.23811E-17	1.23811E-17
13	35	net34	0	0	0.00000	2.29829E-18	2.29829E-18
14	36	net33	0	0	0.00000	2.29829E-18	2.29829E-18

Find Nets: Coupling to: All Nets

Non Complex Logic

Calibre - RVE v2020.3_38.22 : noncomplex_logic.drc.results

File View Highlight Tools Window Setup Help

Filter: Show Unresolved No Results Found

Check / Cell Results

noncomplex_logic LVS Report

OVERALL COMPARISON RESULTS

CORRECT

CELL SUMMARY

Result	Layout	Source
CORRECT	noncomplex_logic	noncomplex_logic

Results

- Extract
- Compa
- Parasit

Reports

- Extract
- LVS R
- Separa

User Files

- LAYOU

Rules

- Rules F

View

- Info

No.	Layout Net	Source Net	R Count	L Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	B1	B1	6	3	0.00000	3.83113E-16	3.83113E-16
2	B2	B2	6	3	0.00000	3.75651E-16	3.75651E-16
3	B3	B3	6	3	1.71521E-19	3.60057E-16	3.60229E-16
4	A1	A1	6	3	0.00000	3.85635E-16	3.85635E-16
5	A2	A2	6	3	0.00000	3.74518E-16	3.74518E-16
6	A3	A3	6	3	1.71521E-19	3.63399E-16	3.63571E-16
7	7	net69	29	14	9.89905E-19	1.06539E-15	1.06638E-15
8	8	net065	27	12	1.12261E-18	9.97134E-16	9.98256E-16
9	9	net38	17	6	5.17210E-19	7.95203E-16	7.95720E-16
10	out	out	4	2	2.88316E-20	2.47636E-16	2.47665E-16
11	gnd	gnd	26	0	4.75300E-19	9.14168E-16	9.14663E-16
12	vdd	vdd	44	0	8.19259E-19	1.56456E-15	1.56538E-15
13	47	net70	0	0	0.00000	2.36777E-17	2.36777E-17

Find Nets: Coupling to: All Nets

Simulation Results and Comparison



PARAMETERS	PVT CONDITION (Worst Case)	COMPLEX LOGIC		NON COMPLEX LOGIC	
		PRELAYOUT	POSTLAYOUT	PRELAYOUT	POSTLAYOUT
TPDR	SS, 125°C, 1.08V	151ps	203ps	206ps	200ps
TPDF	SS, 125°C, 1.08V	360ps	292ps	232ps	222ps
TCDR	FF, -40°C, 1.32V	37.3ps	38.2ps	71.3ps	72.2ps
TCDF	FF, -40°C, 1.32V	48.6ps	45.4ps	76.9ps	76.9ps
TRISE	SS, 125°C, 1.08V	273ps	259ps	130ps	132ps
TFALL	SS, 125°C, 1.08V	408ps	329ps	113ps	110ps
ILEAK	FF, 125°C, 1.32V	60.2nA	63.3nA	101nA	157nA
PDYN	TT, 25°C, 1.2V	50.1nW	48.2nW	62.2nW	90.4nW
PSTATIC	TT, 25°C, 1.2V	443pW	568pW	644pW	709pW

PARAMETER	COMPLEX LOGIC	NON COMPLEX LOGIC
AREA	5.28 μm^2	10.56 μm^2

PPA, Comparison and Conclusion



POWER – Power of Non Complex logic is observed to be more than Complex logic. Power of Post layout simulation is more than Pre layout simulation in both the logics.

PERFORMANCE – For both pre and post layout simulations, the delays for the Complex logic are slightly less than the Non Complex logic. The analysis has been performed under the worst case of PVT condition, so our proposed circuit will work well under all other PVT conditions.

AREA – Area of Complex logic($5.28\mu m^2$) is half of the area of Non Complex logic($10.56\mu m^2$).

LEARNINGS



1. Making layout from scratch (without generating from source).
2. About pc_ct pins (to restrict short circuiting).
3. Sizing beyond theoretical calculation (logical effort).
4. The circuits will be fast for high voltage and low temp. Slow for low voltage and high temperature.
5. Learning about standard cells (DRC's like Poly head to head DRC)
6. Use of M2 for routing.
7. Tradeoff between delays and leakage.
8. Better layouts may lead to reduced delays after PEX.
9. *Area is Gold!!*

