Low voltage power efficient bulk driven Current Mirror

Small size current mirror

Sudhanshu Trivedi MT21212
Akash Saxena MT21185

INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY **DELHI**

Why Current Mirror?

Current mirror = copying/mirroring of current

A current mirror is a circuit that provide a stable replica of reference current source to different section of circuit and independent of output voltage and loading.

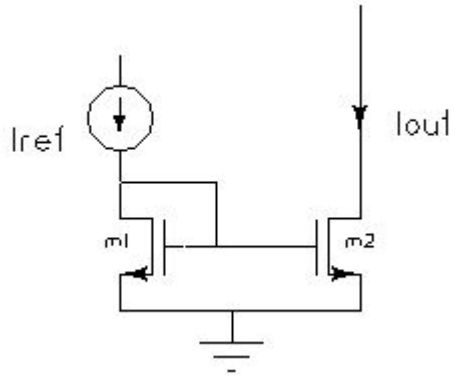
A no. copies of can be generated without much impacting on current source.

Current mirrors find wide application in analog circuits,The current mirror is often used to provide bias currents and active loads in amplifier stages.

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$



Different current mirror circuits are provided over the time and improving performance of previous circuits , like simple current mirror , pmos used high impedance CM,cascoded CM, Self Driven cascode current mirror and many more and they are great in functionality . They all have one thing in common is GATE driven.

Why Bulk driven?

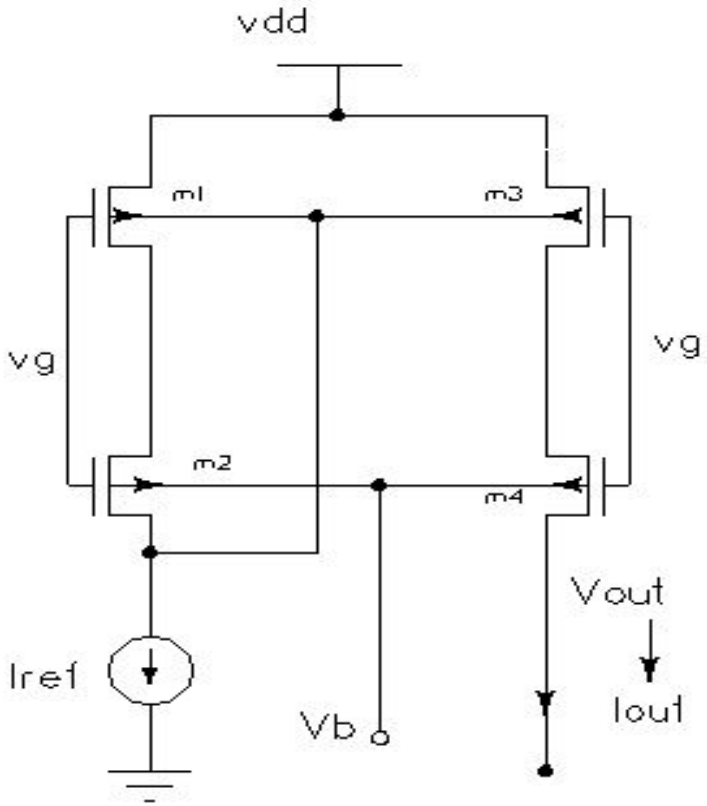
To design chips with smaller size, good performance, and less power consumption, for which the size of CMOS has to be decreases to very small features and dimensions due to which the allowable supply voltage is also decreases but the thing is that the threshold voltage is not decreases as the same rate as of supply voltage.

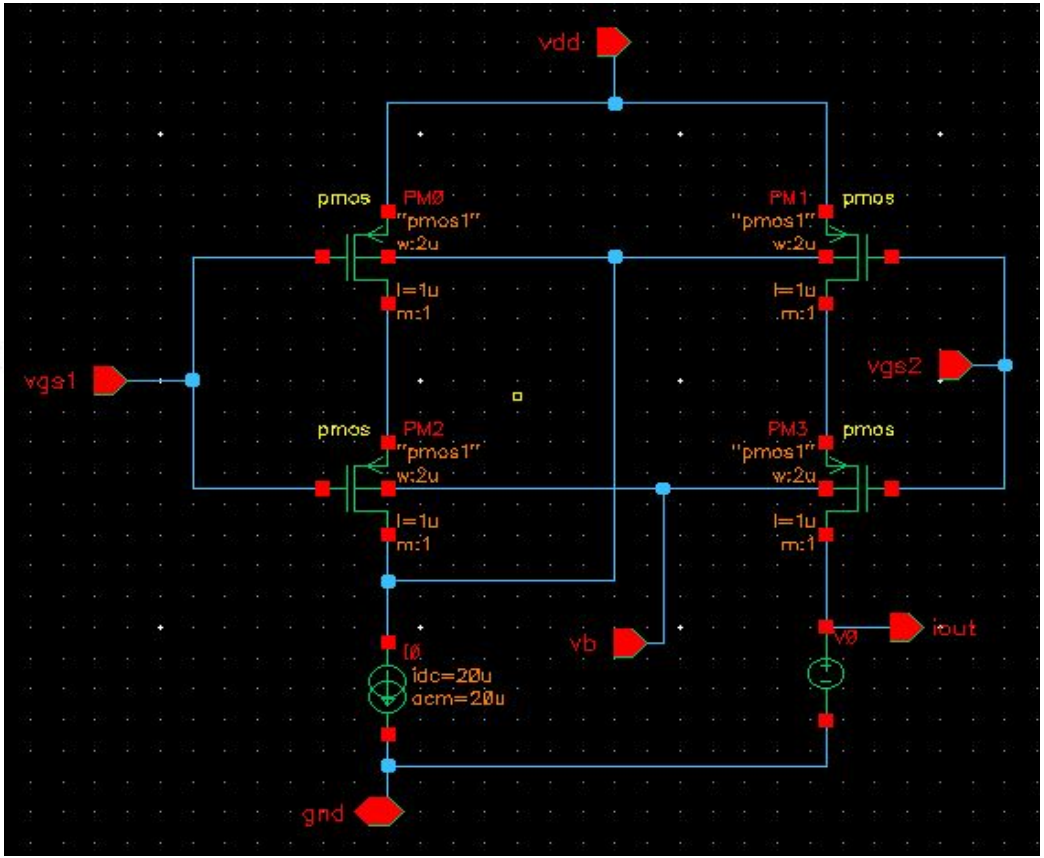
This problem can be potentially solved by Bulk driven technology

Here we are proposing Bulk Driven low voltage low power self biased current mirror (BDCCM)

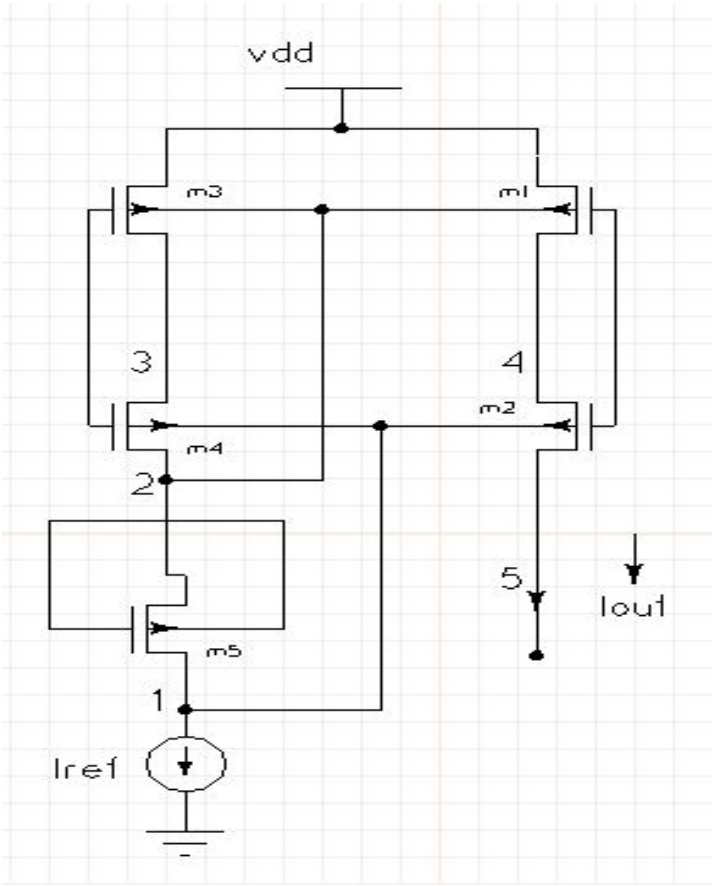
It can be operated at lower operating voltage.

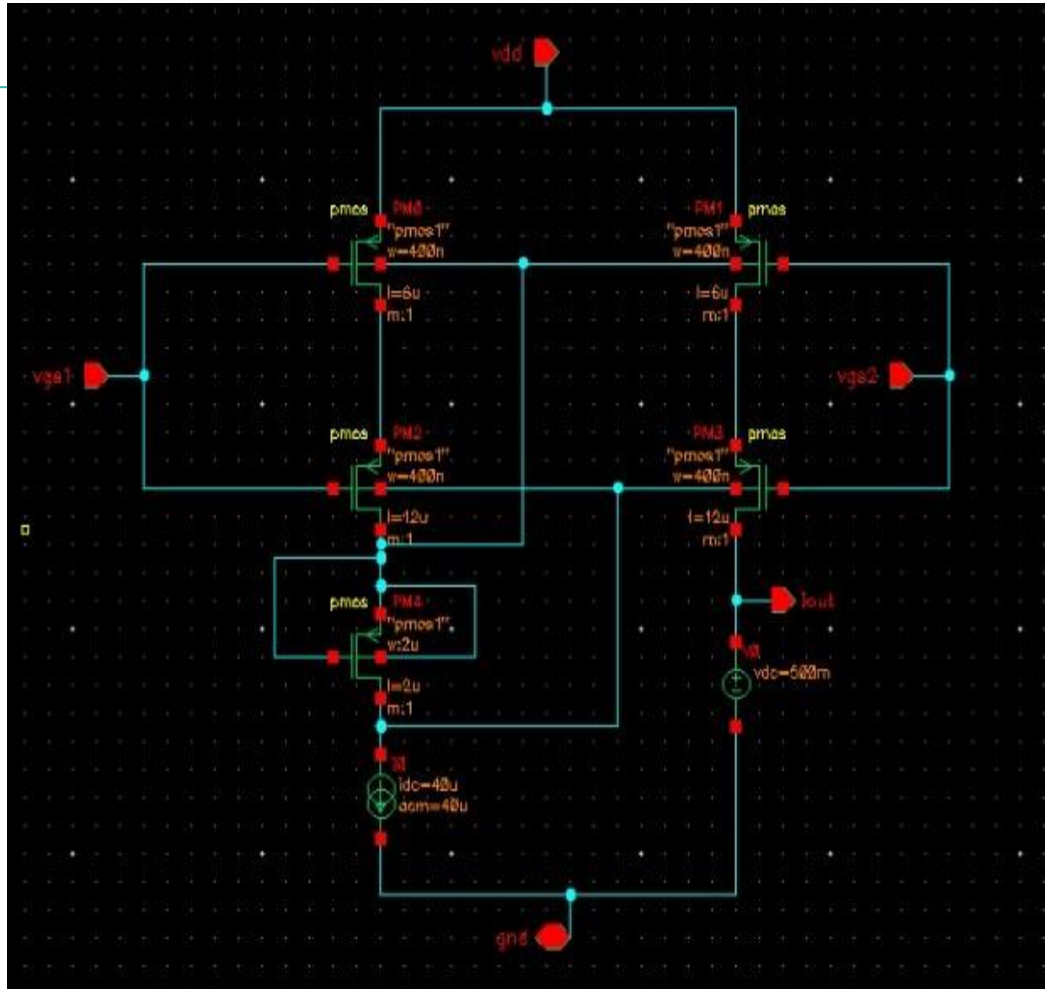
BDCM


vdd
m1
m3
vg
vg
m2
m4
Vout
Iref
Vb
Iout


vdd
pmos
PM0
"pmos1"
w:2u
l=1u
m:1
PM1
"pmos1"
w:2u
pmos
l=1u
m:1
vgs1
vgs2
pmos
PM2
"pmos1"
w:2u
l=1u
m:1
PM3
"pmos1"
w:2u
pmos
l=1u
m:1
I0
idc=20u
acm=20u
Vb
V0
Iout
gnd

Proposed BDCCM





Design specifications and operation

A constant voltage VG (the lowest potential of the circuits normally) is applied to the gate terminals which creates the inversion layer hence forms the conduction channel beneath the gate

The signals are applied at bulk-drain connections

The proposed PMOS BDCCM eliminates the limitation of threshold voltage

Operating voltage vdd=0.5 volt

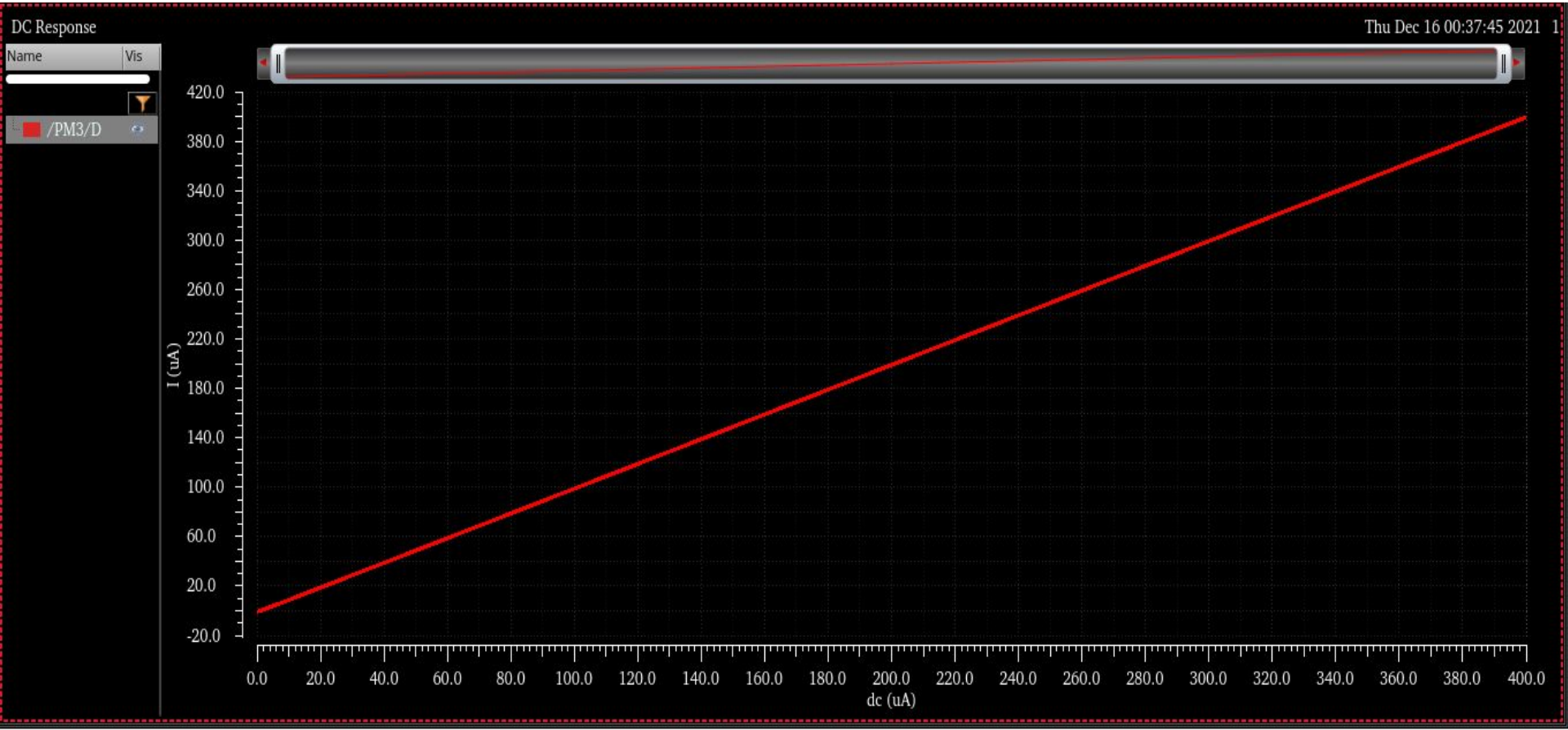
Self biased ckt, as no separate biasing is used

Power Consumption =24 mircoWatt

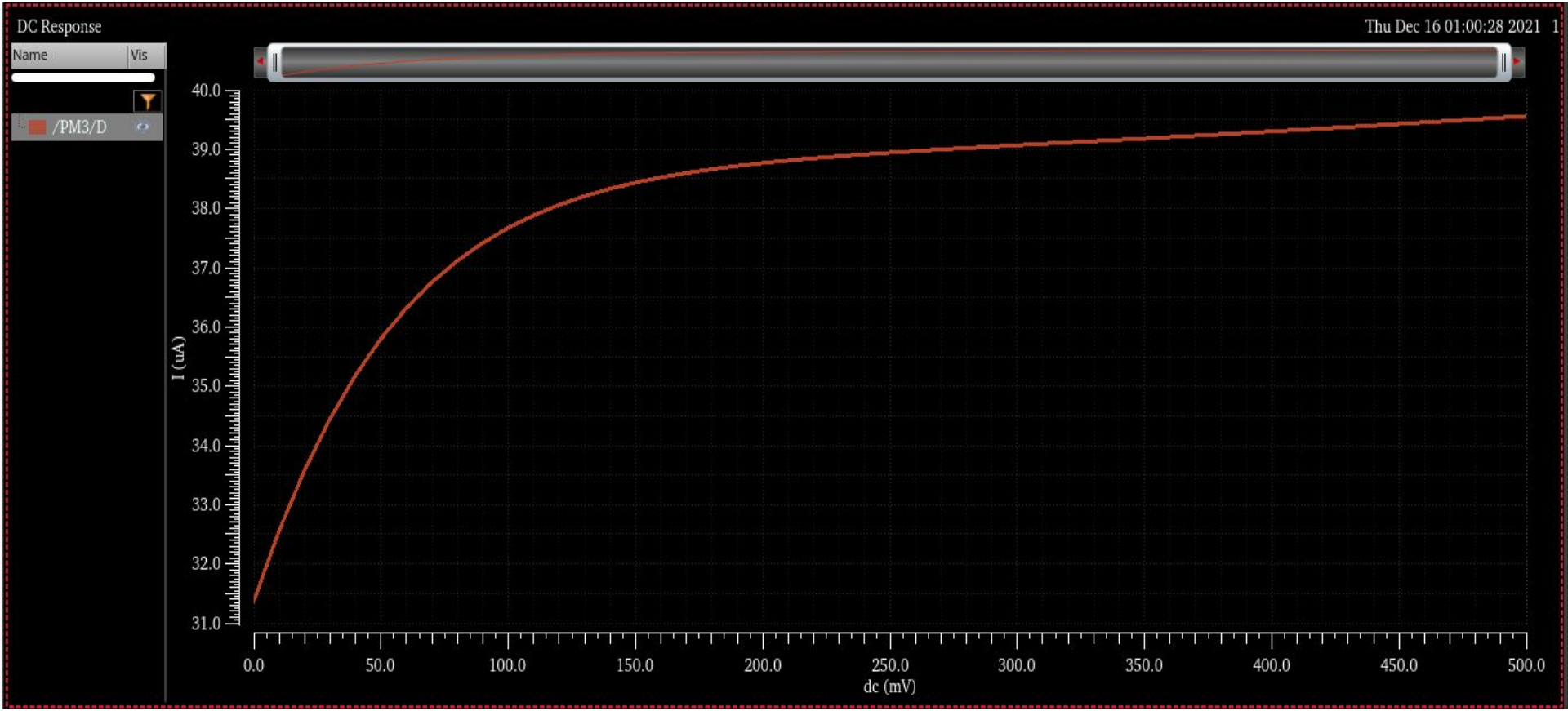
Technology : gpdk 180nm

Transistor	Aspect ratio
M1/M3	0.4/12
M2/M4	0.4/6
M5	2/2
vdd=0.5v	vss=-0.5v

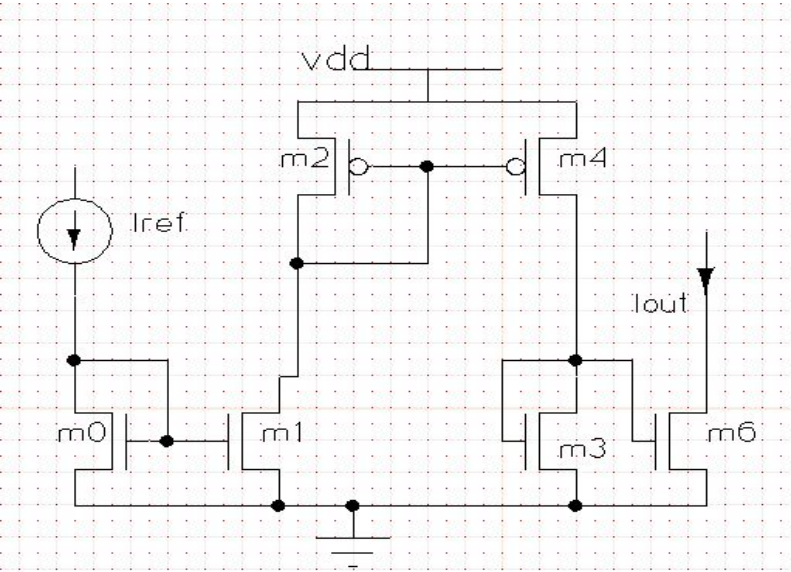
Linearity plot of BDCCM

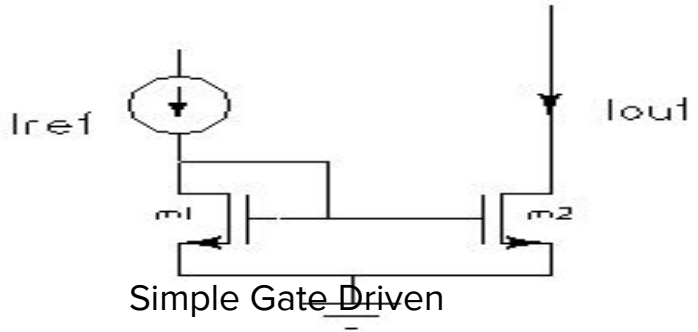


Iout vd Vout plot of BDCCM

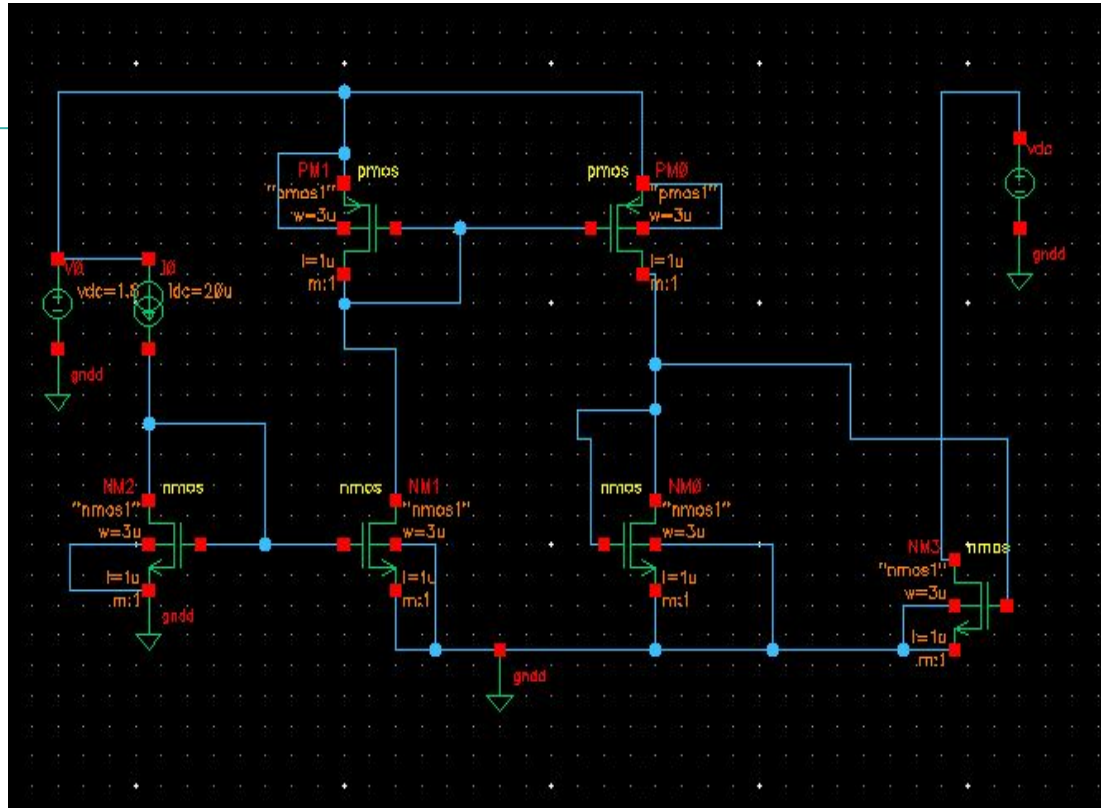


GDCM (Gate Driven)



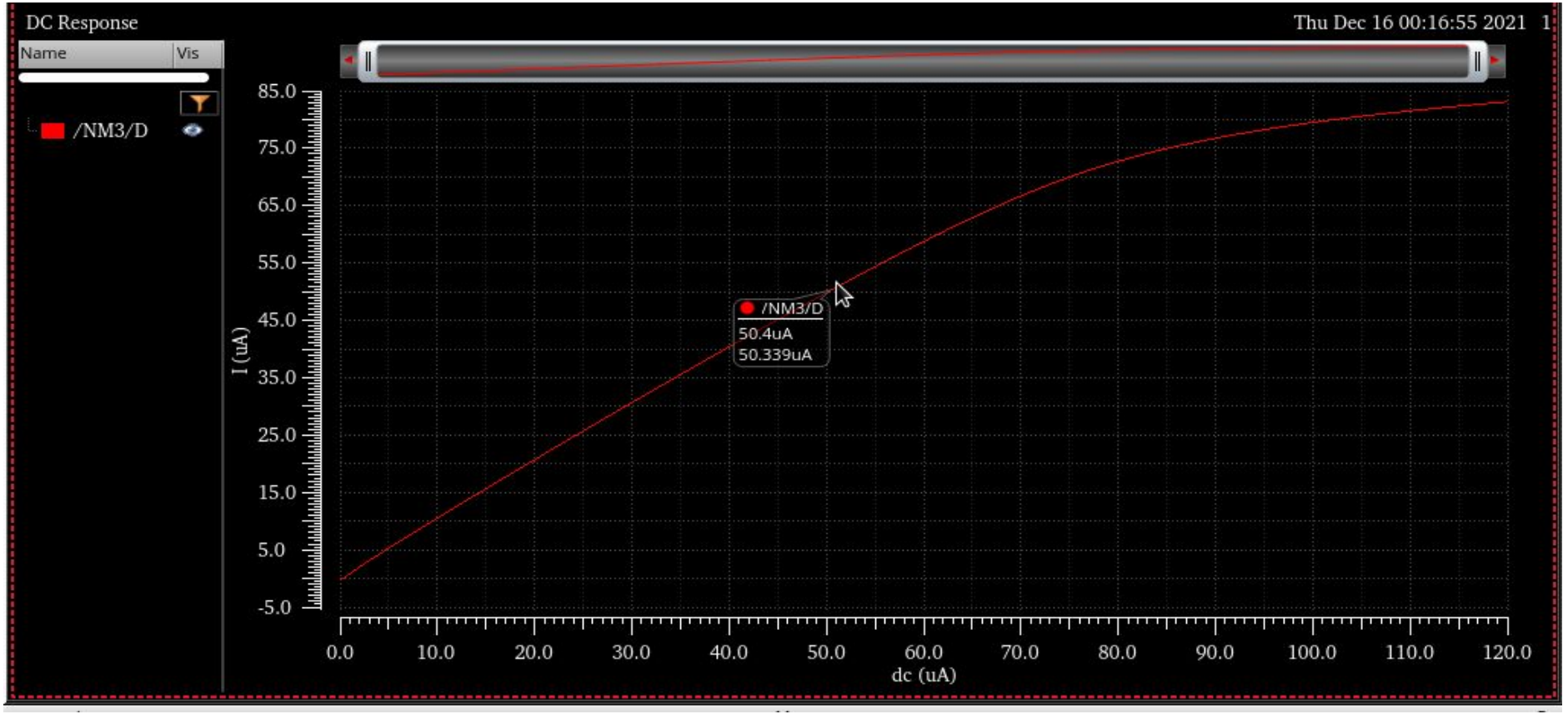


Simple Gate Driven

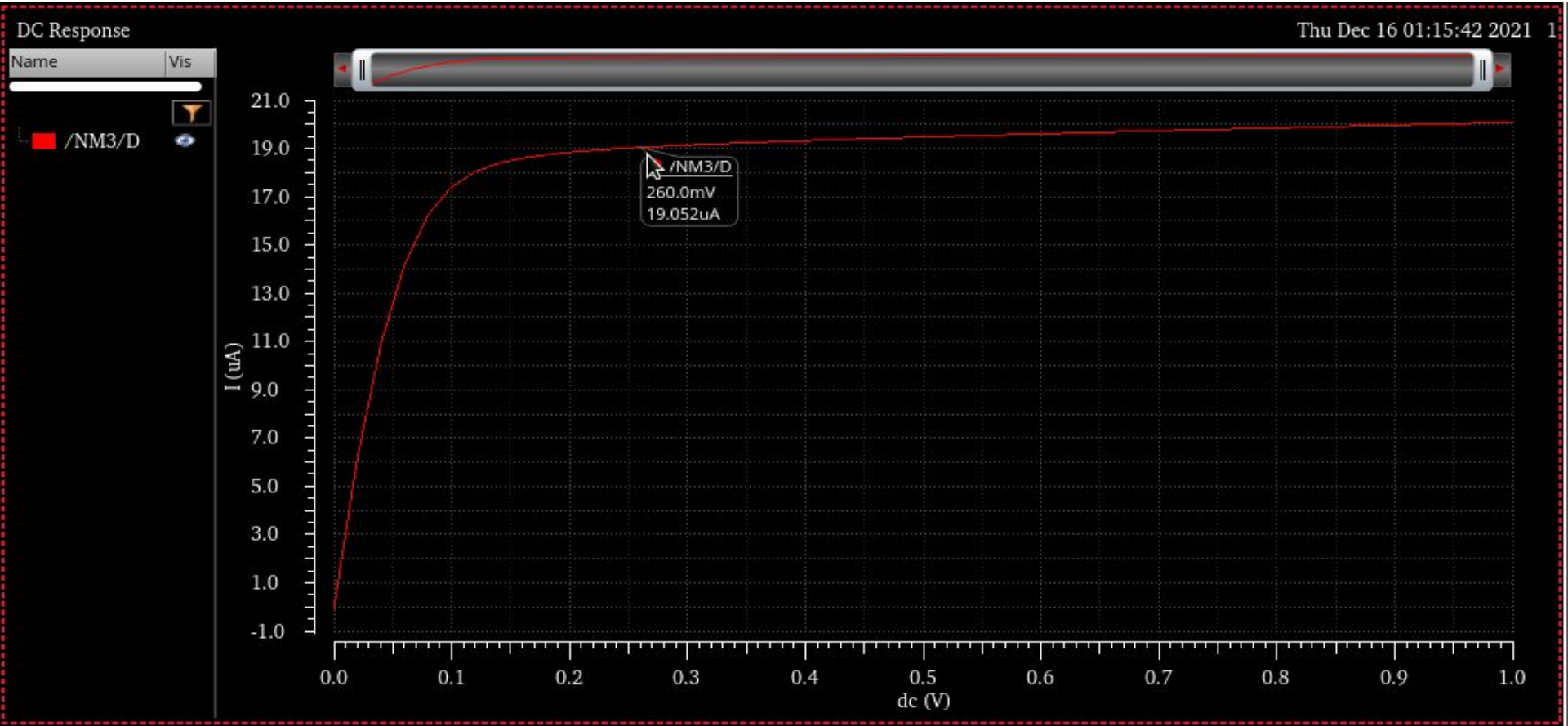


Gate Driven current Mirror
Vdd =1.8 volt
Power consumption=107 MicroWatt

Linearity plot of GDCM



Iout vs Vout plot of GDCM



Challenges

Few random errors are caused when there is a mismatch between the transistor parameters and are unavoidable in the design,It can be reduced in subsequently designing good layout.

Linearity and stability of output current is getting unstable when the design bias and sizes were not symmetric.By proper adjusting it taking care of sizes and bias it was removed.

Comparison table(BDCCM, GDCM and BDCM)

Circuit parameters	**Low Powered BDCCM**	**High Impedance GDCM**	**Low voltage BDCM**
Operating voltage	0.5V	1.8V	0.8V
Current linearity	Very High (Upto 400 uA)	Low (Upto 50 uA)	Low (Upto 100 uA)
DC transmission error	Low	High	Low
Power Dissipation	Low (approx 24 uW)	High (approx 107 uW)	—-
Output characteristics	No threshold limitation	Threshold limitation	No threshold limitation

References

1. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill.

2. Nitika Mahajan, “A Low-Voltage Low-Power Self Biased Bulk-Driven PMOS Cascode Current Mirror”.

3. Naresh Lakkamraju,Ashis Kumar Mal,”A Low Voltage High Output Impedance Bulk Driven Regulated Cascode Current Mirror”

4. Li Yani, Yang Yintang, and Zhu Zhangming “A Novel Low-voltage Low-power Bulk-driven Cascade Current Mirror” 3rd International Conference on Advanced Computer Theory and Engineering (ICACTE)-2010, vol. 3, pp. V3-78 - V3-83.

THANK YOU.