Strong Arm Sense Amplifier

Group Number: 22

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Group Members :

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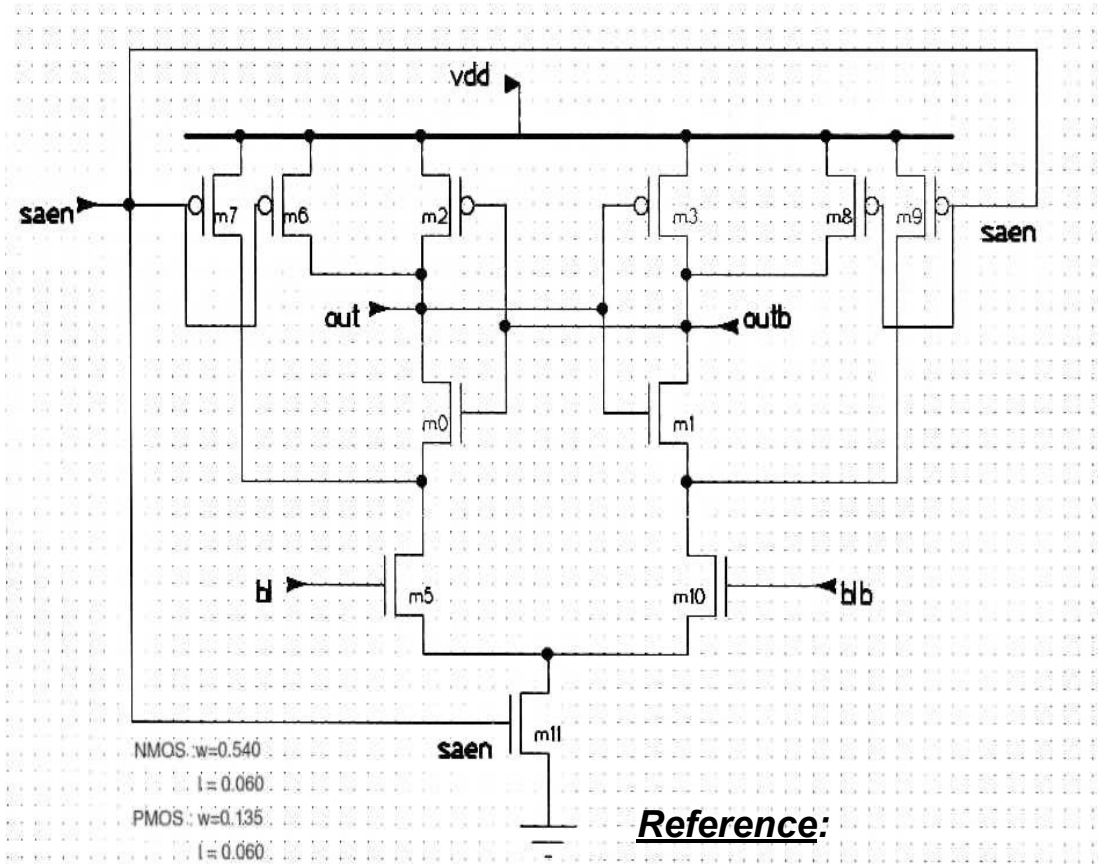
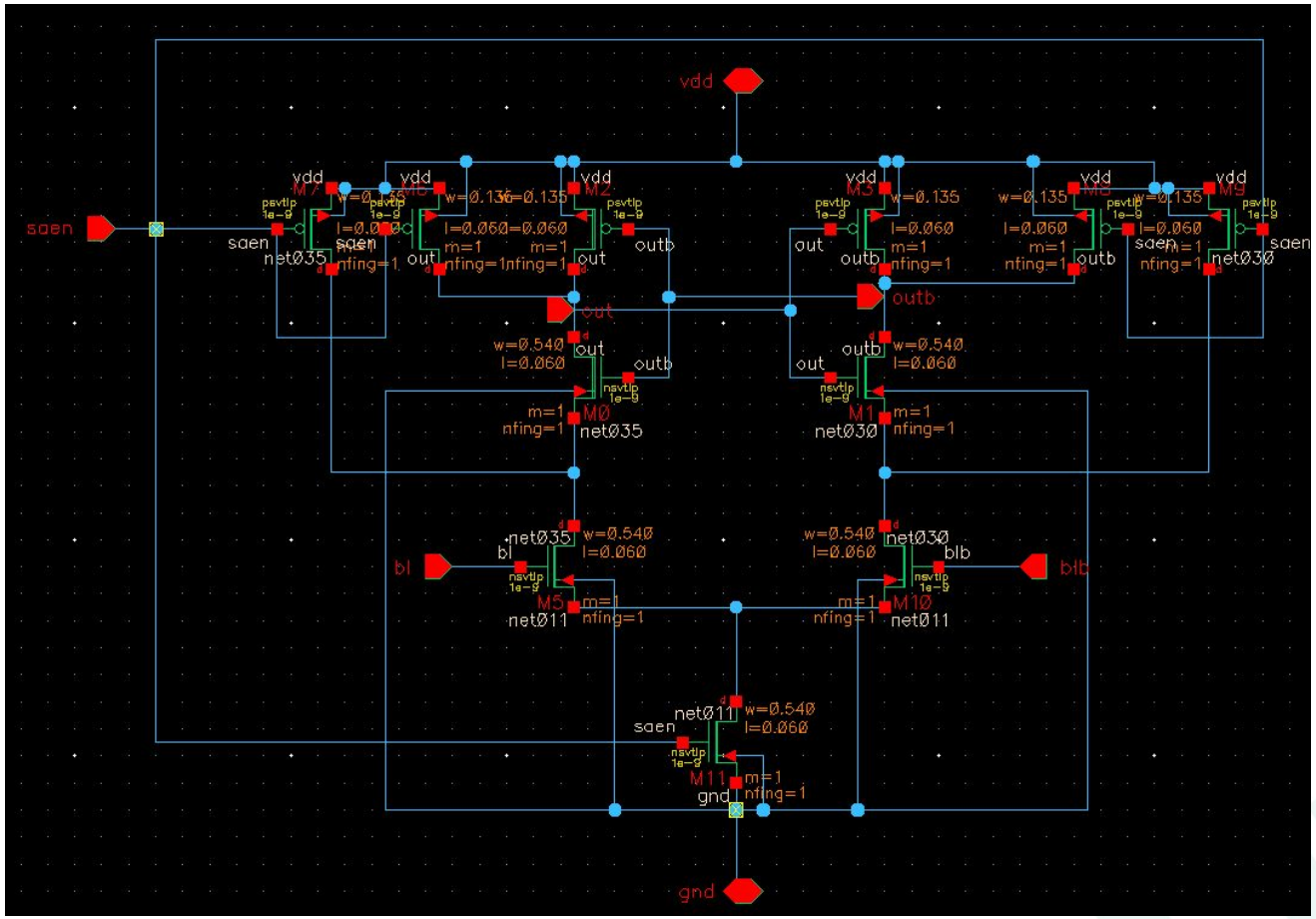
- Tarun – 21106
- Anushka – MT21187
- Sudhanshu – MT21212

Schematic + Sizing

NMOS : 0.54u/0.06u [Footer+Input+Latch]
PMOS : 0.135u/0.06u [Precharge+Latch]

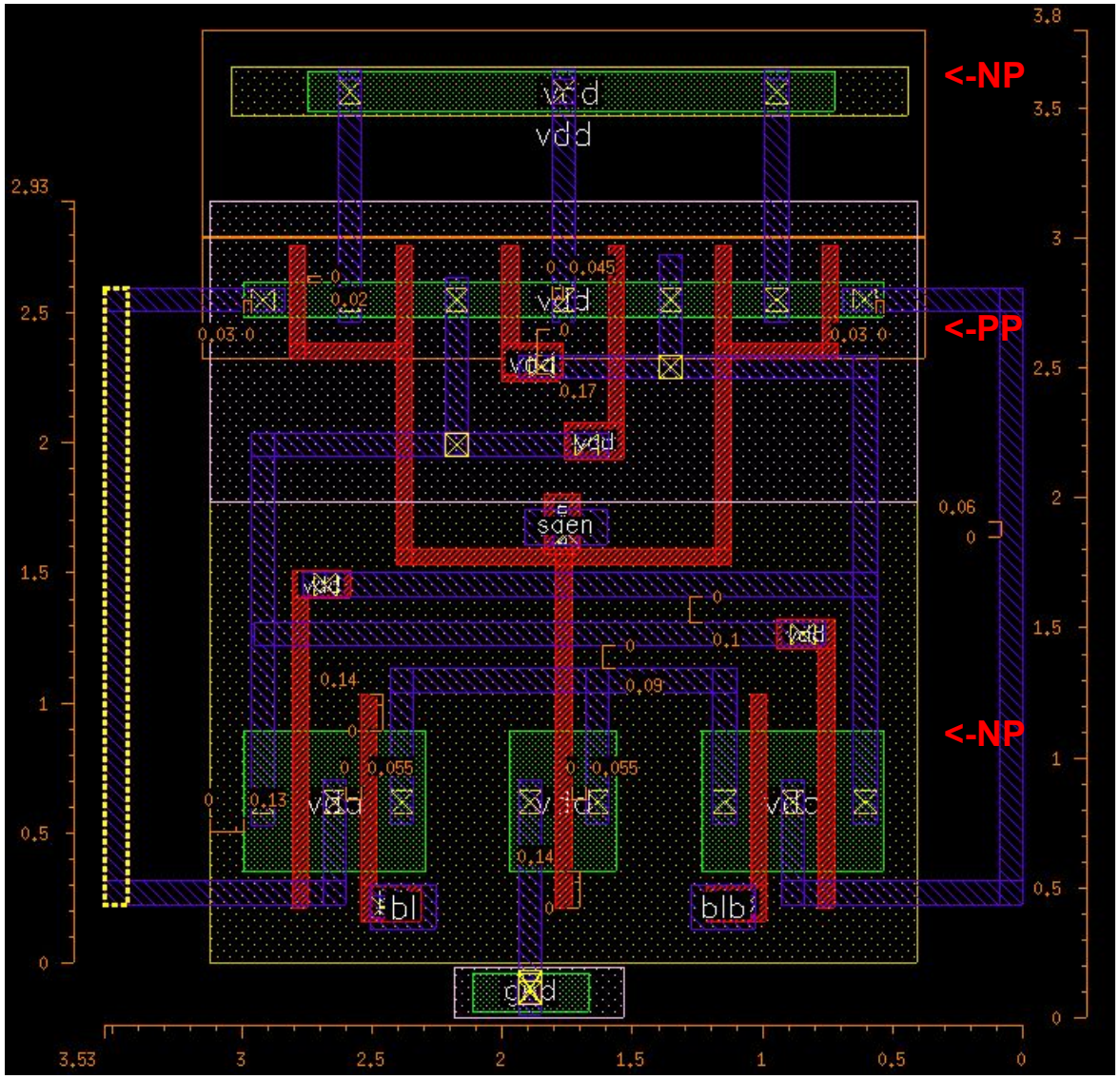


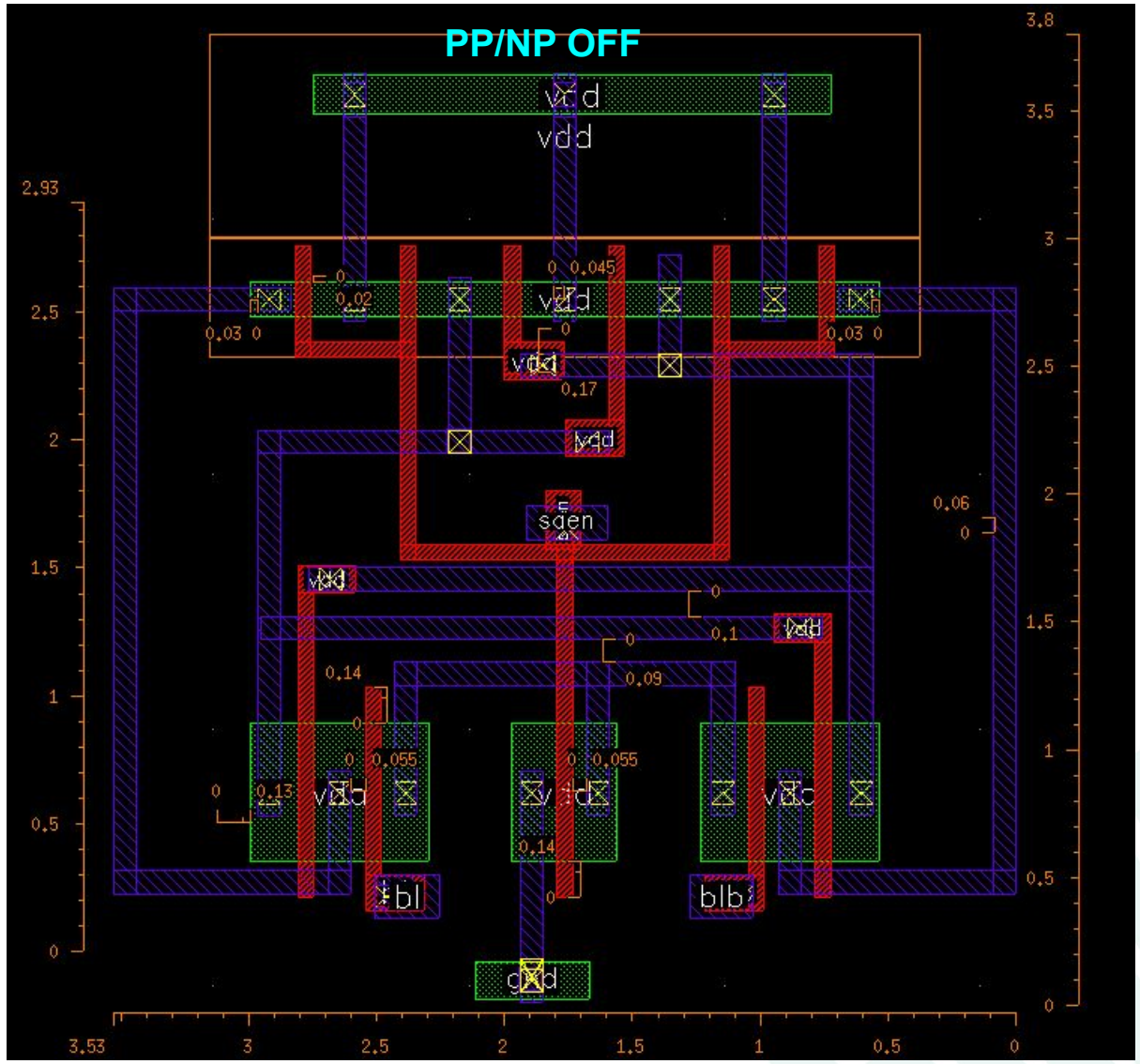


Reference:

https://www.seas.ucla.edu/brweb/papers/Journals/BR_Magzine4.pdf

Layout | Area = 3.8u X 3.53u = 13.414um2

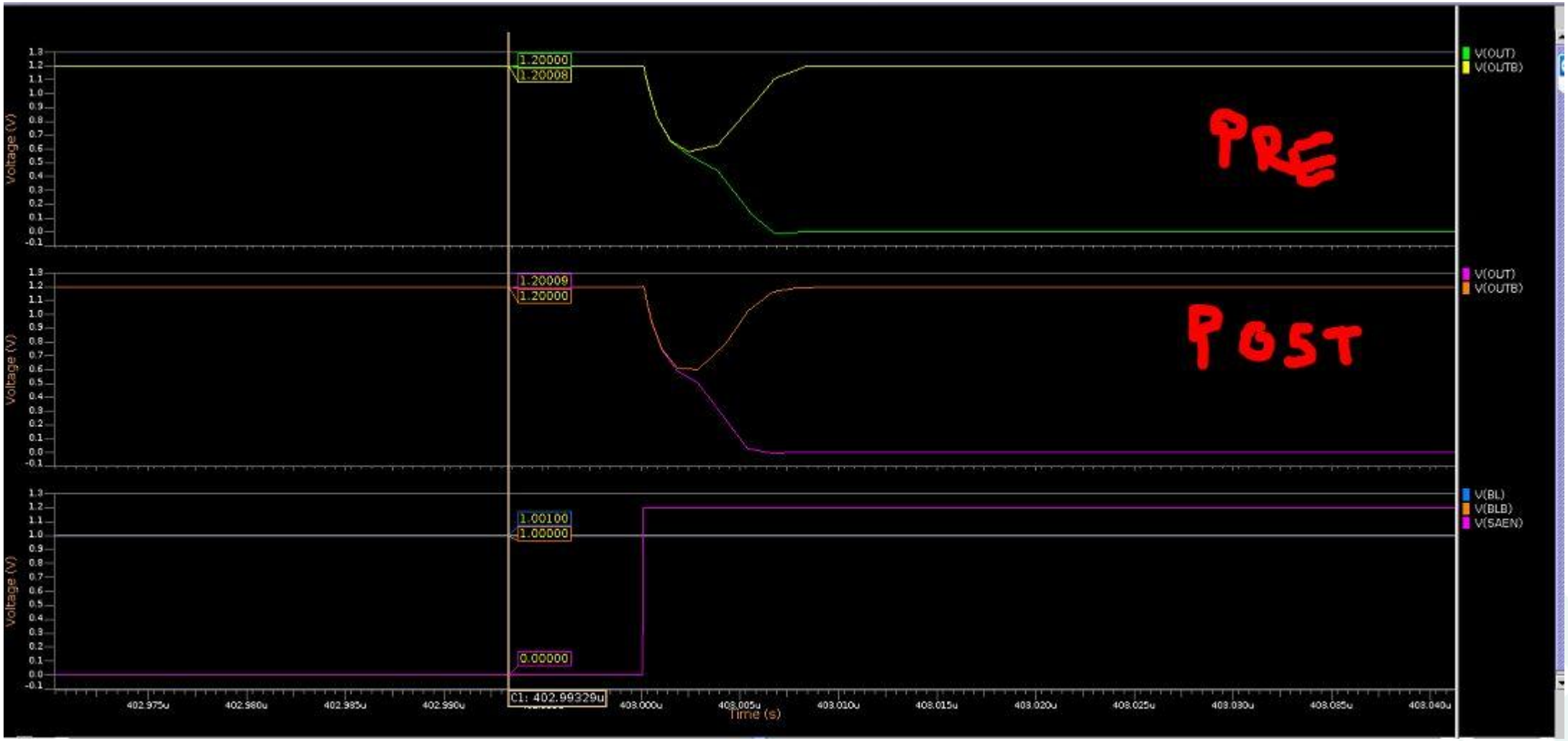




Simulation Waveform | Pre v/s Post

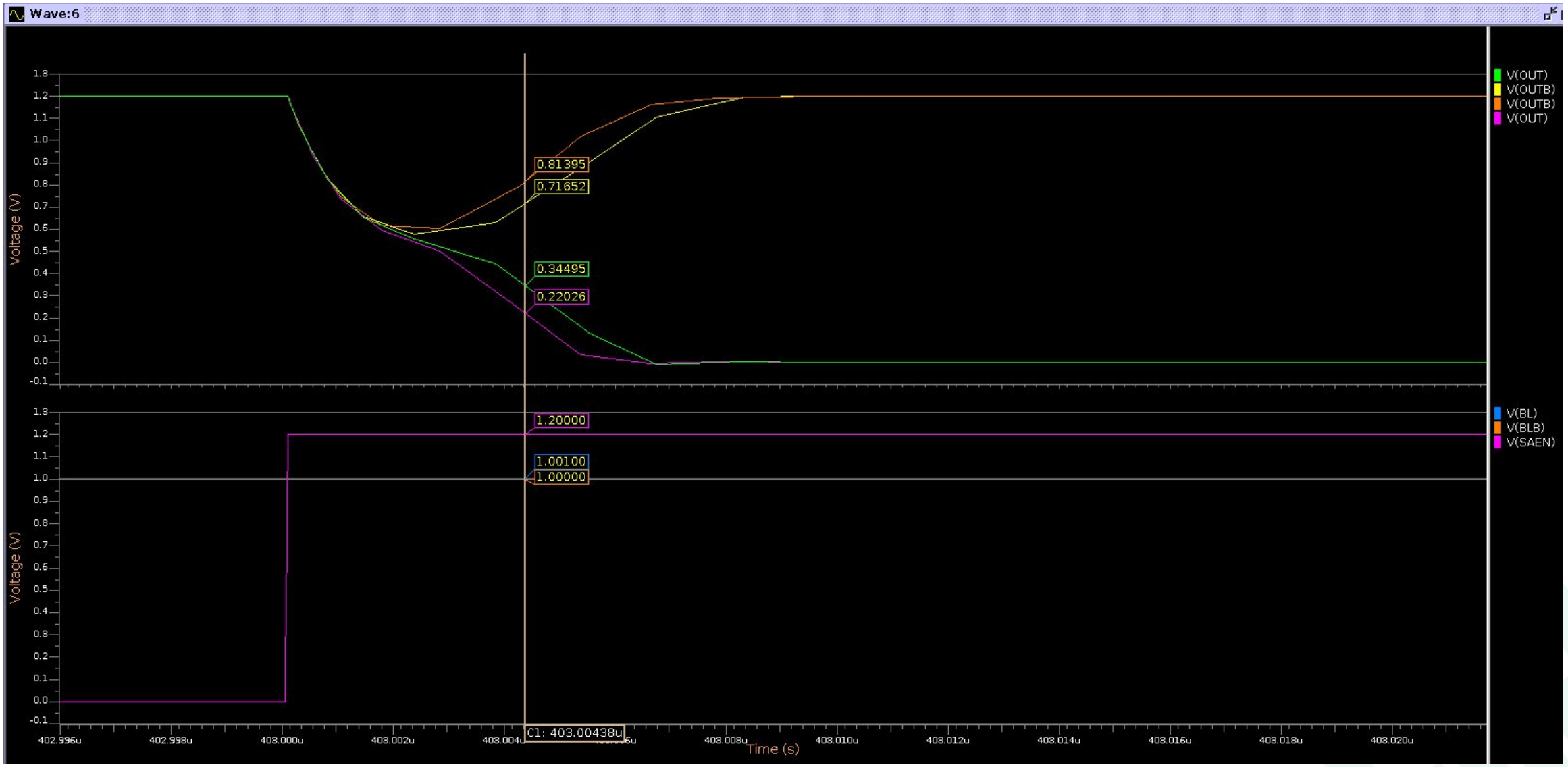
PVT : TT/1.2V/25C

Simulation Waveform | Pre v/s Post



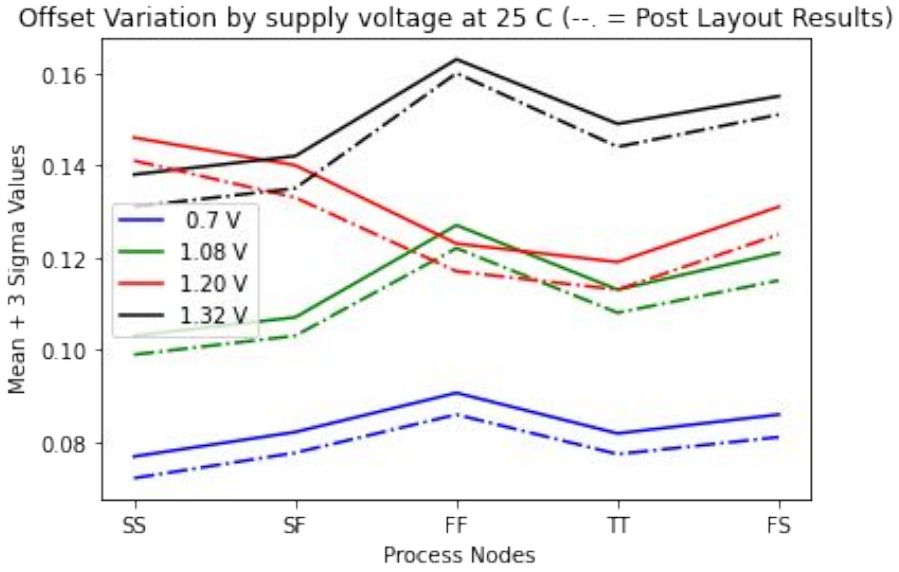
PVT : TT/1.2V/25C

Simulation Waveform | Pre v/s Post

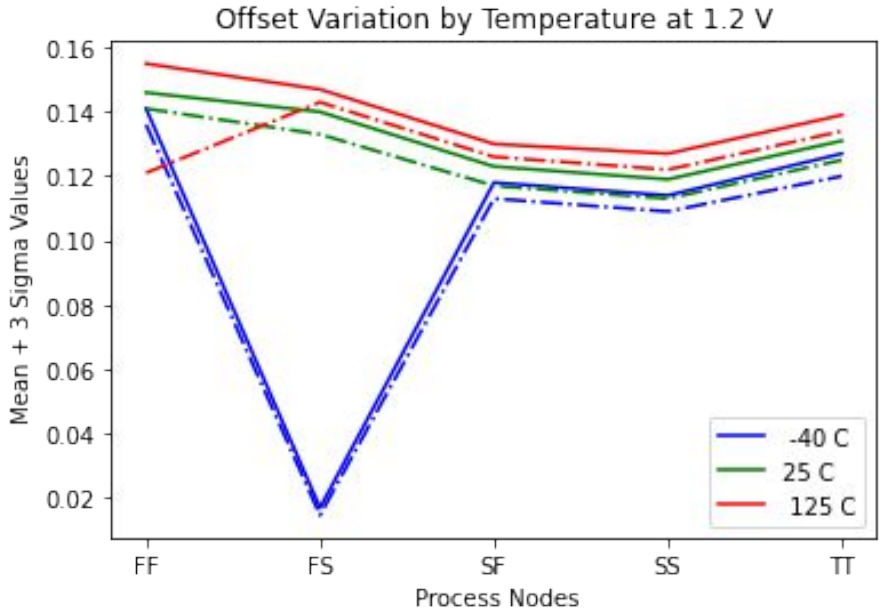


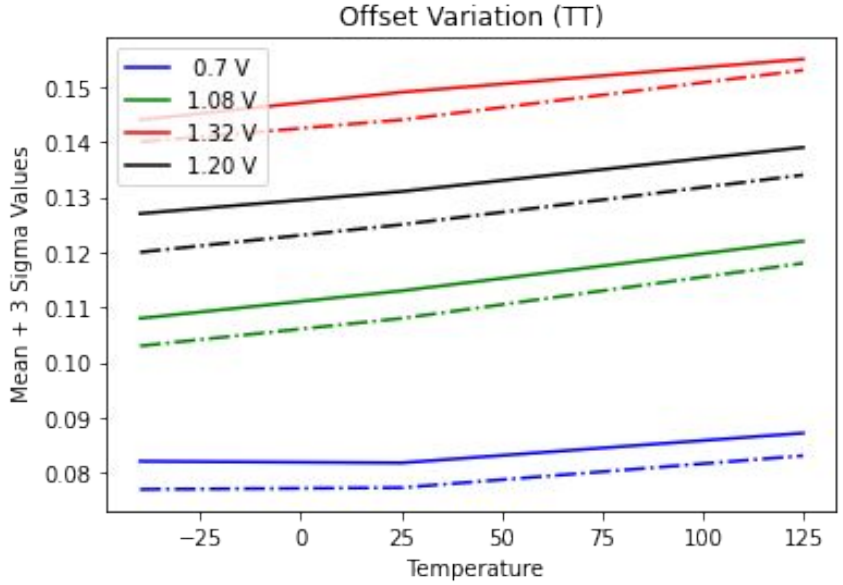
PVT : TT/1.2V/25C

Offset Analysis



—	**PreLayout**
–·–·	**PostLayout**





Offset Analysis

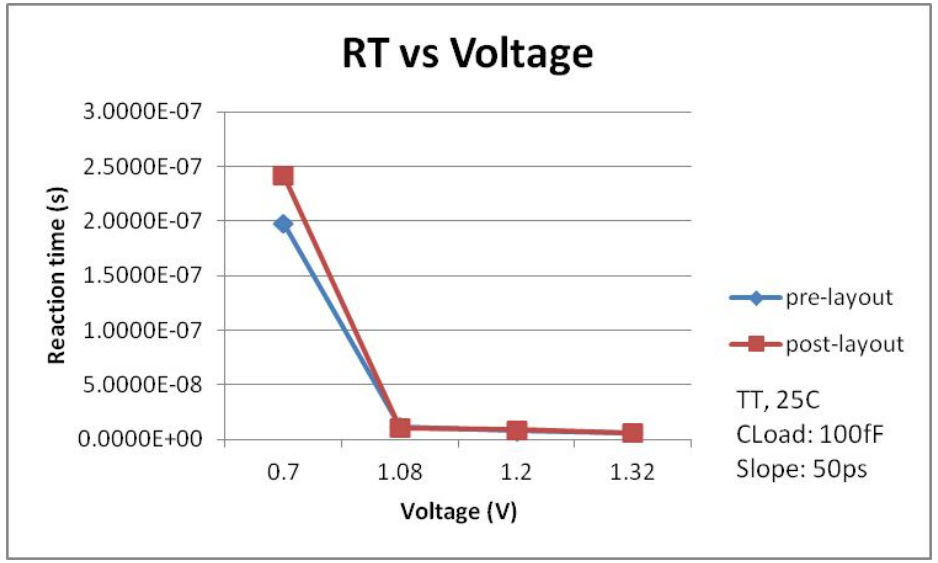
- Worst Case PVT: FF/1.32V/125C
  - Prelayout @ Worst Case = 167mV
  - Postlayout @ Worst Case = 169mV
- Best Case PVT: FS/1.2V/-40C
  - Prelayout @ Best Case = 17mV
  - Postlayout @ Best Case = 15mV

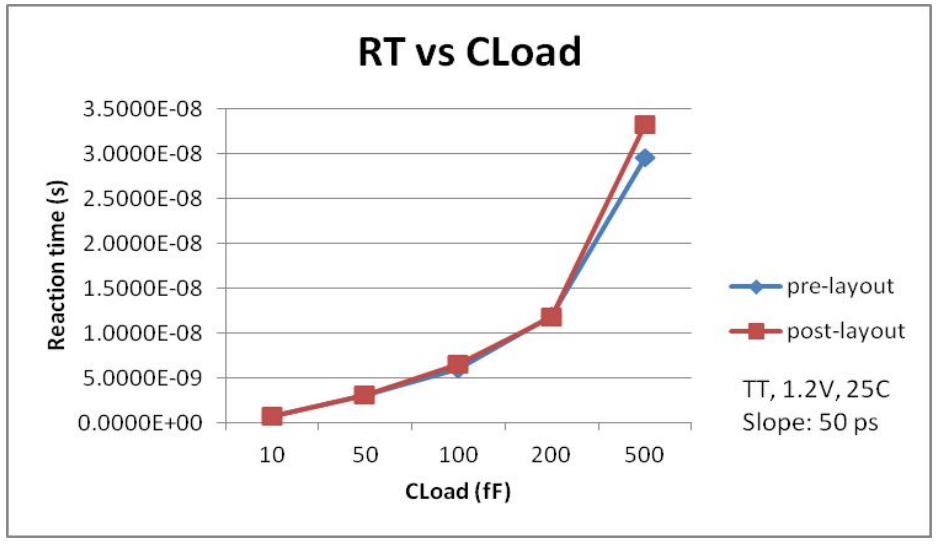
Reaction Time Analysis

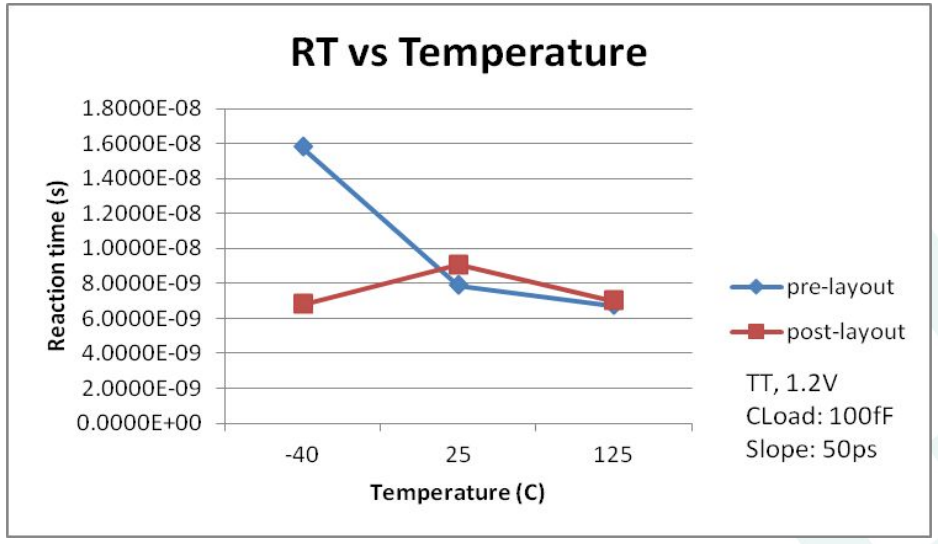
- Time V(OUT) takes to flip (i.e. drop to 10% of supply voltage) after the rising edge of SAEN(50% supply)
- Best and worst cases:

	Minimum RT	**Maximum RT**	**RT @TT,1.2V,25C**
Pre-layout	3.25ns @FF,1.32V,-40C	580ns @SS,0.7V,-40C	5.56ns
Post-layout	3.24ns @FF,1.32V,-40C	769ns @SS,0.7V,-40C	6.24ns

Reaction Time Analysis







Power Analysis

Parameter	Total Power (nW)		Leakage Power (nW)		Dynamic Power (nW)	
Worst PVT	FF/1.32V/25 C		FF/1.32V/25C		FF/1.32V/125C	
Worst PVT value	**PRE** 36.28	**POST** 36.6	**PRE** 34.15	**POST** 34.43	**PRE** 2.13	**POST** 2.2
Best PVT	SS/0.7V/-40 (FF and TT come very close)		TT/0.7V/-40 (SS close)		SS/1.32/-40	
Best PVT value	**PRE** 0.067	**POST** 0.07	**PRE** 0.004	**POST** 0.005	**PRE** 0.046	**POST** 0.05
Value at typical PVT (TT, 1.2, 25 C)	0.398	0.4	0.274	0.28	0.124	0.13

Sweep Analysis : Sizing

SS/0.7V/-40C							
Length= 0.06um							
Width_Footer (um)	Offset(m+3sd) (mV)	Width_Input (um)	Offset(m+3sd) (mV)	Width_Latch (um)	Offset(m+3sd) (mV)	Width_All (um)	Offset(m+3sd) (mV)
0.135	83	0.135	119	0.135	89	0.135	175.4
0.54	86	0.54	60	0.54	86	0.54	89.8
1.08	86	1.08	44	1.08	83	1.08	62.4

PPA & Characterisation

- **Area** = 13.414 um(2)
- **Performance** =
  - Offset follows expected trend only at **1.2V/25C**, i.e., very low value at **FF** and highest value at **SS**
  - Reaction Time follows expected trend also, lowest at FF/1.32V/-40C and highest at SS/0.7V/-40C
- **Power** = Maximum power occurs at FF/1.32V, **25C** for leak+avg & **125C** for dynamic
- **Characterizing design :**
  - PVT = TT/1.2V/25C with following Performance metrics:
    - Offset = 125mV(Post) & 131mV(Pre)
    - Reaction Time = 6.24ns(Post) & 5.56ns(Pre)
    - Avg. Power = 110.5nW(Post) & 99.7(pre)

Work Distribution

- Deepank = Setup + Offset Analysis + Sizing + Layout
- Tarun = Power Analysis + Stick Diagram + Layout
- Anushka = Timing Analysis + Sizing
- Sudhanshu = XCircuit + Power Analysis

Shortcomings & Future Scope:

- Length Should have been taken larger to reduce SD
- Common Centroid should be used to minimise systematic offset
- Output nodes must be connected to inverter instead of a capacitance
- Length of input NMOS should be larger than other NMOS to increase current and reduce effect of mismatches hence decreasing the offset.
- Investigating reason for unexpected trend and fixing it.
- Comparison with design without Stack PMOS instead NMOS used to balance internal node in precharge.