SUBTHRESHOLD LIBRARY DESIGN

by
Shubham Pandey, Neeraj, Abhishek Bidhan, Aakash Gupta, Nikhil Pratap Singh, Faisal Sheikh, Sudhanshu Trivedi, Aayushi Gupta, Harshit Somani, Prapti Makkar

Under the Supervision of
Dr. Anuj Grover

Indraprastha Institute of Information Technology Delhi
December, 2022

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Submitted
in partial fulfillment of the requirements for the degree of
Master of Technology

to

Indraprastha Institute of Information Technology Delhi
December, 2022

Certificate

This is to certify that the thesis titled "**Subthreshold Library Design**" being submitted by **Shubham Pandey, Neeraj, Abhishek Bidhan, Aakash Gupta, Nikhil Pratap Singh, Faisal Sheikh, Sudhanshu Trivedi, Aayushi Gupta, Harshit Somani, Prapti Makkar** to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original research work carried out by them under my supervision. In my opinion, the Capstone has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this Capstone have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

December, 2022

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Acknowledgements

We take this opportunity to express our profound gratitude and deep regards to the Department of Electronics and Communication Engineering at Indraprastha Institute of Information Technology, Delhi, for providing us with this outstanding curriculum in the Master's program. We gratefully acknowledge Professor Dr. Anuj Grover, Associate Professor, Indraprastha Institute of Information Technology - Delhi, for his cordial support, sound guidance, valuable information, monitoring, and encouragement throughout this project.

Abstract

A digital standard cell library has been conceptualized and implemented for 65nm technology. To make the library compatible with a conventional design flow, it has been designed and optimised for a 400 mV supply voltage. This voltage was selected since it is the norm. The isolated parasitic components from each cell were used to characterize the cell. Standard VT (NSVTLP) transistors were used in the development of combinatorial logic gates, which included sequential cells and compound logic gates. Using the library as a starting point, a completely functional Arm Cortex-M0 architecture was developed. The objective was to obtain quantitative data on the performance of the standard cell library in order to validate and assess the library's functionality as a whole.

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CHAPTER - 1
INTRODUCTION

Power consumption has been the most worrisome aspect of the current and impending nanoelectronics era. To meet the requirements for low power consumption, subthreshold functioning is being investigated as a potential solution. Due to the fact that the dynamic power consumption moves in a quadratic fashion while the static power shifts in an exponential fashion with the supply voltage, operating at a voltage that is less than the threshold voltage could result in significant energy savings. Despite the fact that this is the primary benefit of operating below the threshold, there are considerable performance downsides. Due to the fact that performance is not the primary focus of the process, this technique of design is often employed for applications that have restricted access to energy resources. Examples include radio frequency identification, also known as RFID, wireless sensor networks, and biomedical implants. When it comes to the development of digital circuits, "standard cell libraries" and their constituent pieces are the fundamental building blocks. When designing standard cells for this mode of operation, the most crucial thing to consider is the cells' resilience. During subthreshold operation, the cells are more susceptible to process fluctuations, temperature changes, and supply voltage variations. In the section that follows, the design process for an entire custom cell library employing the technique suggested will be detailed.[1]

In contrast to, which examines the issues posed by subthreshold designs in depth, the authors advocate using the reverse short-channel effect to maximize the size of the transistors. In contrast to the subthreshold methodology presented in this study, the authors of provide a subthreshold energy model for estimating the optimal supply voltage in order to minimize energy consumption. In this study, a subthreshold approach is proposed. To connect subthreshold components with above-threshold modules, you will require level shifters that are not only resource-efficient but also highly trustworthy. In the past, efforts have been made to create level changers that are both dependable and effective, as seen in. The notion of a zero-threshold MOSFET-based high-speed level shifter was introduced for the first time in. The pull-up transistor stack utilized in the level shifter proposed in is completely independent of the input voltage. In this case, power consumption is decreased without an increase or decrease in latency. The authors of offer a system for controlling the current over a short circuit as a potential solution to the delay. A level shifter is mentioned as a component of the planned subthreshold library in. This level shifter enables the implementation of systems with multiple voltage supplies.[2]

1.1 CMOS Technology on a Fundamental Level

CMOS-technology employs both N and P type transistors to perform logic operations. The abbreviation CMOS stands for complementary metal-oxide semiconductor. Presently, CMOS technology is largely used to build microprocessors, memory, and ASICs. The primary advantage of CMOS technology over NMOS and bipolar is its significantly lower power dissipation. CMOS circuits nearly never lose power because of static power dissipation, in contrast to NMOS and bipolar circuits. Only if the circuit actually flips will energy be lost. This allows for the integration of many more CMOS gates on an integrated circuit than is possible with NMOS or bipolar technology, resulting in a significant performance increase. The following applets illustrate N-type and P-type transistors, a CMOS inverter, NAND and NOR gates, and an AOI32 complex gate. The section closes with a demonstration of CMOS transmission gates and a D-latch transmission gate. Note that the conductivity of an N-type transistor occurs when its input is set to 1, whereas the conductivity of a P-type transistor occurs when its input is set to 0.[3]

1.2 CMOS INVERTER IS AT STAKE

The Complementary MOS inverter is the most important component of a CMOS gate set. It consists of just two transistors, one of the N-type and the other of the P-type. The applet provides a demonstration of the working of the inverter. The following examples explain the color code for each voltage level: Red represents the logical "1" and the electrical voltage VCC. The color blue indicates 0V or ground. Again, an orange wire indicates a floating wire that is not connected to VCC or GND. After some time, the voltage on such a wire can reach an indeterminate value between VCC and GND due to the effects of parasitic currents. There will be issues when the voltage of a floating wire reaches VCC/2.

When the gate voltage is close to VCC/2 for both N-type and P-type transistors, it indicates that the transistor is conducting. The applet explains the significance of this issue: When both transistors are conducting, there is a straight channel from VCC to GND. This state implies a short circuit, as depicted in light green on the diagram. This scenario results in severe energy loss and may cause the device to fail. If the input voltage is "1" (VCC), the P-type transistor on top is non-conducting and the N-type transistor is conducting, creating a path from GND to output Y. If the input voltage is zero, the top P-type transistor conducts, forming a path between GND and output Y. The output level is "0" given the current circumstances. If the input level is "0", however, the P-type transistor conducts and provides a channel from VCC to the output Y; thus, the output level is "1" and the N-type transistor is blocked. This results in the output level being 1 When the input is floating, it is conceivable for both transistors to be conducting, which can result in a short circuit.

1.3 POWER CONSUMPTION BY THE CMOS INVERTER

We reviewed the CMOS inverter in the last section, which explains why CMOS logic has (nearly) no static power dissipation: If the gate voltage is either 1 or 0, no static current flows through the inverter and there is no conducting path between VCC and GND. This is because there is no conducting path. During normal functioning, a short circuit, as represented in the preceding applet, will occur for the extremely brief duration corresponding to the switching of the gate voltage. When the input voltage is close to VCC/2, only a small percentage of the switching duration is occupied by static current dissipation. Moreover, the remaining fundamental CMOS gates lose virtually minimal static power.

CMOS gates, on the other hand, are known to have a dynamic current dissipation. This effect is evident in the following applet's CMOS inverter. A MOS transistor's gate is comparable to a small capacitor. This produces a very low current, which can be approximated using the formula I = dQ/dt = (Cg * VCC/) (t2-t1).[4]

In contrast, Itotal consumed by a large CMOS device, such as a microprocessor, can be quite high for the following reasons:

- A modern CPU may include approximately five million transistors, which is roughly equivalent to one million gates. During a single cycle, one percent of all gates will swap on average.
- The maximum frequency feasible with an operating voltage of VCC = 3.3V is 200 MHz with a cycle duration of 5 ns.
- In VLSI devices, the capacity of the gate-connecting wires, denoted by Cw, is significantly more than the capacity of the transistor gates, designated by Cg.The typical capacitance of wire-load is about 1 picoFarad.

It is challenging to obtain an accurate estimate of the total current produced by switching short-circuit currents. In this example, however, the current generated by altering the input capacitance is rather substantial.

However, in typical static CMOS integrated circuits, the quiescent current is typically quite modest. For example, a 2Kx8-bit CMOS SRAM requires only 1 uA of power while it is not in use.

The ensuing applet shows a graphical representation of the current loss of the CMOS inverter. If the input voltage remains at either 1 or 0, the inverter will not conduct any current. Either the N-type or P-type transistor will be nonconducting in this case.

- The gates are either replaced or discharged depending on the state of the input switch. To illustrate, the applet will display the motion of an electron.
- The input voltage traverses the region at VCC/2, which contains conducting regions for both transistors, if the input is switched. In other words, there is a brief period of direct current flow via the inverter following each switching operation. This is referred to as a short circuit. Another moving electron illustrates this current quite clearly.

1.4 SYNTHESIZED CELLS

Following are the cells which we have synthesized in our subthreshold library design. It consists of combinational cells and sequential cells. There are 14 basic gates, 14 complex gates, 4 clock cells and 4 sequential cells designed shown below:

COMBINATIONAL CELLS		SEQUENTIAL CELLS	CLOCK CELLS
BASIC GATES	COMPLEX GATES		
NAND2X4	AO212	DFFX1	CLKINVX1
NAND2X6	AO222		
NAND3X5	AO22		
AND2X4	AOI112		
AND3X9	AOI12	DFFX2	CLKINVX10
NOR2X6	AOI212		
NOR3X4	AOI222		
OR2X9	AOI222		
XOR2X6	OA22	DFFX4	CLKBUFX1
XNOR2X6	OAI12		
INVX9	OAI211		
INVX27	OAI212	DFFX8	CLKBUFX10
BFX9	OAI222		
BFX27	OAI22		

Table 1.1 : List of all designed cells

CHAPTER - 2
NEED OF SUBTHRESHOLD LIBRARY

In the middle of the design spectrum, where medium performance and medium power meet, many attempts have been made to find a balance between the different needs for power, space, and performance. But not much research has been done on the two extremes of design: high performance with power limits and acceptable performance with power from the outside. These are the two opposite ends of the design spectrum. Digital logic gates can be run in a region below the threshold to meet the criteria for ultra-low power consumption. We look into a group of CMOS logic devices that have a lower operating threshold than most.

In this field of work, finding ways to design things that use very little power takes priority over how well they work. One way to reach this goal is to run the digital circuitry in a subthreshold mode. One benefit of running the circuit in subthreshold mode is that the subthreshold leakage current can be used as the operational driving current. The subthreshold current goes up by a factor of 10 when the gate voltage goes up by a factor of 10. Because of this exponential relationship, it is expected that the amount of delay will keep getting worse and worse. The results of the simulation show that the drop in power consumption is bigger than the increase in delay. This means that switching energy consumption goes down overall. [5]

2.1 Why the Cmos Does It

Subthreshold logic is a type of logic that works when the voltage Vdd of the power source is less than the threshold voltage Vt of the transistors. This makes sure that the subthreshold zone is used by every single transistor. For our circuit modeling, we use technology with a 65nm process. When Vds is greater than 3kT/q in the area below the threshold, Ids is no longer dependent on Vds. This property has been used a lot in analogue design because it makes for a good source of current that works across the whole rail-to-rail voltage range. The people who make analogue designs have made the most of this trait. Digital circuit designers can use this property by connecting a lot of transistors in a row. This can be done by putting in more transistors. When compared to the drop in Vt that happens in a normal strong inversion zone, the drop in 3kT/q is almost nothing. Most sub-threshold applications use the static CMOS logic style because it is reliable. PseudoNMOS has also been suggested because some of the problems with using it in strong inversions are lessened when it is used in subthreshold situations. Pseudo-NMOS

circuits with a PMOS pull-up that is always on are less sensitive to changes in size but more sensitive to changes in the way they are made. Because of this, the pseudo-NMOS style of logic cannot work well with strong PMOS technologies. This is because the pull-up device may overwhelm the pull-down network, even if scaling is used to stop this from happening. To be more specific, the output low logic level (VOL) distribution may approach VDD. Because of this sensitivity, the number of strong-P processes that can use pseudo-NMOS logic is greatly reduced. Static CMOS logic is more resistant to different process conditions in terms of how it works than other types. As the process balance changes, though, the results of multiple measurements done on static CMOS will show a lot of change. Normal cells are made to work in an environment below the threshold, so this is very bad for them. The process will make the characteristics of representative cell collections very different from one another.

2.2 Possibility to do operations below the threshold

1. Cutting down on the amount of power used The equations for dynamic (Pdyn) and static (Pstat) power are 1 and 2, where an is the activity factor (in%), f is the operating frequency, C is the driving capacitance, Vdd is the supply voltage, and Iof is the leakage current of the circuit.
2. Cutting down on the amount of power used 1) When Vdd goes down, these two parts of power go down as well. For Pdyn, the rate of decline is quadratic. In terms of Pstat, the decrease is a straight line. Pdyn = a · f · C · Vdd 2 (1) Iif f Vdd = Pstat (2) The normal value of Vdd is 1.2 volts, and the technology node used in this study is 65 nanometers. Vt could be higher than 0.5 V depending on a number of factors, like the width or length of the transistor or random oscillations of the dopant. Vt varies for every single transistor. So, with a supply voltage of 0.4 V, the subthreshold can cut Pdyn by up to 15x and Pstat by up to 3.5x.
3. Making it possible to capture energy Most low-power applications now run on batteries, which must either be recharged or replaced when they run out. Because of how the subthreshold design works, the power budget decrease can help get around these problems by letting you go longer without charging or replacing the battery. On the other hand, a lower power budget can make it possible to make ultra-low-power devices that can run on their own and don't need a battery because they can collect energy. When thinking about applications like watches, the goal is to use less energy than the user can provide, and when thinking about wireless sensor networks, the goal is to use less energy than the environment can provide.

2.3 The operational obstacles confronting the subthreshold

1. The ion and Iof f disintegration: The ratio of Ion to Iof f governs the execution of the rise and fall transitions of the output of CMOS standard cells (where Ion is the active current and Iof f is the leakage current of the cell). Consider, for the sake of demonstration, a normal NAND cell with four inputs. During the fall transition of this cell's output, four PMOS transistor branches provide Iof of current, whereas only one NMOS transistor branch contributes Ion current (Figure 1). In this case, if the ratio of Ion to Ion f is low, the four PMOS branches may be stronger than the NMOS branch, but the output of the NAND will not be altered. Ion is decreased in a transistor operating in subthreshold mode and with a lower Vdd, which also improves the ratio of Ion/Iof f in the cell.

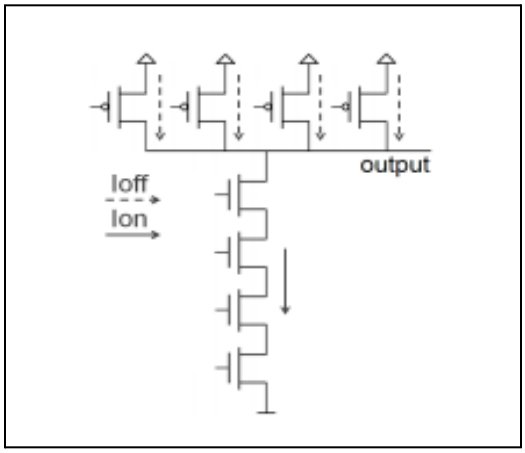


Figure 2.1 : 4 Input NAND gate

When constructing standard cells for subthreshold operation, particular care must be given to prevent Ion/Iof f ratio degradation, which can lead to cell failure. This is because a reduction in this ratio impairs the cell's ability to accomplish its function.

2. The deterioration of subthreshold circuit performance is an additional effect of the drop in the ratio of Ion to Iof f. It is probable that delays will increase by numerous orders of magnitude if attempts are made to reduce energy use. On the other hand, subthreshold designs are functional at greater voltages. By dynamically altering the voltage and frequency, several modes of operation (such as low-power and high-speed) are made possible (DVFS). Even while delays at higher voltages will not be as tiny as they are in circuits designed for super threshold operation, the supply voltage can be adjusted to improve performance as necessary. Increasing the parallelism of

designs at the architecture level is another strategy for enhancing the performance of subthreshold circuits.

3. Sensitivity to variations in Vt: In subthreshold operation, even minute variations in Vt – which can be caused by the size of the transistor, the amount of doping in the channel, the process, or fluctuations in temperature – can substantially affect the currents flowing through the transistors. This makes the ratio of Ion to Iof f and subthreshold circuits vulnerable to variations in Vt.

CHAPTER - 3
DESIGNING OF COMBINATIONAL CELLS

3.1 BASIC GATES

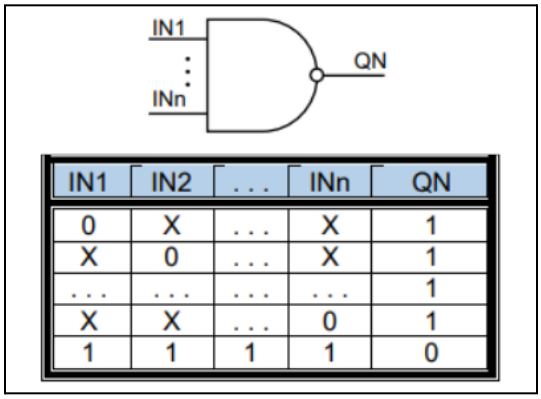
The primary combinational standard cells we made are mentioned below along with their frequency of operation.

BASIC GATES	FREQUENCY (MHz)
NAND2X4	1.55
NAND2X6	4.56
NAND3X5	1.58
AND2X4	2.43
AND3X9	1.66
NOR2X6	2.50
NOR3X4	0.416
OR2X9	2.702
XOR2X6	0.45454
XNOR2X6	2.155
INVX9	0.375
INVX27	10
BFX9	3.33
BFX27	11.11

Table 3.1 : List of basic gates designed along with their frequency of operation

3.1.1 SIZING AND DRIVE STRENGTH DESIGNING OF NAND GATE

Three different types of Nand gates are made with different numbers of inputs and drive strengths, that is NAND2X4, NAND2X6, NAND3X5.



IN1	IN2	. . .	INn	QN
0	X	. . .	X	1
X	0	. . .	X	1
. . .	. . .	. . .	. . .	1
X	X	. . .	0	1
1	1	1	1	0

Figure 3.1 : NAND gate with logic symbol and truth table[38]

NAND2X1, NAND2X4, NAND2X6, NAND3X1, NAND3X5 are developed.by changing the drive strength. The different strengths are obtained by changing the sizes of the transistors by multiplying the static current of the reference gate with the drive strength required. Reference gate is considered of unit strength and was obtained for the minimum sizing at which the rise and fall delays were almost equal.

2 INPUT NAND	Istatic	Drive Strength
NAND2X1	190.34nA	X1
NAND2X4	763.39nA	X4
NAND2X6	1.15uA	X6

Table 3.2 : 2 - input NAND gate with different strengths

3 INPUT NAND	Istatic	Drive Strength
NAND3X1	195.41nA	X1
NAND3X5	979.66nA	X5

Table 3.3 : 3 - input NAND gate with different strengths

To define the drive strength Istatic is measured accordingly by applying a 0.8*vdd supply to the output port and selecting the input combinations for rising and falling accordingly.

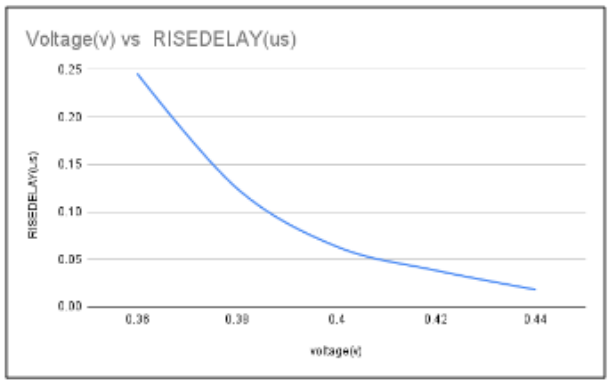
3.1.2 CHARACTERIZATION OF NAND GATE

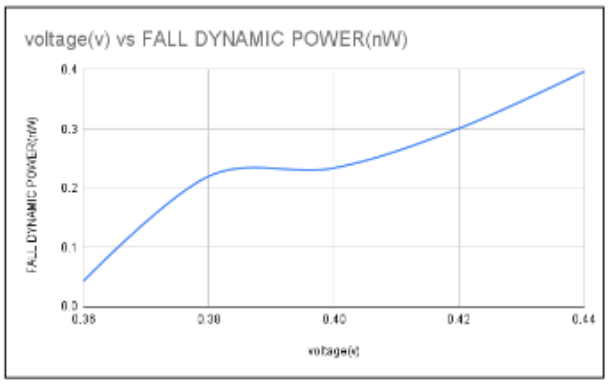
Worst Case Delays are shown below using worst case PVT condition *PVT SS,0.4V,-40°C.* Worst case delays for the NAND2X4,NAND2X6, NAND3X5 are shown at the worst case PVT and Input conditions.

BASIC GATE CELLS	RISE DELAY	FALL DELAY	RISE TRANSITION	FALL TRANSITION	RISE DYNAMIC POWER	FALL DYNAMIC POWER
NAND2X4	3.66E-07	7.64E-07	5.81E-07	9.91E-07	7.36E-09	1.80E-09
NAND2X6	1.02E-07	1.02E-07	1.85E-07	1.19E-07	1.03E-08	6.25E-08

Table 3.4 : Worst case delays and dynamic power of NAND gate with different strengths

The variations of the NAND2X4 parameters are observed with the operating voltages 0.4v, ±5% and ±10% which are shown below:





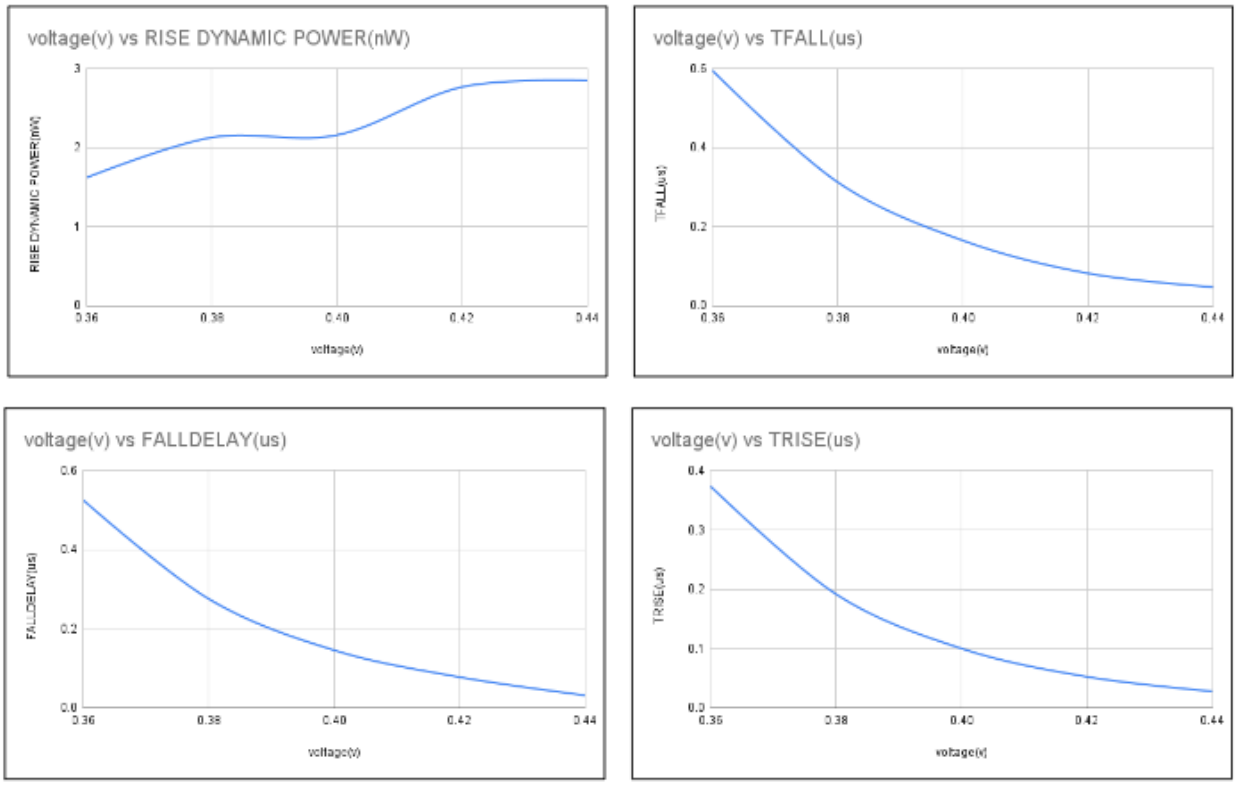


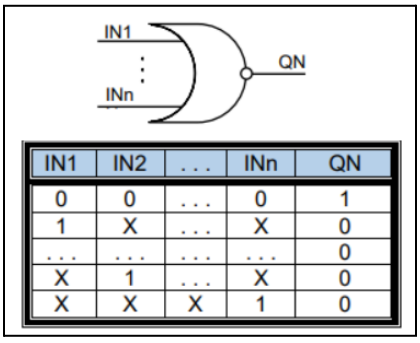
Figure 3.2 : Voltage vs Delays and Dynamic power variation of NAND gate

OBSERVATION:

As we can see from the above graphs the RISEDELAY, FALLDELAY, TRISE &TFALL are decreasing with the increase in the voltage and the RISE and FALL dynamic powers are increasing with the increase in supply as power quadratically depends on the voltage.

3.1.3 SIZING AND DRIVE STRENGTH DESIGNING OF NOR GATE

Two different types of Nor gates are made with different numbers of inputs and drive strengths, that is, NOR2X6, NOR3X4.



IN1	IN2	. . .	INn	QN
0	0	. . .	0	1
1	X	. . .	X	0
. . .	. . .	. . .	. . .	0
X	1	. . .	X	0
X	X	X	1	0

Figure 3.3 : NOR gate with logic symbol and truth table[38]

NOR2X1, NOR2X6, NOR3X1, NOR3X4 are designed.

2 INPUT NOR	Istatic	Drive Strength
NOR2X1	219.710nA	X1
NOR2X6	1.310uA	X6

Table 3.5 : 2 - input NOR gate with different strengths

3 INPUT NOR	Istatic	Drive Strength
NOR3X1	195.078nA	X1
NOR3X4	781.63nA	X4

Table 3.6 : 3 - input NOR gate with different strengths

To define the drive strength Istatic is measured accordingly by applying a 0.8*vdd supply to the output port and selecting the input combinations for RISE and FALL accordingly.

3.1.4 CHARACTERIZATION OF NOR GATE

Worst Case Delays are shown below using worst case PVT condition *PVT SS,0.4V,-40°C.* Worst case delays for the NAND2X4, NAND2X6, NAND3X5 are shown at the worst case PVT and Input combinations.

Cell	RISE DELAY	FALL DELAY	RISE TRANSITION	FALL TRANSITION	RISE DYNAMIC POWER	FALL DYNAMIC POWER
NOR2X6	1.20E-06	6.59E-07	8.53E-07	5.39E-07	2.60E-09	2.65E-09

Table 3.7 : Worst case delays and dynamic power of NOR gate

The variations of the NOR2X6 parameters with the operating voltages **0.4v, ±5% and ±10%** are shown below:

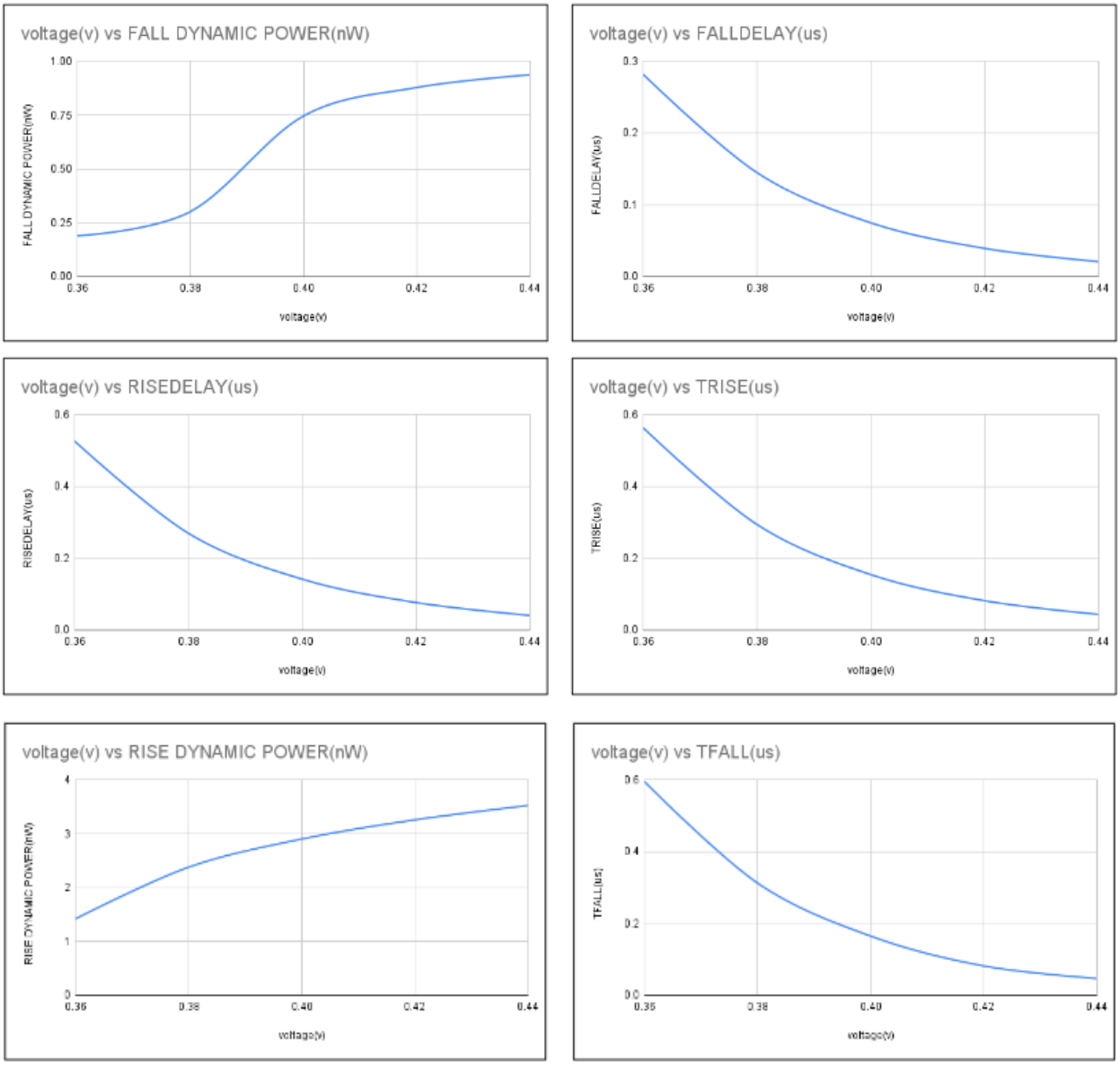


Figure 3.4 : Voltage vs Delays and Dynamic power variation of NOR gate

OBSERVATION:

As we can see from the above graphs the RISEDELAY, FALLDELAY, TRISE & TFALL are decreasing with the increase in the voltage and the RISE and FALL dynamic powers are increasing with the increase in supply as power quadratically depends on the voltage

3.1.5 APPLICATION AREAS

Subthreshold digital circuits will only be practical for applications that do not require a high level of performance but do require low power consumption. This application includes hearing aids, pacemakers, wristwatches with computing capability, and self-powered devices. Subthreshold circuits can also be applied to applications with bursty characteristics and long periods of inactivity. During the subthreshold portion of the idle time T, the original active period T in the critical inversion area (top off) is lengthened (bottom half). In both cases, the same number of operations are performed, but the subthreshold process consumes considerably less energy.

3.2 COMPLEX GATES

The complex combinational standard cells we made are mentioned below along with their frequency of operation.

Cell	Frequency(MHz)
AO212X4	0.44
AO222X4	0.35
AO22X9	1.46
AOI112X4	0.52
AOI12X6	0,66
AOI212X4	0.397
AOI222X4	0.335
AOI22X6	0.456
OA22X4	0.412
OAI12X5	0.56
OAI211X5	0.66
OAI212X5	0.375
OAI222X5	0.69
OAI22X6	0.85

Table 3.8 : List of complex gates designed along with their frequency of operation

3.2.1 INTRODUCTION

Similar to NMOS technology, CMOS gates are capable of effectively accomplishing specific logic tasks. Despite the fact that the gates themselves are uncomplicated, they are regarded as complicated gates since they implement a complex logic function. Combinations of AND-OR-INVERT and OR-AND-INVERT gates are a common example of complex gates found in virtually every cell library. The gate for the logic function Y =!((A B) | (C D E)), which represents the NOT of the OR of two ANDs, is a typical example of an AOI32 gate. This gate is illustrated in the following applet. It simply requires 10 transistors (5 pairs of N-type and P-type transistors, one pair for each input). In order to simplify the circuit schematic, the complete input wires are not depicted. All input lines are instead split in half and linked to their respective N-type and P-type transistors. To toggle the input voltage for input A, for example, you can click either the N-type or P-type gate associated with input A's transistor. Notably, N-type and P-type routes in this gate are once again complementary. Connecting transistors of type P in series is equivalent to connecting transistors of type N in parallel, and vice versa.

The generalization to further complicated gates should be simple. Again, gates with more than three transistors connected in series are not used. The majority of cell library gates range between AOI21 and OAI21 and aOI33 and OAI33. AND-OR-Invert (AOI) and OR-AND-Invert (OAI) are often employed in circuit design due to the fact that their fabrication using MOSFETs is simpler and more efficient than the sum of the individual gates. In CMOS circuits, it is simple to design AOI and OAI gates. AOI gates offer the advantage of requiring fewer transistors (or gates) than independent implementations of AND, NOT, and OR. This results in an increase in speed, a drop in power, a decrease in area, and perhaps a reduction in fabrication costs.[1]

3.2.2 A0I (AND-OR-INVERTER) Cell

The A0I (AND-OR-INVERTER) is also referred to as the AND-OR Inverter. AND-OR-Invert (A0I) logic or say gates are two-level logic functions composed of one or more AND gates and a NOR gate. Individual construction of AND, OR, and NOT gates reduces the number of transistors in A0I gates. A two-level complex logic cell consisting of one or more AND gates and a NOR gate, the AND-OR-Invert (AOI) gate is also known as the AND-OR-Invert (NOR) gate. The companion to the OR-AND-Invert Gate is the AOI gate.

$$Q=\text{invert}((A \wedge B) \vee (C \wedge D))$$

Despite the fact that there is no official symbol for AND-OR-Invert gates, the following symbol is commonly used to represent them.

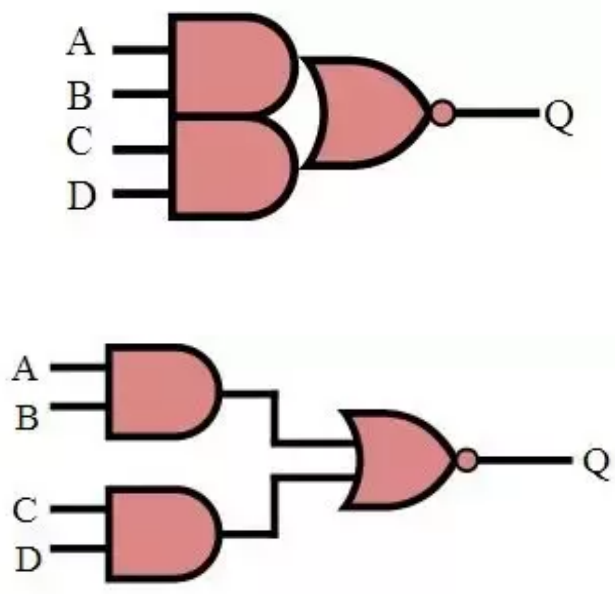


Figure 3.5 : And Or Invert (AOI)[38]

AND-OR-Invert gates are essential in CMOS logic because, despite their behavior, they can execute two levels of logic with a single level of transistors.

3.2.3 OAI (OR-AND-INVERTER) Cell

OAI is occasionally known as OR-AND Inverter. OR-AND-Invert (OAI) logic or say gates are constructed by combining one or more NAND gates with an OR gate. By constructing AND, OR, and NOT gates separately, the number of transistors in OAI gates is minimized.

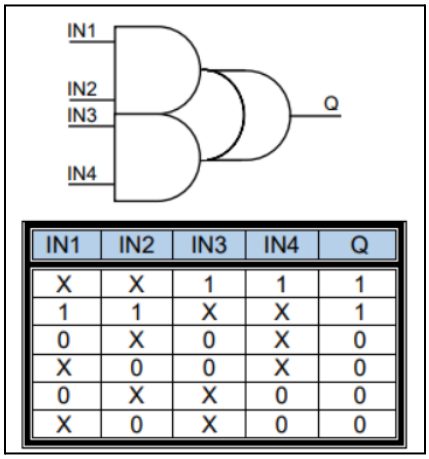
The OR-AND-Invert (OAI) gate is a two-level complex logic cell consisting of one or more NAND gates and an OR gate. The OAI Gate complements the AND-OR-Invert Gate.

$$Q=\text{invert}((A \vee B) \wedge (C \vee D))$$

The primary gate standard cells we made are mentioned below along with their frequency of operation.[1]

3.2.4 CHARACTERIZATION OF AO22 GATE

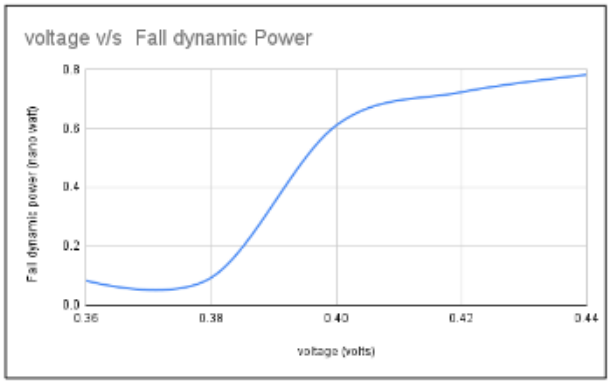
Generalized Symbol for AO22 complex gate along with truth table is shown below:

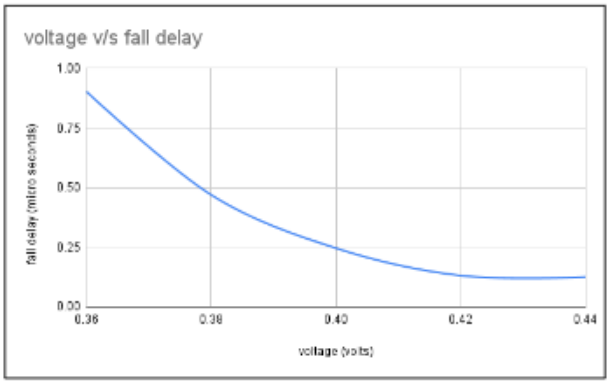


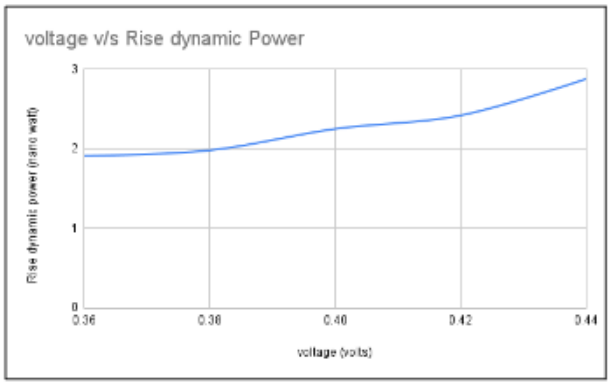
IN1	IN2	IN3	IN4	Q
X	X	1	1	1
1	1	X	X	1
0	X	0	X	0
X	0	0	X	0
0	X	X	0	0
X	0	X	0	0

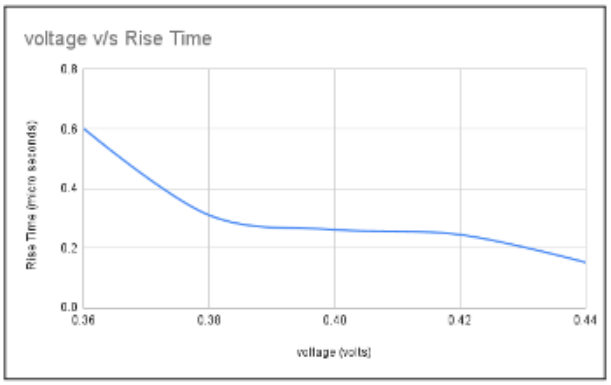
Figure 3.6 : AO22 gate with logic symbol and truth table[38]

The variations of the AO22X4 parameters with the operating voltages **0.4v, ±5% and ±10%** are shown below









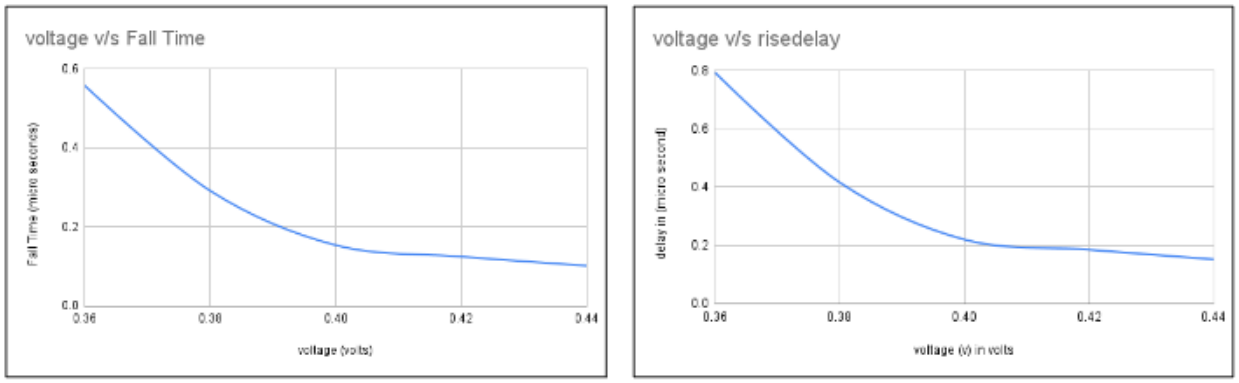


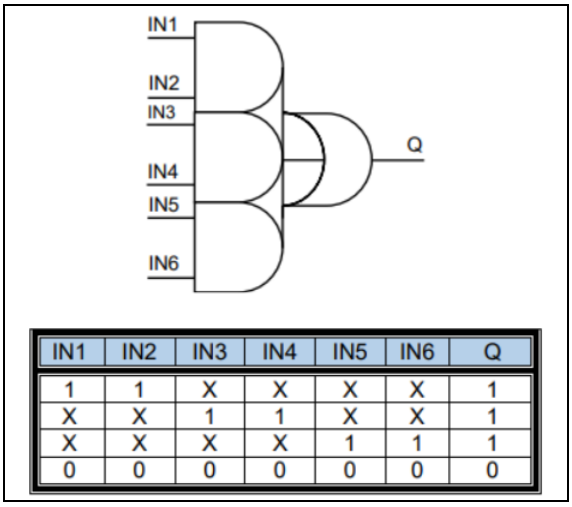
Figure 3.7 : Voltage vs Delays and Dynamic power variation of AO22 gate

OBSERVATION:

As we can see from the above graphs the RISEDELAY, FALLDELAY, TRISE &TFALL are decreasing with the increase in the voltage and the RISE and FALL dynamic powers are increasing with the increase in supply as power quadratically depends on the voltage.

3.2.5 CHARACTERIZATION OF AO222 GATE

Generalized Symbol for AO222 complex gate along with truth table is shown below:



IN1	IN2	IN3	IN4	IN5	IN6	Q
1	1	X	X	X	X	1
X	X	1	1	X	X	1
X	X	X	X	1	1	1
0	0	0	0	0	0	0

Figure 3.8 : AO222 gate with logic symbol and truth table[38]

The variations of the AO222 parameters with the operating voltages **0.4v, ±5% and ±10%** are shown below:

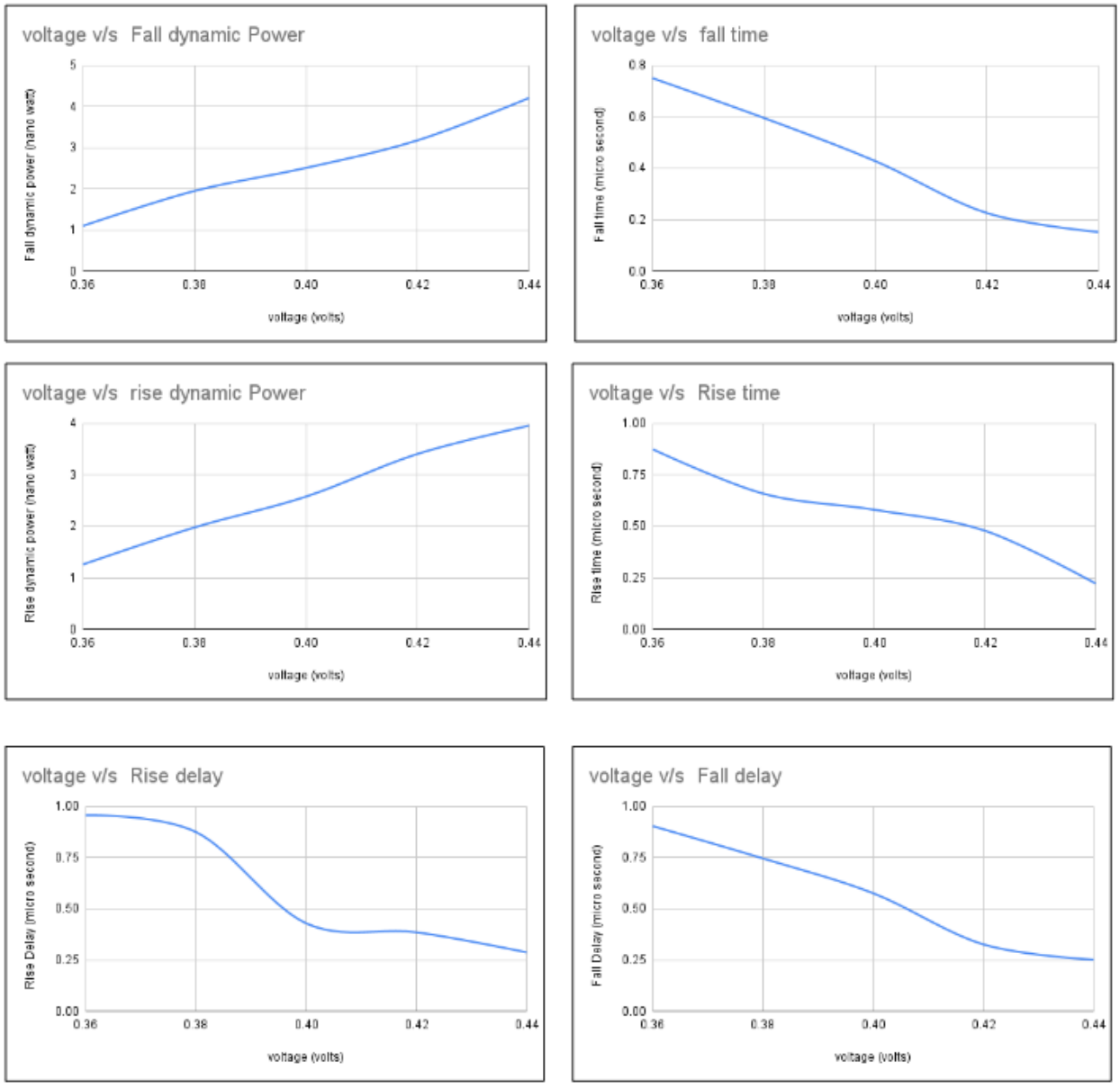


Figure 3.9 : Voltage vs Delays and
Dynamic power variation of AO222 gate

3.2.6 PARAMETERS VS DRIVE STRENGTH

The variations of the different parameters such as RISE DELAY ,FALL DELAY, TRISE ,TFALL and the RISE & FALL DYNAMIC POWERS with the strength of the various AO222 gates are shown below:

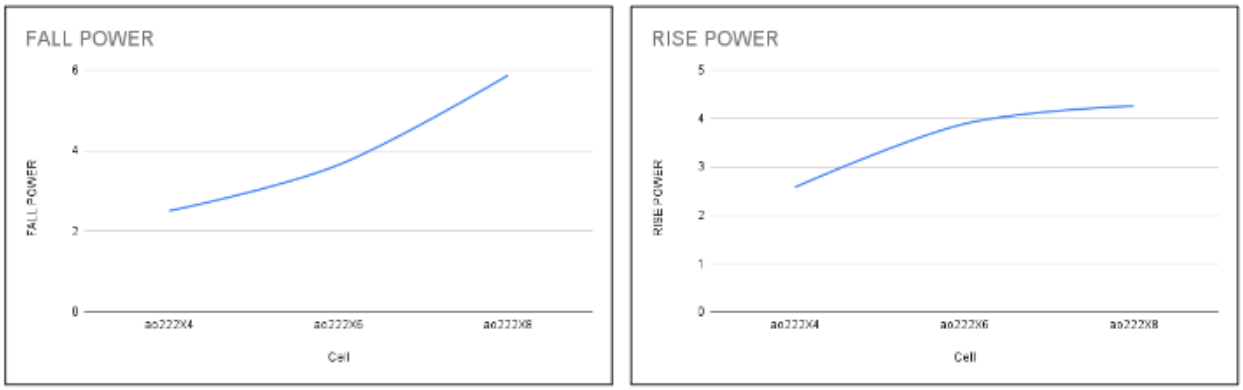
AO222	Istatic	Drive Strength
AO222X4	517.32nA	X4
AO222X6	778.27nA	X6
AO222X8	1.47uA	X8

Table 3.9 : List of complex gate with different strength and their static current

To define the drive strength Istatic is measured accordingly by applying a 0.8*vdd supply to the output port and selecting the input combinations for RISE and FALL accordingly.

Cell	RISE DELAY(us)	FALL DELAY(us)	RISE TRANSITION(us)	FALL TRANSITION(us)	RISE DYNAMIC POWER(us)	FALL DYNAMIC POWER(nW)
AO222X4	0.425	0.576	0.581	0.428	2.58	2.51
AO222X6	0.395	0.407	0.498	0.385	3.89	3.65
AO222X8	0.277	0.367	0.298	0.296	4.36	5.87

Table 3.10 : Worst case delays and dynamic power of AO222 gate with different strengths



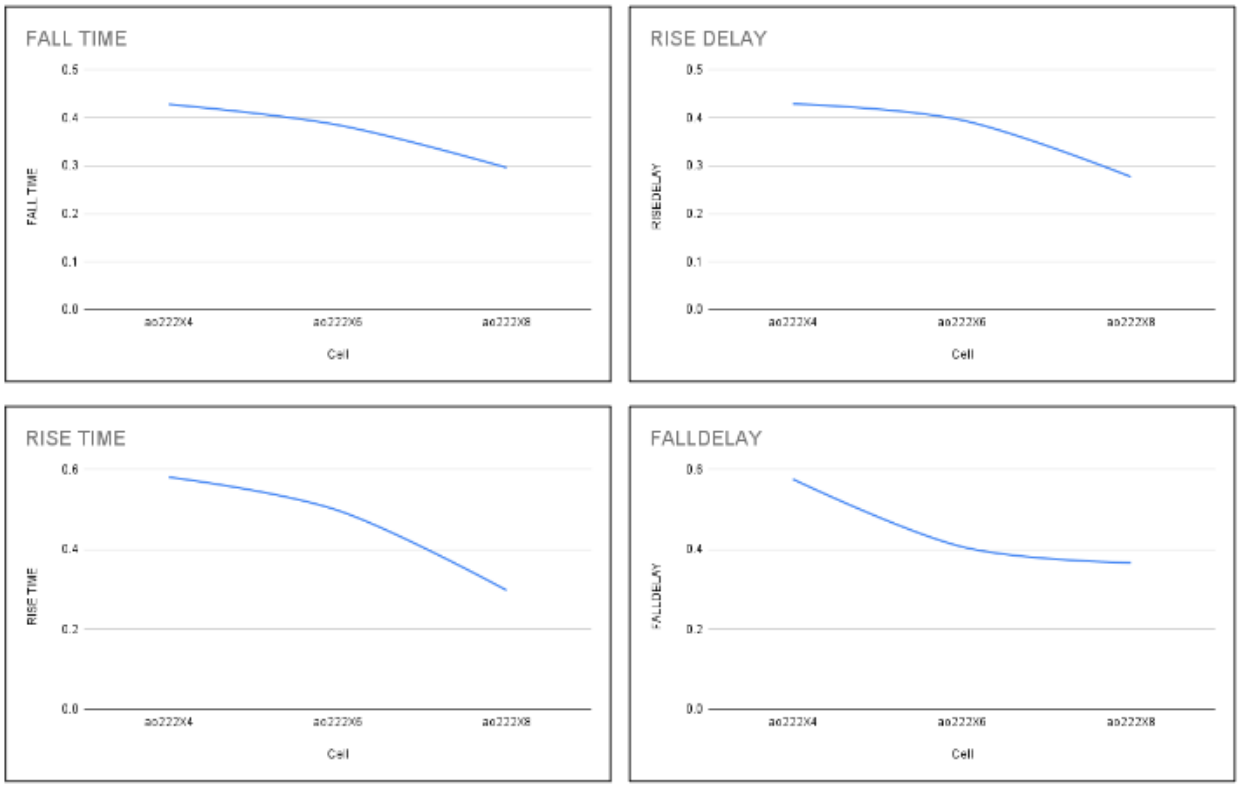


Figure 3.10 : Drive strength vs Delays and Dynamic power variation of NAND gate

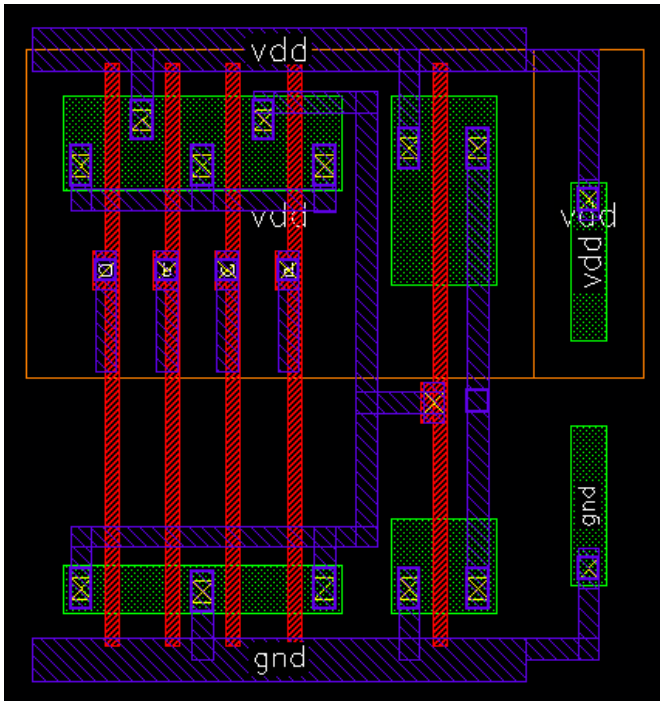
OBSERVATION:

we can see from the above graphs the RISEDELAY, FALLDELAY, TRISE &TFALL are decreasing with the increase in the strength of the cell and the RISE and FALL dynamic powers are increasing with the increase in strength of the gate as the sizes of the transistors are increasing as we increase the strength of the gate.

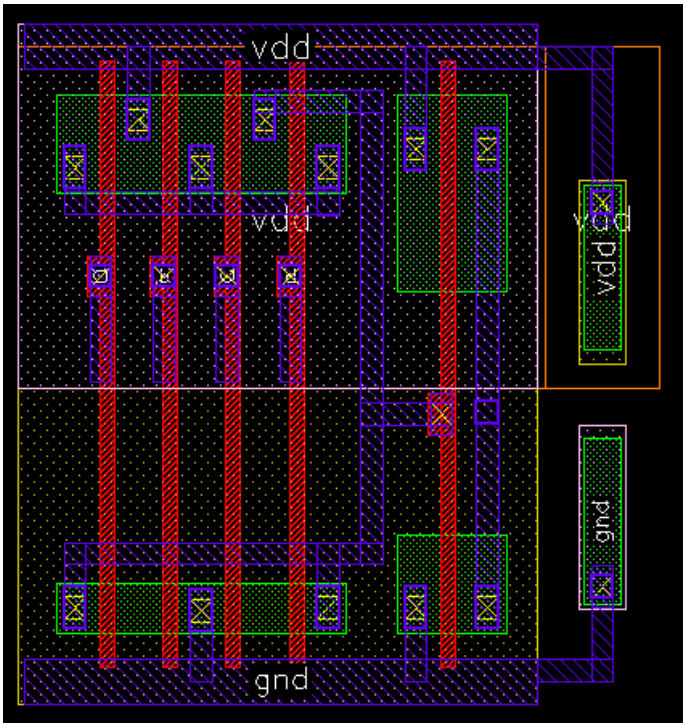
3.2.7 SOME COMPLEX GATE LAYOUTS

AO22

Without PP & NP layer

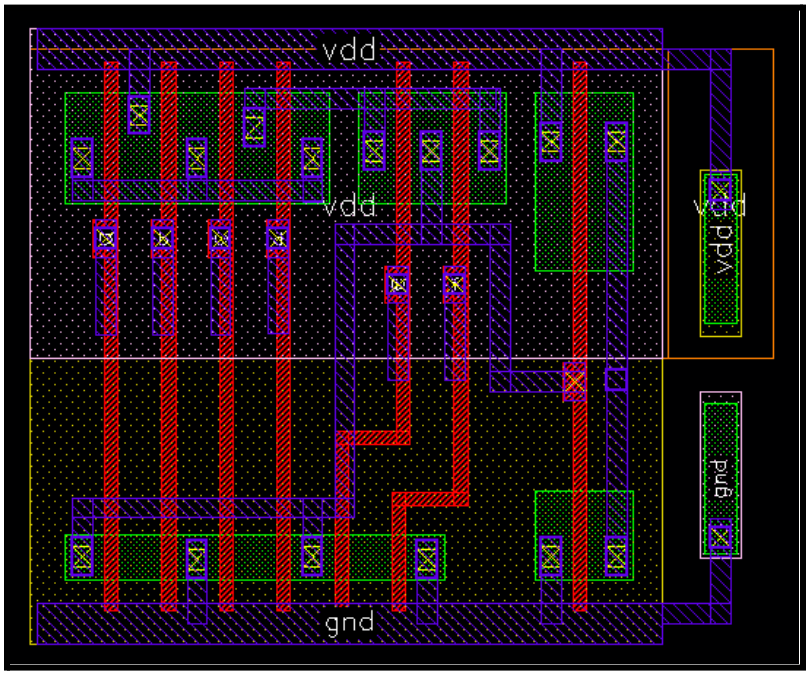


With PP & NP layer

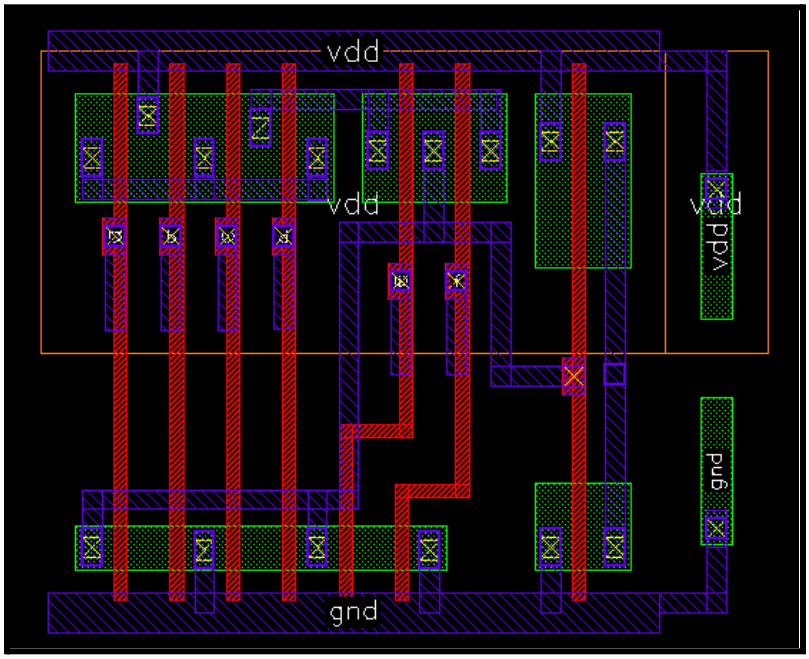


AO222

With PP & NP layer



Without PP & NP layer



CHAPTER 4
DESIGNING OF SEQUENTIAL CELLS

4.1 THE CMOS TRANSMISSION GATE

A single nMOS or pMOS pass transistor suffers from a threshold drop. If used alone, additional circuitry may be needed to pull the output to the rail. Transmission gates solve this problem but require two transistors in parallel. The resistance of a unit-sized transmission gate can be estimated as R for the purpose of delay estimation. Current flows through the parallel combination of the nMOS and pMOS transistors. One of the transistors is passing the value well and the other is passing it poorly; for example, a logic 1 is passed well through the pMOS but poorly through the nMOS.[19]

4.2 The CMOS D-Latch

T-gates enable the efficient execution of a number of essential logical operations in CMOS technology. The following applet demonstrates maybe the most significant application. A conventional D-latch (level-controlled flip-flop) can be made from four 2-input NAND gates. Therefore, one D-latch requires 16 transistors. The applets illustrate how a D-latch can be implemented with only 8 transistors (2 inverters and 2 T-gates) if both the clock signal and the inverted clock signal are available, resulting in a 50% decrease in transistors and, thus, chip-area. If the inverted clock is unavailable, a second inverter is required to provide the control signal for the two T-gates, reducing the number of transistors from 16 to 10.

The function of the T-gate D-latch is simple to comprehend. If the C input is a 1, the input T-gate is conducting and the data input value is connected to the first inverter input, producing!D. The second inverter generates!!D = D, or Q is equal to D. (the latch is transparent).

If the C input is zero, the first T-gate is closed and the feedback T-gate is open (since its R contact is connected to Q, which still equals D). The Q signal is therefore supplied back to the first and second inverters by the circuit (!Q and!!Q=Q, respectively). The value of Q is therefore retained until the C input returns to the value '1'.

4.3 FLIP-FLOP

As flip-flops are essential components of sequential logic circuits, their power consumption has become an important design consideration. One of the most efficient ways to achieve low-power design is to reduce the supply voltage. As the relationship between delay and supply voltage is exponential, scaling the supply voltage has a negative effect on the performance of the circuit.
There are three important timing parameters for a flip-flop: setup time (Tsu), hold time (Thold), and propagation delay (Tc-Q).

Tsu indicates the amount of time before the clock's end that the input (D) must be valid.
Several variables must be considered while purchasing very low-voltage flip-flops. The circuits are subject to failure when the supply voltage lowers because they cannot maintain rail-to-rail voltage changes due to diminished Ion/Ioff and noise margins, while the external noise stays constant.
Typically, traditional flip-flops, such as the TGMS, maintain the signal via feedback logic with inverters.
Typical flip-flops, such as the TGMS, maintain the signal via feed-back logic and inverters.

When scaling subthreshold flip-flops, it is recommended to use a different p/n ratio than normal super threshold CMOS. The pMOS and nMOS transistors at the switching point should conduct the same current for low Vdd operation.

By operating in the subthreshold region, it is possible to limit the discharge of dynamic nodes, which, if not taken into account during circuit design, could influence the dependability of dynamic cells. This reduces the influence of subthreshold leakage, hence shortening the maximum holding period of dynamic cells.

In order to reduce C-Q latency, the usual method includes pMOS devices that are many times larger than the nMOS devices used in inverters.

4.3.1 METASTABILITY

Metastability of flip-flops is increasingly considered in the design of dependable synchronous and asynchronous systems, particularly in the subthreshold region, where it decreases exponentially with decreasing supply voltage. This work examines in depth the construction of subthreshold metastable-hardened flip-flops. By appropriately scaling transistors utilizing either transconductance or load variation and by creating the inverter pair in the flip-flop master-stage with low-Vth, the time-resolving constant can be significantly reduced. Even while the concept of energy harvesting in sub-threshold devices is enticing, system dependability must take reliability issues into account. Timing components such as flip-flops and latches are crucial to the digital system because they synchronize the data flow with the CLK signal. During synchronization, a flip-flop frequently enters an undesired third state when the output sits between logic "0" and "1" and generates metastability. If data changes occur within the setup and hold time limits of a flip-aperture flop (tap), the output may become unpredictable and require an indefinite amount of time to stabilize.[37]

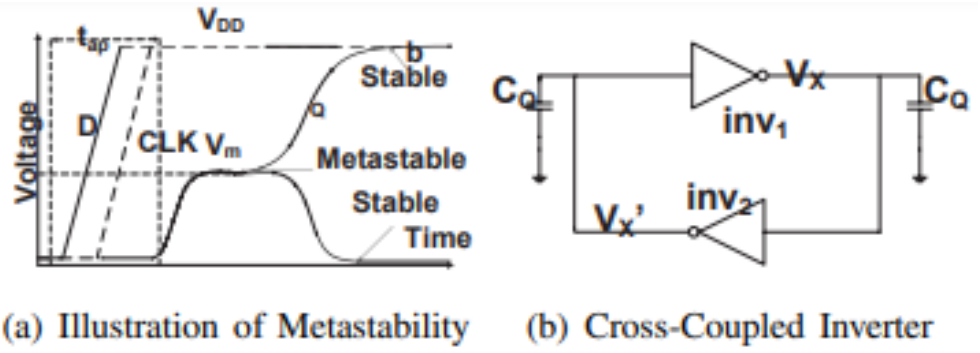


Figure 4.1 : Cross coupled Inverter and Metastability [37]

4.3.2 SIZING

Sizing has been done in such a way that the metastability window shrinks, as per the stick diagram we were following the maximum size of NMOS was 0.43um and that of PMOS is 0.6um . We swept the width of both NMOS and PMOS the best results we were getting at NMOS=0.2um and PMOS=0.41um. At this sizing we were getting the metastability window of 6.83 ns. After getting this sizing to change the driving strength we have changed the sizes of inverter connected to the output in such a manner that we get Icout of that strength i.e. if Icout of X1 is y then Icout of X2 is 2y.

4.3.3 SCHEMATIC

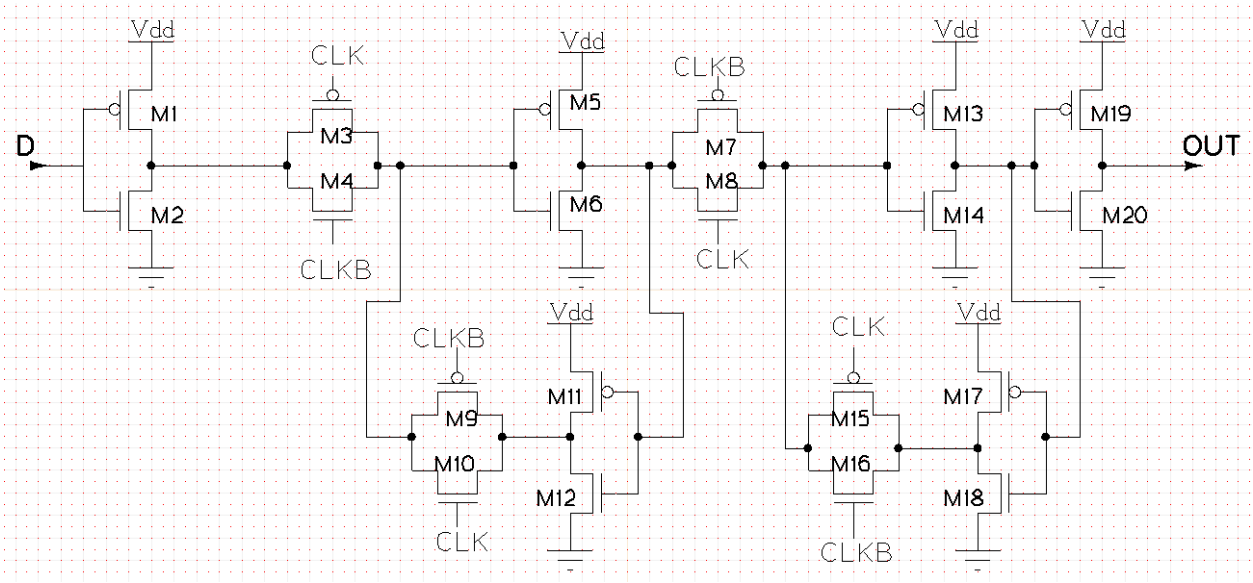


Figure 4.2 : Transmission gate based Flip Flop

We have designed 4 flip flops of different drive strengths that is X1, X2, X4, X8. We have changed the size of inverter connected to output to get larger load current as per the required drive strengths.

Sizing of output inverter :-

Size of M19	Size of M20	Drive Strength
0.41	0.23	X1
0.78	0.42	X2
2.19	1.12	X4
5.59	2.76	X8

Table 4.1 : Sizing of output inverter with different strengths

4.3.4 PARAMETERS VS DRIVE STRENGTH

The variations of the different parameters such as Metastability Window ,Clock to Q Delay, Dynamic Power and Leakage Power with the strength of the various Flip flop are shown below:

Flip-Flop	Metastability Window	CLK_Q Dealy	Dynamic Power	Leakage Power
X1	6.83E-09	7.15E-08	4.66E-08	3.85E-13
X2	7.08E-09	5.80E-08	5.69E-08	4.41E-13
X4	7.15E-09	9.24E-08	7.84E-08	4.53E-13
X8	7.17E-09	15.80E-08	8.33E-08	4.83E-13

Table 4.2 : Metastability window, Clock to Q delay, dynamic and leakage power of different strengths

4.3.5 PARAMETERS VS OPERATING VOLTAGES

Voltages	Metastability Window	CLK_Q Dealy	Dynamic Power	Leakage Power
0.36	1.44E-08	1.68E-07	2.79E-08	3.61E-13
0.38	9.68E-09	1.10E-07	3.99E-08	4.42E-13
0.4	6.83E-09	7.15E-08	4.66E-08	3.85E-13
0.42	4.78E-09	4.82E-08	5.14E-08	4.06E-13
0.44	3.56E-09	3.32E-08	5.64E-08	5.01E-13

Table 4.3 : Metastability window, Clock to Q delay, dynamic and leakage power with changing voltage

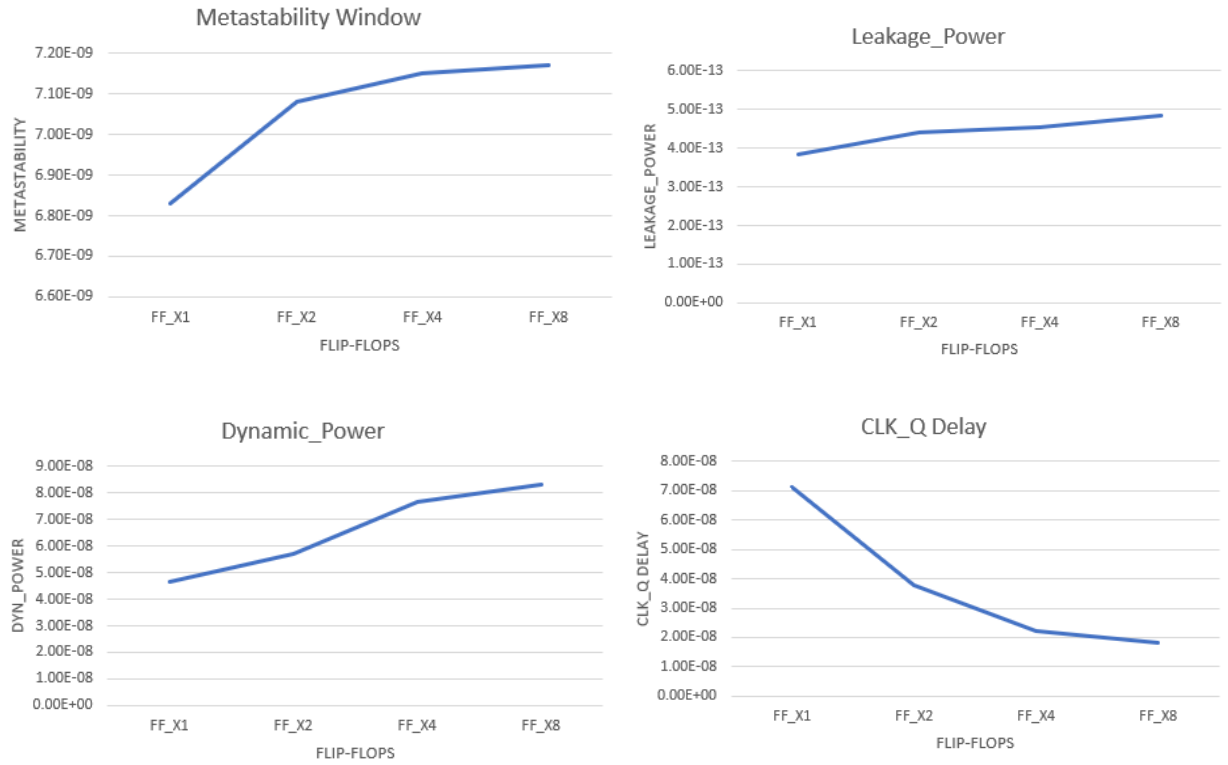
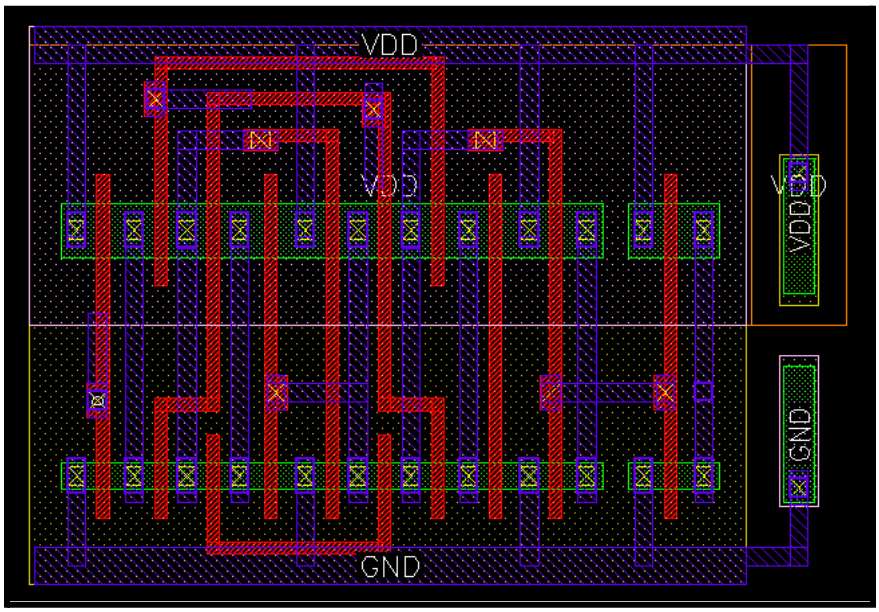


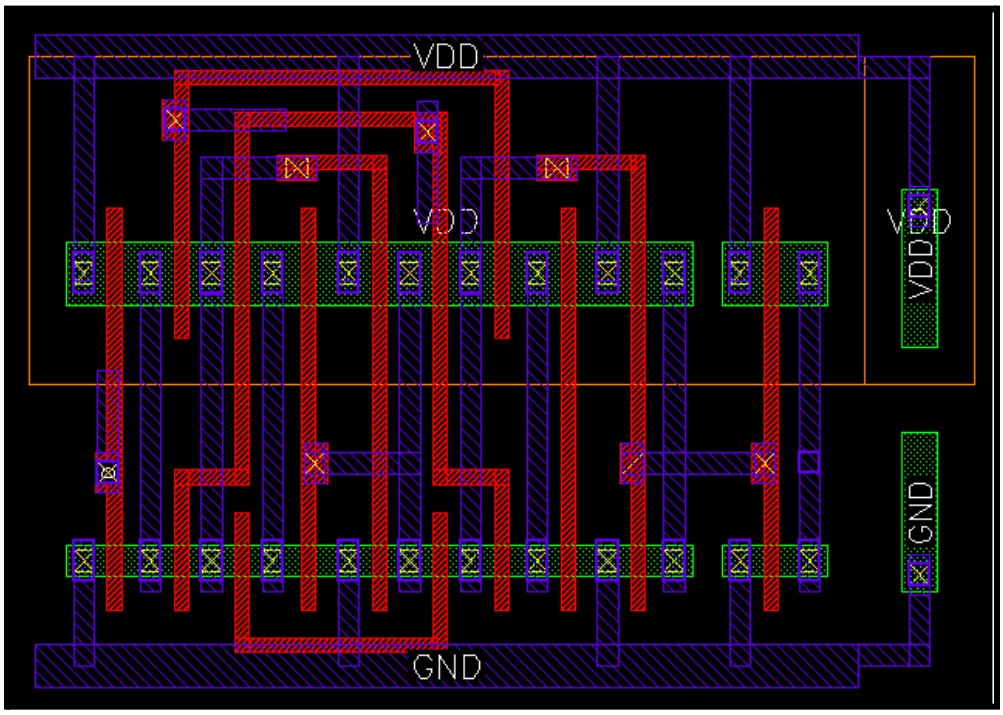
Figure 4.3 : Metastability window, Clock to Q delay, dynamic and leakage power vs different strengths

4.3.6 LAYOUTS

With PP Layer



Without PP Layer



CHAPTER - 5

DESIGNING OF CLOCK INVERTER AND CLOCK BUFFER

The main characteristics of clock inverter and clock buffer is that both rise and fall time should be equal. The sizing of both clock inverter and clock buffer was done keeping this fact intact and try to have equal rise and fall time across the whole temperature range of the operation.

5.1 Layout of clock buffer

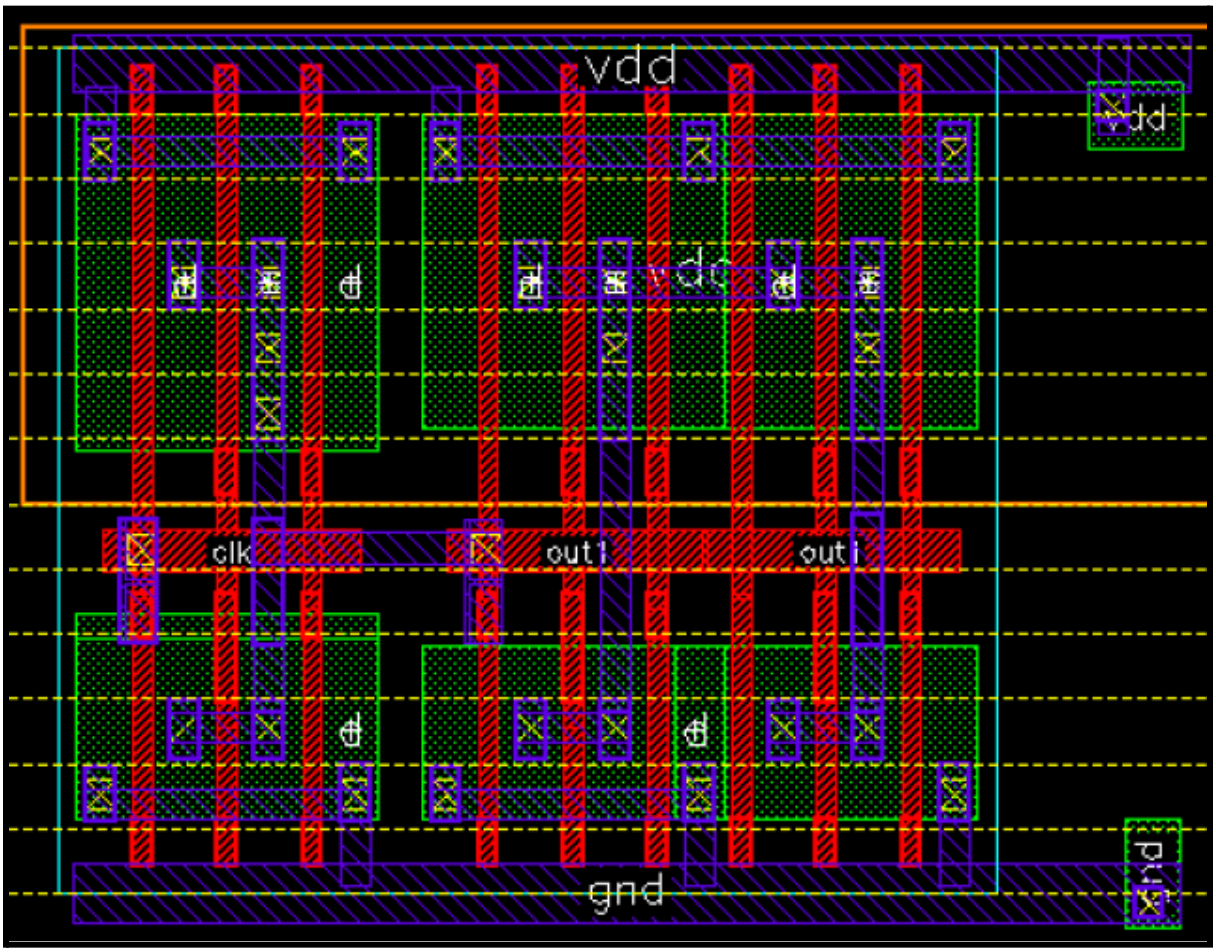


Figure 5.1 : Clock Buffer Layout

5.2 Layout of the clock inverter

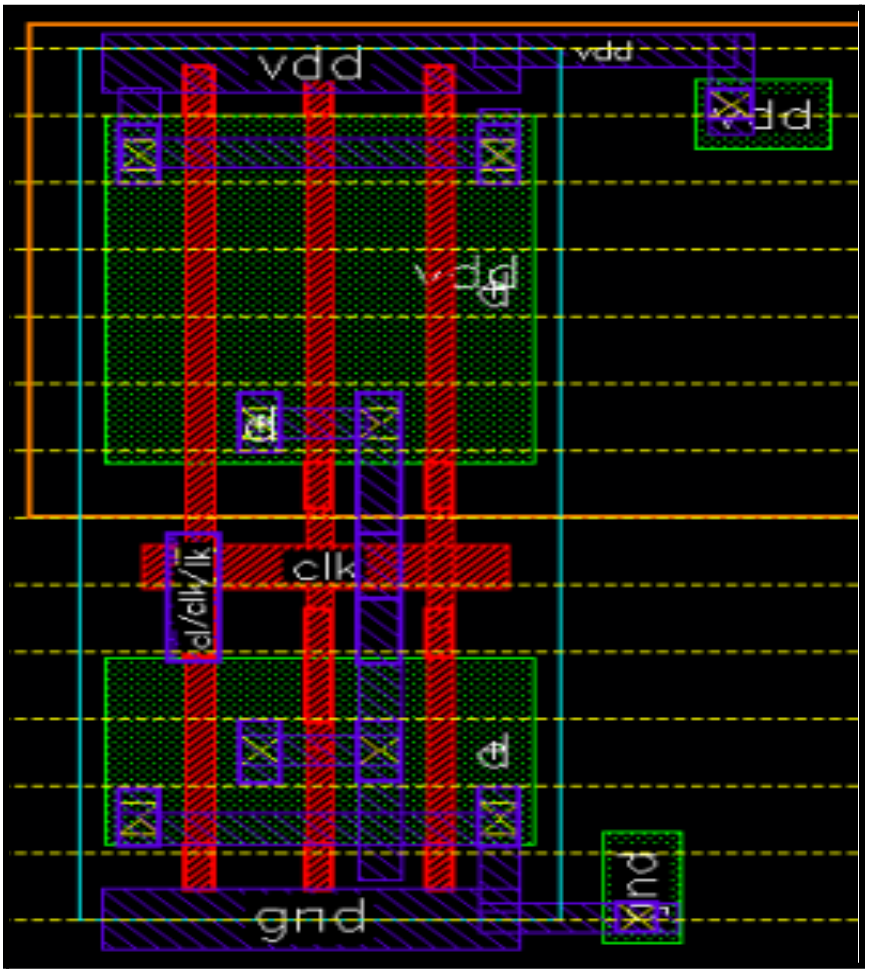


Figure 5.2 : Clock Inverter Layout

5.3 Results of different parameter values with voltage and process corner variation

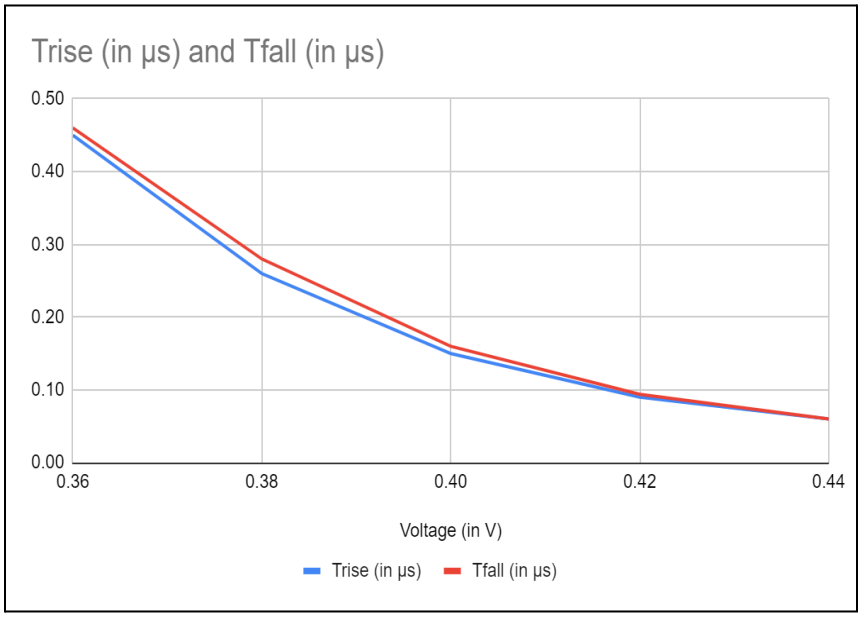


Figure 5.3 : Variation of rise and fall time with ±10% voltage variation

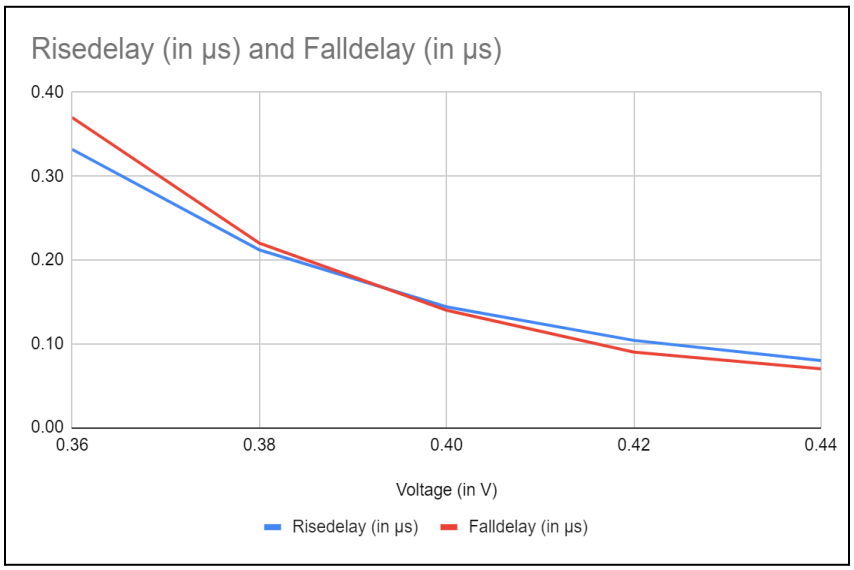


Figure 5.4 : Variation of rise delay and fall delay with ±10% voltage variation

Both graphs depict that the rise and fall delay as well as rise and fall time are equal, with the parameters following an approximate exponential curve across the voltages ranging from 0.36V to 0.44V. There is an exponential increase in all the parameter values at lower voltages.

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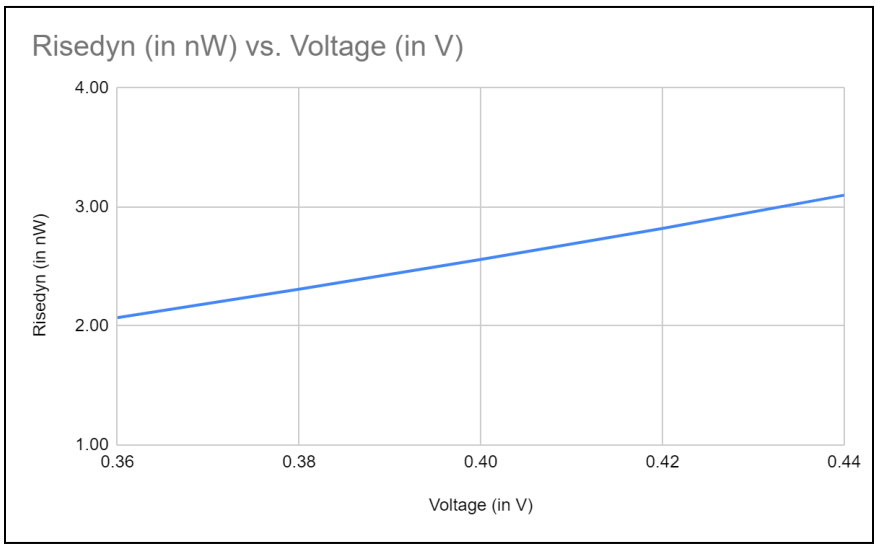

Figure 5.5 : Variation of rise dynamic power with ±10% voltage variation

Similar trend for rise dynamic power with voltage is observed. At higher voltages, the rise dynamic power is getting increased as it is directly proportional to the square of the voltage

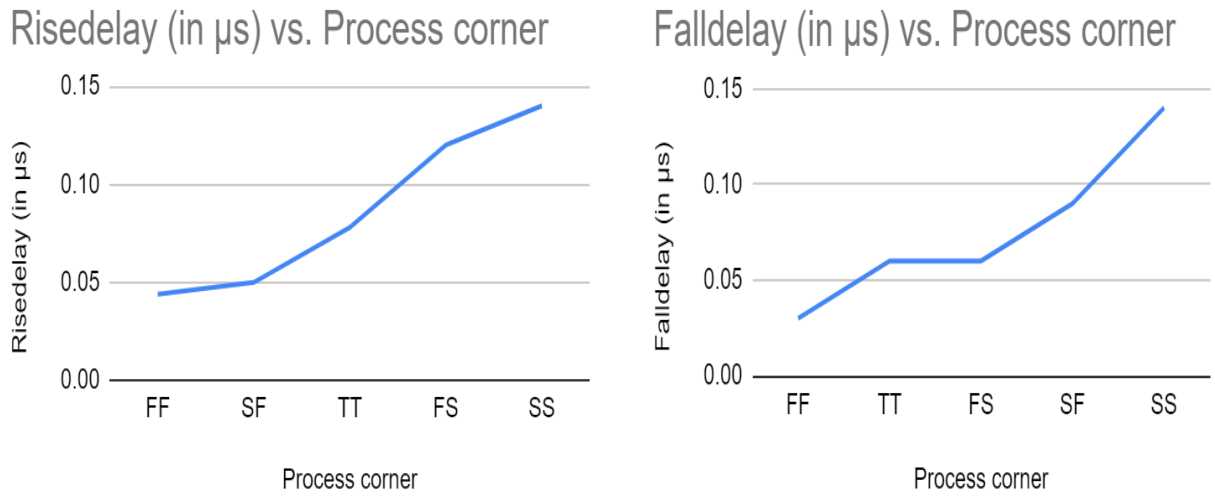

Figure 5.6 : Variation of rise delay and fall delay at different process corners

The rise delay and fall delay are plotted for different process corners and it is observed that worst corner for both is SS and the best corner where the delays are minimum is FF.

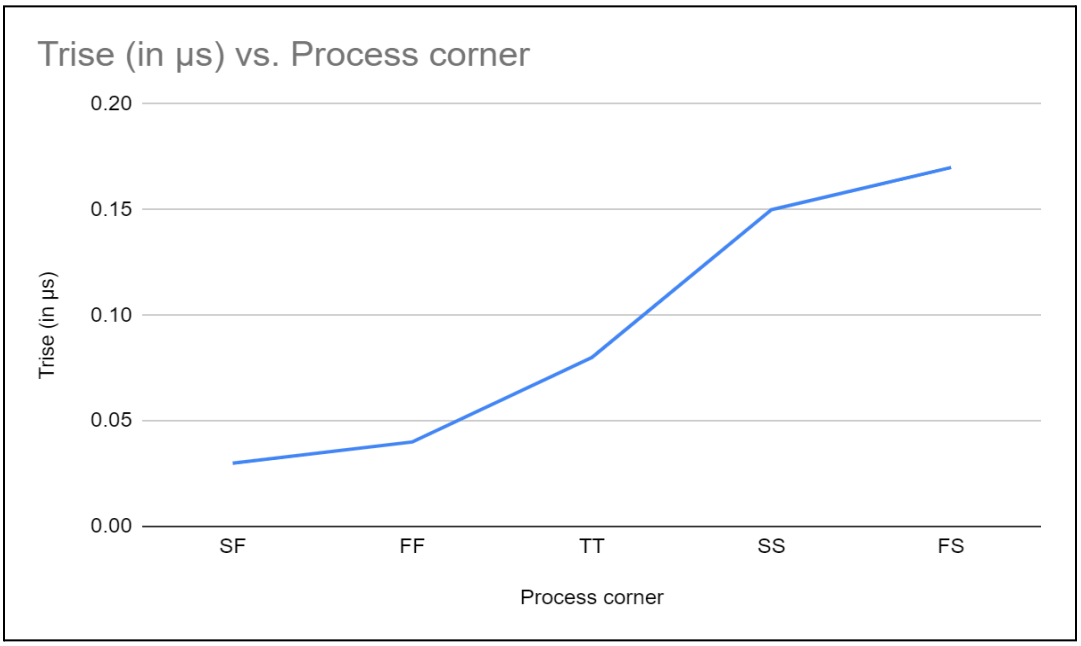

Figure 5.7 : Variation of rise time at different process corners

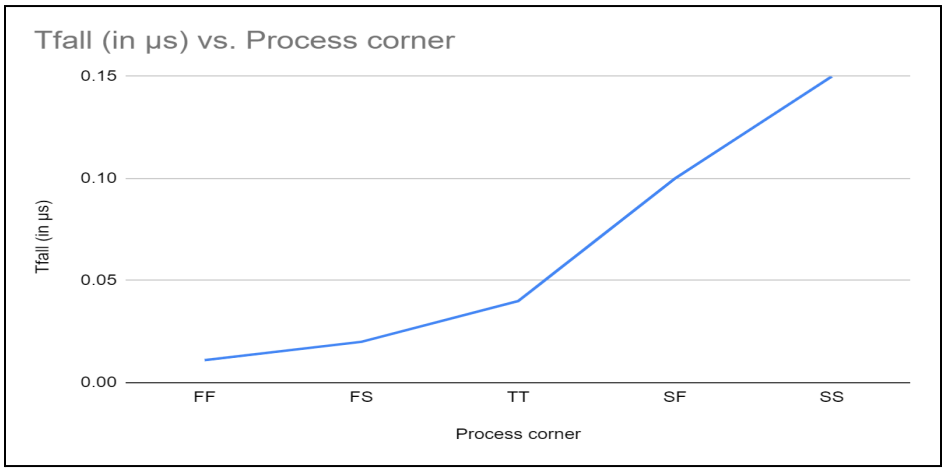

Figure 5.8 : Variation of fall time at different process corners

Similarly trends for rise time and fall time are depicted, where the maximum rise time is obtained at FS corner and minimum at SF. For fall time, maximum fall time is at SS corner and minimum at FF corner.

5.4 Parameters vs Drive Strengths

To compare between both the drive strength, delays for both the buffers (BUFX1 and BUFX10) are plotted on the same graph, it is observed that at lower voltages there is an exponential increase in the delays. Similar trend is observed for rise time and fall time variation with voltage. The values degrades exponentially at lower voltage of operation i.e. 0.36V.

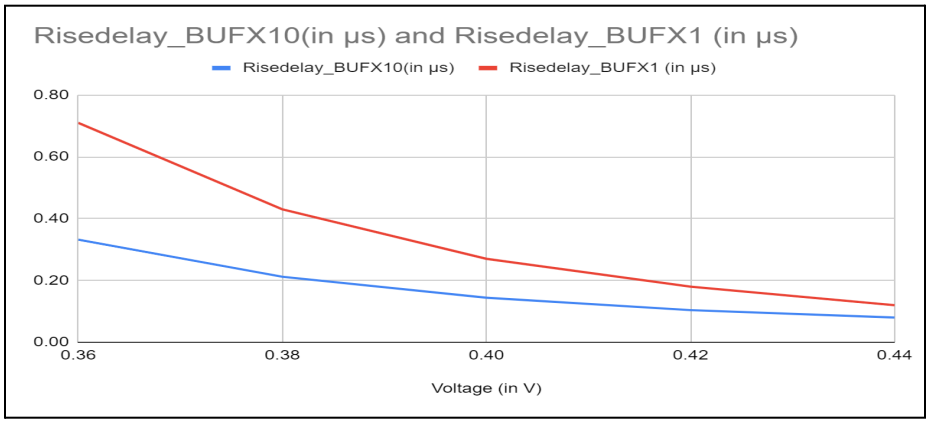

Figure 5.9 : Variation of rise delay for X1 and X10 drive strength clock buffer

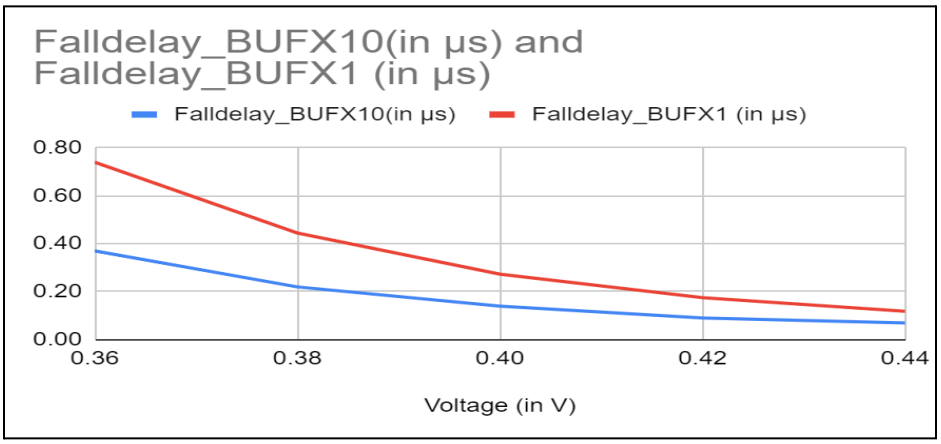

Figure 5.10 : Variation of fall delay for X1 and X10 drive strength clock buffer

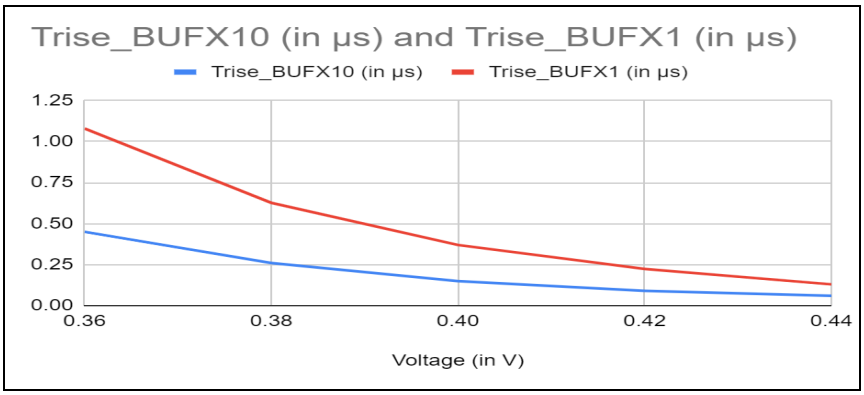

Figure 5.11 : Variation of rise time for X1 and X10 drive strength clock buffer

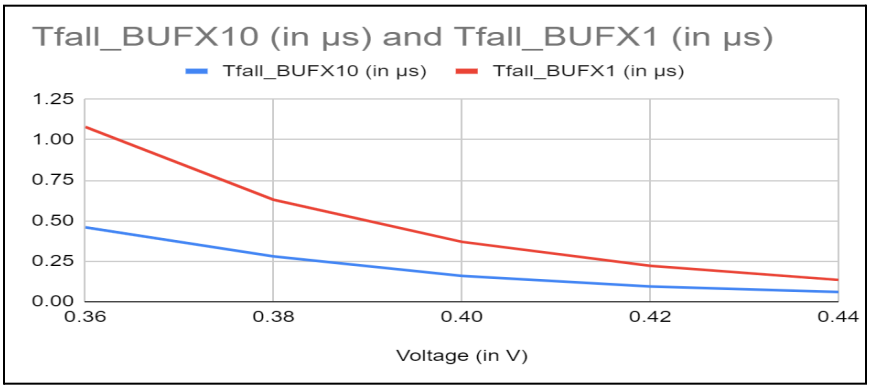

Figure 5.12 : Variation of fall time for X1 and X10 drive strength clock buffer

Similar trend for inverters is observed for all the parameters as shown in the below graphs. The rise time,fall time,rise delay,fall delay value degrades significantly at lower voltage of operation.

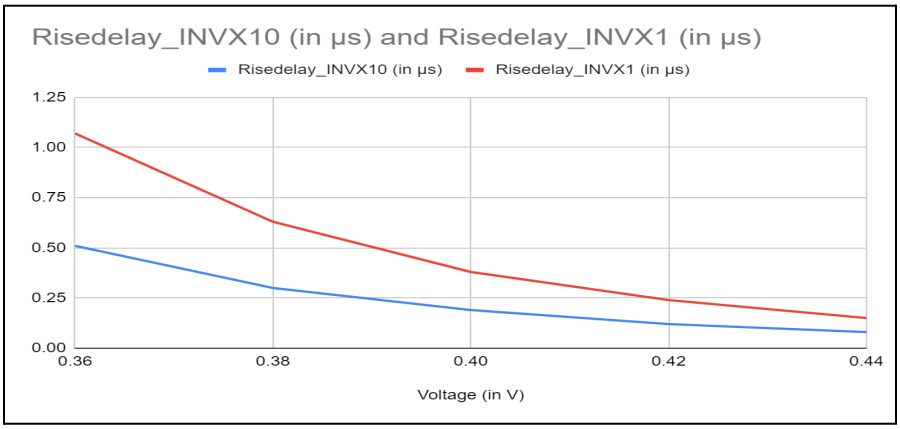

Figure 5.13 : Variation of rise delay for X1 and X10 drive strength clock inverter

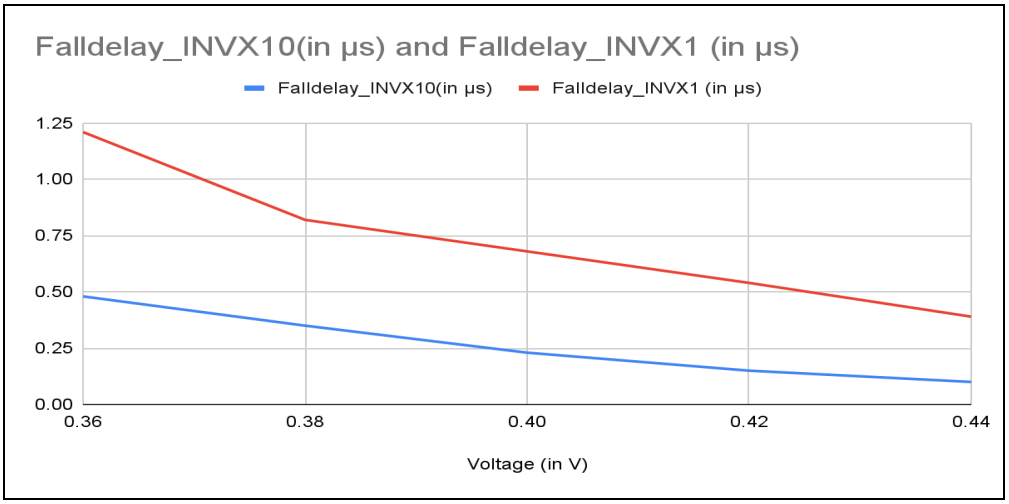

Figure 5.14 : Variation of fall delay for X1 and X10 drive strength clock inverter

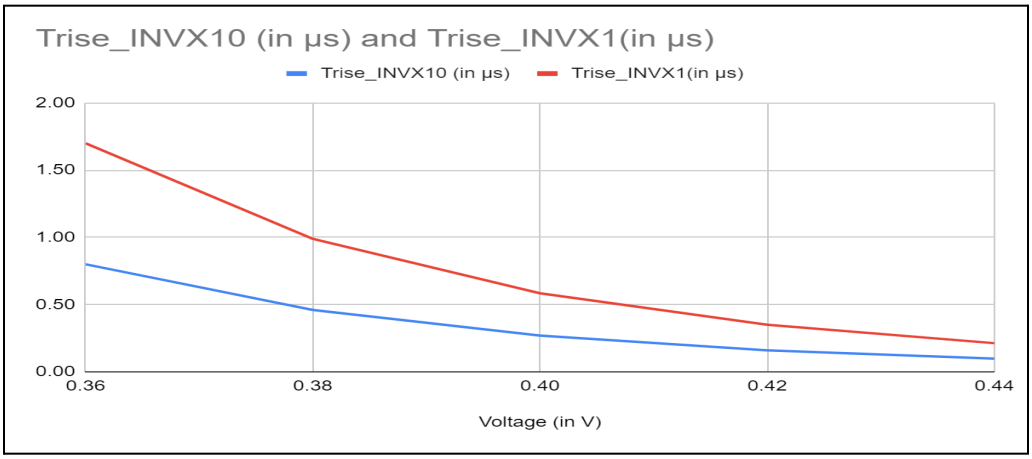

Figure 5.15 : Variation of rise time for X1 and X10 drive strength clock inverter

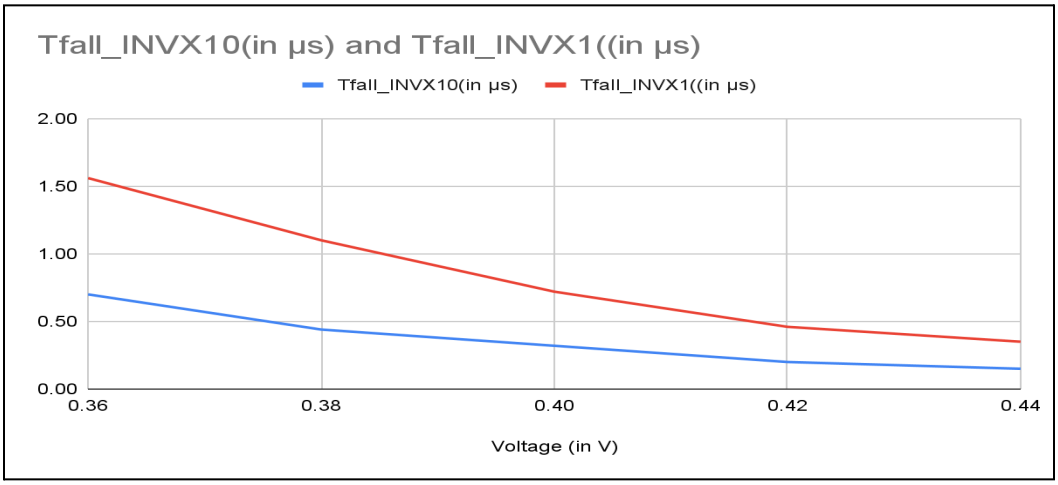

Figure 5.16 : Variation of rise time for X1 and X10 drive strength clock inverter

CHAPTER -6
SYNTHESIS

The ARM CortexM processor family is tailored for cost and power-sensitive MCUs and mixed-signal devices, and soft cores and hard cells are available in FPGAs. Cortex-M solutions are available in FPGAs from Altera (the Cortex-M1 is offered as a soft core) and Actel (the Cortex-M1 is delivered as a soft core and the Cortex-M3 as a hardened block), but not Xilinx. In addition, ARM has produced a cost-effective, streamlined version of the Cortex-M0 CPU (Cortex-M0 DesignStartTM) that may be synthesized into an FPGA or used for silicon implementations.

6.1 Families of Processors from ARM

The Cortex family of ARM processors comprises cores ranging from low-cost microcontroller solutions to high-end processors capable of supporting large complex operating systems.Cortex-M0 is the least advanced processor in the Cortex-M family. This series of embedded processors allows for a variety of trade-offs between price, design simplicity, power, performance, and computational capability.The Cortex-M0 CPU aims for low power consumption and a small footprint to compete with high-end 8-bit and 16-bit processors, but it maintains code compatibility with the other family members, such as the Cortex-M3 processor. The smallest Cortex-M0 processor has approximately 12,000 gates and an 84W/MHz power rating.

6.2 Cortex M0 Architecture

The Figure 6.1 displays a Cortex-M0 processor with a three-stage pipeline based on the ARMv6-M architecture (Von Neumann). The Cortex-M0 CPU uses a modified version of the Advanced Microcontroller Bus Architecture (AMBA®), the AMBA-Lite bus to connect with various peripherals.

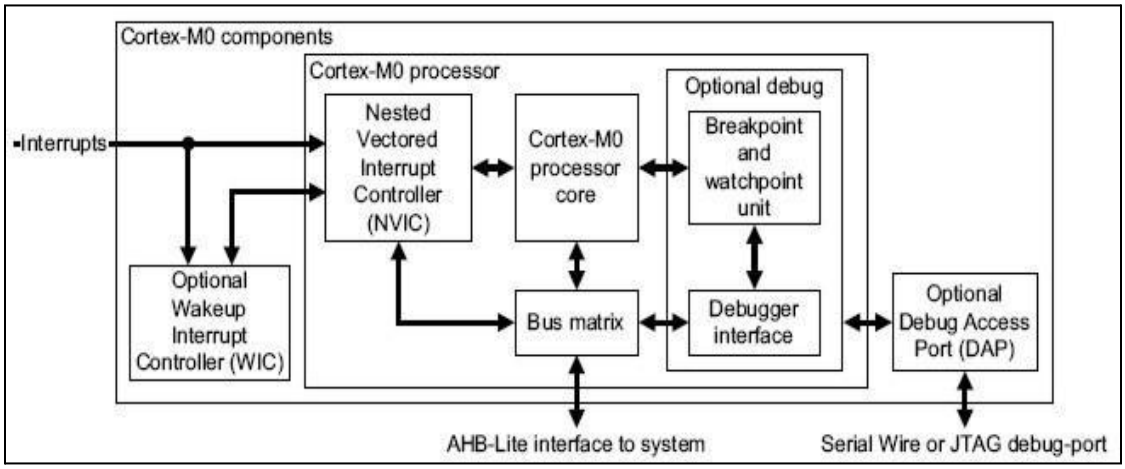

Figure 6.1 : Cortex M0 Architecture[27]

This bus was designed as a high-performance bus for processor-to-peripheral operations that require a wide bandwidth or high throughput. Typically, the Cortex-M0 is the lone master device on the bus, with all peripherals serving as slaves; however, the bus specification permits a multimaster system. The main essential aspects of the bus are single or burst transfers, single cycle transfers, tri-state buffers, and configurable bus width configurations (32, 64, 128, 256,512, or 1024 bits).

6.3 Synthesizing on Cortex M0

For benchmarking initially the performance of CortexM0, we performed the synthesis and STA at SS, 0.58V,125°C. The motivation behind choosing 0.58V was since it is a lower voltage which is closer to the operation in subthreshold region and it would help us to benchmark the performance more closely with the library designed at 0.4V. For this PVT, synthesis was done at different time periods and timing constraints were made tighter to extract the best performance from the cortex M0. The maximum operating frequency obtained is 44.44 MHz with a huge penalty on area and power. Interestingly if you want to achieve more frequency with a liberty in area and power consumption, still you can't go beyond 44.44 MHz .The tool tries to add large cells of higher drive strength to obtain even higher frequency however it fails and STA checks cannot be cleared. The best frequency achievable is 44.44 MHz at the given PVT of SS, 0.58V,125°C. Though the final frequency achievable is 44.44 MHz,the decision has to be taken considering all the parameters and application i.e. tradeoff between performance, power and area. To model and understand this,the synthesis is performed at different timing constraints and area,power and maximum frequency are tabulated to have the idea of every parameter and then decide the constraints as per the application.

Constraint time period (in ns)	Area	No of cells used	Leakage Power (μW)	Dynamic Power(μW)	Total Power (μW)	Sign off time (in ns)	Final operating freq (in MHz)
90 ns	40859	8844	7.93	57.86	65.79	90.85	11.01
80 ns	41056	8919	8.01	64.72	72.74	80.85	12.37
70 ns	41255	9099	8.07	73.25	81.32	70.8	14.12
60 ns	41401	8994	8.11	84.69	92.82	61.1	16.37
40 ns	42178	9497	8.46	126.35	134.82	41.5	24.10
20 ns	58583	14151	14.69	541	556	22.5	44.44

Table 6.1 : PPA (Power Performance Area) analysis at SS, 0.58V,125°C

The area, power and frequency tradeoff analysis are also being performed at SS,0.7V,-40°C , FF, 0.7V, 125°C and TT, 0.7V, 25°C. These all PVTs will determine the best and worst frequency of operation we can achieve at a given voltage of 0.7volts.

The constraint time period is reduced and then the synthesis is done by making the timing constraints tighter and tighter until we extract the best performance at SS, 0.7V, -40°C. The maximum achievable operating frequency at SS 0.7V,-40°C is 57.57 MHz. To obtain this frequency, higher power and area are required thus again a tradeoff between the PPA and the way to decide would be the need of the application and the constraint that it poses.

Constraint time period (in ns)	Area	No of cells used	Leakage Power (nW)	Dynamic Power(µW)	Total Power (µW)	Final Sign off time period	Freq (in MHz)
80	40856	8807	3.24	90.14	90.22	81	12.35
70	41007	8870	3.28	102.56	102.575	71.1	14.06
60	41323	8987	3.33	118.77	118.78	61.2	16.34
40	41703	9256	3.35	173.81	173.81	41	24.39
10	60882	15293	5.98	1574	1575	17.37	57.57
5	61431	15836	6.02	3081	3181	17.37	57.57

Table 6.2 : PPA (Power Performance Area) analysis at SS, 0.7V, -40°C

Similarly, the analysis is done at FF, 0.7V, 125°C and the results are tabulated in the Table 6.3. The maximum achievable operating frequency at FF, 0.7V, 125°C is 231.48 MHz.

Constraint time period (in ns)	Area	No of cells used	Leakage Power (µW)	Dynamic Power(µW)	Total Power (µW)	Final Sign off time period (in ns)	Final Freq (in MHz)
17	40157	8950	113.46	418.5	532	17.6	56.82
10	41918	9453	118.46	706.5	824	10.6	94.34
5	48076	11622	153.18	1474.6	1628	5.3	188.68
3	61812	15524	227.8	2523	2750	4.32	231.48

Table 6.3 : PPA (Power Performance Area) analysis at FF, 0.7V, 125°C

Similarly, the analysis is done at TT, 0.7V, 25°C and the results are tabulated in the Table 6.4. The maximum achievable operating frequency at TT, 0.7V, 25°C is 119.05 MHz.

Constraint time period (in ns)	Area	No of cells used	Leakage Power (nW)	Dynamic Power (μW)	Total Power (μW)	Final Sign off time period (in ns)	Freq (in MHz)
10	47533	11356	661	753	754	10.5	95.24
5	61644	16020	984	3335	3336	8.4	119.05

Table 6.4 : PPA (Power Performance Area) analysis at TT, 0.7V, 25°C

As the frequency at which synthesis is done is increased, no of cells being used are increased, the tool tries to use large cells and correspondingly the dynamic and leakage power also increases.

6.4 Synthesis results with PVT variations

To summarize the maximum frequency obtained at a given voltage of 0.58V with different process corners and temperature is depicted. Maximum frequency observed at the respective PVT is mentioned in the Table 6.5. The best PVT is FF, 0.7V, 125°C and the worst turns out to be SS, 0.7V, -40°C.

PVT	**Maximum operating frequency (in MHz)**
SS 0.7 -40°C	57.57
TT 0.7 25°C	119.04
FF 0.7 125°C	231.481

Table 6.5 : Maximum achievable operating frequency at different PVT conditions

The temperature inversion is observed and at lower temperature and at SS corner, the delays are increased, area is increased and hence more time period is required to have positive slack and have no violations during sta sign off and hence giving us a maximum operating frequency of 57.57 MHz at SS, 0.7V, -40°C. When operating at FF and higher temperature i.e. 125°C, the overall delays are less,

corresponding to less area and lesser time period is required for positive slack and hence the frequency of operation is increased.

The below table shows the effect of temperature variation keeping the process corner and voltage of operation constant. The trend obtained is similar i.e. at higher temperature, the achievable operating frequency is more and at less temperature, lower frequency of operation is obtained. This is due to the temperature inversion phenomenon.

PVT	**Maximum operating frequency (in MHz)**
SS 0.58 -40°C	10.6487
SS 0.58 -20°C	13.364
SS 0.58 125°C	44.44

Table 6.6 : Effect of temperature on the achievable frequency

The effect due to voltage variations at a constraint time period of 70ns (at frequency of synthesis 14.28MHz.)with two different voltages i.e. 0.58V and 0.7V is studied and results are summarized in the table 6.7.

PVT	Area	No of cells used	Leakage Power (nW)	Dynamic Power(µW)	Total Power (µW)	Final Sign off time period (in ns)	Freq (in MHz)
SS 0.58 -40°C	54791	13338	2.38nW	137.6	137.615	94	10.64
SS 0.7 -40°C	41007	8870	3.28nW	102.56	102.575	71.1	14.06

Table 6.7 : Effect of voltage at synthesis time period of 70ns

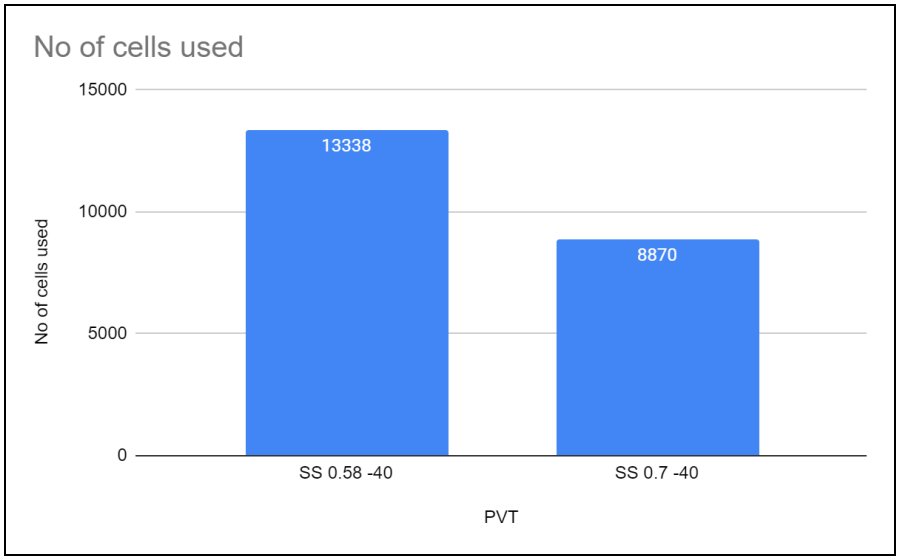

Figure 6.2 : Number of cells used with different PVT's

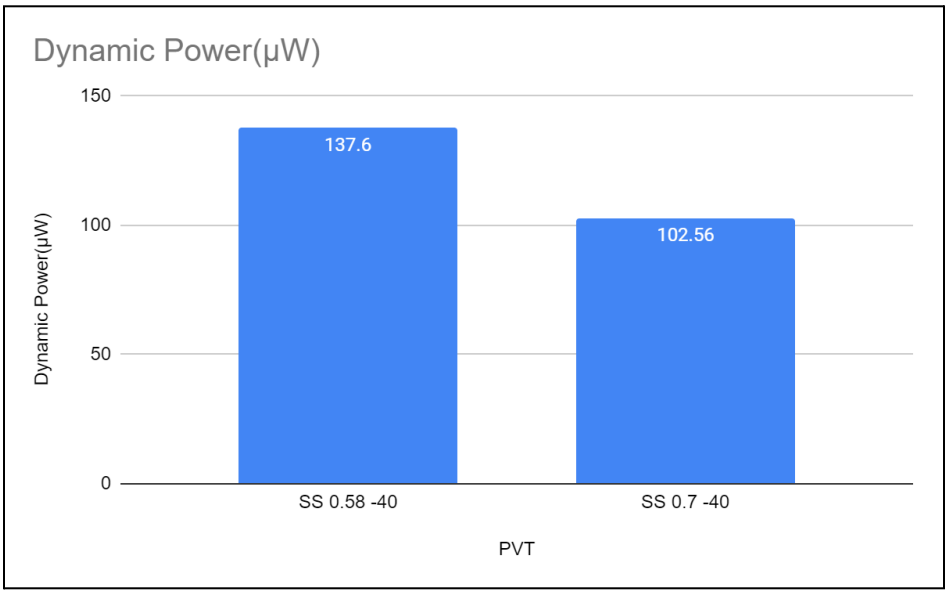

Figure 6.3 : Dynamic Power at different PVT's

It is observed that as we lower down the voltage of operation, the total no of cells used are increased, increasing the overall leakage and dynamic power consumption. This variation is observed when the frequency of synthesis is kept constant i.e. 14.28MHz. Also the frequency of operation at lower voltage is low compared to the frequency of operation at higher voltage.

Now we created a library which has only 40 cells and then tried obtaining the results with limited no of cells in the library. As the .lib now has lesser no of cells with limited variations of drive strength, the tool cannot optimise much and the performance is lesser as compared to the case when we have entire library available for synthesis.

Results with library having only 40 cells at SS 0.58V -40 are as follows :

Constraint time period (in ns)	Area	No of cells used	Leakage Power (nW)	Dynamic Power(µW)	Total Power (µW)	Final Sign off time period	Freq (in MHz)
90	53039	14508	2.78nW	127.55	127.565	105.5	9.48
80	53277	14702	2.81nW	143.18	143.191	104.8	9.54

Table 6.8 : PPA analysis with limited cells in the library

Results with entire library at SS 0.58V -40°C are as follows :

Constraint time period (in ns)	Area	No of cells used	Leakage Power (nW)	Dynamic Power (µW)	Total Power (µW)	Final Sign off time period	Final Freq (in MHz)
90	53822	12994	2.33nW	104.1	104.12	97.15	10.29
80	54844	13291	2.38nW	122.52	122.532	96.8	10.33

Table 6.9 : PPA analysis with whole library at SS, 0.58V, -40°C

Worst path at @ SS,0.58V, -40°C

```
Path 1: MET Setup Check with Pin u_cortexm0_u_top_u_sys_u_core_u_ctl/alu_en_reg/CP
Endpoint:   u_cortexm0_u_top_u_sys_u_core_u_ctl/alu_en_reg/D     (v) checked with  leading edge of 'HCLK'
Beginpoint: u_cortexm0_u_top_u_sys_u_core_u_ctl/rb_addr_reg[1]/Q (v) triggered by  leading edge of 'HCLK'
Path Groups: {HCLK}
Other End Arrival Time          0.000
- Setup                         4.559
+ Phase Shift                  96.800
- Uncertainty                   0.100
= Required Time                92.141
- Arrival Time                 92.127
= Slack Time                    0.014
```

o

Figure 6.4 : Worst path at SS,0.58V, -40°C

When the synthesis was performed at 0.4V at our designed library, it was able to perform synthesis using combinational cells present, but was unable to take up any of the sequential cell. To verify this, we used the flip flops and latch of a already characterized library in our .lib and checked for synthesis, still the library was unable to pick up any of the sequential cell.

CHAPTER -7
CONCLUSION AND FUTURE SCOPE

This report has seen different aspects of the subthreshold library, like how its gates are useful in low-power applications. At an operating voltage of 0.4 V, we saw a significant dip in dynamic power consumption. In this project, we designed basic gates like AND, NAND, NOR, XOR, etc., along with complex gates like OAIs and AOIs, then we designed sequential elements for our library, i.e., flip-flops. At last, we designed clock inverters and clock buffers to complete our library with 36 cells. For each gate, we have also characterized them for different drive strengths like X2, X4, X10, etc. For each gate, we characterized it based on its propagation delays, dynamic and leakage powers, and transition time. We took all the values for every parameter of gates and merged them in a single file with .lib format using python scripting. At last, we synthesized our generated library on the Cortex-M0 processor in the cadence genus. Further we benchmarked the performance of cortex M0 at various voltages and PVT conditions. We compared with the library at 0.58V for comparison between subthreshold and near threshold region . At the initial stage, we faced difficulties in the sizing of gates for such low voltage operation, also it was quite a challenge for all of us as a team to write an effective python script to compile all data related to gates in .lib format.

In the future, we can work on the scripting part, and write more efficient code. We can also add more cells in our designed library, and add sequential gates with scan cells for design for testability purposes.

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