Course No : IC 150
Course Name: Applied Digital Logic Design
First Tierce Examination ,
Feb. 6th 2019, 8:30 AM-10 AM
Max. Marks 40

Note:

- Neat Drawing of circuits bocks is mandatory. Answers involving figures where lines, blocks etc. are strike-off will not be marked.
- The whole circuit block diagram must be drawn in one page.
- Assumptions if any regarding specifications of a design can me made; they are to be written before the starting of the answer and underlined.

Q1. [2+2+2+2+2] Number System Conversion: Illustrate all the steps

(a) Convert 101.68 in Decimal to Binary
(b) Convert 101001.1011 in Binary to Decimal
(c) Convert 110100111 in Binary to Hexa-Decimal
(d) Convert 772.453 in Octal to Decimal

Q2. [3+3+4 Marks]

(a) Compute 12 - 15 using 2's complement arithmetic, illustrating all the steps.
(b) Compute 12 - 15 using BCD arithmetic, illustrating all the steps.
(c) Explain the general logic behind working of 2's complement arithmetic.

Q4. [3+3+4 Marks]

(a) Compute 12 - 15 using X-3 (excess 3) arithmetic, illustrating all the steps.
(b) Compare the techniques: BCD versus X-3

Q4. [15 Marks]

Write a Verilog code with comments (Behavioural) to implement 2's complement 4 bit adder/ subtractor i.e., A + B or A – B. There are 3 inputs viz. (i) **A** and **B** are 4 Bit unsigned numbers and (ii) a control line **C**, which is used to choose the mode of operation i.e., +/-. The output comprises (i) **Out**, which is a 4 Bit unsigned number representing the result of the computation (ii) **Overflow** (which is a 1 Bit number) used to represent if there is overflow in the result and (iii) **Sign** (which is a 1 Bit number), if 1, represents a negative number as the result and if 0, represents a positive number as the result.

Note: DO NOT USE A Subtractor

Explain the logic of the code

Q4. [5 Marks]

Write a Verilog code with comments to implement a majority vote selector. There are 5 inputs viz. (i) **A1,A2,A3,A4,A5.** The output comprises (i) **out** (1 Bit number), which is 1, if majority of the inputs Bits are 1, else 0.

Third Tierce Examination
IC 150
1.5 Hours
Maximum Marks 40

Note: All Verilog codes MUST have detailed comments. The codes must be neatly written, without striking etc. Else, makes will be deduced for illegible writing.
ALL PARTS of a question MUST be answered in sequence.

1. **Marks [7 + 5 Marks]**
Design a Verilog code to implement a 3 Bit sequential Multiplier. The I/O specifications are in the table below.

Sr. No.	Name of the I/O	Direction	Width	Description
1	a	Input	3	Data Input (Operand 1)
2	b	Input	3	Data Input (Operand 2)
3	Start	Input	1	Start Multiplication (when 1, the shift and add operations take place at each clock edge. Also, Rst must be 0.)
4	Rst	Input	1	Reset Input (when 1, the output Op is 000000 and ready_out is 0)
5	Clk	Input	1	Clock Input
6	Op	Output	6	Multiplied Output
7	Ready_out	Output	1	After the multiplication operation is complete, its value is 1. THIS IS TO BE DISPLAYED in LED. As the multiplier is 3 Bits, Ready_out is 1 after 3 clock pulses of Rst

Now, modify the code, so that if any of the operands **(a or b)** is less than 3 Bits, then the output is ready before 3 clock cycles.

2. **Marks [5+3+5]**
Write a Verilog code for sequence checker for the input pattern "EVEN number 0s AND EVEN number of 1s" . Write a test bench for its validation. Also, draw the state machine diagram for the checker.

3. **Marks [15]**
Assume that there is a Bit 8-processor with the following major units (i) One 8 Bit Accumulator, (ii) Eight, 8 Bit General Purpose Registers and (iii) 8 Bit ALU to perform addition.

Design its instruction set for operations (i) LOAD to Accumulator form registers (ii) LOAD to Accumulator Immediate from Instruction, (iii) STORE from Accumulator to registers (iv) ADD immediate value in Instruction to Accumulator, (v) ADD value in a register to the value in Accumulator, (vi) Halt.

Write a Verilog code for this simple processor. Also, write a test bench to validate its working and explain the Test Bench.

QUIZ

3. Design a sequence checker for the input pattern "EVEN number of 0's and EVEN number of 1s". Also, draw the state machine for the design.

4. Design a Verilog code to implement a 4 Bit sequential Multiplier. The I/O specifications are in the table below.

Sr. No.	Name of the I/O	Direction	Width	Description
1	a	Input	4	Data Input (Operand 1)
2	b	Input	4	Data Input (Operand 2)
3	Start	Input	1	Start Multiplication (when 1, the shift and add operations take place at each clock edge. Also, Rst must be 0.)
4	Rst	Input	1	Reset Input (when 1, the output Op is 00000000 and ready_out is 0)
5	Clk	Input	1	Clock Input
6	Op	Output	8	Multiplied Output
7	Ready_out	Output	1	After the multiplication operation is complete, its value is 1. Since, the design is 4 bit sequential multiplier, after 4 clock edges of Start, its value will be 1

No. of zeros = 3
No. of 1's = 3

010101

4
4