Mohit Kumar
1204900

IC150: Applied Digital Logic Design

July 23, 2021
10-11:30AM

First Tierce Examination

Max Marks: 50

Notes:

1. Answer all questions. The exam is only conducted in the offline mode.
2. Write your name on the question paper as well as on the answer sheets.

Q1 (3, 3, 3, 3, 2, 2 Marks):

(a) Convert the following numbers to the given radix using successive division methods.
   (i) 'h451C to radix 10 (decimal)
   (ii) 'b101101101 to radix 16 (hexadecimal)

(b) Convert the following numbers to the given radix using multiplication methods.
   (i) 'd743 to radix 16 (hexadecimal)
   (ii) 'h12C to radix 2 (binary)

(c) Give the representation of –'d23 (minus twenty three in decimal) in binary using 6 bits and 2's complement representation.

(d) What is the value of 'b10110111 in decimal assuming 2's complement representation?

Q2 (3, 4, 8, 3 Marks):

You are given the following Verilog description.

```
module FA(input A, input B, input C_in, output S, output C_out);
   assign {C_out, S} = {1'b0, A} + B + C_in;
endmodule
module unknown(input [3:0]P, input [3:0]Q, input R, output [3:0]S,
               output T);
   wire [3:0]U;
   FA zero(.A(P[0]), .B(Q[0]), .C_in(R), .S(S[0]), .C_out(U[0])),
      one(.A(P[1]), .B(Q[1]), .C_in(U[0]), .S(S[1]), .C_out(U[1])),
      two(.A(P[2]), .B(Q[2]), .C_in(U[1]), .S(S[2]), .C_out(U[2])),
      three(.A(P[3]), .B(Q[3]), .C_in(U[2]), .S(S[3]), .C_out(U[3]));
  assign T = U[3];
endmodule
```

1. What does this module **unknown** implement?
2. Draw the schematic of the circuit that is represented by this module **unknown**.

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3. Write a Verilog test bench that provides the following inputs to the module **unknown** in sequence with 2 time unit delays between each step. The test bench should display the time of simulation and the S and T outputs of module **unknown** along with input P, Q and R.

   P = 'd4, Q = 'd7, R = 'd0
   P = 'd3, Q = 'd9, R = 'd1
   P = 'HD, Q = 'H7, R = 'd0
   P = 'H2, Q = 'HA, R = 'd1
   P = 'd9, Q = 'HB, R = 'd1

4. Provide the output of your test bench.

Q3 (16 marks):

Write a Verilog code that takes a signal Clk of frequency f as input and generates two outputs C1 and C2 with the following specifications. (See the waveform below for more clarity).

C1 is high for two cycles of Clk and low for three cycles of Clk. The frequency of signal C1 is $f/5$.

C2 is high for one cycle of Clk, then low for four cycles of Clk, then high for two cycles of Clk and then low for three cycles of Clk. The frequency of signal C2 is $f/10$.

Hint: Use a counter and decode the count values for generating C1 and C2.