

LIC: LECTURE

Static and Dynamic Op Amp Limitations

- DYNAMIC OP-AMP LIMITATIONS: INTRODUCTION
 - (i) Open Loop Response
 - (ii) Single Pole Open-loop Gain
 - (iii) Transient Response
 - (a) Rise Time
 - (b) Slew Rate- Definition and Limitations

DYNAMIC OP-AMP LIMITATIONS

- Till now, we have assumed op-amps with extremely high open-loop gains, regardless of frequency.
- A practical op amp provides high gain only from dc up to a given frequency, beyond which gain decreases with frequency and the **output is also delayed with respect to the input**.
- These limitations have a profound impact on the closed-loop characteristics of a circuit: they **affect both its frequency and transient responses**, and also its input and output impedances.

DYNAMIC OP-AMP LIMITATIONS

OPEN LOOP RESPONSE

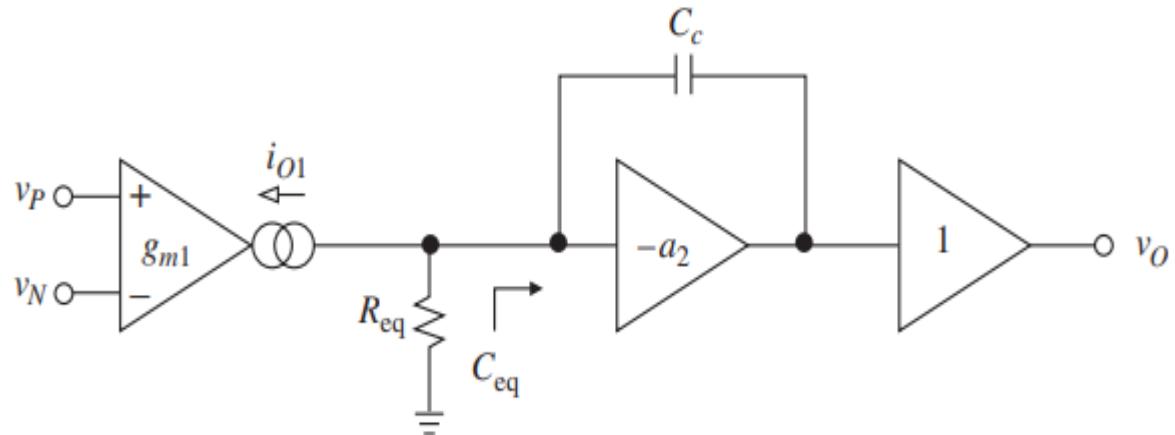
- The most common open-loop response is the dominant-pole response.
- As, its frequency profile is primarily controlled by a single pole.
- At low frequencies, where C_c acts as an open circuit:

$$V_0 = 1 \times -a_2 \times (-Req \cdot i_{o1})$$

$$V_0 = g_{m1} R_{eq} a_2 \times (V_p - V_n)$$

- The low-frequency gain, called the dc gain and denoted as a_0 ,

$$a_0 = g_{m1} R_{eq} a_2$$



Simplified Op-Amp Block diagram

gm1=transconductance gain of the first stage

-a2=voltage gain of the second stage (inverting stage)

Req, Ceq= Net equivalent resistance and capacitance between the node common to the first and second stage, and ground.

DYNAMIC OP-AMP LIMITATIONS

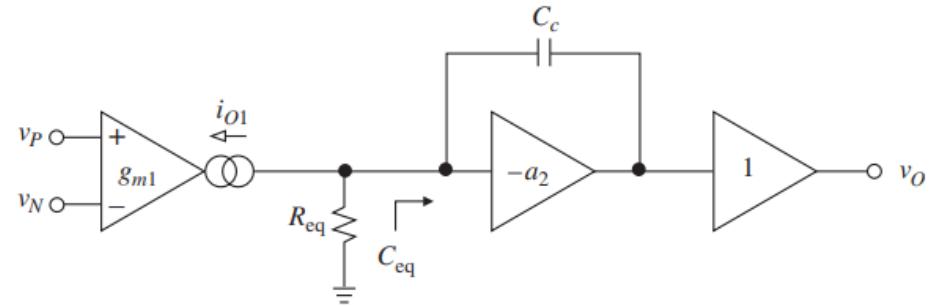
OPEN LOOP RESPONSE

- Increasing the operating frequency will bring the impedance of C_{eq} into the circuit, causing gain to roll off with frequency because of the LPF action provided by R_{eq} and C_{eq} .
- Gain starts to roll off at the frequency f_b that makes:

$$|Z_{Ceq}| = R_{eq} \quad \text{or} \quad R_{eq} = \frac{1}{2\pi f_b C_{eq}}$$

$$f_b = \frac{1}{2\pi R_{eq} C_{eq}}$$

This frequency (f_b), is called as dominant-pole frequency.



Simplified Op-Amp Block diagram

gm1=transconductance gain of the first stage

-a2=voltage gain of the second stage (inverting stage)

Req, Ceq= Net equivalent resistance and capacitance between the node common to the first and second stage, and ground.

DYNAMIC OP-AMP LIMITATIONS

Single Pole Open Loop gain

- Assume that the open-loop gain $a(s)$ possesses just a single pole; this, both to facilitate our mathematical manipulation and to help us develop a basic feel for the effect of the gain roll-off on the closed-loop parameters. Gain can be written as:

$$a(s) = \frac{a_0}{1 + s/w_b}$$

Where, S is the complex frequency

a_0 =Open loop DC gain

w_b = s-plane pole location

or

In terms of frequency:

$$a(if) = \frac{a_0}{1 + if/f_b}$$

where j is the imaginary unit ($j^2 = -1$), and $f_b = \omega_b/(2\pi)$ is the *open-loop -3-dB frequency*, also called the *open-loop bandwidth*. We calculate gain magnitude and phase as

$$|a(jf)| = \text{mag } a(jf) = \frac{a_0}{\sqrt{1 + (f/f_b)^2}}$$

$$\angle a(jf) = \text{ph } a(jf) = -\tan^{-1}(f/f_b)$$

DYNAMIC OP-AMP LIMITATIONS

Single Pole Open Loop gain

- The gain is high and approximately constant only from dc up to f_b . Past f_b it rolls off at the rate of -20 dB/dec , until it drops to 0 dB (or 1 V/V) at $f=f_t$.
- This frequency f_t** is called the **unity-gain frequency**, or also the transition frequency.
- Because it marks the transition from amplification (positive decibels) to attenuation (negative decibels).

$$1 = \frac{a_0}{\sqrt{1 + (f_t/f_b)^2}} \quad \text{and } f_t \gg f_b$$

$$1 = \frac{a_0}{f_t/f_b} \quad \text{We get, } f_t = a_0 f_b$$

- Over the frequency region $f \gg f_b$ the op amp behaves as an integrator, and that its gain-bandwidth product, defined as $\text{GBP} = |a(jf)| \times f$, is constant.

So, $\text{GBP} = f_t \quad \text{For; } f \gg f_b$

- For this reason, op amps with dominant-pole compensation are also referred to as constant-GBP op amps.
- Increasing (or decreasing) f by a given amount in the region of integrator behavior will decrease (or increase) $|a|$ by the same amount.**

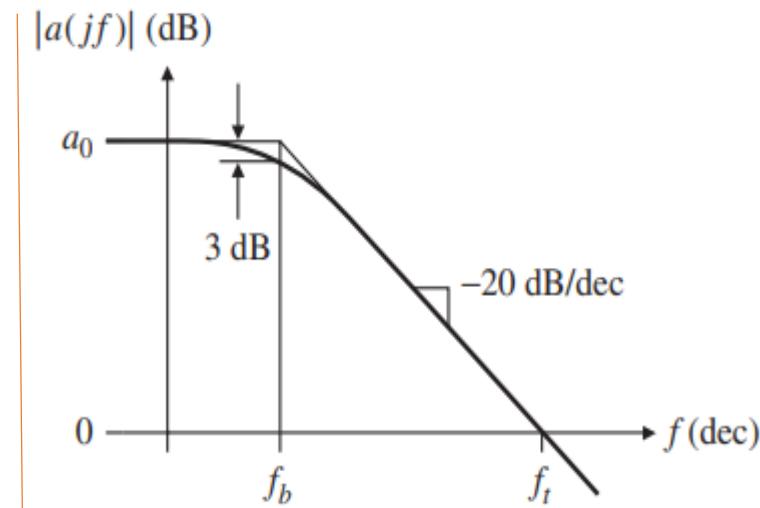


Fig. Single-pole open-loop gain

TRANSIENT RESPONSE

- That is, the response to an input step as a function of time.
- This response, like its frequency domain counterpart, varies with the amount of feedback applied.

Calculation of Rise Time t_R : Small signal B.W. of voltage follower is f_t . The freq. response can be written as:

$$A(jt) = \frac{1}{1 + jf/f_t}$$

Where, $S = -2\pi f t$ (pole)

- Subjecting the voltage follower of Fig. to an input voltage step of sufficiently small amplitude V_m will result in the well-known exponential response

$$V_0(t) = V_m(1 - e^{-t/\tau})$$

$$\text{where, } \tau = \frac{1}{2\pi f_t}$$

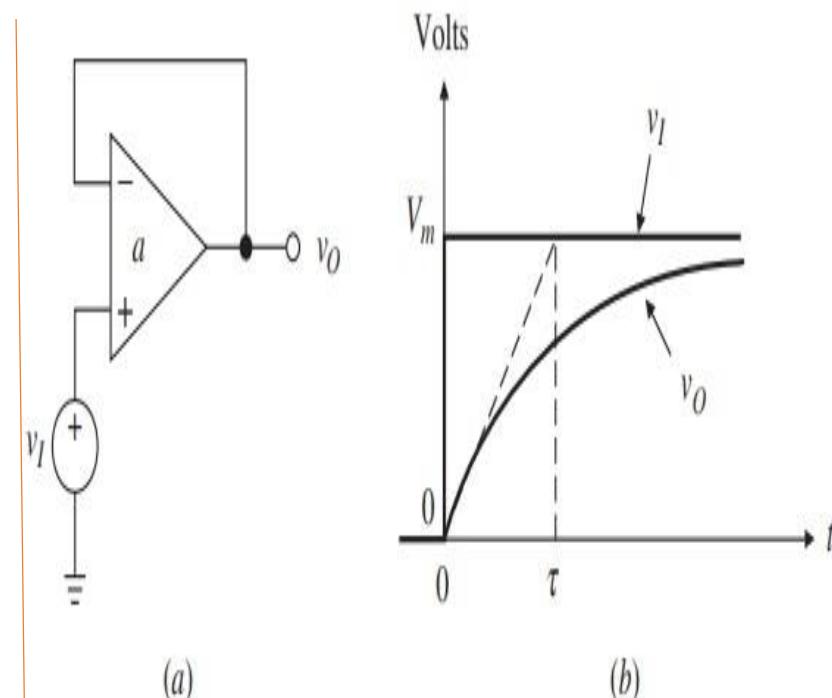
- The time t_R it takes for ' V_0 ' to swing from 10% to 90% of ' V_m ' is called the rise time.

- It provides an indication of how rapid the exponential swing is. So,

$$t_R = \tau(\ln 0.9 - \ln 0.1), \text{ or}$$

$$t_R = \frac{0.35}{f_t}$$

- This provides a link between the frequency-domain parameter f_t and the time domain parameter t_R .**

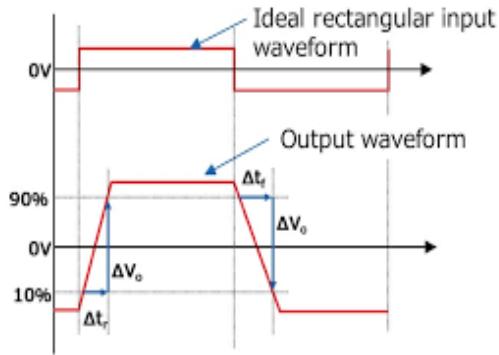


FIGURE

Voltage follower and its small-signal step response.

TRANSIENT RESPONSE

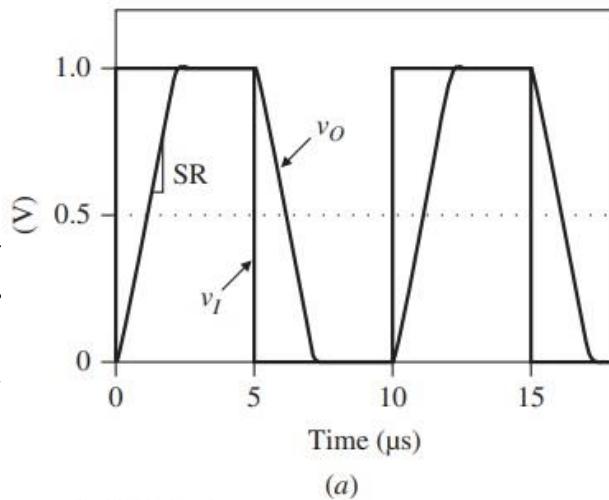
Calculation of Slew Rate ($SR = \Delta V / \Delta t$): Max. rate of change of an op-amps output per unit time (change of voltage or current per unit time)



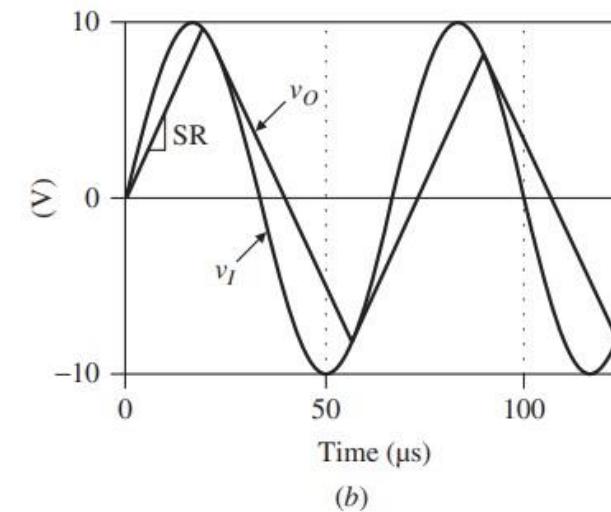
SLEW RATE LIMITATIONS: The rate at which V_o changes with time is highest at the beginning of the exponential transition.

$$V_o(t) = V_m(1 - e^{-t/\tau}) \quad \frac{dV_o}{dt} = \frac{V_m}{\tau} \quad (\text{at } t=0)$$

- If we increase V_m , the rate at which the output slews will have to increase accordingly in order to complete the 10%-to-90% transition within the time t_R .
- In practice it is observed that above a certain step amplitude the output slope saturates at a constant value called the slew rate (SR). The output waveform, rather than an exponential curve, is now a ramp.
- **SR** is a nonlinear large-signal parameter, while t_R is a linear small signal parameter.



(a)



(b)

FIGURE
Slew-rate limited responses of the 741 follower (a) a pulse and (b) a sinusoid.

- The output-step magnitude corresponding to the onset of slew-rate limiting is such that $V_{om(\text{crit})}/\tau = SR$.

$$V_{om(\text{crit})} = \frac{SR}{2\pi f_t}$$

LIC: LECTURE NON LINEAR CIRCUITS

- Non Linear Circuits: Introduction
- Voltage Comparators
 - (a) Introduction
 - (b) Threshold Detector
 - (c) General Purpose IC Comparators
 - (d) Comparator Applications
 - (a) Level Detector
 - (b) On-off Control
 - (c) Window Detector
 - (d) Pulse Width Detector

LINEAR VS NONLINEAR CIRCUIT

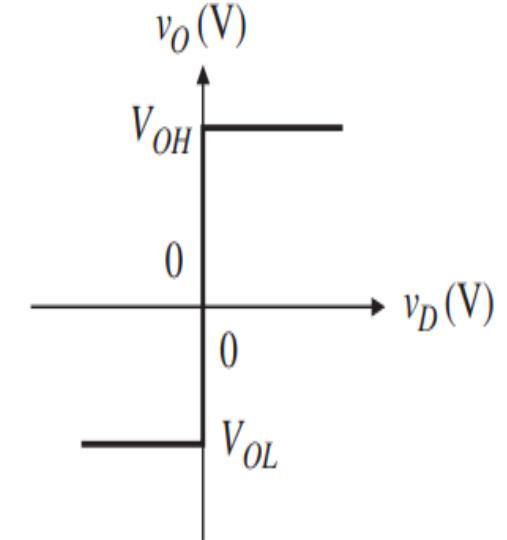
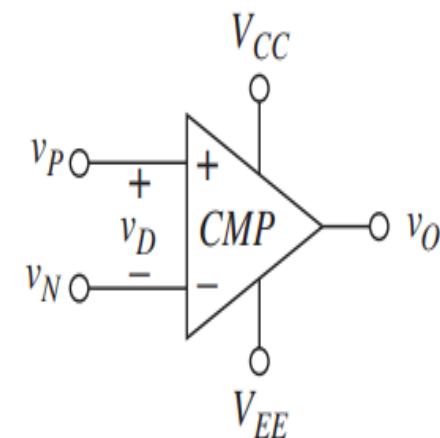
- Linearity in **LINEAR CIRCUITS** is achieved by
 - (a) *Using negative feedback* to force the op amp to operate within its linear region
 - (b) *Implementing the feedback network with linear elements.*
- **NON LINEARITY** is obtained by:
 - Using a high-gain amplifier with positive feedback, or even with no feedback at all, causes the device to operate primarily in saturation.
 - This biastable behavior is highly non-linear and forms the basis of *Voltage Comparators and Schmitt trigger.*
 - Implementing the feedback network with Nonlinear elements, such as diodes and analog switches.
 - This originates the discussion of *Precision Rectifier, Peak Detector, Sample & Hold Circuits.*

VOLTAGE COMPARATOR

- The function of a voltage comparator is to compare the voltage V_P at one of its inputs against the voltage V_N at the other, and output either a low voltage V_{OL} or a high voltage V_{OH} .
- V_P and V_N are analog variables because they can assume a continuum of values.
- V_O is a binary variable because it can assume only one of two values, V_{OL} or V_{OH} .
- It is fair to view the comparator as a one-bit analog-to-digital converter.
- At the origin, the curve is a vertical segment, indicating an infinite gain there, or $V_O/V_D = \infty$. Away from the origin, the VTC consists of two horizontal lines positioned at $V_O=V_{OL}$ and $V_O=V_{OH}$.

$$v_O = V_{OL} \quad \text{for } v_P < v_N$$

$$v_O = V_{OH} \quad \text{for } v_P > v_N$$



"VTC-Non-Linear"

$V_O = V_{OL}$ for $V_D < 0$ V, and
 $V_O = V_{OH}$ for $V_D > 0$ V

VOLTAGE COMPARATOR

- In high-speed applications it is of interest to know how rapidly a comparator responds as the input state changes from $VP < VN$ to $VP > VN$, and vice versa. Comparator speed is characterized in terms of the response time, also called the propagation delay t_{PD} .
- Response Time or Propagation Delay (t_{PD}) is defined as the time it takes for the output to accomplish its 50% of its transition in response to a predetermined voltage step at the input.
- Though the input step magnitude is typically on the order of 100 mV, its limits are chosen to barely exceed the level required to cause the output to switch states. This excess voltage is called the input overdrive V_{od} .

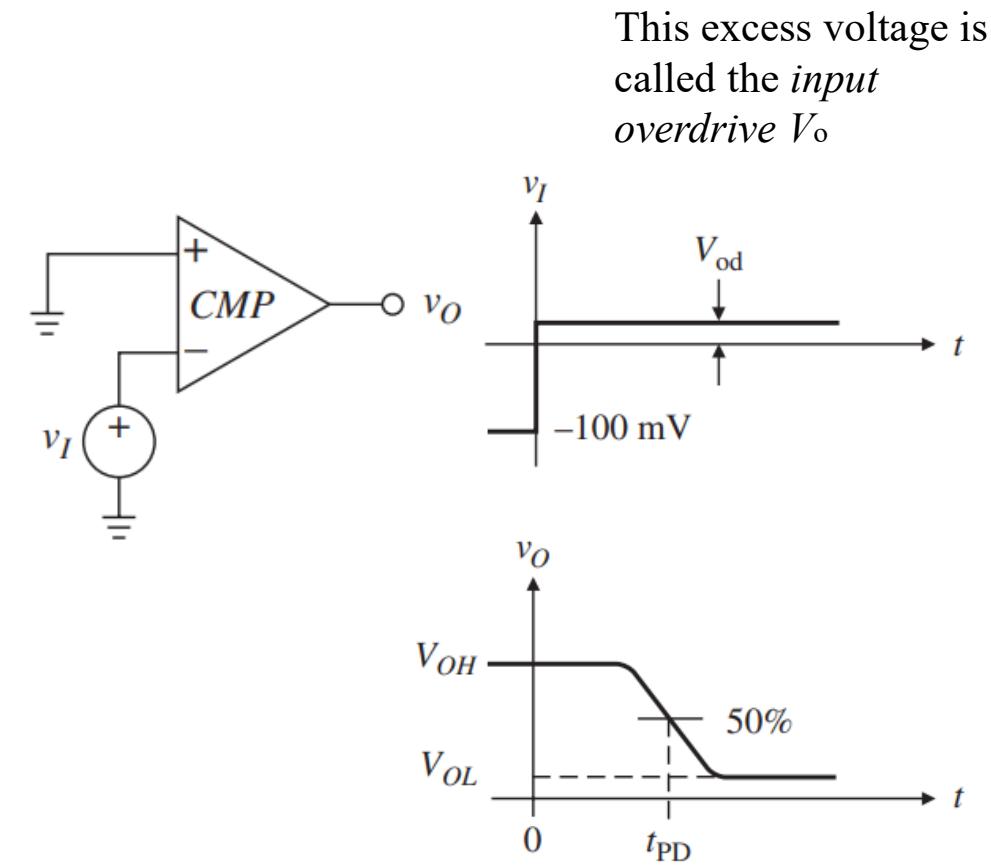
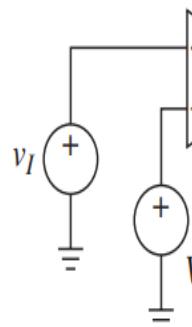


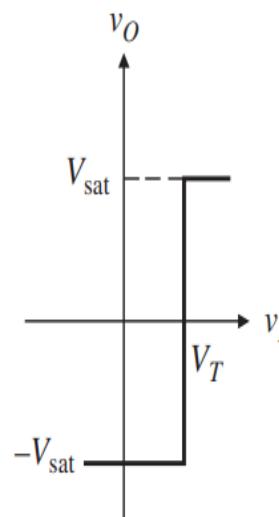
Fig. The response time of a comparator

Threshold Detector

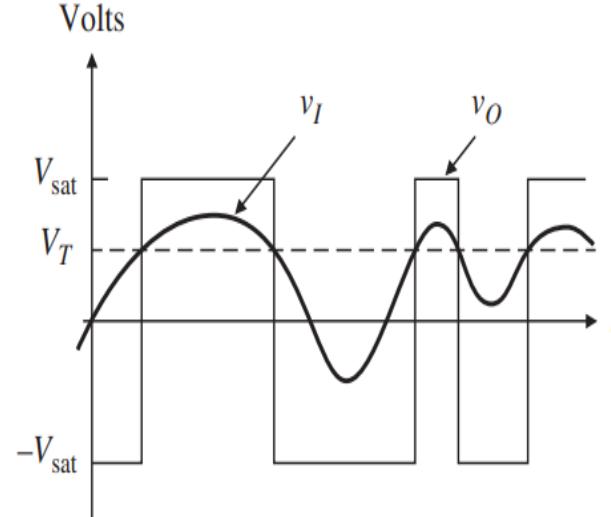
- Since V_O goes high whenever V_I rises above V_T , the circuit is aptly called a *threshold detector*. If $V_T = 0$ V, the circuit is referred to as a *zero-crossing detector*.
- It is important to realize that when used as a comparator, the op amp has no control over V_N due to the absence of feedback. The amplifier now operates in the open-loop mode and, because of its extremely high gain, it spends most of its time in saturation.
- Though the output transitions in *Fig. c* have been shown as instantaneous, we know that in practice they take some time due to slew-rate limiting.
- For 741 op amp, the time to accomplish 50% of the output transition would have been $t_R = V_{sat}/SR = (13\text{ V})/(0.5\text{ V}/\mu\text{s}) = 26\text{ }\mu\text{s}$, an intolerably long time in many applications.



(a)



(b)



(c)

$v_I < V_T \quad v_O = -V_{sat} \cong -13\text{ V}$.

$v_I > V_T \quad v_O = +V_{sat} \cong +13\text{ V}$.

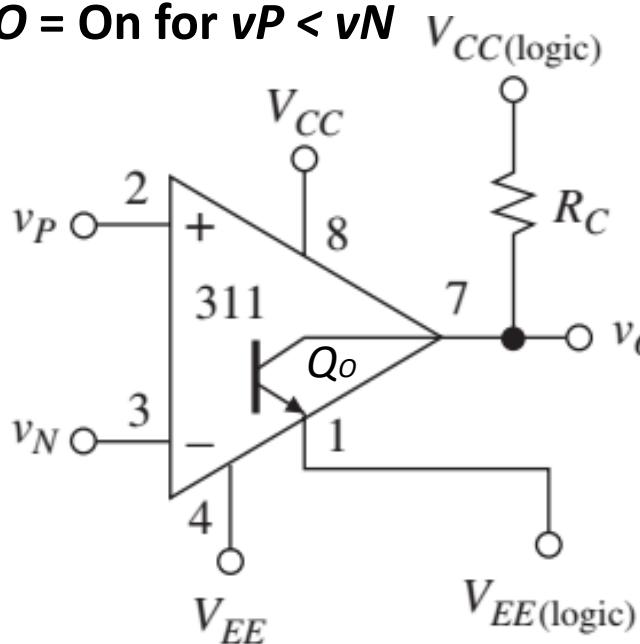
$V_T = 0\text{ V}$ zero-crossing detector.

General-Purpose IC Comparators- LM311

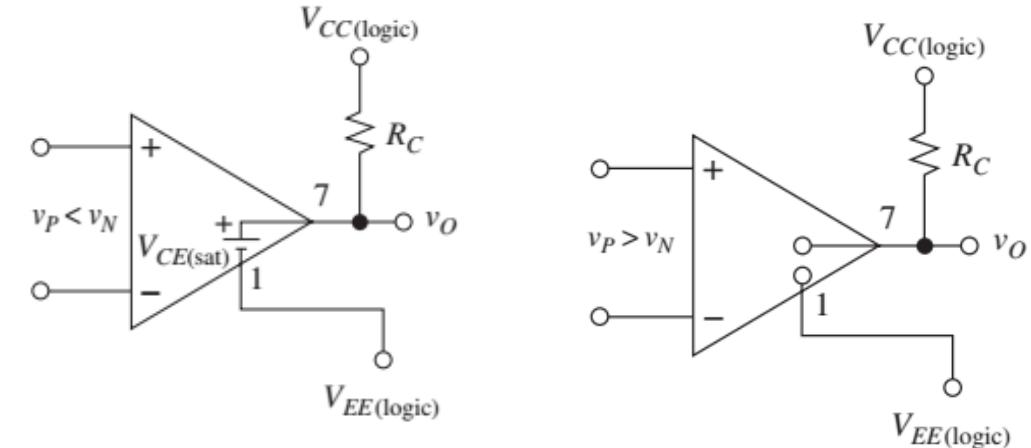
- The most popular voltage comparators is the LM311.
- Circuit operation is such that for $v_P < v_N$, QO is in heavy conduction; for $v_P > v_N$, the base drive is removed and QO is thus in cutoff.

$QO = \text{Off for } v_P > v_N$

$QO = \text{On for } v_P < v_N$



Biasing the LM311 output stage
with a pullup resistance R_C



Equivalent circuits for the
(a) "output low" and (b) "output high" states

- For $v_P < v_N$, QO saturates and is thus modeled with a source $V_{CE}(\text{sat})$. So, $v_O = V_{EE}(\text{logic}) + V_{CE}(\text{sat})$. Typically $V_{CE}(\text{sat}) \sim = 0.1 \text{ V}$.
- For $v_P > v_N$, QO is in cutoff and is modeled with an open circuit as in (b) by the pullup action of R_C .

$$v_O = V_{OL} \cong V_{EE}(\text{logic}) \quad \text{for } v_P < v_N$$

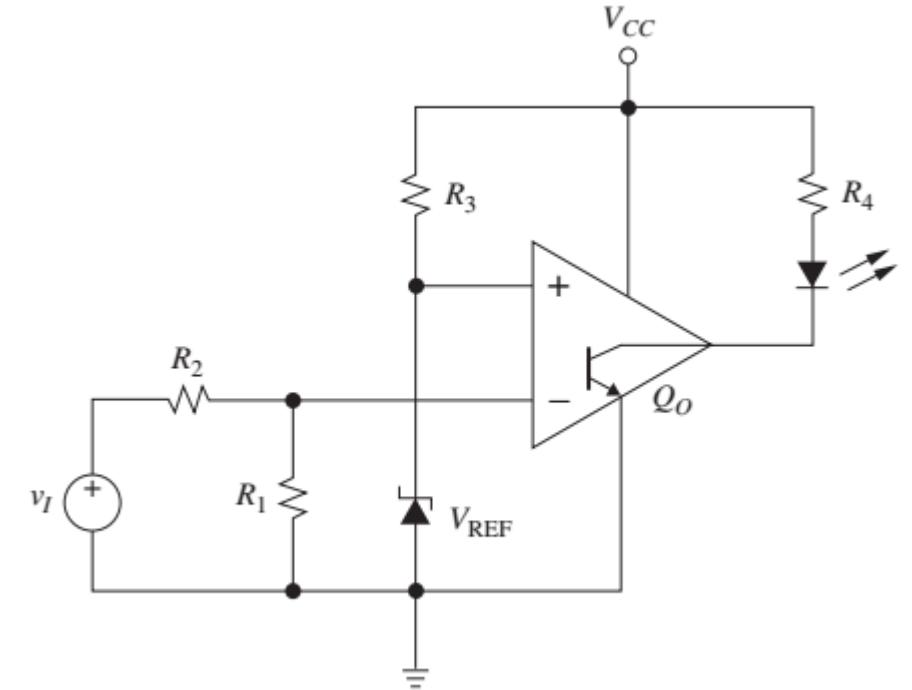
$$v_O = V_{OH} \cong V_{CC(\text{logic})} \quad \text{for } v_P > v_N$$

COMPARATOR APPLICATIONS

- Comparators are used in various phases of signal generation and transmission, as well as in automatic control and measurement.
- They appear both alone or as part of systems, such as A-D converters, switching regulators, function generators, V-F converters, power-supply supervisors, and a variety of others.
- - (a) Level Detector
 - (b) On-off Control
 - (c) Window Detector
 - (d) Pulse Width Detector

Level Detectors

- To monitor a physical variable that can be expressed in terms of a voltage, and signal whenever the variable rises above (or drops below) a prescribed value called the *set value*.
- The detector output is then used to undertake a specific action as demanded by the application.
- Eg: The activation of a warning indicator, such as a light-emitting diode (LED) or a buzzer, the turning on of a motor or heater, or the generation of an interrupt to a microprocessor.
 - The basic components of a level detector are:
 - (a) a voltage reference V_{REF} to establish a stable threshold,
 - (b) a voltage divider R_1 and R_2 to scale the input v_I
 - (c) a comparator.



Basic level detector with optical indicator

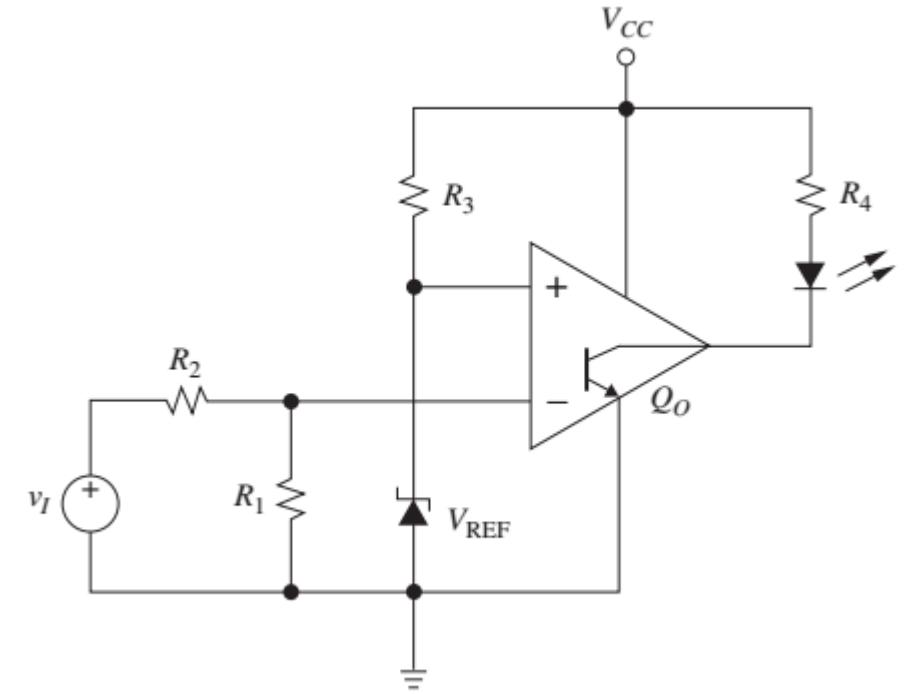
Level Detectors and On-Off Control

For, $V_{REF} = [R_1/(R_1 + R_2)] \times V_I$; the output trips

Assuming, the special value of $V_I = V_T$

$$V_T = (1 + R_2/R_1)V_{REF}$$

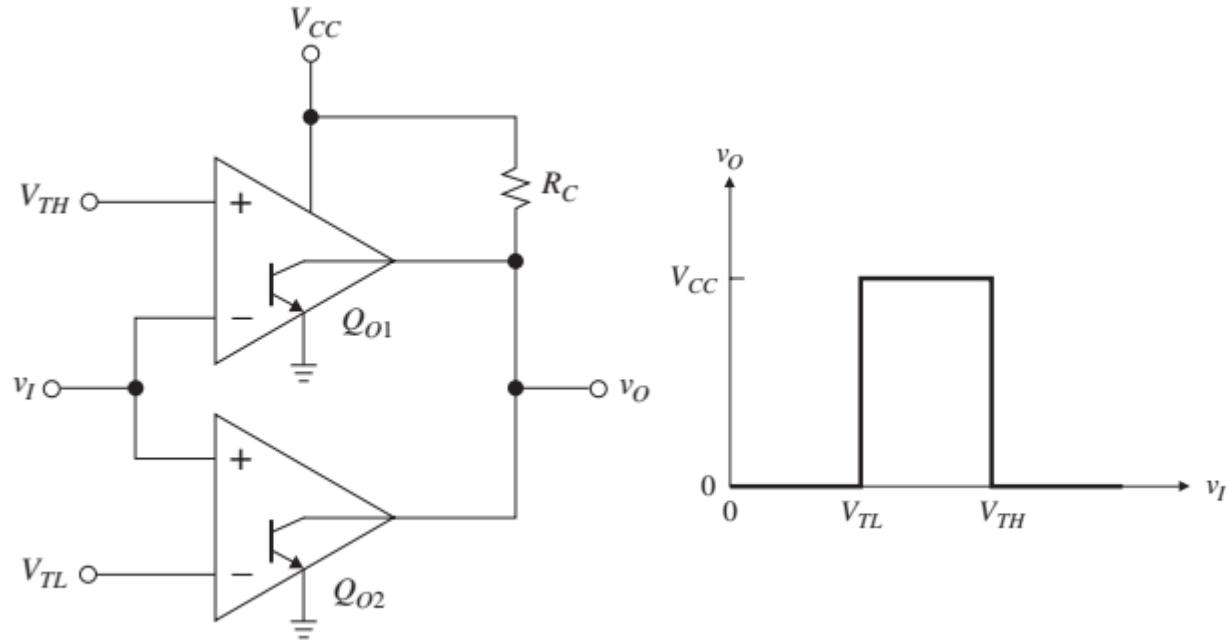
- For; $V_I < V_T$, Q_O is off: LED is off.
- For; $V_I > V_T$, Q_O is saturated: LED glows.; It indicates that V_I rises above V_T .
- *Interchanging the input pins will make the LED glow whenever, V_I drops below V_T .*
- **R3 function is to bias the ref. diode and that of R4 is to set the LED current.**
- If V_I is V_{CC} itself, the circuit will monitor its own power supply and function as an overvoltage indicator.
- If the input pins are interchanged with each other so that $V_N = V_{REF}$ and $V_P = V_I / (1 + R_2/R_1)$, then we have an undervoltage indicator.



Basic level detector with optical indicator

Window Detectors

- **window comparator**, is to indicate when a given voltage falls within a specified **band, or window**.



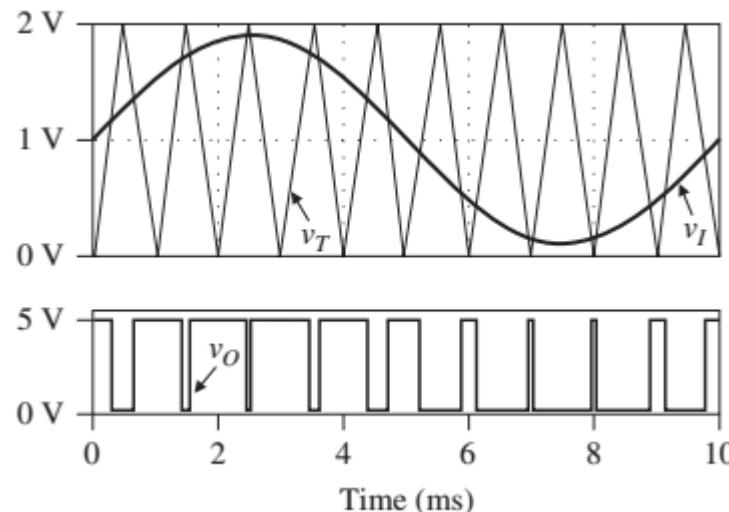
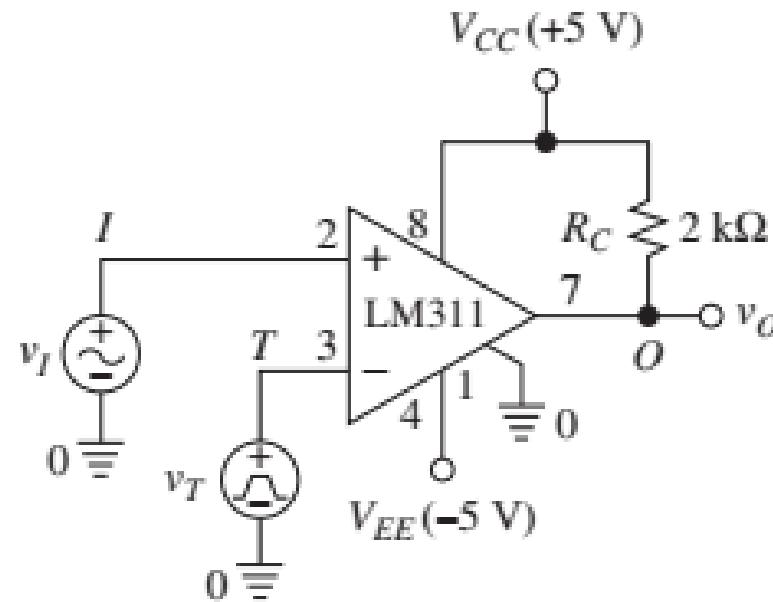
Status	Top Comparator	Bottom Comparator	Q_{O1}	$Q_{O2}^{(a)}$	V_O
$V_I < V_{TL}$	V_{OH}	V_{OL}	OFF	ON	V_{OL}
$V_{TL} < V_I < V_{TH}$	V_{OH}	V_{OH}	OFF	OFF	V_{OH}
$V_{TH} < V_I$	V_{OL}	V_{OH}	ON	OFF	V_{OL}

Pulse-Width Modulation

- If a voltage comparator is made to compare a slowly varying signal v_I against a high frequency triangular wave v_T , the outcome v_O is a square wave with the same frequency as v_T , but with its symmetry controlled by v_I

The degree of symmetry of v_O is expressed via the *duty cycle*

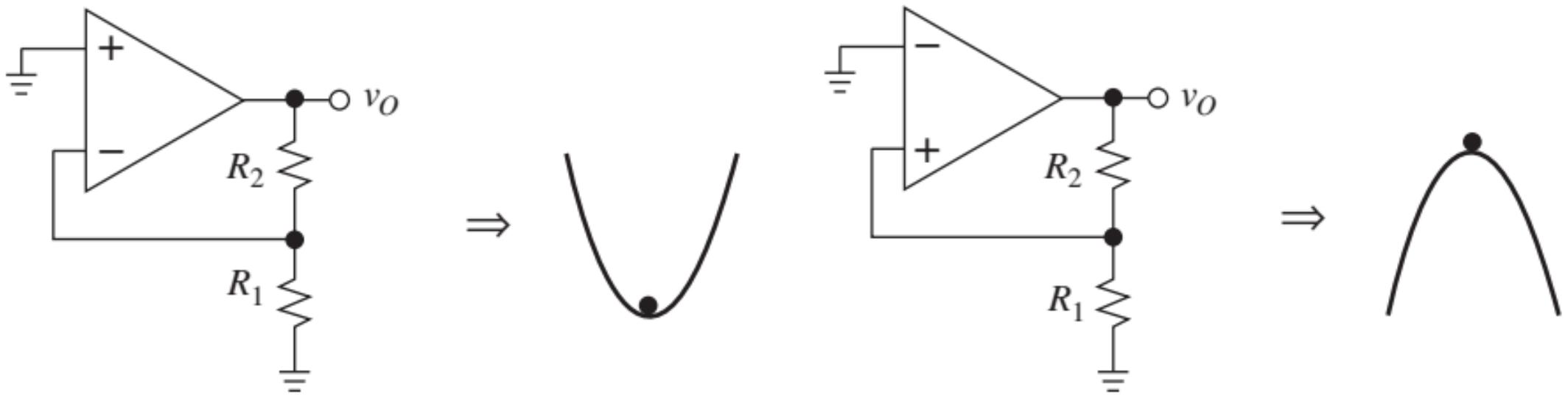
$$D(\%) = 100 \frac{T_H}{T_L + T_H}$$



LIC: LECTURE NON LINEAR CIRCUITS

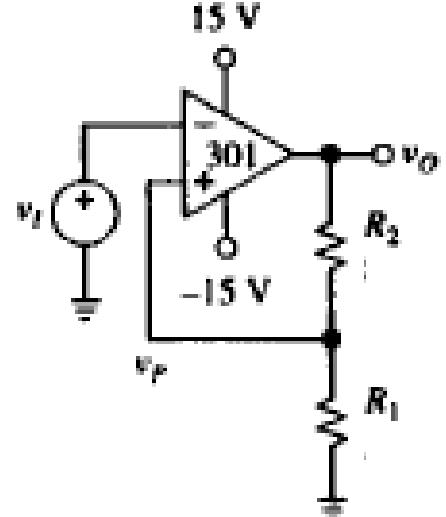
- Outcomes of Positive Feedback
- Schmitt Trigger
- Operation of different types of Schmitt Trigger
 - (a) Inverting Schmitt Trigger
 - (i) Symmetric
 - (ii) Asymmetric
 - (b) Non-Inverting Schmitt Trigger

POSITIVE FEEDBACK

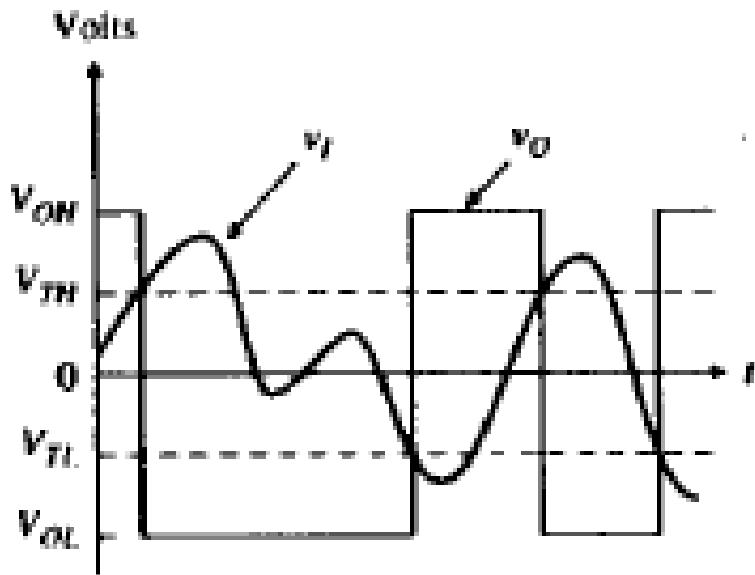


While negative feedback tends to keep the amplifier within the linear region, positive feedback forces it into saturation.

SCHMITT TRIGGER



Is a inverting Schmitt Trigger



$$V_P = \frac{R_1}{R_1 + R_2} V_0$$

$$v_I < V_P$$

$$v_O = +V_{sat} \cong +13 \text{ V}$$

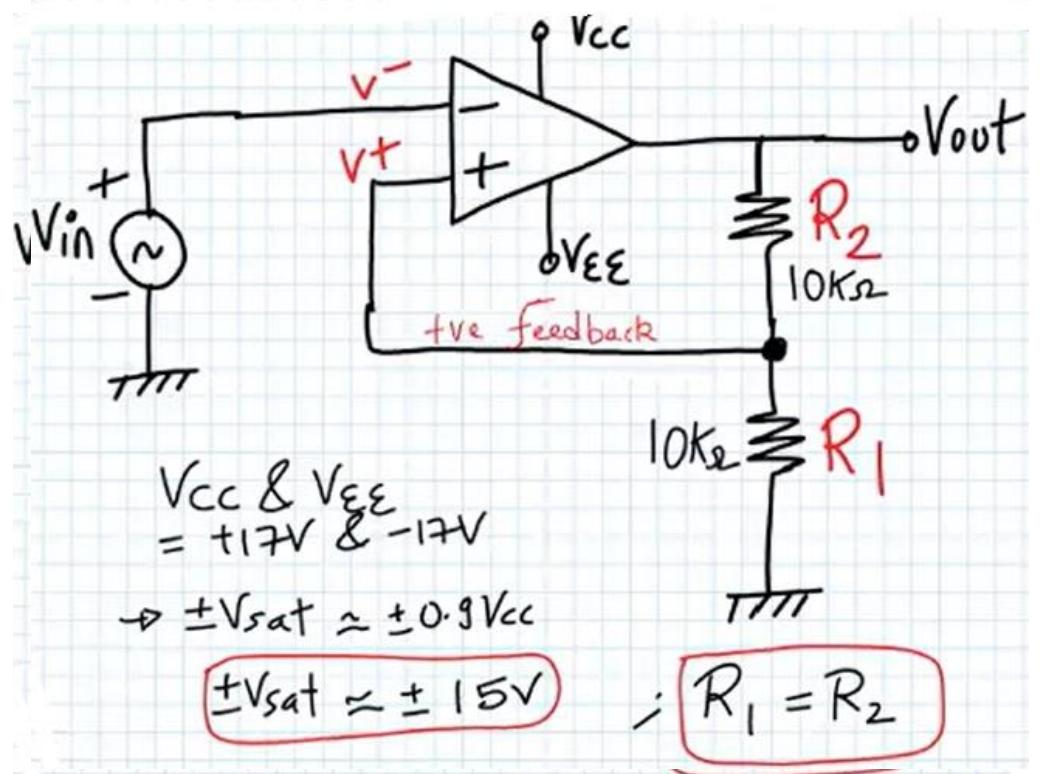
$$v_I > V_P$$

$$v_O = -V_{sat} \cong -13 \text{ V}$$

$$V_{TH} = \frac{R_1}{R_1 + R_2} V_{OH}$$

$$V_{TL} = \frac{R_1}{R_1 + R_2} V_{OL}$$

- SCHMITT TRIGGER is a logic unit circuits that uses hysteresis to apply positive feedback to the non-inverting input of a comparator or differential amplifier.
- This allows the output to retain its value until changes sufficiently to trigger a change.



③ Suppose V_{in}^o goes more & more negative

i.e. $V_{in}^o \rightarrow -1, -2, -3, -4, -5, \dots$

Will o/p state change?

NO

O/P will stay at $+15V$ (since $V^+ > V^-$)

$$\boxed{V_{out} = +V_{sat}}$$

$$\boxed{V_{out} = +15V}$$

$$7.5V \quad (-1, -2, -3, -4, -5)$$

① Assume $R_1 = R_2 = 10K\Omega$, $V_{CC} = 17V$, $V_{EE} = -17V$,
ie $\boxed{\pm V_{sat} = \pm 15V}$

② When V_{in}^o is at OR i.e. $\boxed{V^- = 0}$

Output V_{out} will be at $+V_{sat}$ ie $+15V$
($\because V^+ > V^-$)

$$\begin{aligned} V_{out} &= \frac{R_2}{R_1 + R_2} \times V_{in}^o = \left(\frac{10K}{10K + 10K} \right) \times V_{in}^o \\ V^+ &= \frac{V_{out}}{2} = \frac{+V_{sat}}{2} = \frac{15}{2} = 7.5V \end{aligned}$$

④ Suppose $V_{in}^o = 1V$ then increased to $2V, 3V, 4V, 5V, 6V, 7V$

Will o/p state change

NO

O/P will stay at $+15V$ ($V^+ > V^-$)

$$\boxed{V_{out} = +V_{sat}}$$

$$\boxed{V_{out} = +15V}$$

$$7.5V \quad 1, 2, 3, 4, 5, 6 \& 7V$$

Suppose $V_{in} = 7.4V$; $V^+ \rightarrow 7.5V$ & $V^- = 7.4V$

Will o/p state change

NO

Op will stay at +15V ($V^+ > V^-$) ; $V_{out} = A_{OL}(V^+ - V^-)$

$$\begin{aligned} V_{out} &= +V_{sat} \\ V_{out} &= +15V \end{aligned}$$

A_{OL} : Open loop gain of opamp

$$V_{out} = 2 \times 10^5 (7.5 - 7.4)$$

$$V_{out} = (2 \times 10^5 \times 0.1)$$

HUGE No.

⑥ Suppose $V_{in} = 7.6V$; $V^+ = 7.5V$ & $V^- = 7.6V$

Will o/p state change

YES

Op switches state & becomes -15V ($V^+ < V^-$)

$$\begin{aligned} V_{out} &= -V_{sat} \\ V_{out} &= -15V \end{aligned}$$

$$\begin{aligned} V_{out} &= 2 \times 10^5 (7.5 - 7.6) \\ V_{out} &= -2 \times 10^5 \times 0.1 \end{aligned}$$

HUGE No.

⑦ The moment o/p goes to -15V

$$\begin{aligned} V_{out} &= -15V \rightarrow V^+ = \frac{V_{out}}{2} = -7.5V \\ \text{i.e. } V^+ &= -7.5V \text{ now} \end{aligned}$$

Suppose V_{in} becomes to drop 7.5V, 5V, 1V, 0V & then V_{in} goes -ve -1, -3, -5, -7V

Will o/p state change?

NO

Op will stay at -15V ($V^+ < V^-$)

$$\begin{aligned} V_{out} &= -V_{sat} \\ V_{out} &= -15V \end{aligned}$$

$$\begin{aligned} -7.5V &\\ 7.5V, 5V, 3V, 1V, 0V, -1V, -3V, \\ -5V, -7V & \end{aligned}$$

Suppose V_{in} becomes -7.6V

Will o/p state change

YES

Op switches to +15V since ($V^+ > V^-$)

$$\begin{aligned} \therefore V_{out} &= +V_{sat} \\ V_{out} &= +15V \end{aligned}$$

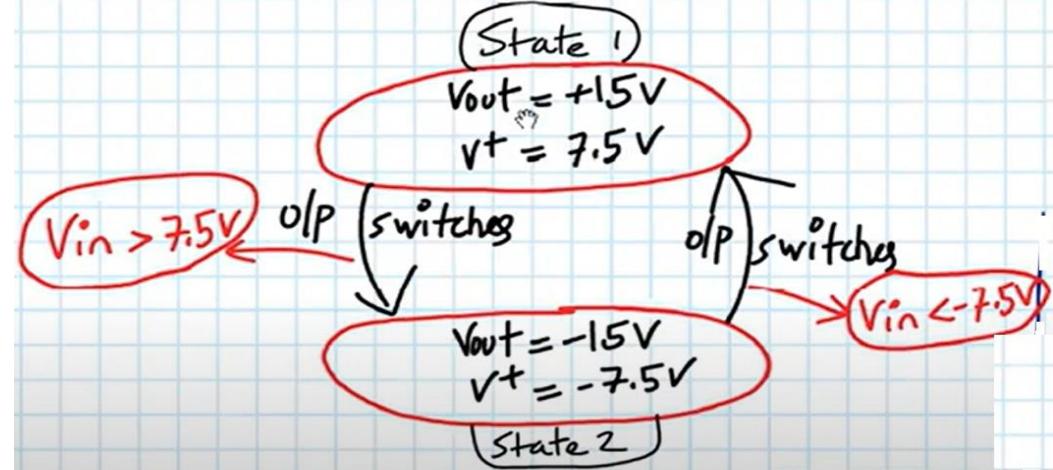
$$\begin{aligned} V_{out} &= 2 \times 10^5 (V^+ - V^-) \\ &= 2 \times 10^5 \times (-7.5 - (-7.6)) \\ V_{out} &= +2 \times 10^5 \times 0.1 \end{aligned}$$

HUGE No.

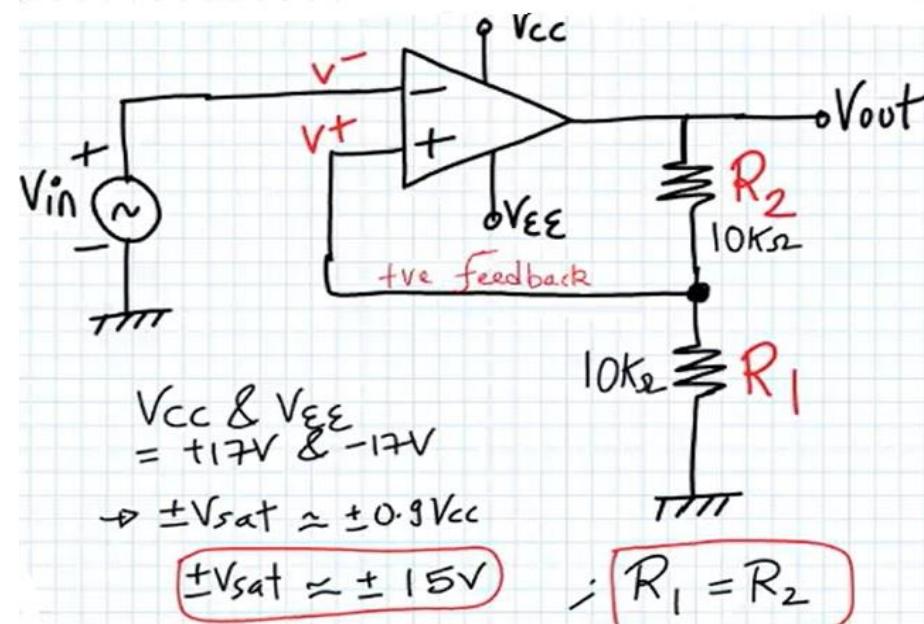
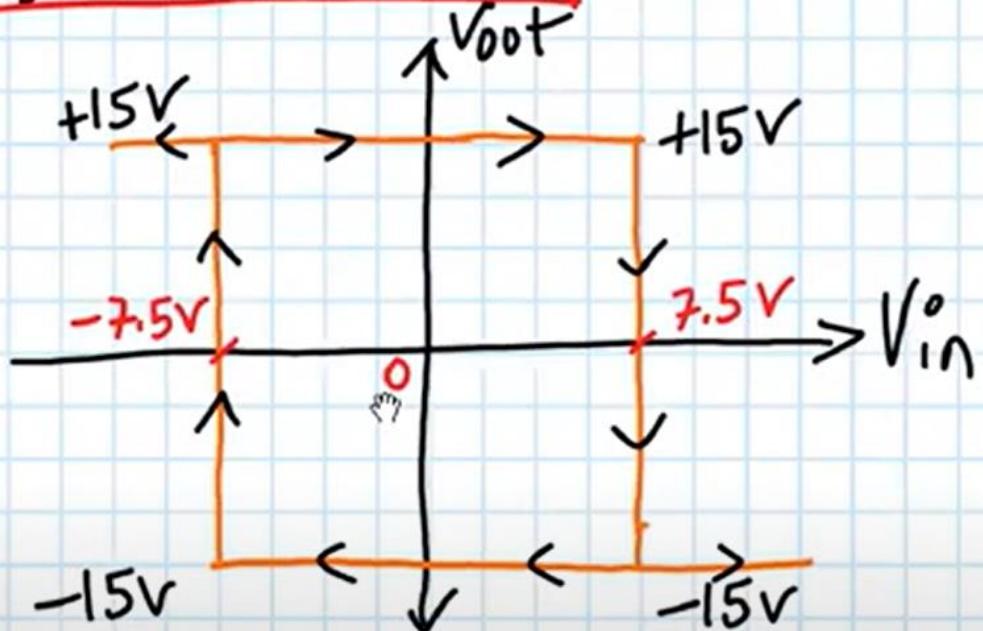
The moment o/p goes to +15V

$$V^+ = \frac{V_{out}}{2} = +7.5V \text{ i.e. } V^+ = +7.5V \text{ now}$$

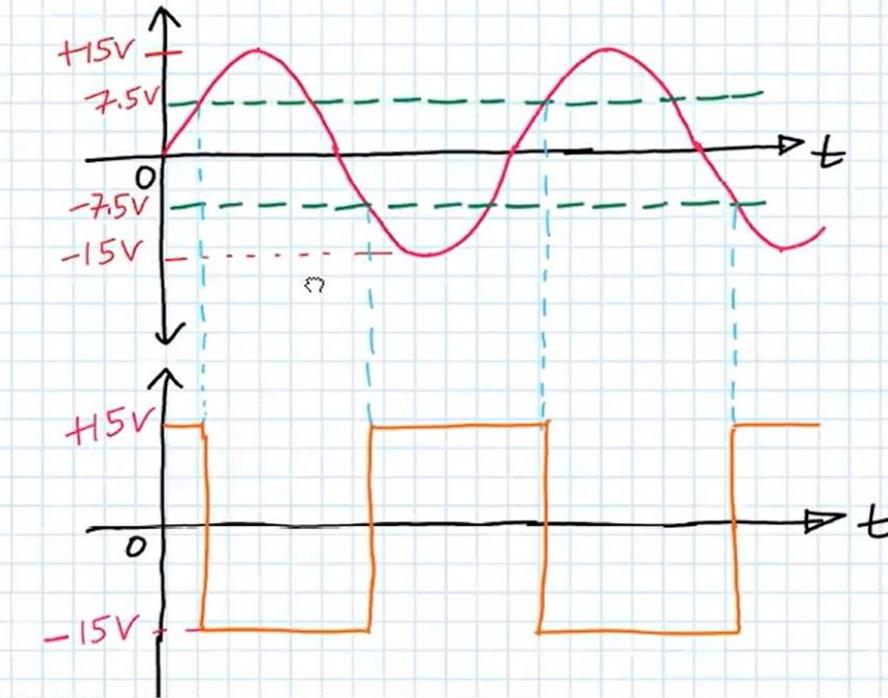
let's draw Memory / State diagram:-



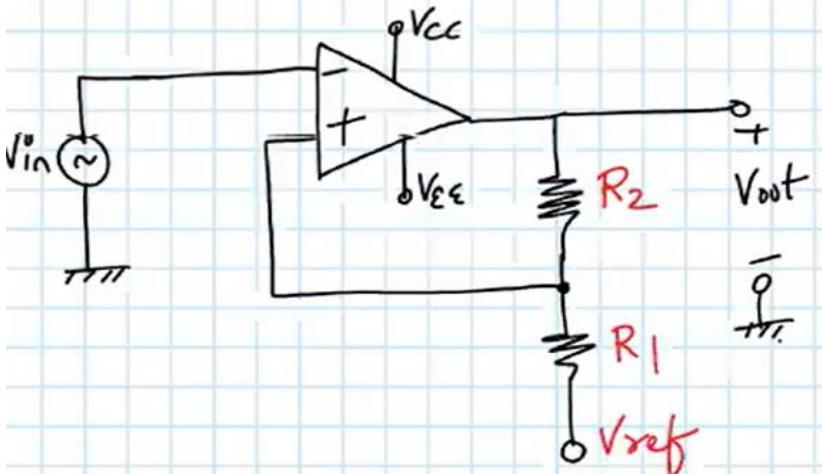
Hysteresis Concept:



* I/P - o/p waveforms w.r.t time for Inverting Schmitt Trigg

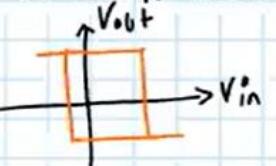


* Important Note:- (Inverting Schmitt trigger with Asymmetric Hysteresis :-)

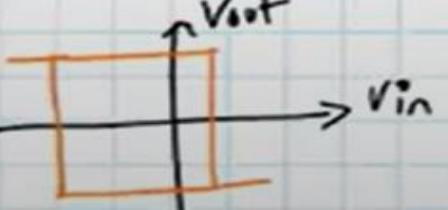


→ By adding external reference voltage V_{ref} , we can shift the hysteresis curve to the right or left.

a) +ve V_{ref} → will shift hysteresis curve to the right



-ve V_{ref} → will shift hysteresis curve to the left



Hysteresis voltage V_H for inverting Schmitt trigger is given by,

$$V_H = V_{UTP} - V_{LTP}$$

$$V_H = 2 \left(\frac{R_1}{R_1 + R_2} \right) V_{sat}$$

Center voltage of hysteresis is given by

$$V_{ctr} = \frac{V_{UTP} + V_{LTP}}{2}$$

Design Problems

* Design an inverting Schmitt trigger with the following specifications:-

Supply voltages is $\pm 12V$, $V_{UTP} = +5V$, $V_{LTP} = -5V$

* Design an Inverting Schmitt trigger whose upper threshold point is at $+4V$ & lower threshold point is at $-2V$. Opamp is powered with $\pm 11V$ supply.

* Design an Inverting Schmitt trigger whose upper threshold point is at +4V & lower threshold point is at -2V. Opamp is powered with $\pm 11V$ supply.

Solution:-

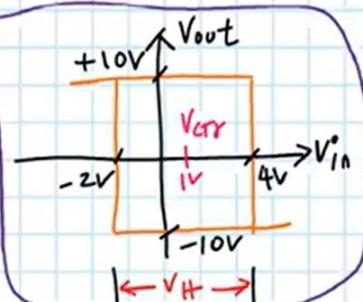
Given :- $V_{UTP} = +4V$, $V_{LTP} = -2V$

Assume : $\pm V_{sat} = 0.9 \times \pm V_{cc} \approx 0.9 \times 11$

i.e $\boxed{\pm V_{sat} \approx \pm 10V}$

Hysteresis voltage V_H for inverting Schmitt

Our Goal is to obtain



$$\frac{R_1}{R_1+R_2} = \frac{6}{20}$$

$$\text{i.e } 3R_1 + 3R_2 = R_1 \times 10$$

$$\text{i.e } 3R_2 = 7R_1$$

$$R_2 = \frac{7}{3} R_1$$

let $\boxed{R_1 = 10\text{ k}\Omega (\text{std})}$

$$\therefore R_2 = \frac{7}{3} \times 10\text{ k}\Omega = \underline{23.33\text{ k}\Omega}$$

Let $\boxed{R_2 = 24\text{ k}\Omega (\text{std})}$

Hysteresis voltage V_H for inverting Schmitt trigger is given by,

$$V_H = V_{UTP} - V_{LTP}$$

$$= 4 - (-2)$$

$$\boxed{V_H = 6V}$$

$$\text{Also, } V_H = 2 \left(\frac{R_1}{R_1+R_2} \right) V_{sat}$$

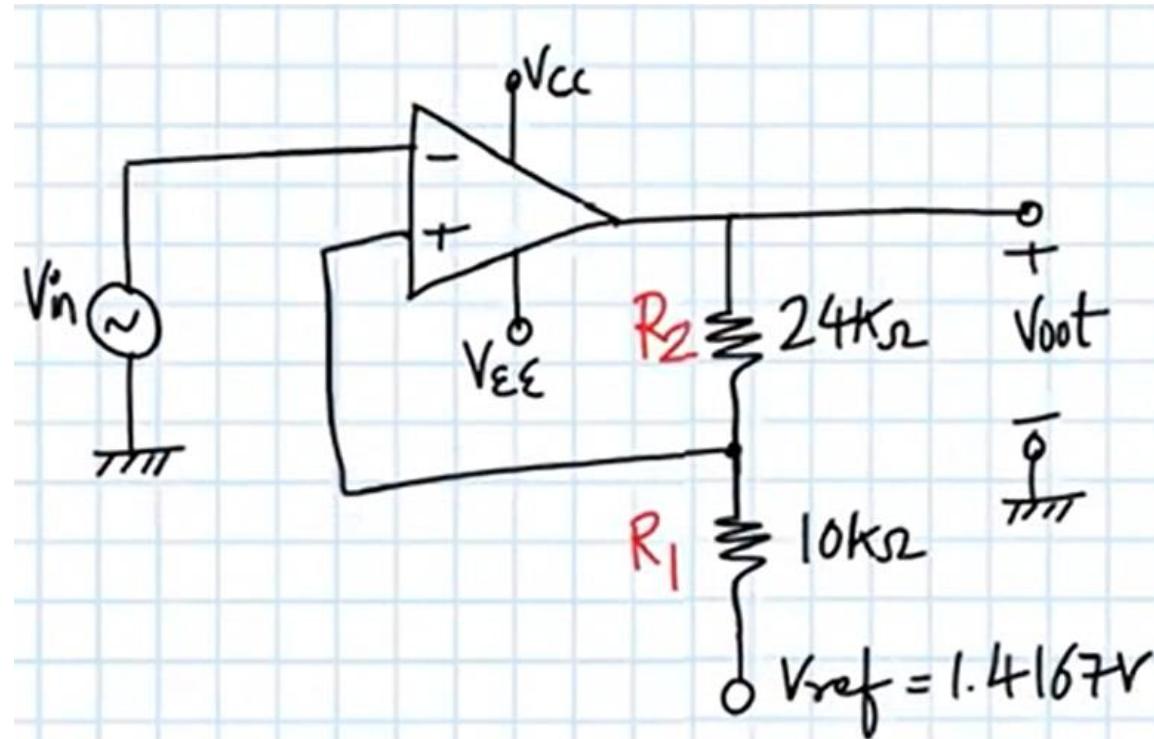
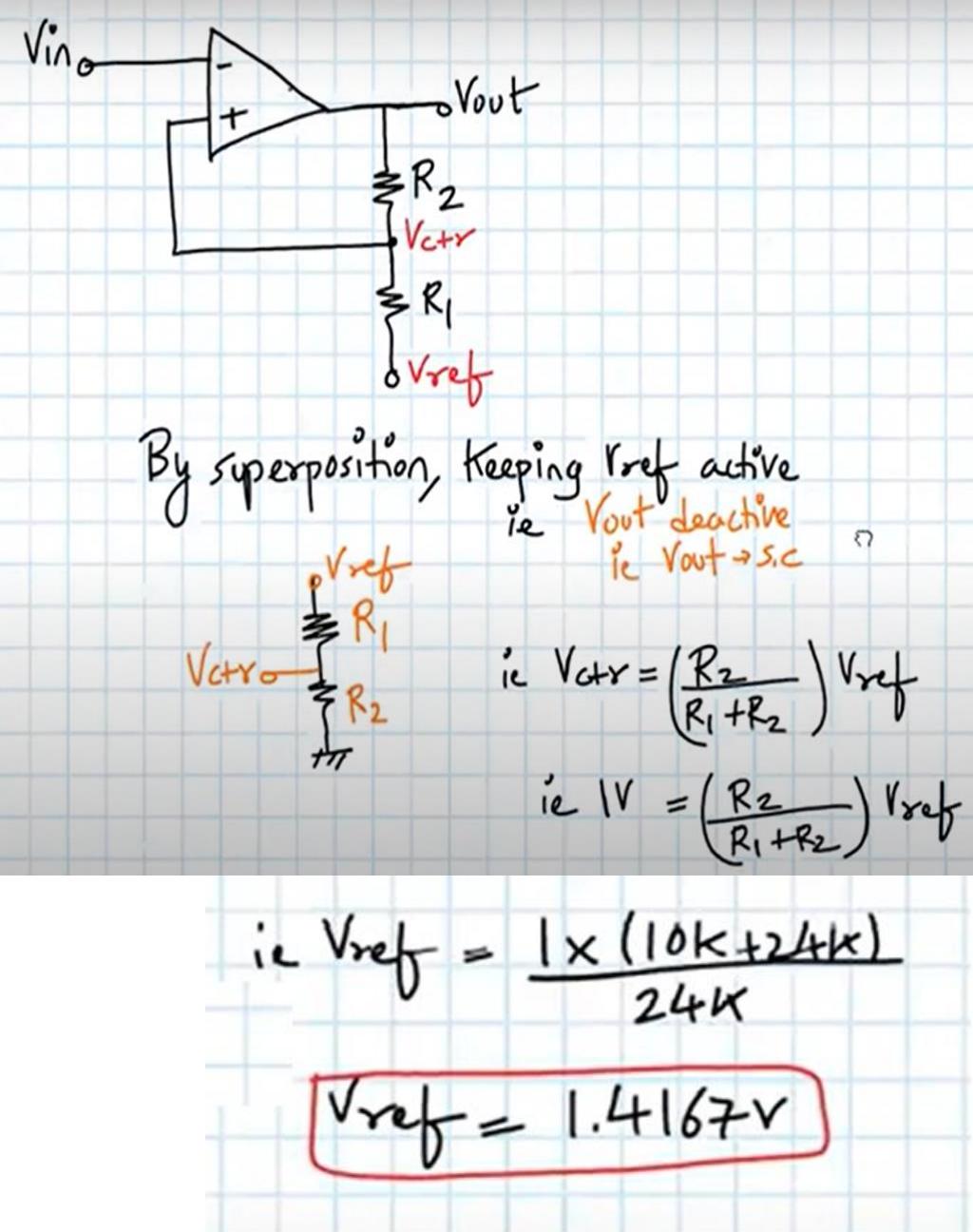
$$\text{i.e } 6 = 2 \left(\frac{R_1}{R_1+R_2} \right) \times 10$$

$$\frac{R_1}{R_1+R_2} = \frac{6}{20}$$

Center voltage of hysteresis is given by

$$V_{ctr} = \frac{V_{UTP} + V_{LTP}}{2} = \frac{4 + (-2)}{2}$$

$$\boxed{V_{ctr} = 1V}$$



LIC: LECTURE NON LINEAR CIRCUITS

- Outcomes of Positive Feedback
- Schmitt Trigger
- Operation of different types of Schmitt Trigger
 - (a) Inverting Schmitt Trigger
 - (i) Symmetric
 - (ii) Asymmetric
 - (b) Non-Inverting Schmitt Trigger
- Precision Rectifier

* Non-Inverting Schmitt Trigger (Opamp with positive feedback)

① Circuit uses a positive feedback

i.e. the voltage divider network consisting of (R_1 & R_2)
feedbacks a part of output voltage to non-inverting input

② Let us assume that,

- a) Output voltage V_{out} is at negative saturation level ($-V_{sat}$)
- b) Input V_{in} is increasing from 0V

③ KCL at node v_t gives,

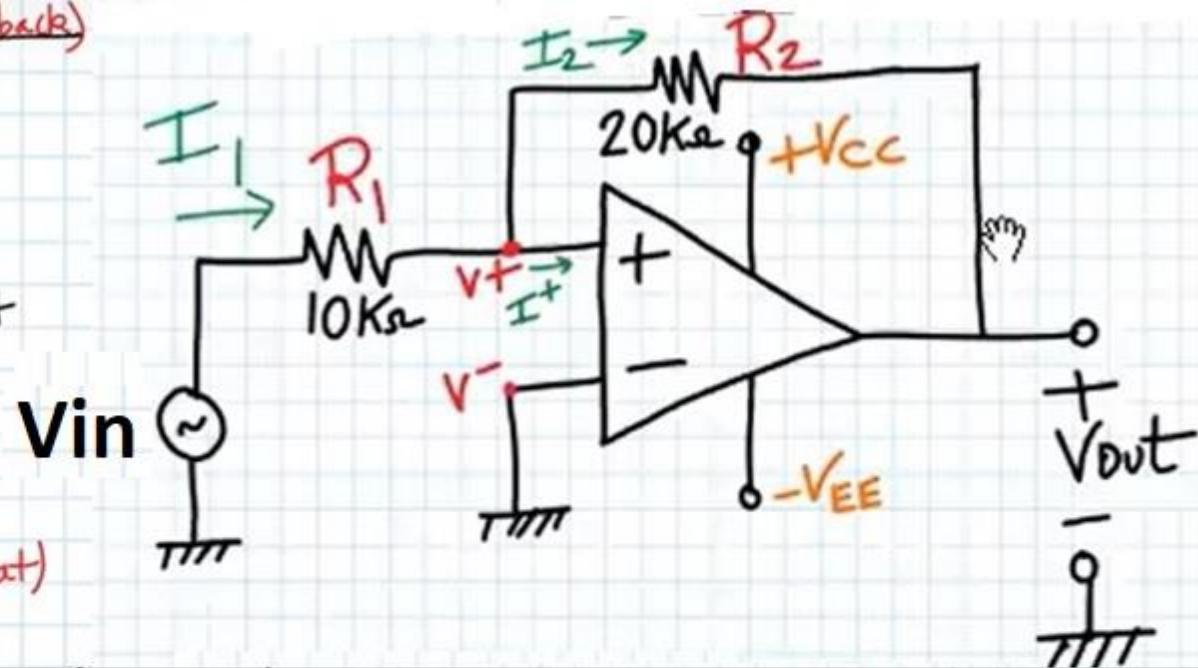
$$I_1 = I_2 + I^+$$

$$\frac{V_{in} - v^+}{R_1} = \frac{v^+ - V_{out}}{R_2} + 0 \quad (I^+ \approx 0, \text{ since opamp has very high input impedance})$$

$$v^+ \left(\frac{1}{R_2} + \frac{1}{R_1} \right) = \frac{V_{in}}{R_1} + \frac{V_{out}}{R_2}$$

$$v^+ \left(\frac{R_1 + R_2}{R_1 R_2} \right) = \frac{V_{in}}{R_1} + \frac{V_{out}}{R_2}$$

$$v^+ = \left(\frac{R_2}{R_1 + R_2} \right) V_{in} + \left(\frac{R_1}{R_1 + R_2} \right) V_{out} \quad \dots \dots \textcircled{1}$$



$$\textcircled{4} \quad V_{id} = v^+ - v^-$$

From circuit, $v^- = 0$

i.e. $\textcircled{4} \quad V_{id} = v^+$

⑤ The output switches from one saturation level to another when $V_{id} \rightarrow 0$ i.e. $v^+ \rightarrow 0$

From eqn ①, $0 = \left(\frac{R_2}{R_1 + R_2} \right) V_{in} + \left(\frac{R_1}{R_1 + R_2} \right) V_{out}$

i.e. $\textcircled{5} \quad V_{in} \left(\frac{R_2}{R_1 + R_2} \right) = - \left(\frac{R_1}{R_1 + R_2} \right) V_{out}$

i.e. $\textcircled{5} \quad V_{in} = - \frac{R_1}{R_2} V_{out} \quad \dots \dots \textcircled{2}$

⑥ The input voltage V_{in} triggers (changes the state) the output voltage V_{out} everytime it exceeds certain voltage levels known as "upper threshold point" & "lower threshold point".

⑦ When $V_{out} = -V_{sat}$, then the value of V_{in} required to switch the o/p voltage V_{out} from $-V_{sat}$ to $+V_{sat}$ is called "Upper threshold voltage" (V_{UTP})

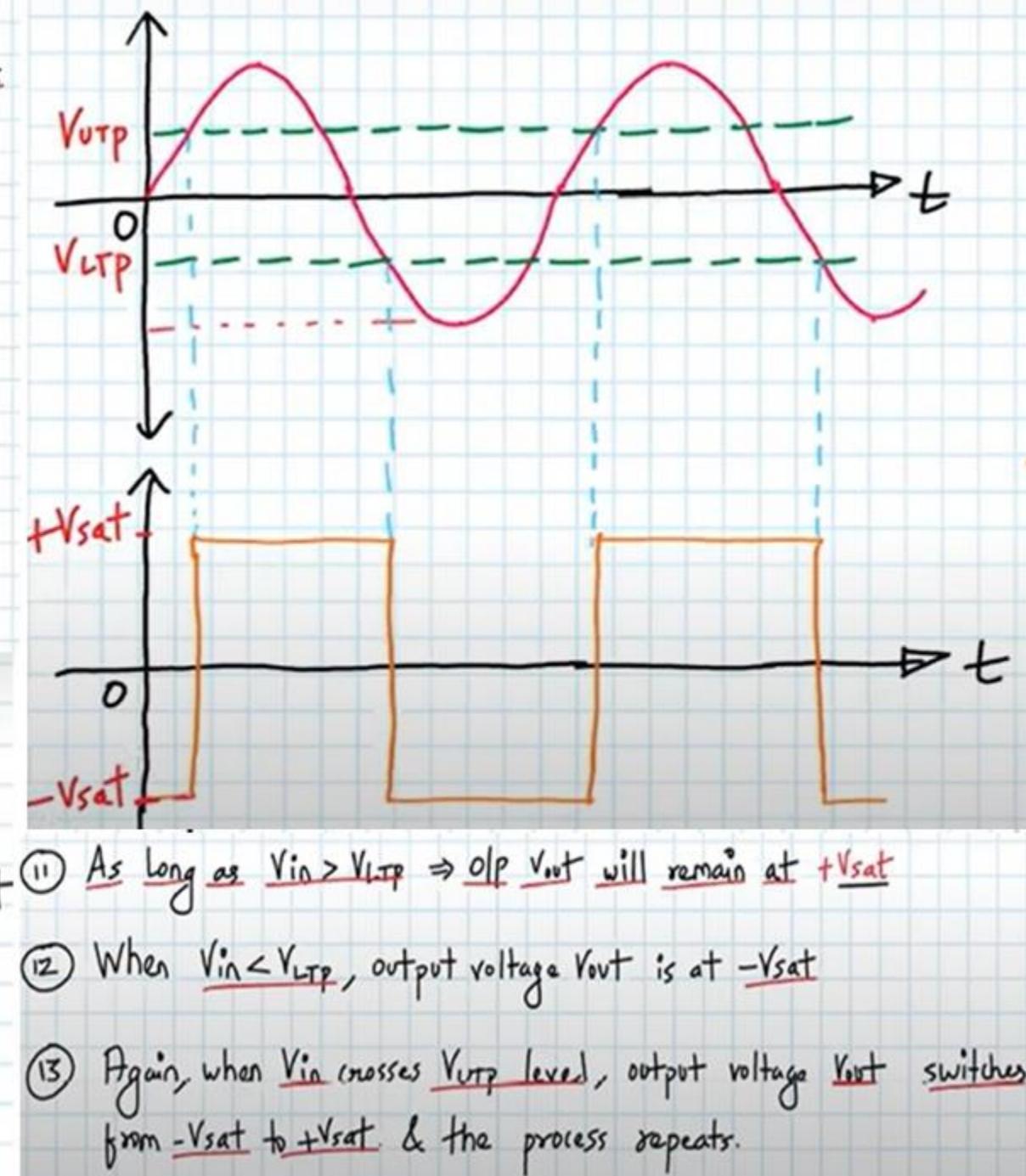
$$\therefore V_{UTP} = -\frac{R_1}{R_2} \times (-V_{sat}) \quad \dots \dots \textcircled{3}$$

⑧ As long as $V_{in} < V_{UTP} \Rightarrow$ o/p stays at $-V_{sat}$

⑨ When $V_{in} > V_{UTP}$, output V_{out} is at $+V_{sat}$

⑩ When $V_{out} = +V_{sat}$, then the value of input voltage V_{in} required to switch the output voltage from $+V_{sat}$ to $-V_{sat}$ is called "Lower threshold voltage" (V_{LTP})

$$\text{ie } V_{LTP} = \left(-\frac{R_1}{R_2}\right)(+V_{sat}) \quad \dots \dots \textcircled{4}$$



⑪ As long as $V_{in} > V_{UTP} \Rightarrow$ o/p V_{out} will remain at $+V_{sat}$

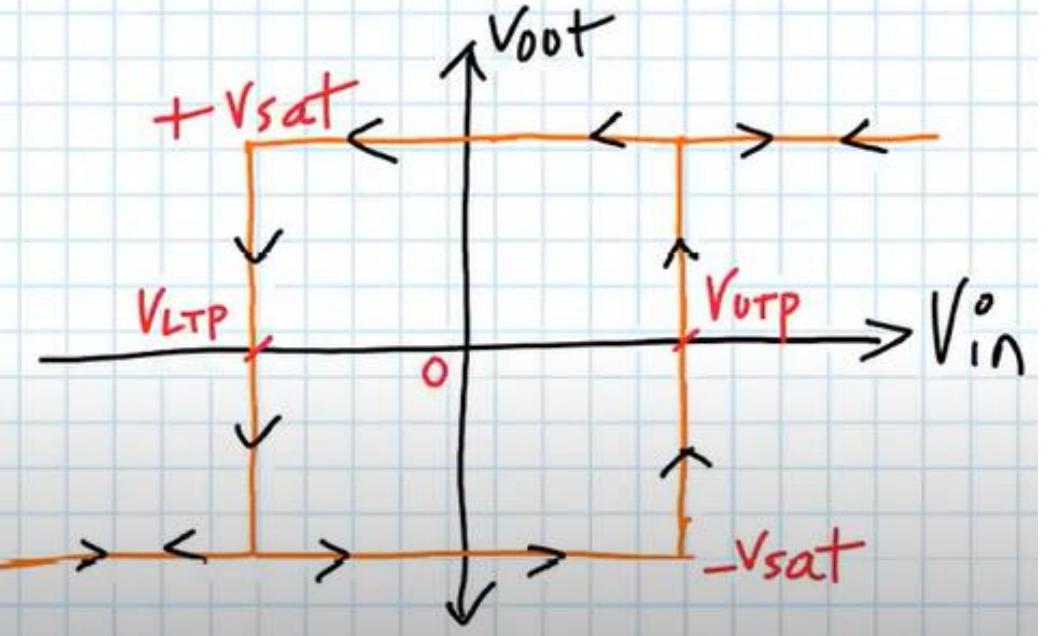
⑫ When $V_{in} < V_{LTP}$, output voltage V_{out} is at $-V_{sat}$

⑬ Again, when V_{in} crosses V_{UTP} level, output voltage V_{out} switches from $-V_{sat}$ to $+V_{sat}$. & the process repeats.

HYSTERESIS CURVE

- Hysteresis is the technique of forcing the output of regenerative comparator to switch at two different I/p levels known as V_{UTP} & V_{LTP}
- These two switching levels (V_{UTP} & V_{LTP}) are automatically produced by the feedback network R_1 & R_2 .

Hysteresis Curve



① When input V_{in} is between V_{UTP} & V_{LTP} ($V_{LTP} < V_{in} < V_{UTP}$), the output V_{out} of schmitt trigger is constant ie either at $-Vsat$ or $+Vsat$ i.e o/p does not switch over.

② The amount of hysteresis is defined by the difference of the two triggering levels (V_{UTP} & V_{LTP})

$$③ V_H = V_{UTP} - V_{LTP}$$

$$V_H = \left[-\frac{R_1}{R_2} (-Vsat) \right] - \left[-\frac{R_1}{R_2} (+Vsat) \right]$$

$$V_H = \left(\frac{R_1}{R_2} \right) [(+Vsat) - (-Vsat)] \quad \begin{array}{l} \text{If } +Vsat = +12V \\ -Vsat = -12V \end{array}$$

$$V_H = \frac{2R_1}{R_2} (+Vsat)$$

④ As long as the noise voltage is less than V_H , output state does not change.

⑤ Thus non-inverting Schmitt trigger circuit eliminates false triggering due to noise.

⑥ The circuit which converts any irregular shaped waveform to a square wave or pulse is known as "Schmitt trigger".

Design Problems

* Design an non-inverting Schmitt trigger with the following specifications:-

Supply voltages is $\pm 13V$, $V_{UTP} = +6V$, $V_{LTP} = -6V$

* Design an non-inverting Schmitt trigger with the following specifications:-

Supply voltages is $\pm 13V$, $V_{UTP} = +6V$, $V_{LTP} = -6V$

Now, since V_{UTP} & V_{LTP} are symmetric, we can consider one (either V_{UTP} & V_{LTP}) & proceed.

$$\text{ie } V_{UTP} = -\frac{R_1}{R_2} (-V_{sat})$$

$$\text{ie } 6 = \frac{R_1}{R_2} \times 12$$

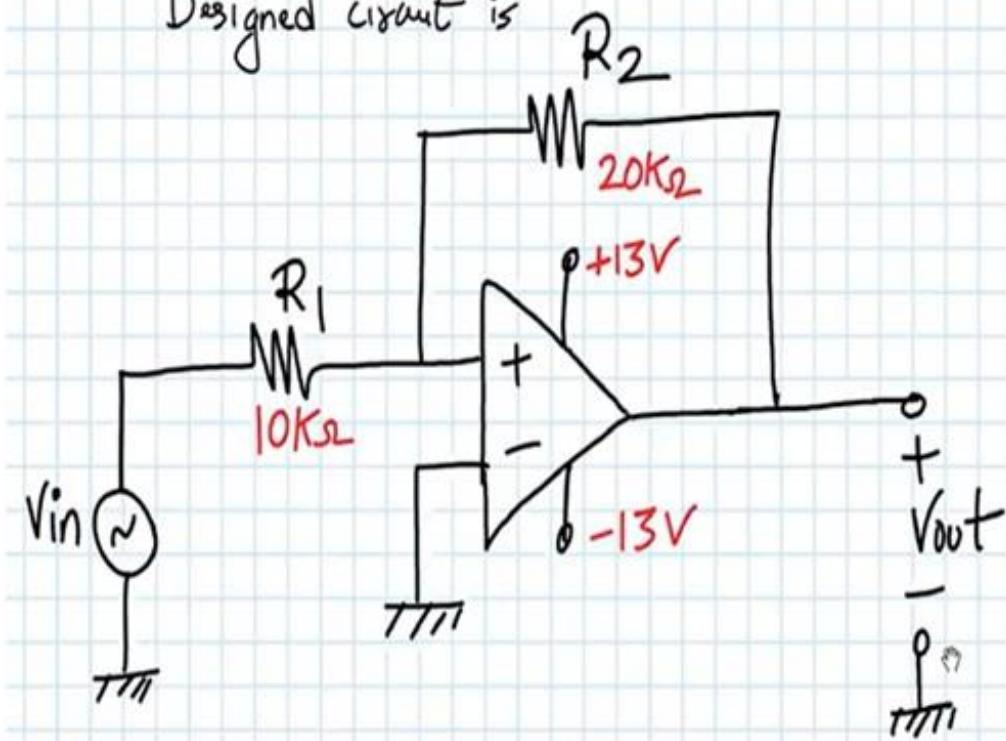
$$\text{ie } \frac{R_2}{R_1} = 2$$

$$\rightarrow R_2 = 2R_1$$

$$\text{Let } R_1 = 10K\Omega$$

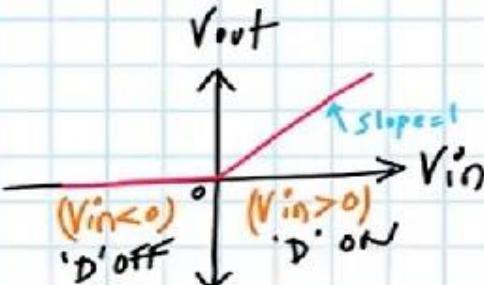
$$\therefore R_2 = 20K\Omega$$

Designed circuit is



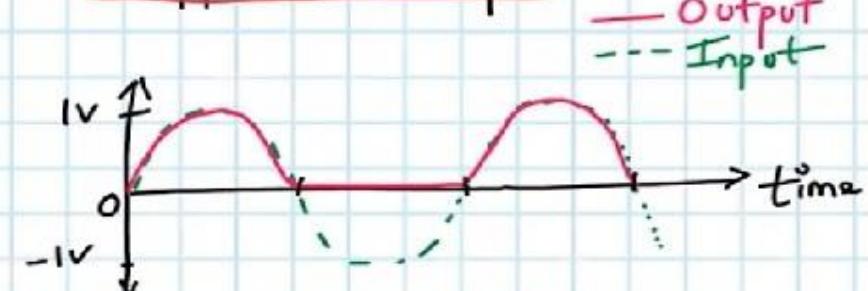
PRECISION RECTIFIER

a) Ideal Half wave rectifier:



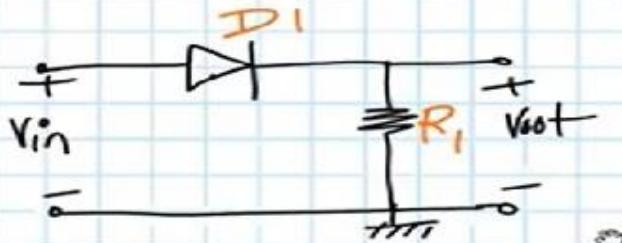
VTC curve

Suppose V_{in} : 1V peak



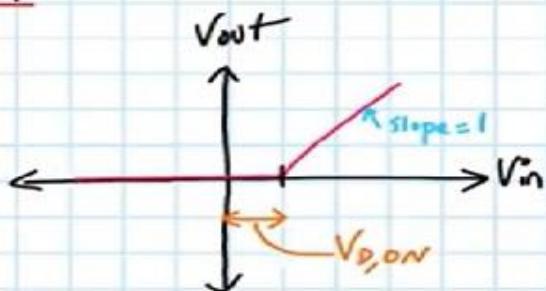
$V_{in}(t)$ & $V_{out}(t)$

b) Practical Half-wave rectifier:-



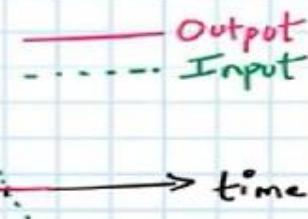
$V_{D,ON}$: Diode voltage drop

→ Conduction is possible only if V_{in} exceeds $V_{D,ON}$



VTC curve

$D1 'ON'$ $\rightarrow V_{in} > V_{D,ON}$
 $D1 'OFF'$ $\rightarrow V_{in} < V_{D,ON}$



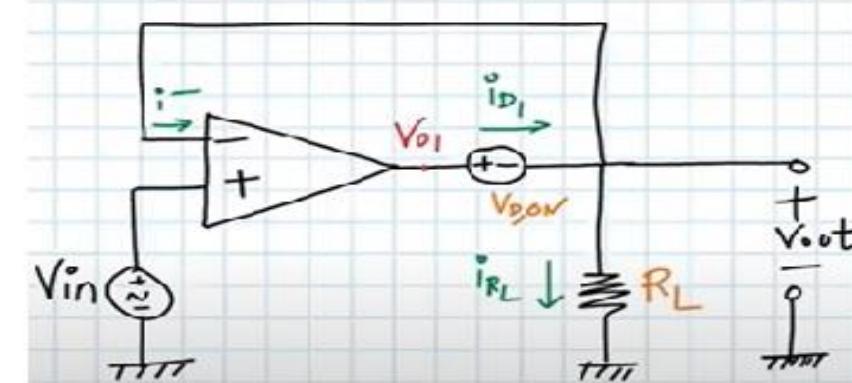
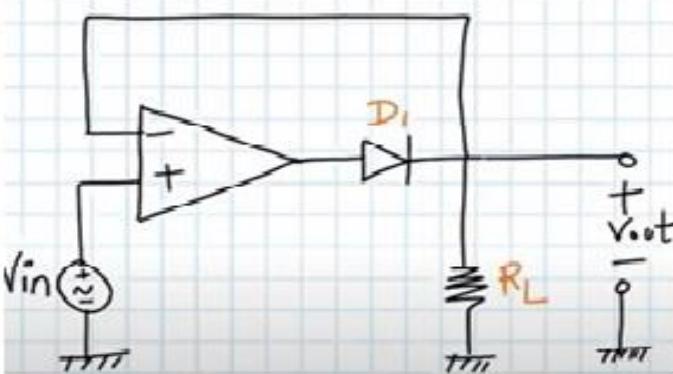
$V_{in}(t)$ & $V_{out}(t)$

→ Clearly, output voltage V_{out} is NOT what we would like it to be !!

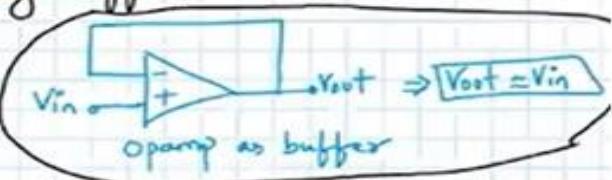
→ Need of an improved circuit which can rectify even small values of input V_{in} .

PRECISION RECTIFIER

$V_{in} = +ve$



Dindo D_+ is conducting : The feedback loop is closed, and thus for the voltage buffer, we have seen earlier.



Since the input current $i^- \approx 0$ (\therefore Input impedance of opamp is very high)

$$\therefore i_{RL} = i_{D1}$$

for an opamp, $V_{out} = A_{OL}(V^+ - V^-)$; $A_{OL} \rightarrow$ open-loop gain of opamp $\approx 2 \times 10^5$

$$i.e. V^+ - V^- = \frac{V_{out}}{A_{OL}}$$

But $V_{out} = V_{D,ON} + V_{out} = 0.7 + V_{out}$
i.e. $V^+ - V^- = \frac{V_{out} + 0.7V}{A_{OL}} \approx 0V$

$$V_{out} = V^- \approx V^+$$

Also, $V^+ \approx V_{in}$ (\because V_{in} connected to non-inverting terminal of opamp)
i.e. $V_{out} \approx V_{in}$

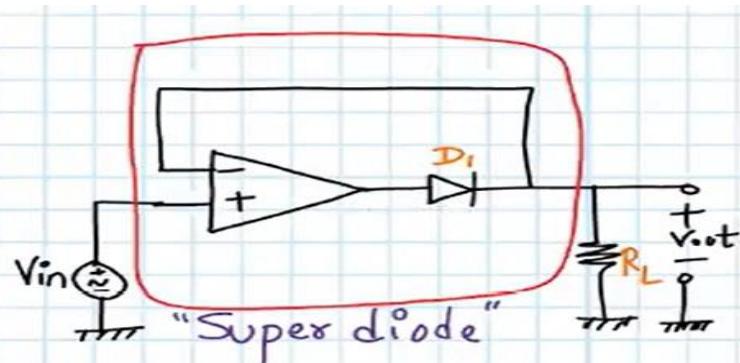
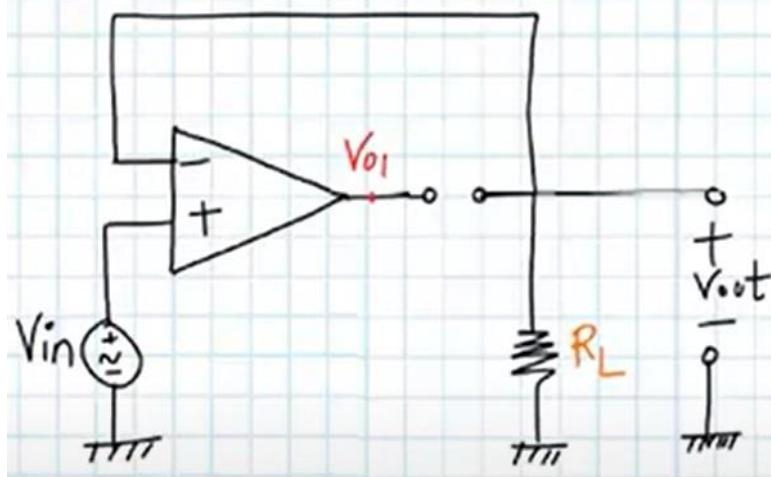
This situation arises only if $i_D > 0$ (since the diode can conduct in the forward direction)

i.e. $i_{RL} > 0 \rightarrow V_{out} = i_{RL} R_L > 0$, and therefore $V_{out} = V_{in} > 0V$

i.e. In this case, when D_+ is conducting & if V_{in} is +ve
i.e. $V_{in} > 0V \Rightarrow V_{out} = V_{in}$

PRECISION RECTIFIER

$V_{in} = -ve$



Observations:-

- ① The circuit is called "super diode" (an ideal diode) with $V_{D,ON} = 0V$
- ② When D_1 conducts, the opamp operates in the linear region, and we have $V^+ \approx V^-$
- ③ When D_1 is OFF, the opamp operates in the saturation region, $V^- = 0$, $V^+ = V_{in}$ and $V_{O1} = -V_{sat}$

1) Diode D_1 is not conducting: Diode D_1 is OFF ie D_1 is replaced by an open-circuit.

$$\therefore V_{out} = 0V$$

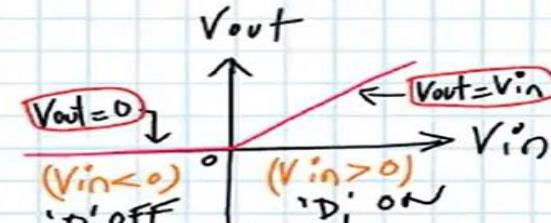
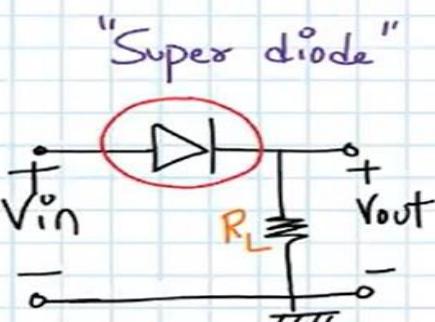
2) What about V_{O1} ?

→ Since the opamp is now in the open-loop configuration, a very small V_{in} is enough to drive it to saturation.

3) Note that CASE (II) occurs when $V_{in} < 0V$

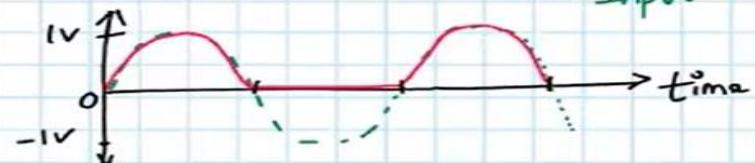
→ Since, $V^+ - V^- = V_{in} - 0 = V_{in}$ & V_{in} is negative

$$V_{O1} = A_{OL}(-V_{in}) \Rightarrow V_{O1} = -V_{sat} \text{ ie } V_{O1} \text{ is driven to } -V_{sat} \text{ (negative saturation)}$$



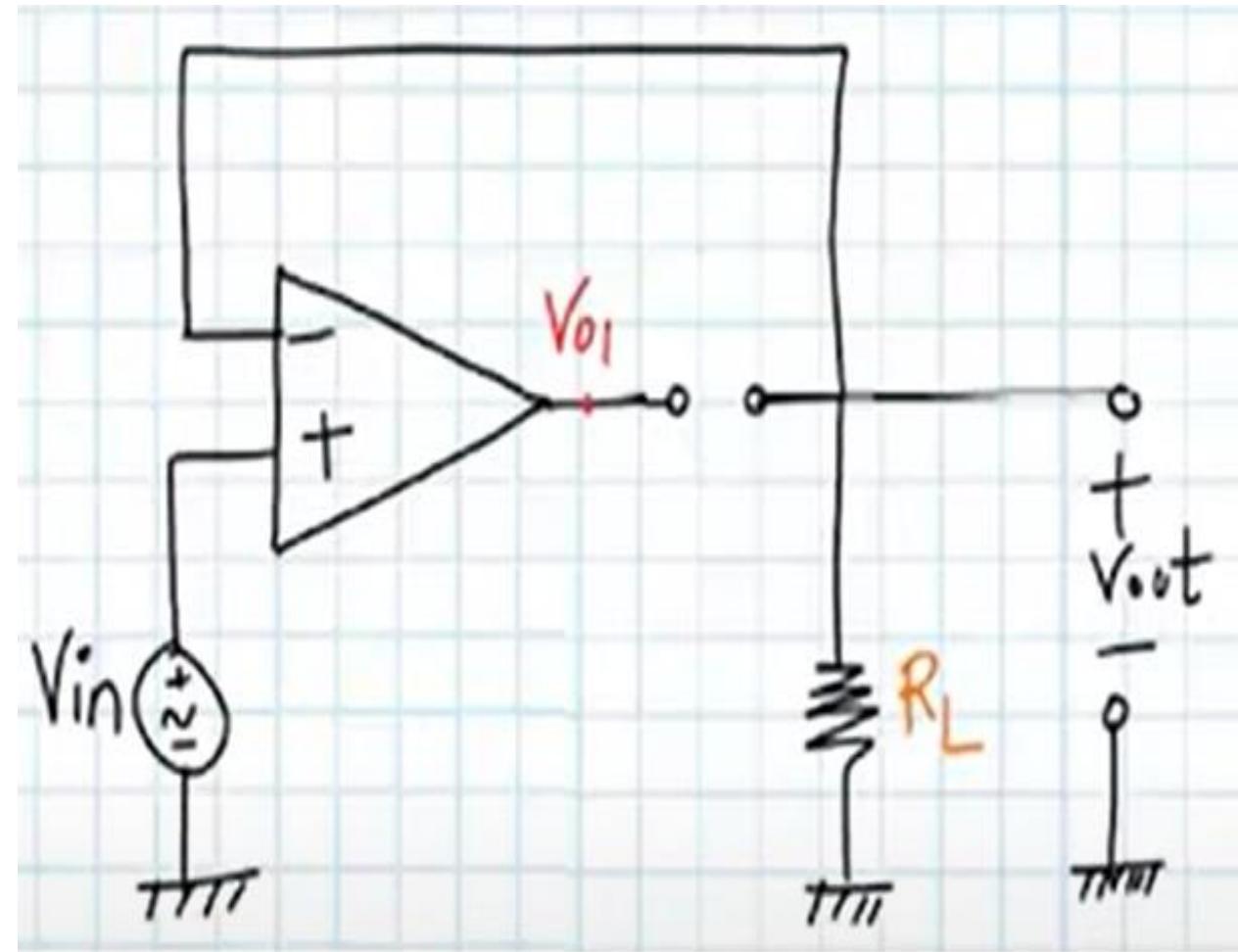
VTC curve

Suppose $V_{in}: 1V_{peak}$



$V_{in}(t)$ & $V_{out}(t)$

PRECISION RECTIFIER ($V_{in}=-ve$)



1) Diode D_1 is not conducting: Diode D_1 is OFF ie D_1 is replaced by a open-circuit.

$$\therefore V_{out} = 0V$$

2) What about V_{o1} ?

→ Since the opamp is now in the open-loop configuration, a very small V_{in} is enough to drive it to saturation.

3) Note that CASE(II) occurs when $V_{in} < 0V$

→ Since, $V^+ - V^- = V_{o1} - 0 = V_{in}$ & V_{in} is negative

$$V_{o1} = A_{OL}(-V_{in}) \Rightarrow V_{o1} = -V_{sat} \text{ ie } V_{o1} \text{ is driven to } -V_{sat} \text{ (negative saturation)}$$

LIC: LECTURE NON LINEAR CIRCUITS

- ✓ Need of Precision Rectifier
- ✓ Basic Half Wave Precision Rectifier
- Improved Half Wave Precision Rectifier
- Full Wave Precision Rectifier

Improved Half Wave PR

① The improvement we are looking in basic precision rectifier is that → opamp should NOT enter saturation region, since it does it will affect the speed of the circuit.

→ let's discuss how this circuit works:

CASE I: Diode D_1 conducts

① As Diode D_1 conducts, inner loop is complete; opamp operates in linear region.

② As per virtual ground concept,

$$V^+ = 0V \quad (V^+ \text{ is at real ground})$$

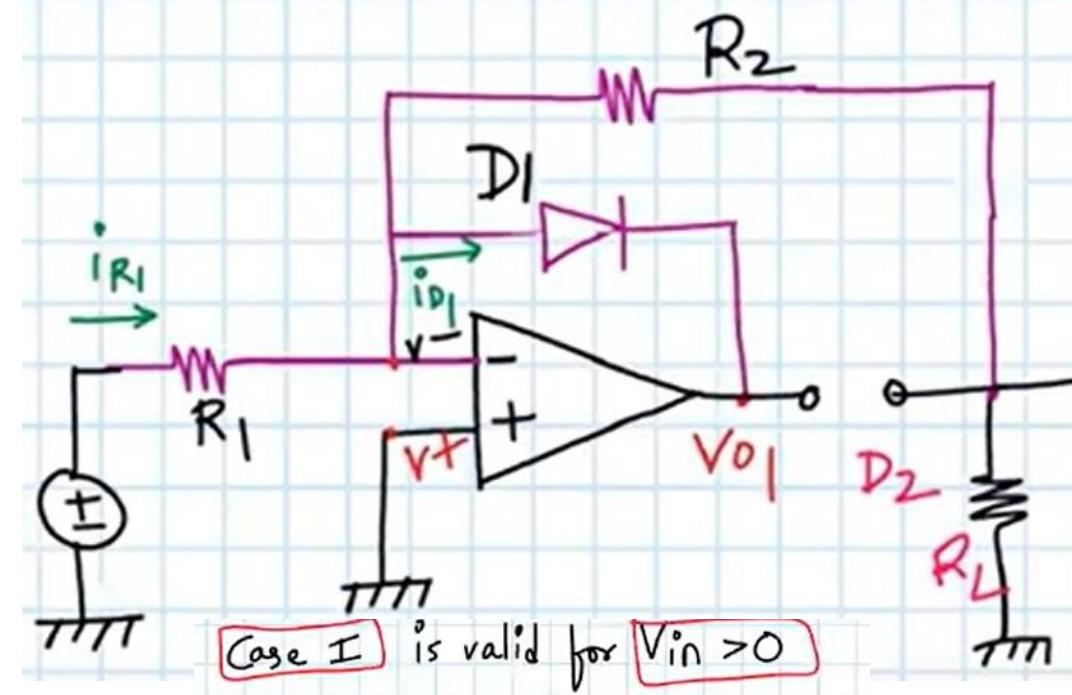
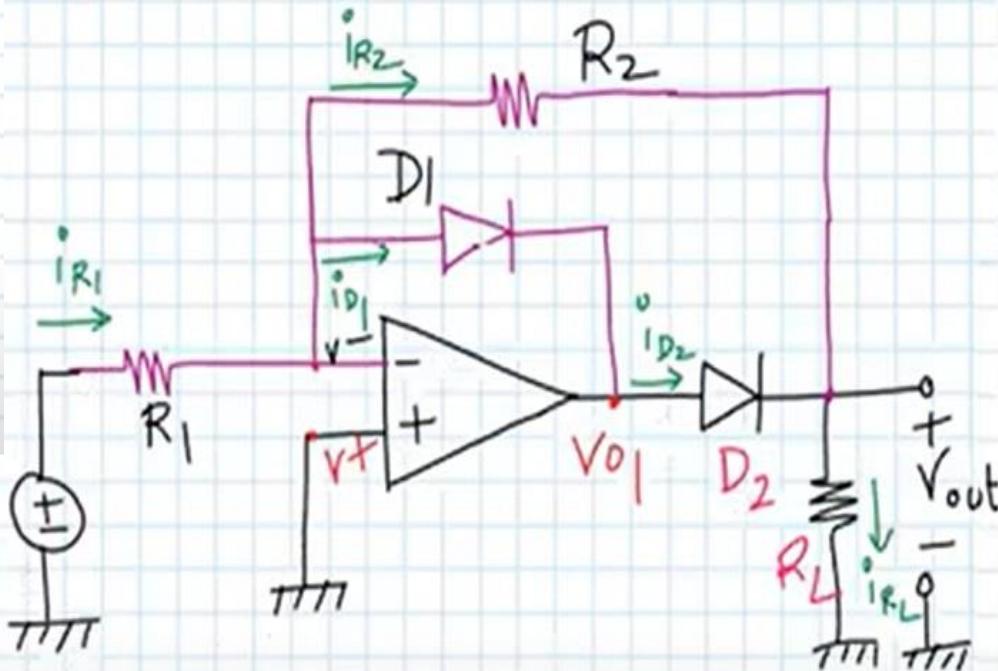
$$V^+ \approx V^- \approx 0V$$

$$\text{③ Now, } V_{O1} = 0 - V_{D1,ON} = 0 - 0.7V \rightarrow V_{O1} = -0.7V$$

↓
Diode drop $\sim 0.7V$

④ Since, $V_{O1} = -0.7V \rightarrow$ Diode D_2 cannot conduct.

$$\text{⑤ Current } i_{R_2} = 0 ; i_{R_L} = 0$$



CASE II: Diode D_1 is OFF

① Diode D_1 will be OFF when

$$V_{in} < 0V$$

② In this case, D_2 conducts

& closes the feedback loop

through R_2 ie opamp operates
in the Linear region.

Virtual ground concept ,

$$V^+ \approx V^- \approx 0V$$

circuit 2.1, we have $V^- + i_{R_2} \times R_2 - V_{out} = 0$

$$V_{out} = V^- + i_{R_2} \times R_2 ; i_{R_1} = i_{R_2} (\because i^- = 0)$$

$$i_{R_2} = \frac{V^- - V_{in}}{R_1} (\because V^- \approx 0)$$

$$i_{R_2} = \frac{0 - V_{in}}{R_1}$$

$$\Rightarrow V_{out} = 0 + \left(\frac{0 - V_{in}}{R_1} \right) R_2$$

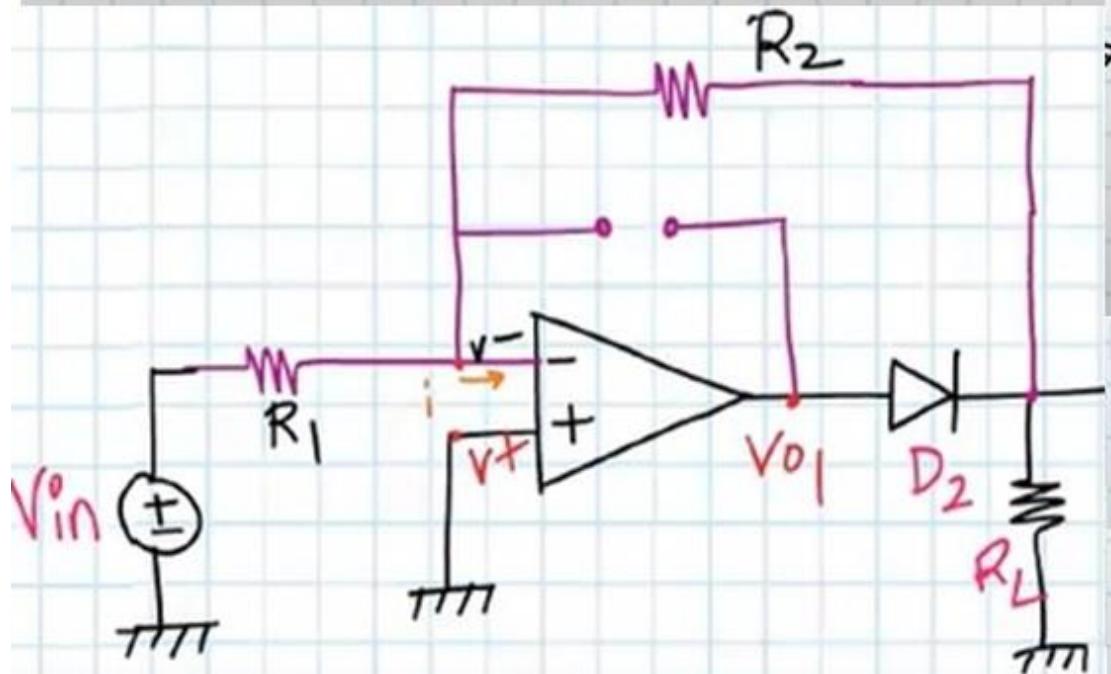
$$V_{out} = - \frac{R_2}{R_1} V_{in}$$

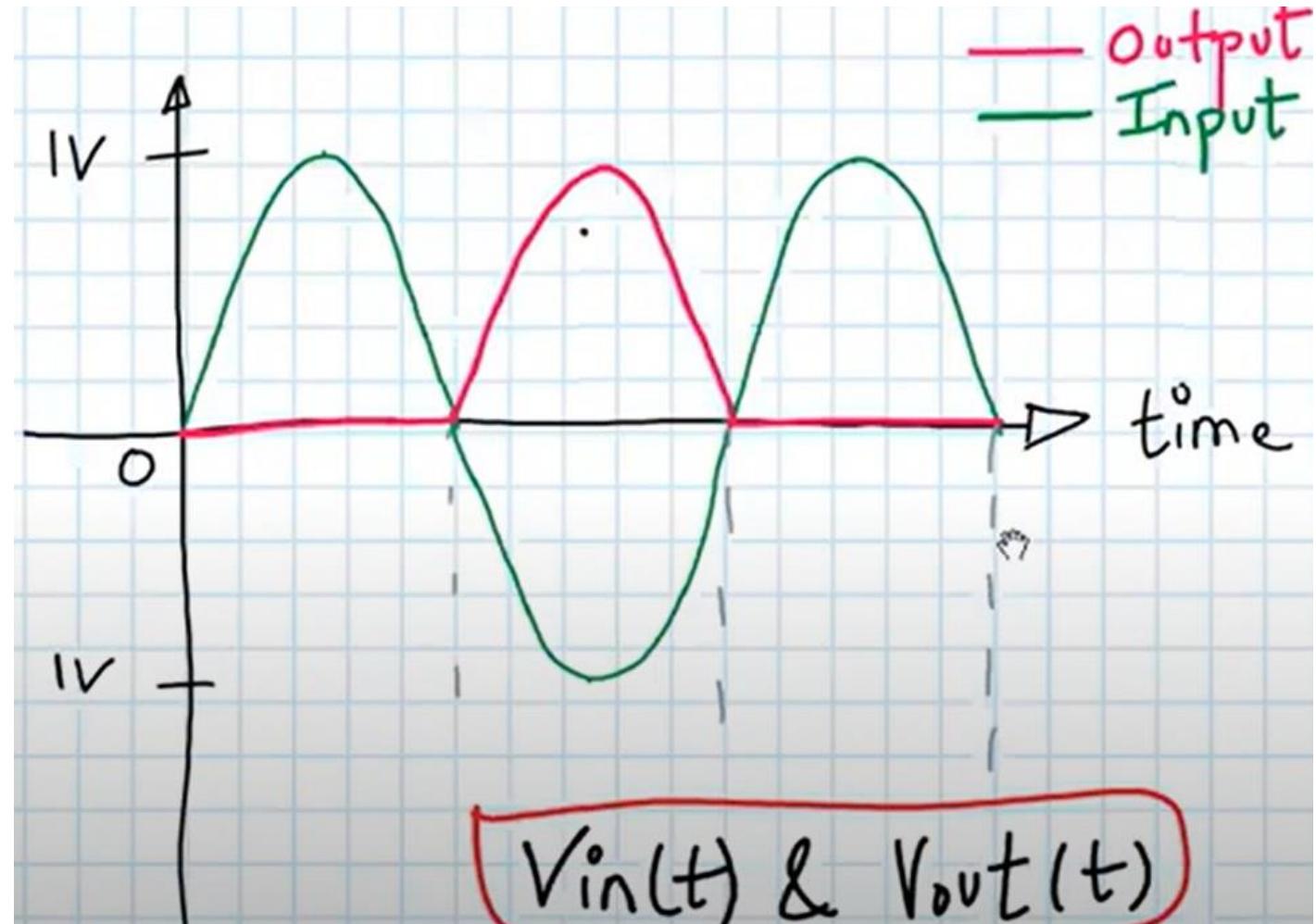
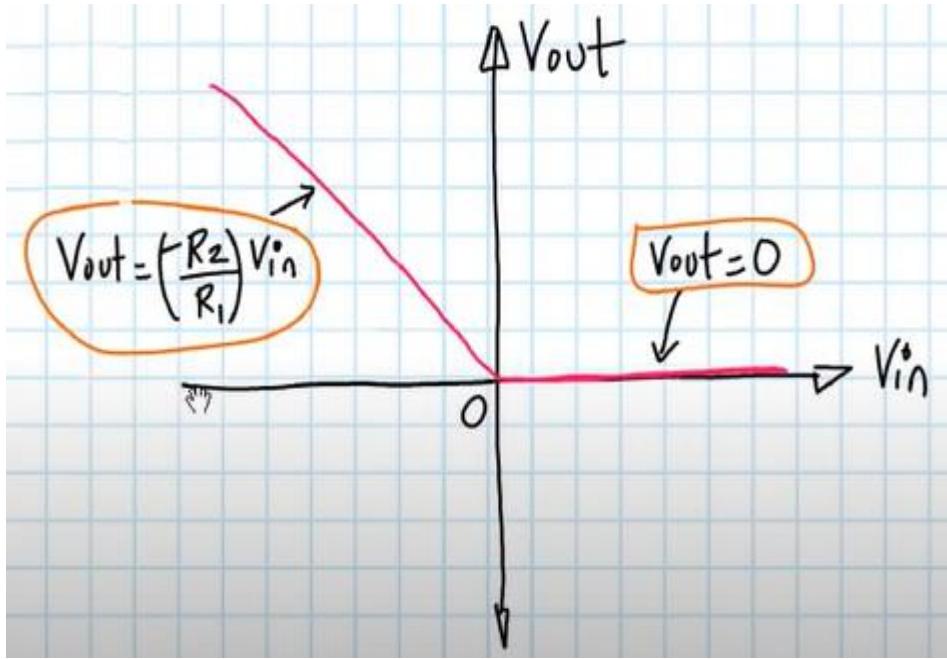
Valid for $V_{in} < 0$

If $R_1 = R_2 = R$

$$V_{out} = - \frac{R}{R} V_{in}$$

$$V_{out} = - V_{in} \quad \text{for } V_{in} < 0$$



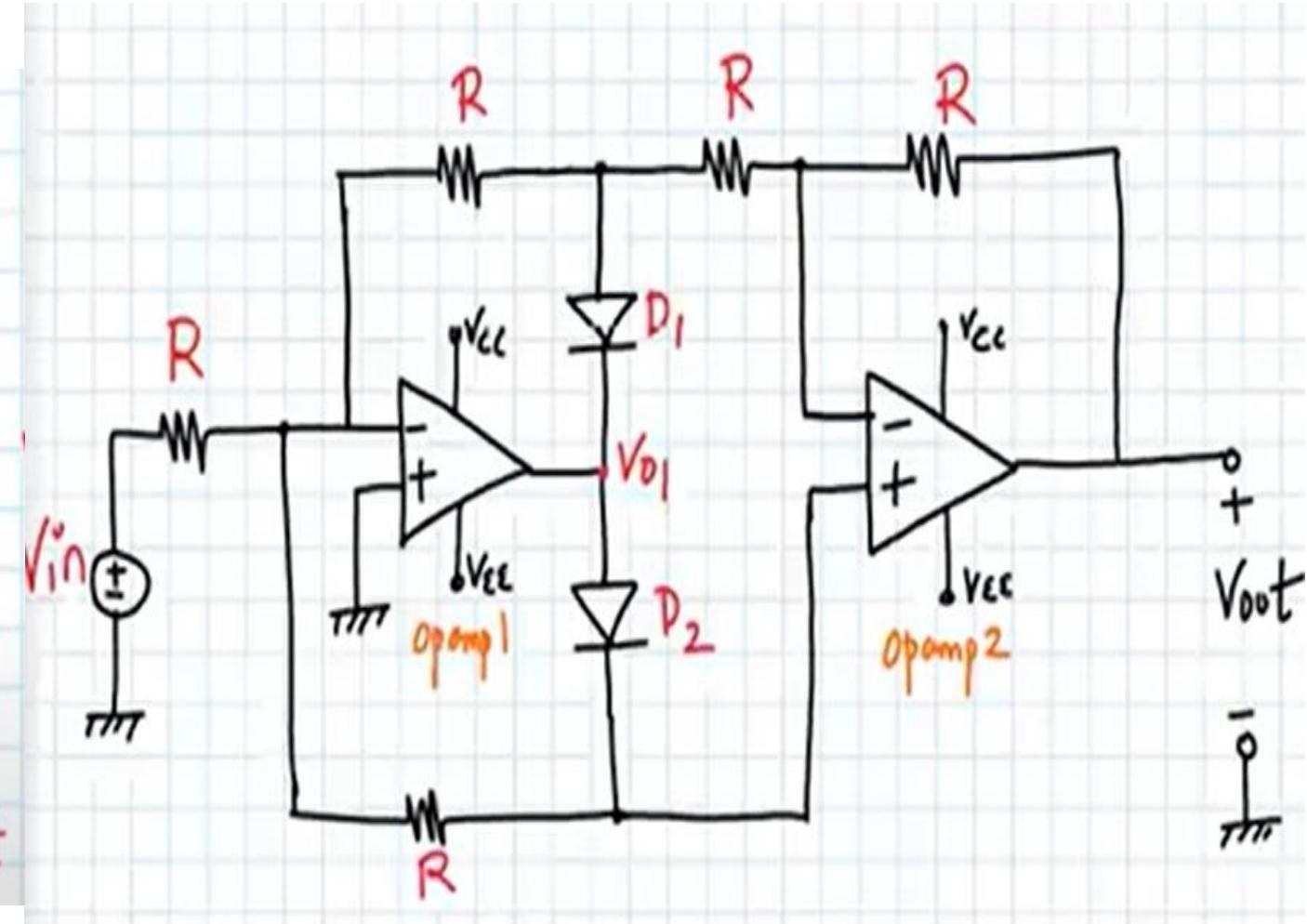


FULL WAVE PRECISION RECTIFIER

① Circuit 1.1 provides full-wave rectification even for smaller input voltages.

② In order to analyze the working of the circuit, we need to consider the following two scenario's.

- a) During positive half cycle of input
- b) During negative half cycle of input



Scenario 1:

a) During positive half cycle of input, output of opamp 1 i.e. V_{O1} is negative

b) \therefore Diode D_1 is forward-biased and conducting.
(i.e. D_1 can be replaced by a short-circuit)

Diode D_2 is reverse biased and it is OFF
(i.e. D_2 can be replaced by an open-circuit)

c) \therefore The circuit 1.1 is modified & becomes circuit 1.2

i) Since opamp 1 is operating in linear region, we can use

ii) From circuit 1.2, V^+ is at ground for opamp 1

i.e. $V^+ = 0$; $V^- \approx V^+ \approx 0V$ (By virtual ground)

f) \therefore Circuit 1.2 is further modified & reduces to as shown in circuit 1.3

From circuit 1.3, we have

i) Output V_{O1} of opamp 1 is given by,

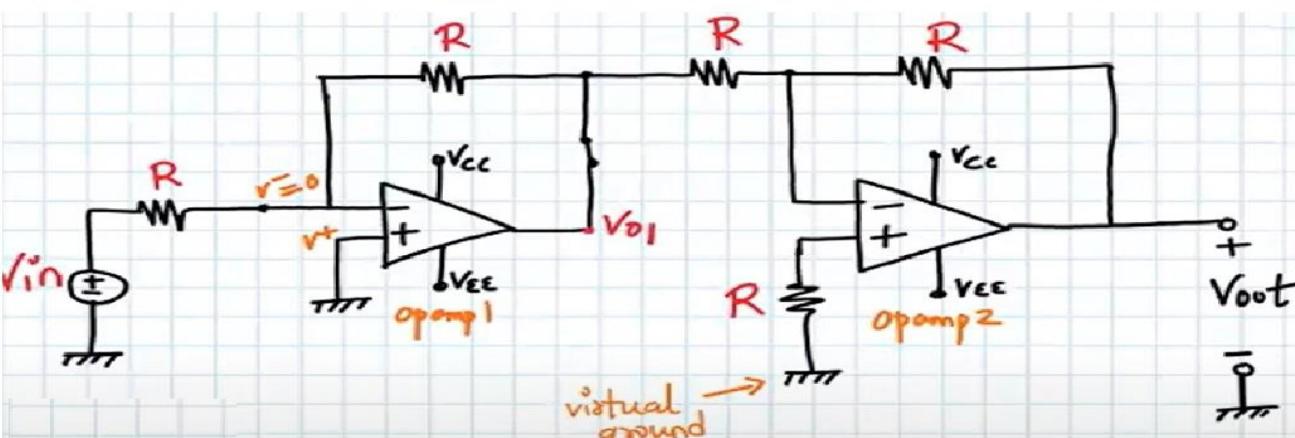
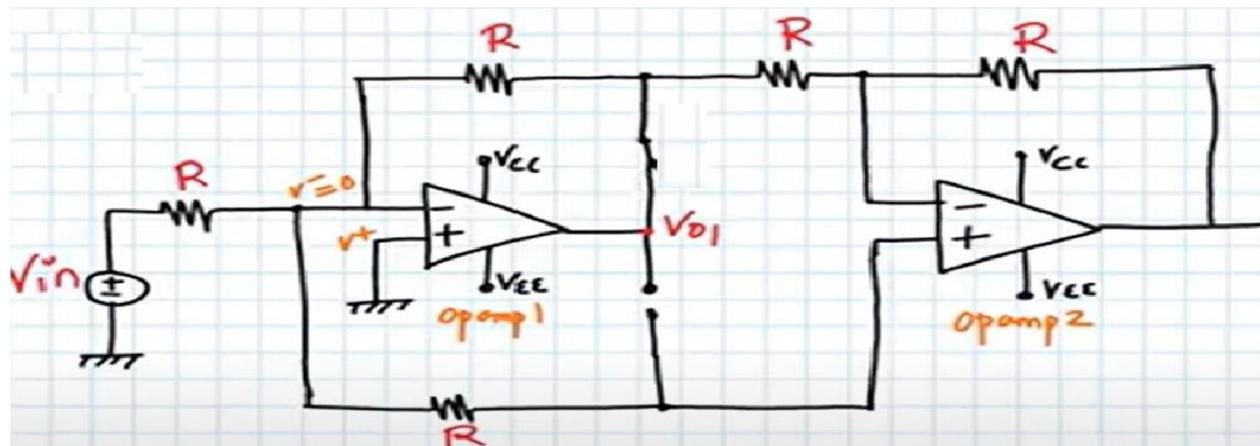
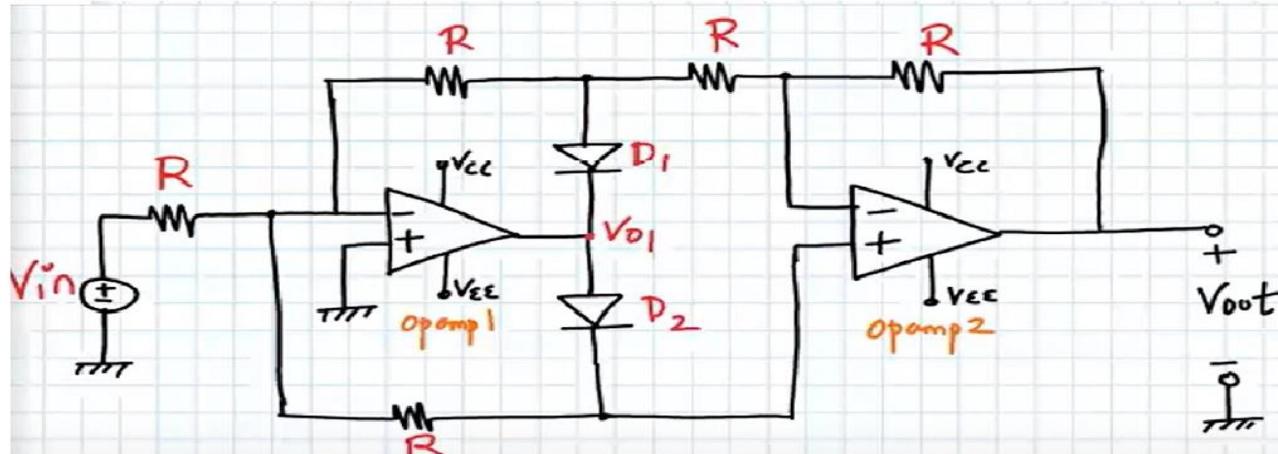
$$V_{O1} = -\left(\frac{R}{R}\right) \times V_{in}$$

$V_{O1} = -V_{in}$ i.e. opamp 1 is working as inverter

ii) Output of opamp 2 is given by,

$$V_{out} = -\left(\frac{R}{R}\right) V_{O1} = -(-V_{in})$$

i.e. $V_{out} = V_{in}$... During positive half cycle



Scenario 2:

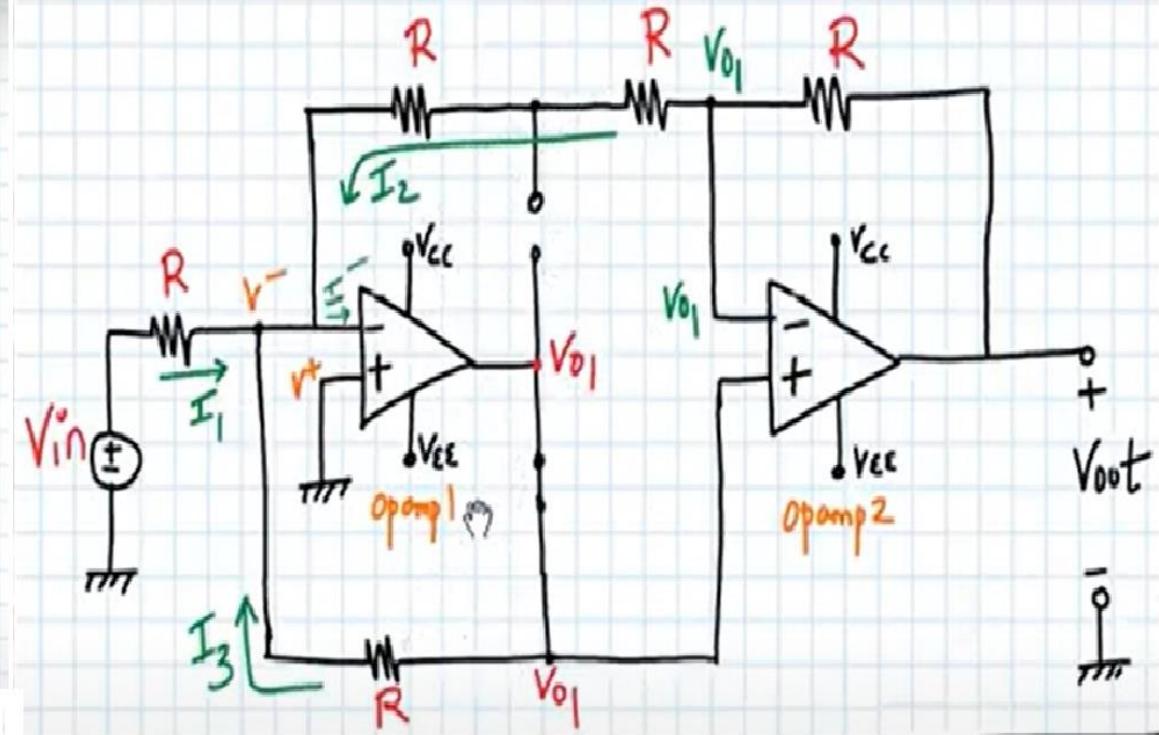
a) During negative half cycle of input,

o/p of opamp 1 is positive

b) \therefore Diode D_2 is forward biased and conducting.
(i.e. D_2 can be replaced by a short-circuit)

Diode D_1 is reverse biased and it is OFF
(i.e. D_1 can be replaced by an open-circuit)

c) \therefore The circuit 1.1 is modified & becomes circuit 2.1



d) Applying KCL at node v^- of opamp 1, we get

$$I_1 + I_2 + I_3 = I^-$$

$$\text{i.e. } \frac{V_{in} - v^-}{R} + \frac{V_{o1} - v^-}{2R} + \frac{V_{o1} - v^-}{R} = 0$$

$$\text{i.e. } \frac{V_{in}}{R} + \frac{V_{o1}}{2R} + \frac{V_{o1}}{R} = 0$$

$$\text{i.e. } V_{o1} \left(\frac{1}{2R} + \frac{1}{R} \right) = -\frac{V_{in}}{R}$$

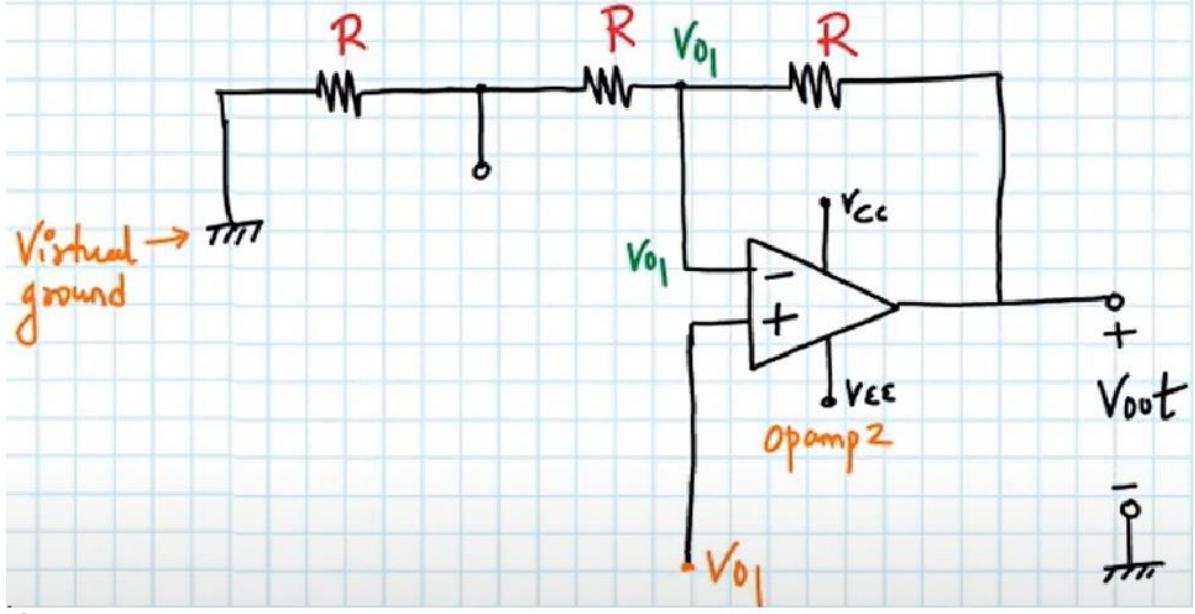
$$\text{i.e. } V_{o1} \left(\frac{3R}{2R} \right) = -\frac{V_{in}}{R}$$

$$\text{i.e. } V_{o1} = -\frac{2}{3} V_{in}$$

..... (2)

($I^+ = 0$, since input impedance is very high)

(For opamp 1, v^+ term i.e. $v^+ = 0$
By virtual ground con)



i.e. output voltage of opamp 2 is given by,

From circuit 2.2, it's evident that

opamp 2 is in non-inverting mode,

$$\text{i.e } V_{out} = \left(1 + \frac{R}{2R}\right) V_{o1}$$

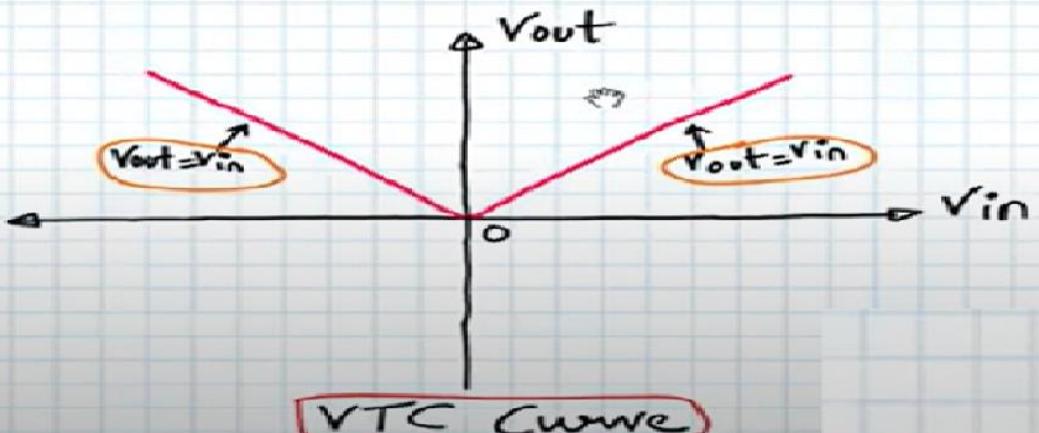
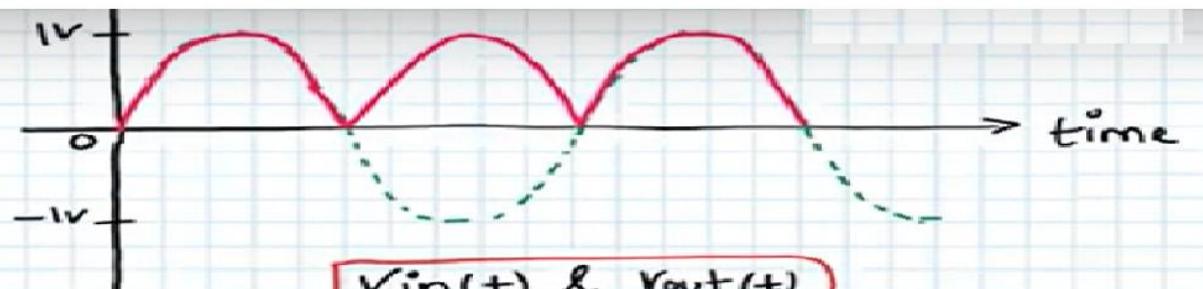
$$V_{out} = \left(1 + \frac{1}{2}\right) \left(-\frac{2}{3} V_{in}\right) = \left(\frac{3}{2}\right) \left(-\frac{2}{3}\right) V_{in}$$

$$\text{i.e } V_{out} = -V_{in}$$

i.e $V_{out} = V_{in}$ During negative half cycle of V_{in}
 i.e. opamp simply follows the input during negative half cycle of V_{in}

Outcomes:

- ① Irrespective of whether input V_{in} is positive or negative, Output voltage V_{out} always follows the input in positive direction.
- ② The above circuit 1.1 works as a Precision Full-wave rectifier
 i.e. it is able to rectify even v. low amplitude input's without any problem.

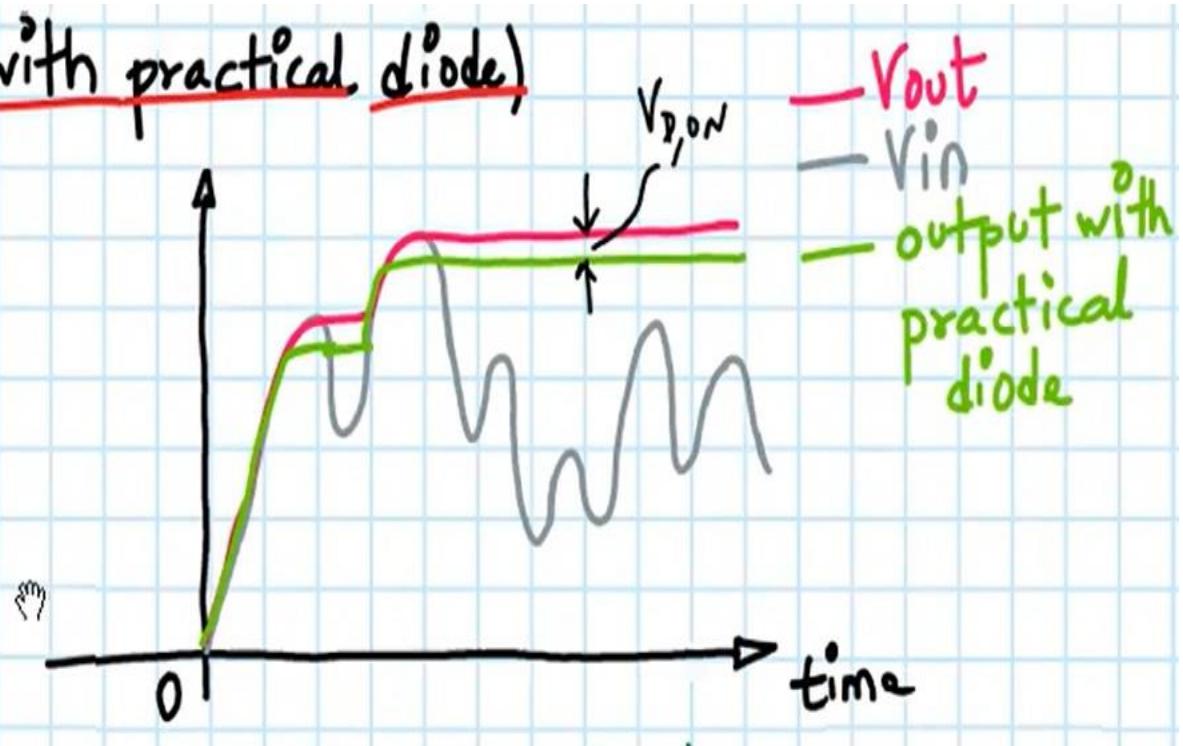
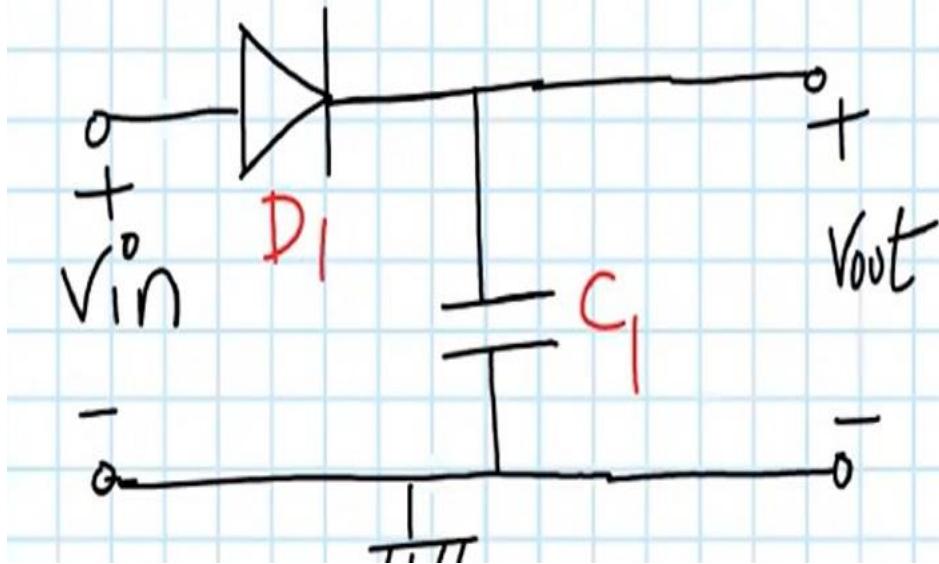


LIC: LECTURE NON LINEAR CIRCUITS

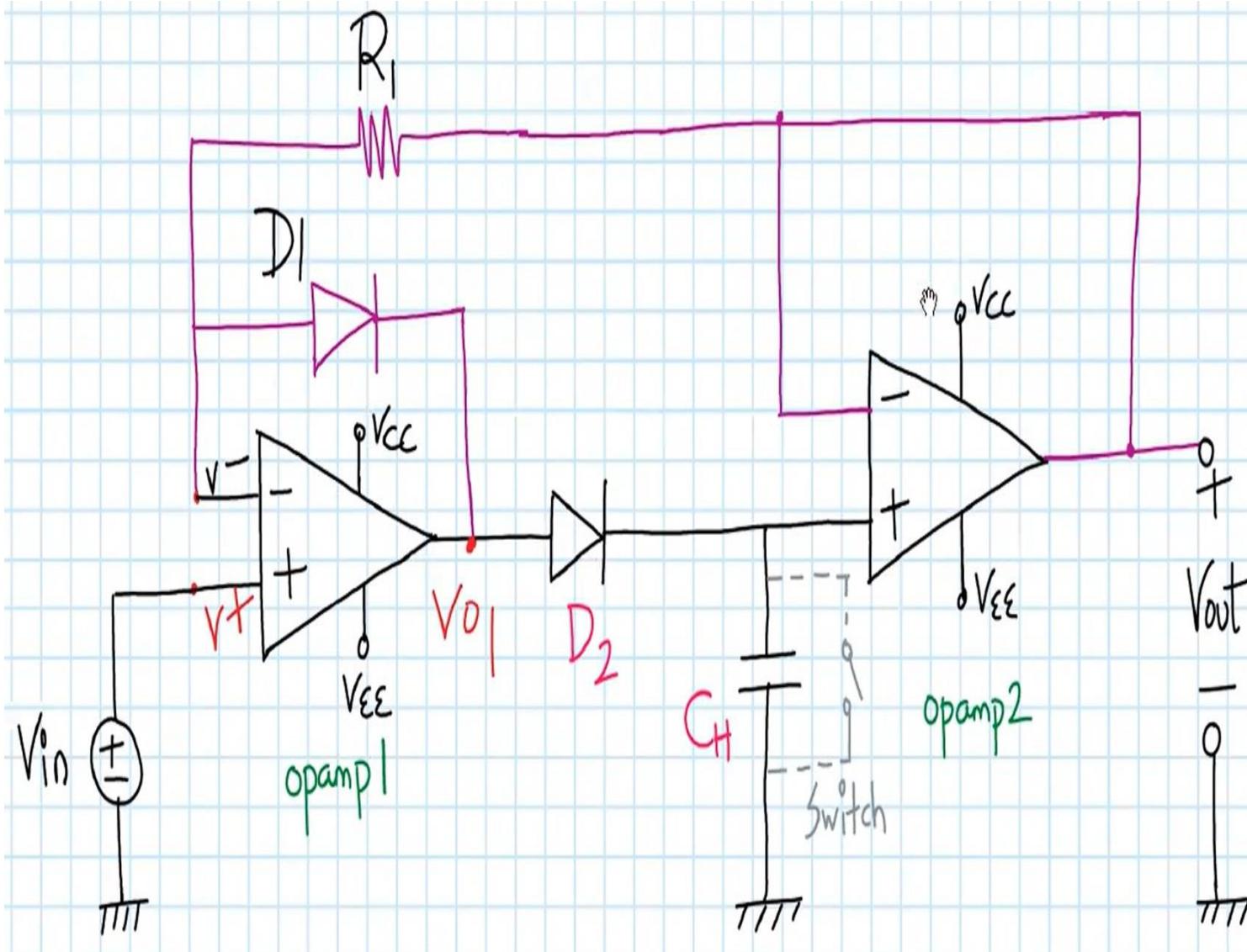
- ✓ Improved Half Wave Precision Rectifier
- ✓ Full Wave Precision Rectifier
- Peak Detector Circuit
 - Disadvantage of Basic Peak Detector
 - Op-Amp based Peak Detector
- Sample and Hold Circuit

Basic Peak Detector

Simple Peak detector circuit: (with practical diode)



Op-Amp based Peak Detector



Op-Amp based Peak Detector: Track Mode

During positive half cycle of input (ie when $V_{in} > 0$), output of opamp1 is positive i.e. $V_{o1} \rightarrow$ positive

This will turn OFF Diode D₁ & turn ON diode D₂.

Opamp1 sources current to charge the capacitor C via Diode D₂ to the peak value of input voltage V_{in} .

Output of opamp1 ie V_{o1} rides on diode drop voltage above output V_{out}

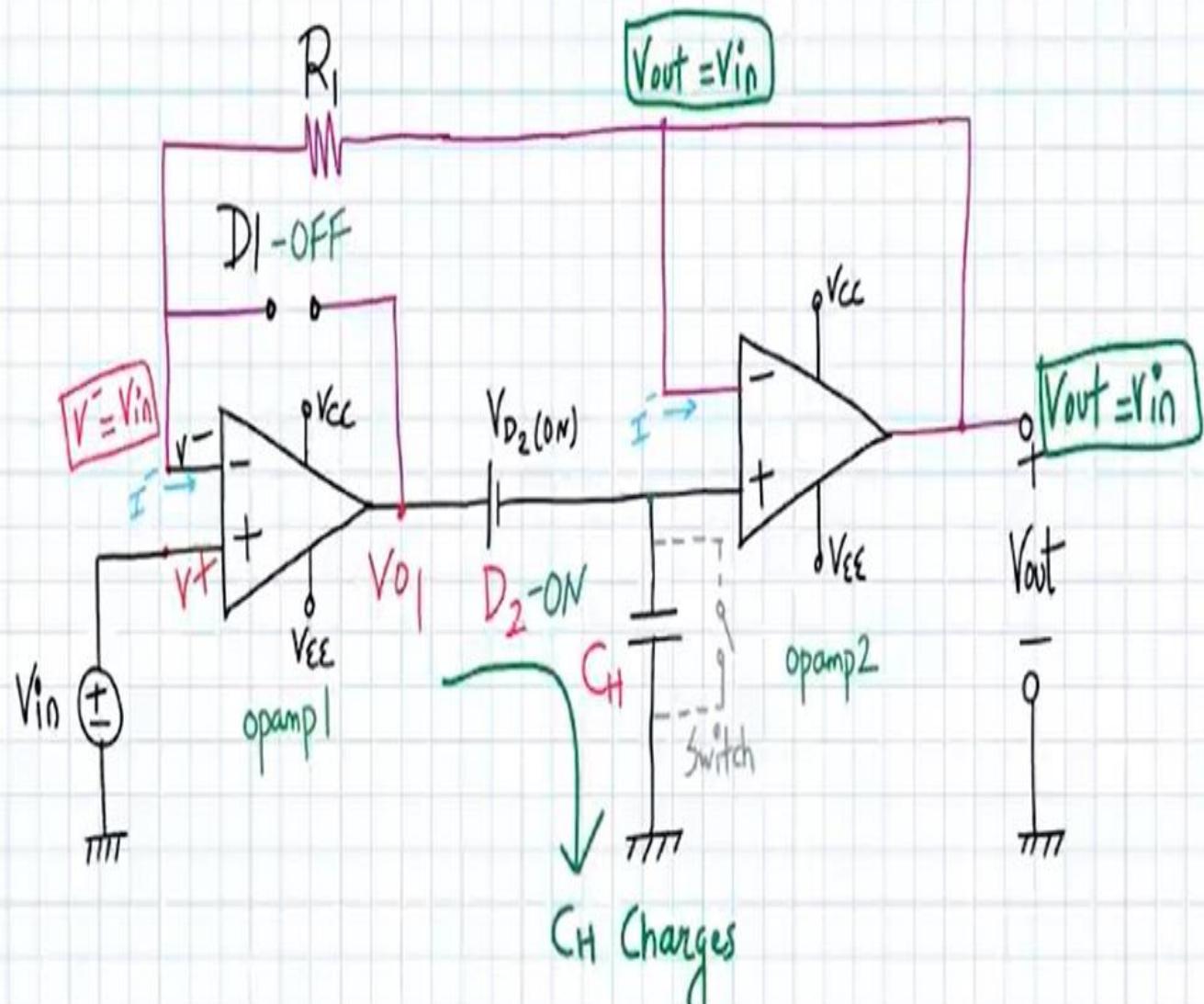
$$\text{i.e. } V_{o1} = V_{out} + V_{D_2, \text{ON}}$$

Opamp uses the feedback path D₂-Opamp2-R₁ to maintain a virtual short between its inputs.

Since no current flows through R₁, the result is that the output V_{out} will track input V_{in} . This is called the "TRACK MODE"

Opamp during track mode works in linear region

Scenario 1: TRACK MODE



Op-Amp based Peak Detector: Hold Mode

After input reaching peak, input V_{in} starts to decrease, causing the output V_{out} of opamp1 also to decrease.

Consequently, Diode D_2 turns OFF & diode turns ON, thus providing an alternative feedback path for opamp1.

For opamp1, by virtual-short concept

$$V^+ = V_{in}; V^- \approx V_{in}$$

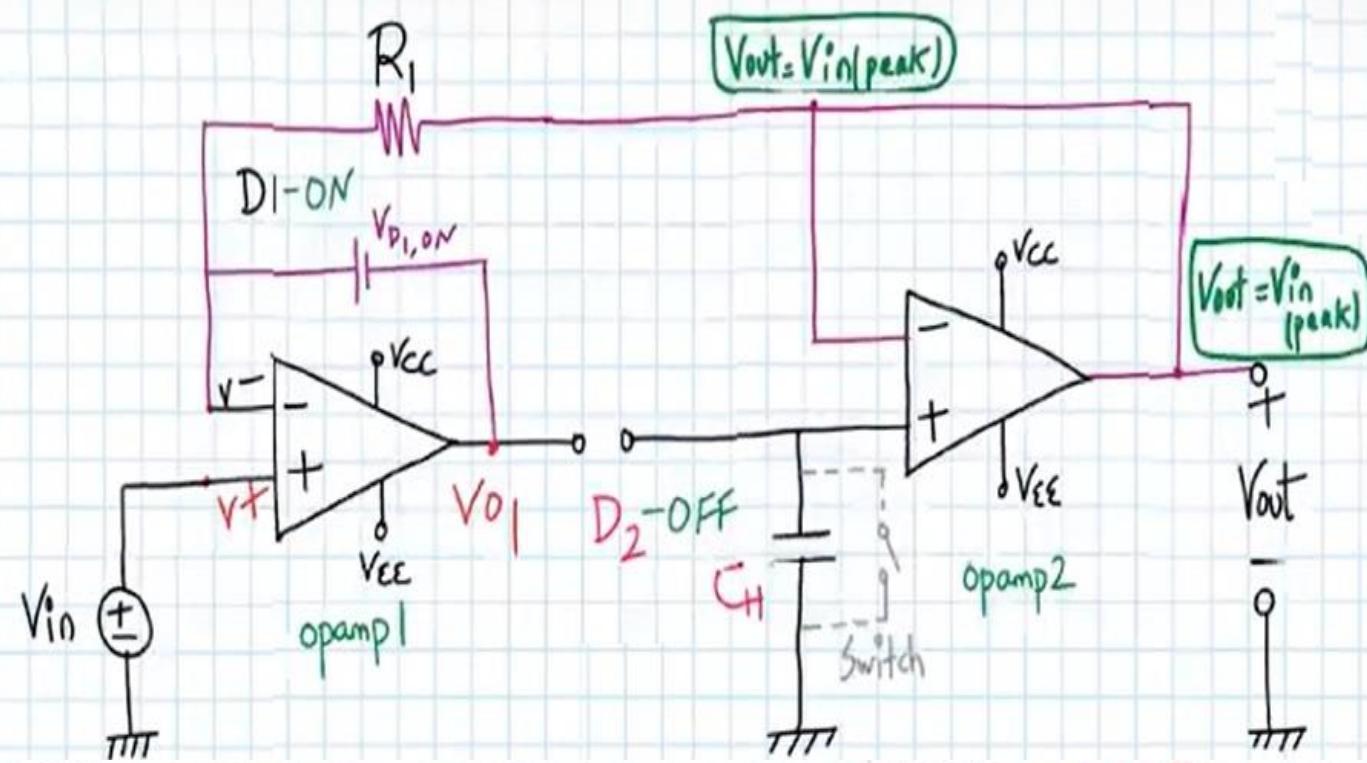
$$\therefore V_{O1} = V_{in} - V_{D1,ON}$$

i.e. The output of opamp1 now rises a diode drop below V_{in} .

After reaching the peak, input peak decreases, during this time, the capacitor C_H voltage remains constant;

i.e. the capacitor C_H will hold current peak value.

Scenario 2: HOLD MODE



This mode of operation is called "HOLD MODE"

The capacitor C_H does not discharge, because of the high input impedance of the voltage follower opamp2.

\therefore Output voltage V_{out} remains constant until V_{in} increases again.

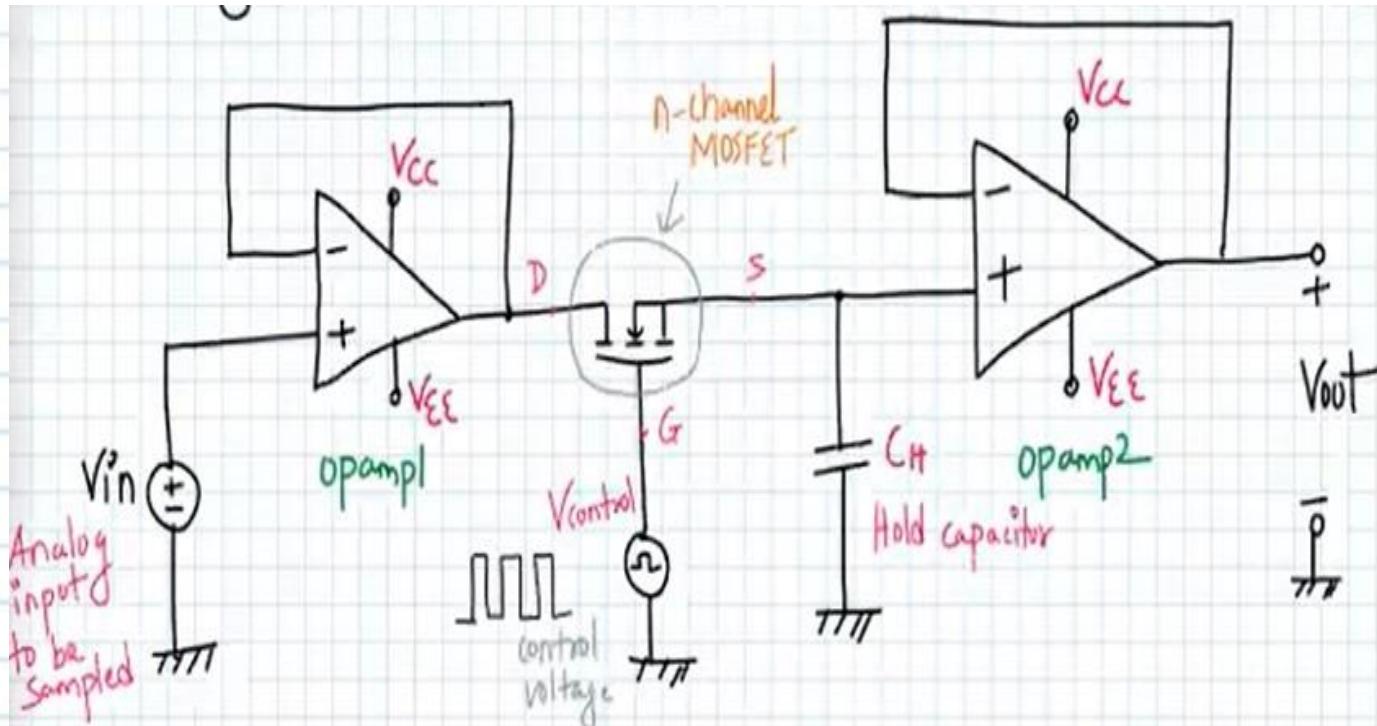
SAMPLE AND HOLD CIRCUIT

① Opamp1 & Opamp2 are working as buffer/voltage followers

② N-channel E-MOSFET works as a switch that is controlled by control voltage $V_{Control}$.

③ Hold capacitor C_H job is to hold the sampled (stores the charge) input signal value.

④ A analog signal V_{in} to be sampled is applied to non-inverting input of opamp1 (ie to the drain of E-MOSFET) & the control voltage $V_{Control}$ (in the form of pulses(samples)) is applied to the gate terminal of E-MOSFET.



Applications of sample & Hold circuit:

- ① Analog to digital converter circuits (ADCs)
- ② Digital Imaging systems (as a part of ADC)
- ③ Set-Top Boxes (as a part of ADC)
- ④ Digital interfacing circuit
- ⑤ Pulse code modulation systems

SAMPLE AND HOLD CIRCUIT (Sample/Track Mode)

- ① During the track mode, E-MOSFET is "ON" & it behaves as a closed switch (since control voltage applied at gate is HIGH) (+5V)

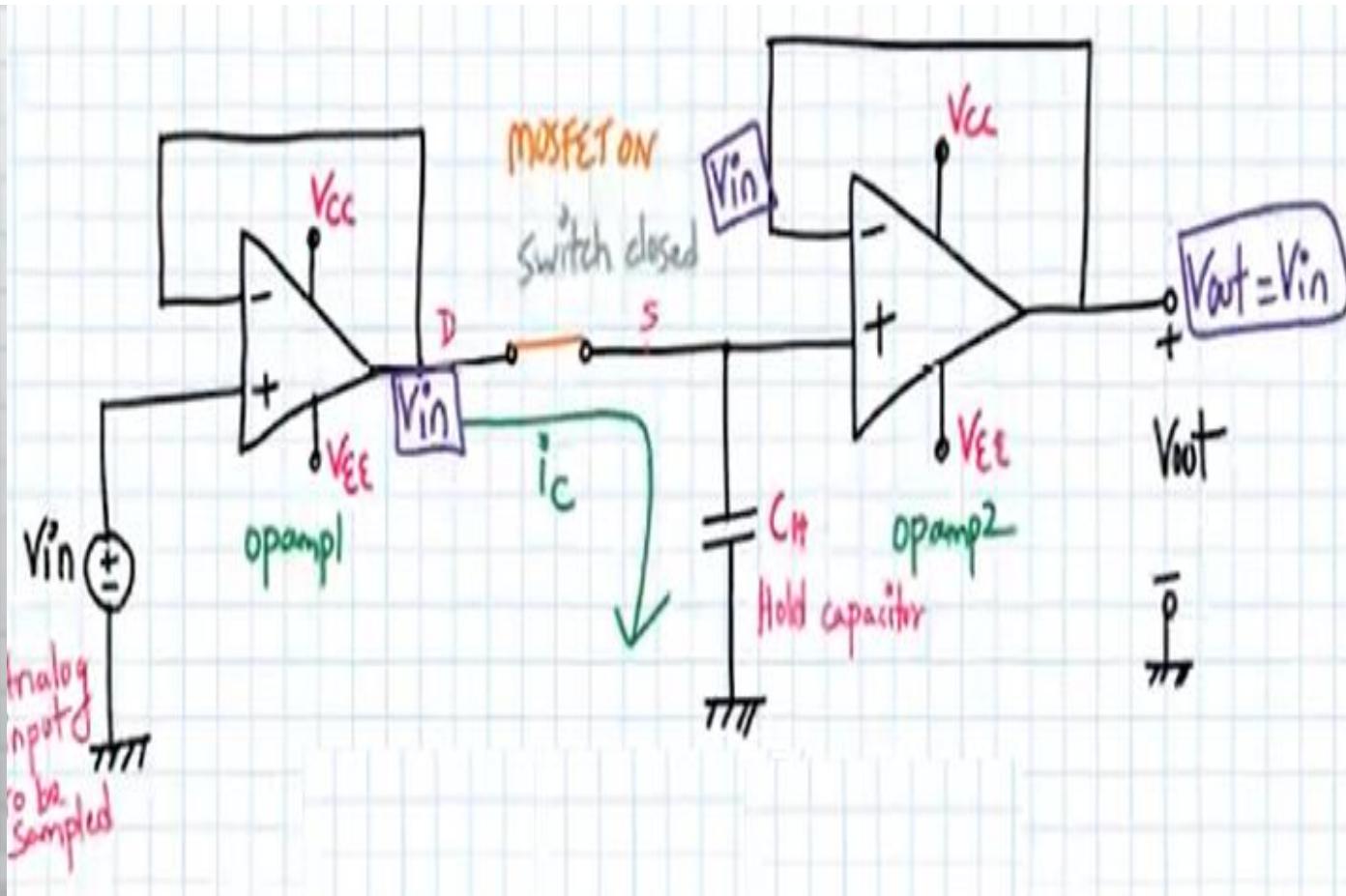
② Opamp acts as a voltage-follower & since the switch is closed. (MOSFET ON)

③ Capacitor C_H charges to the instantaneous value of the input V_{in}

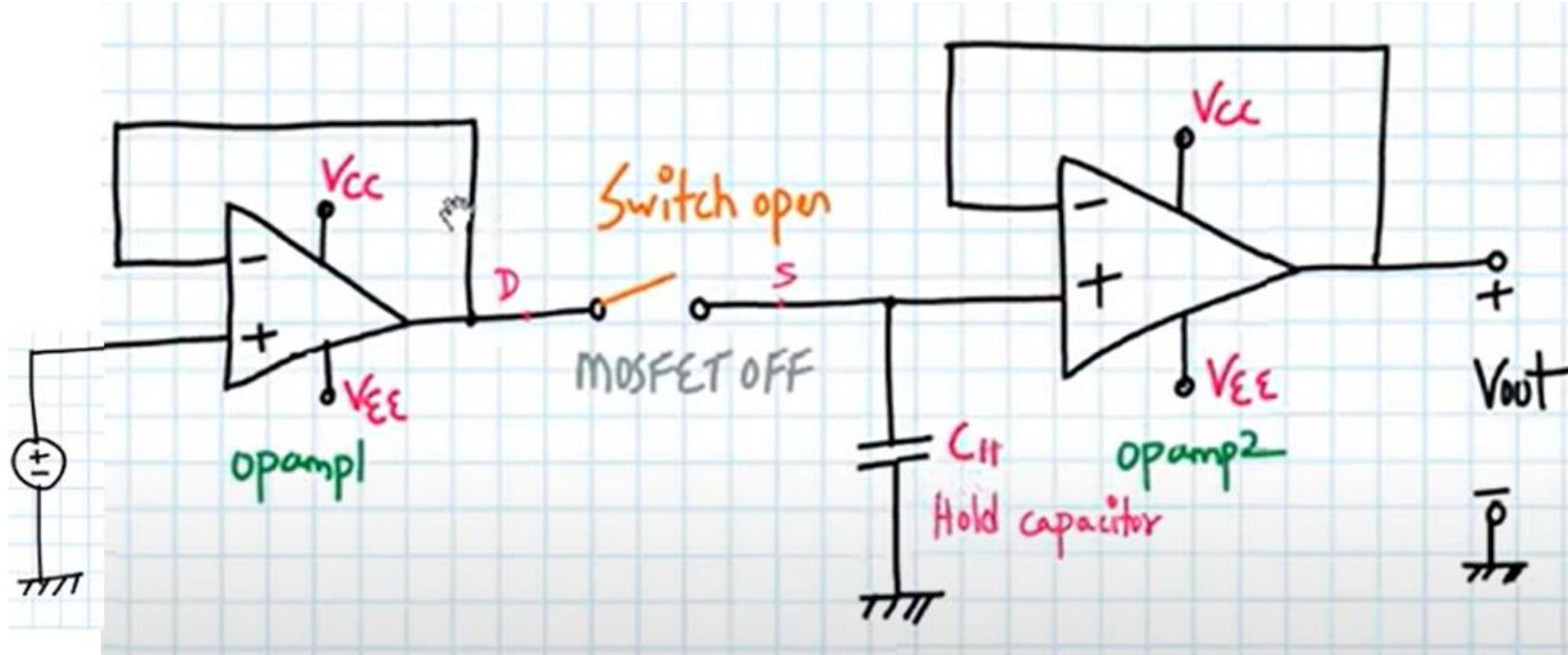
C_H charges with a charging time constant $T_C = (R_o + R_{on}) \times C_H$

$R_o \rightarrow$ O/P resistance of voltage follower opamp (which is low)

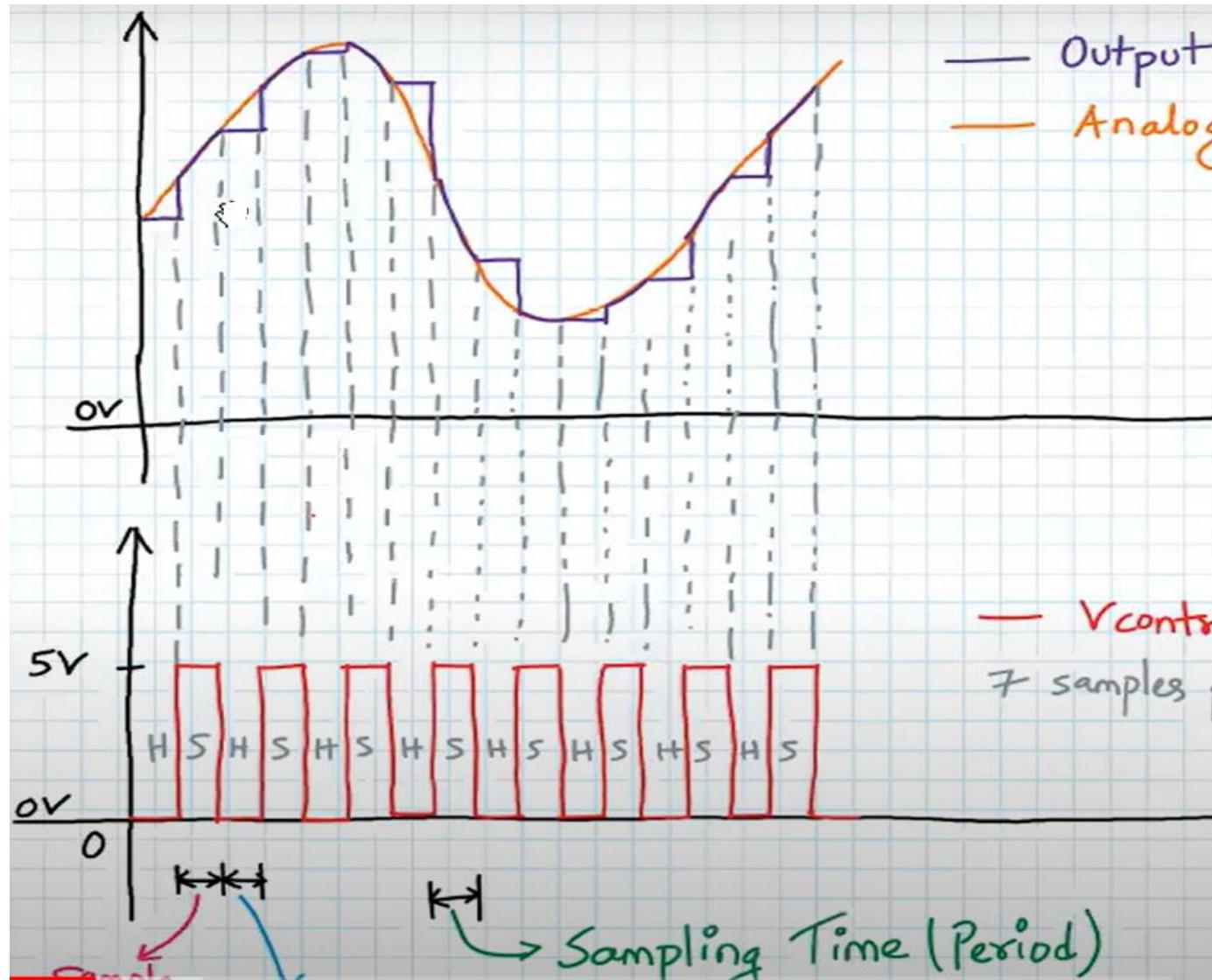
$T_C = R_{on} \times C_H$



SAMPLE AND HOLD CIRCUIT (HOLD MODE)



SAMPLE AND HOLD CIRCUIT (HOLD MODE)



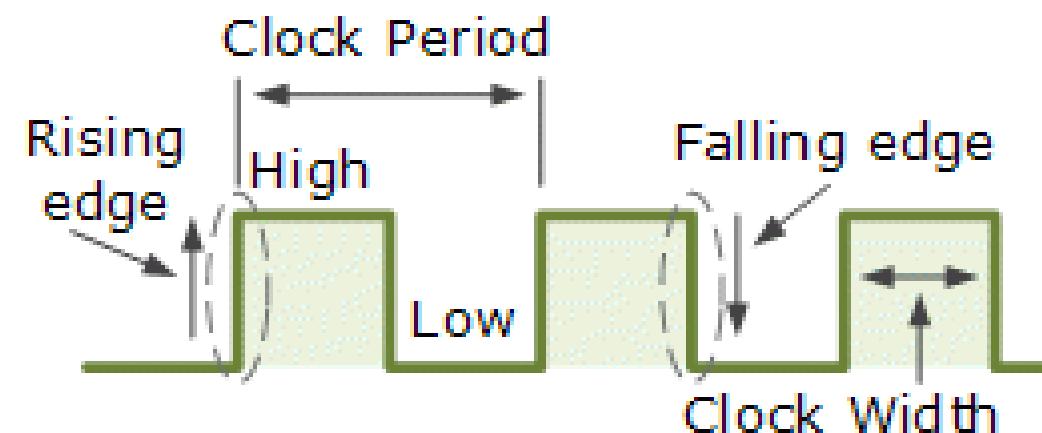
LIC: LECTURE

Signal Generators

- Multivibrator: Need and Different Types
 - Astable Multivibrator
 - Monostable Multivibrator
 - Bistable Multivibrator
- Astable Multivibrator
 - Working Principal
 - Calculation of Time Period
 - Design Example

Multivibrator

- The Multivibrator is the electronic circuit which is used to implement two state devices like oscillator, timer and flip-flops.
- Here, the two states refer to the two voltage levels of the Multivibrators.
- Depending upon the number of stages, the multivibrator can be divided into three types.

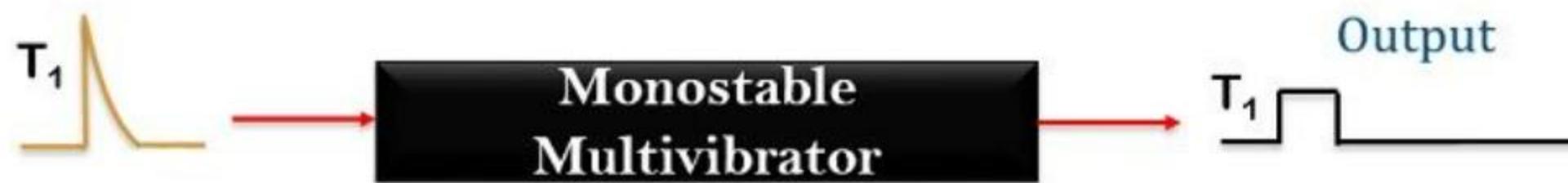


Multivibrator

Astable – A *free-running multivibrator* that has NO stable states but switches continuously between two states this action produces a train of square wave pulses at a fixed frequency. (Eg. Relaxation Oscillator)



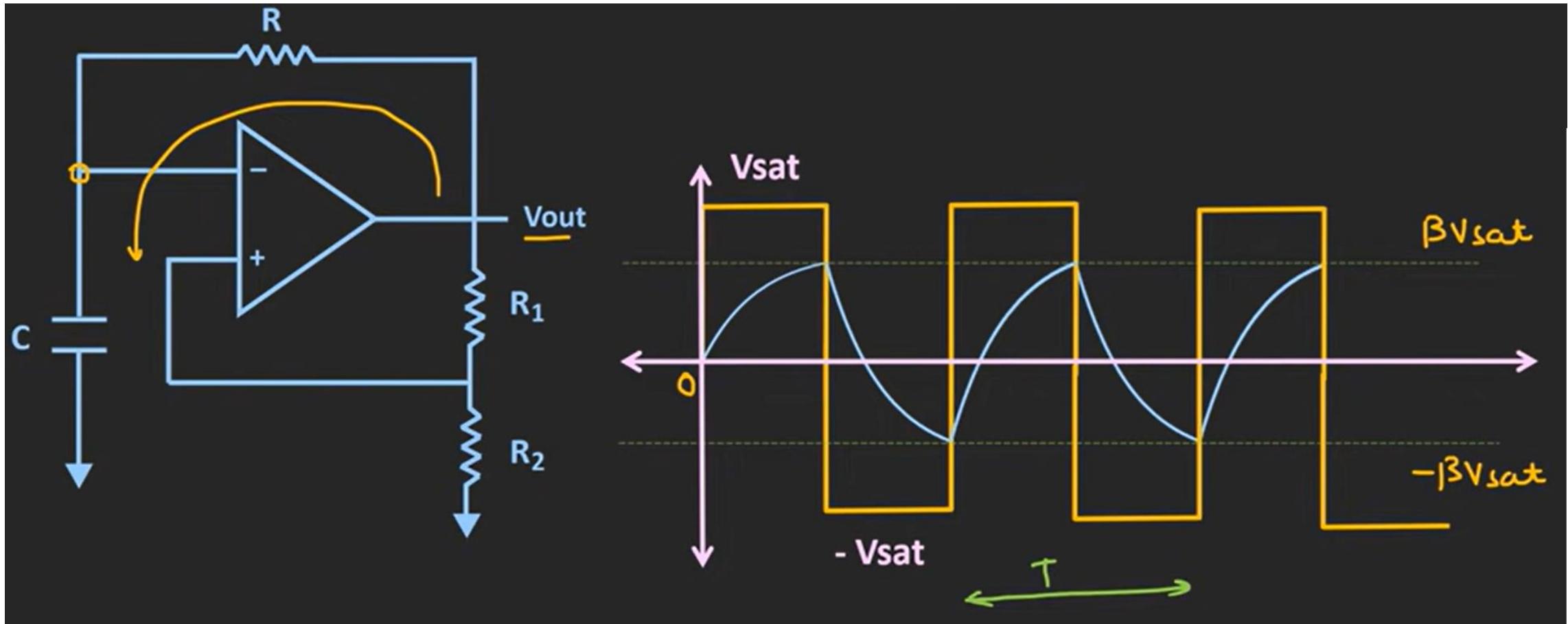
Monostable – A *one-shot multivibrator* that has only ONE stable state and is triggered externally with it returning back to its first stable state. (Eg. Timer applications)

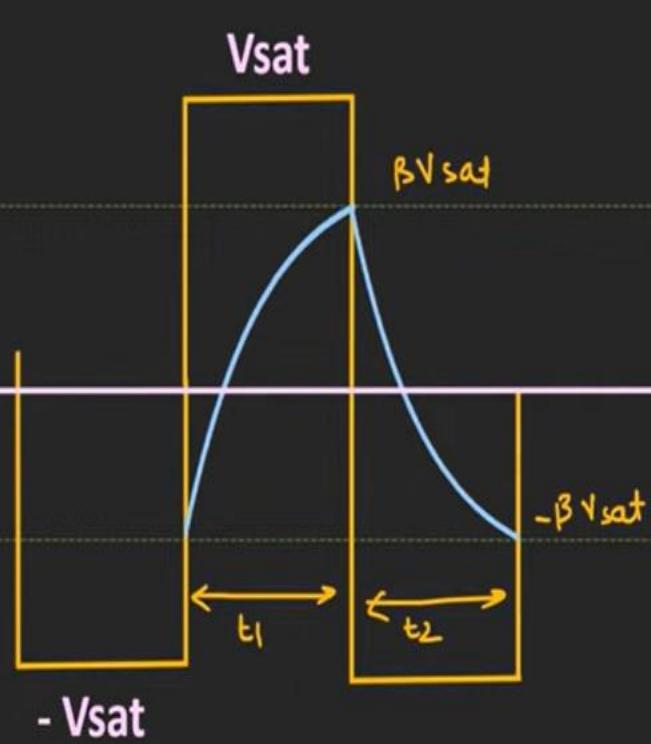


Bistable – A *flip-flop* that has TWO stable states that produces a single pulse either positive or negative in value. (Eg.-Sequential Circuits)



ASTABLE MULTIVIBRATOR (Free Running Multivibrator)





ASTABLE MULTIVIBRATOR

Derivation of Time Period
($T=t_1+t_2$)

Calculation of charging time- t_1

$$V_C(t) = V_{Final} + [V_{Initial} - V_{Final}] e^{-t/RC}$$

$$V_{Final} = V_{sat}$$

$$V_{in} = -\beta V_{sat}$$

$$V_C(t_1) = V_{sat} + [-\beta V_{sat} - V_{sat}] e^{-t_1/RC}$$

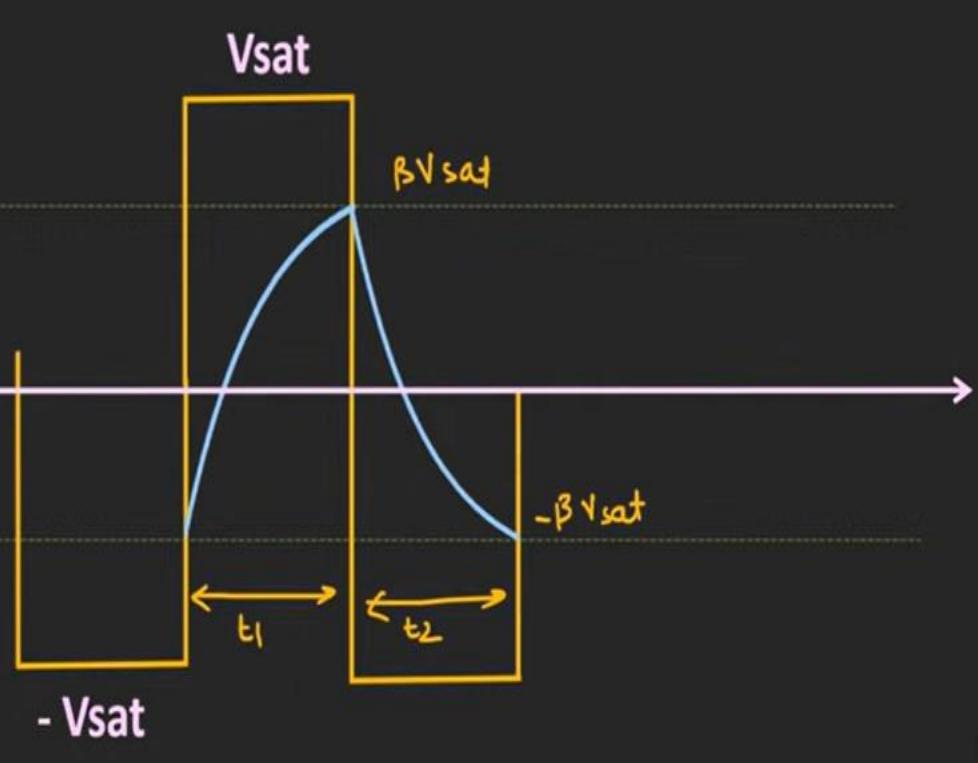
$$\beta V_{sat} = V_{sat} - [1 + \beta] V_{sat} e^{-t_1/RC}$$

$$\beta - 1 = -[1 + \beta] e^{-t_1/RC}.$$

$$\left[\frac{1 - \beta}{1 + \beta} \right] = e^{-t_1/RC}$$

$$\Rightarrow t_1 = -RC \ln \left[\frac{1 - \beta}{1 + \beta} \right]$$

$$t_1 = RC \ln \left[\frac{1 + \beta}{1 - \beta} \right]$$



$$V_C(t) = V_{Final} + [V_{Initial} - V_{Final}] e^{-t/RC}$$

$$V_{Initial} = \beta V_{sat} \rightarrow -\beta V_{sat}$$

$$V_{Final} = -V_{sat}$$

$$V_C(t_2) = -V_{sat} + [\beta V_{sat} - (-V_{sat})] e^{-t_2/RC}$$

$$-\beta V_{sat} = -V_{sat} + V_{sat} \times (1+\beta) \times e^{-t_2/RC}$$

$$\frac{1-\beta}{1+\beta} = e^{-t_2/RC}$$

$$\Rightarrow t_2 = RC \times \ln \left(\frac{1+\beta}{1-\beta} \right)$$

$$T = t_1 + t_2 = 2t_1 = 2RC \ln \left(\frac{1+\beta}{1-\beta} \right)$$

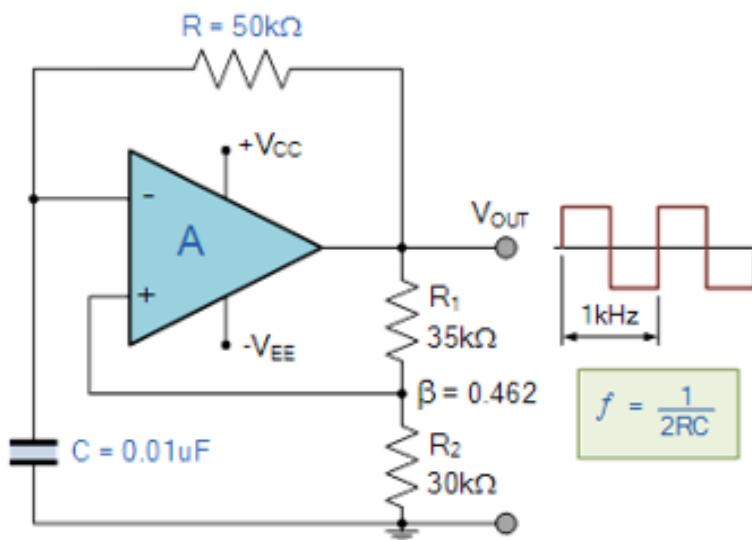
ASTABLE MULTIVIBRATOR

Derivation of Time Period
($T=t_1+t_2$)

Calculation of discharging time-t₂

Design Problem-1

An op-amp multivibrator circuit is constructed using the following components. $R_1 = 35\text{k}\Omega$, $R_2 = 30\text{k}\Omega$, $R = 50\text{k}\Omega$ and $C = 0.01\mu\text{F}$ and powered with $V_{cc}=11\text{V}$, $V_{EE}=-11\text{V}$ DC supply. Calculate the circuits frequency of oscillation.



$$\beta = \frac{R_2}{R_1 + R_2} = \frac{30\text{k}\Omega}{35\text{k}\Omega + 30\text{k}\Omega} = 0.462$$

$$T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right) = 2RC \ln\left(\frac{1+0.462}{1-0.462}\right)$$

$$T = 2 \times (50\text{k}\Omega \times 0.01\mu\text{F}) \times \ln(2.717)$$

$$\therefore T = 0.001 \times 1 = 0.001\text{Sec or } 1\text{mS}$$

$$\therefore f = \frac{1}{T} = \frac{1}{0.001} = 1,000\text{Hz or } 1\text{kHz}$$