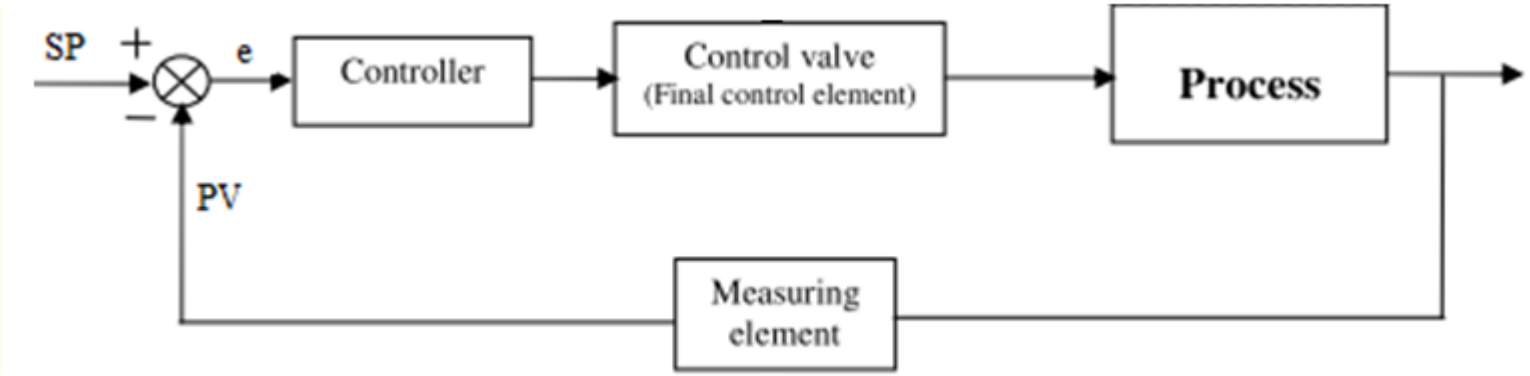
Components of a Closed Loop Control System

Closed loop control system:

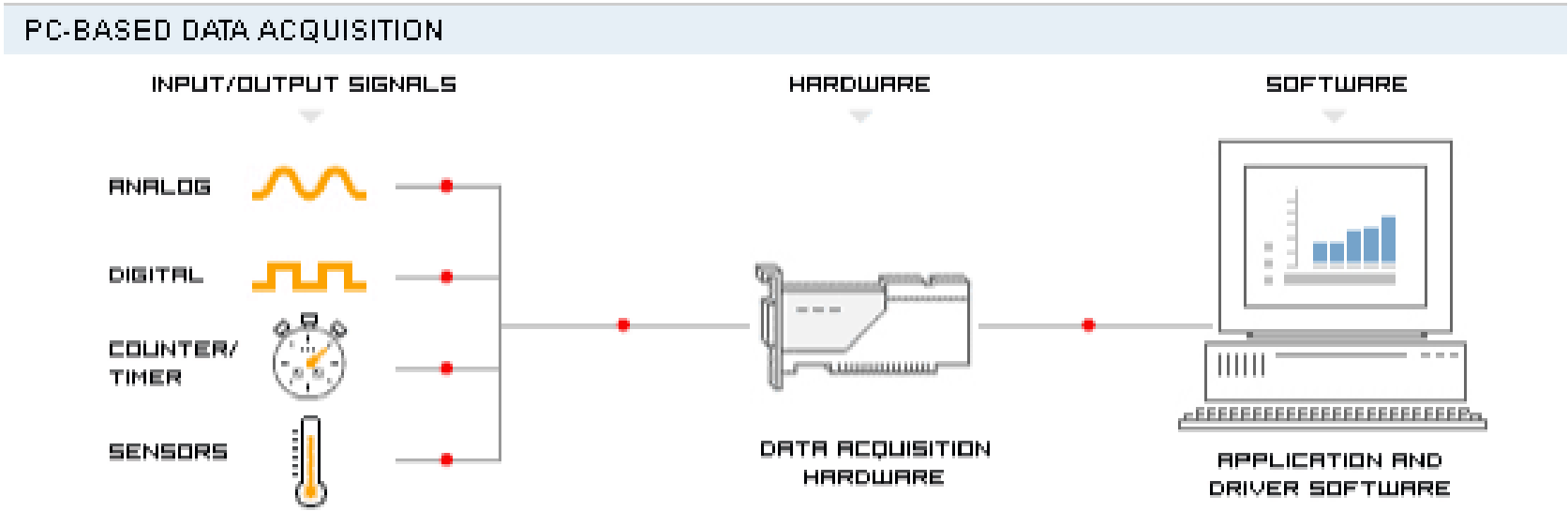


Components:

- Plant / Process
- Sensor
- Controller
- Actuator

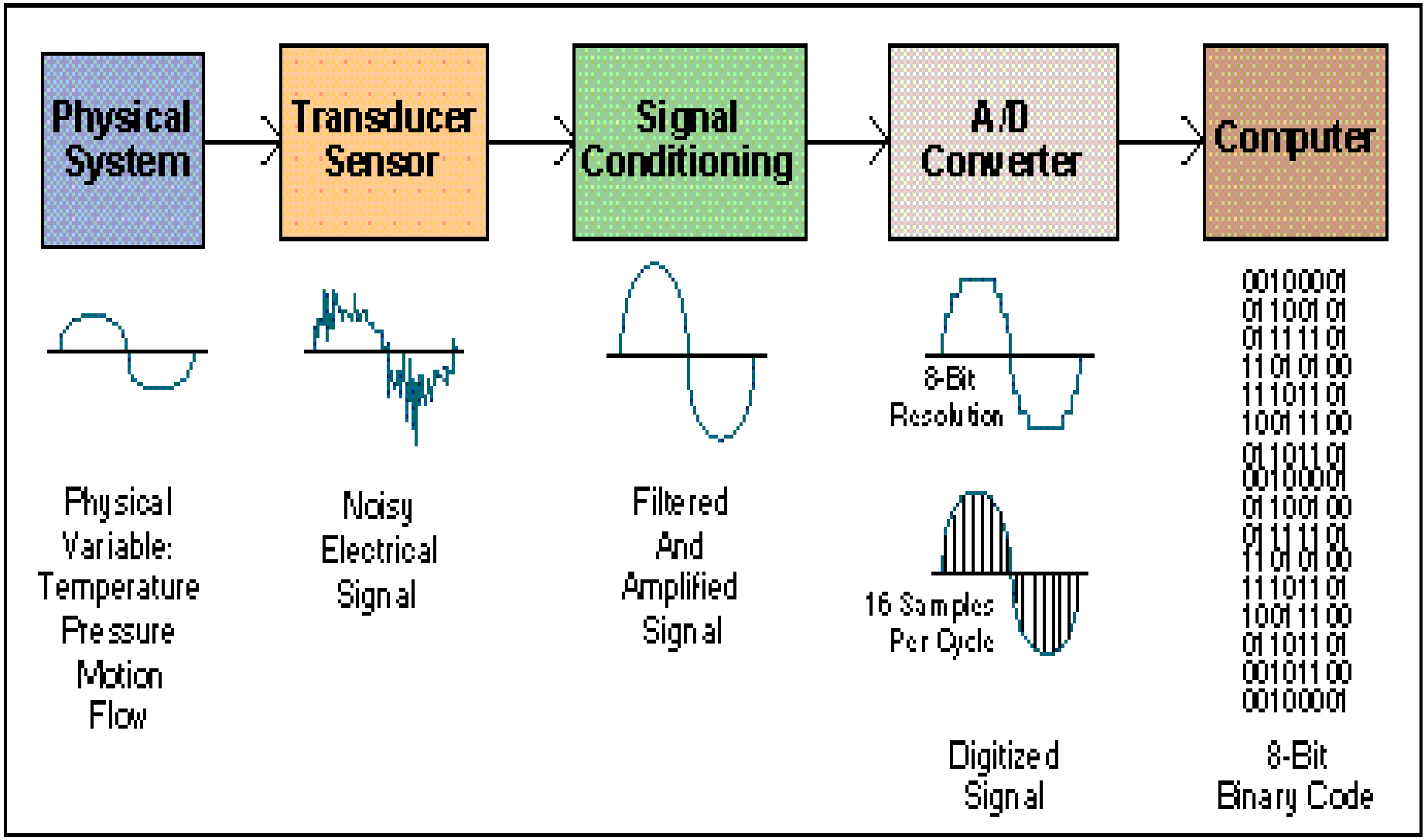
ADC & DACs ?

Components of a Closed Loop Control System



- DAQ typically convert analog into digital values and digital to analog.
- data acquisition system consists of :
  - Sense physical variables
  - Condition the electrical signal
  - Convert the signal into a digital format
  - Process, analyze, store, and display

Block Diagram



DAQ System

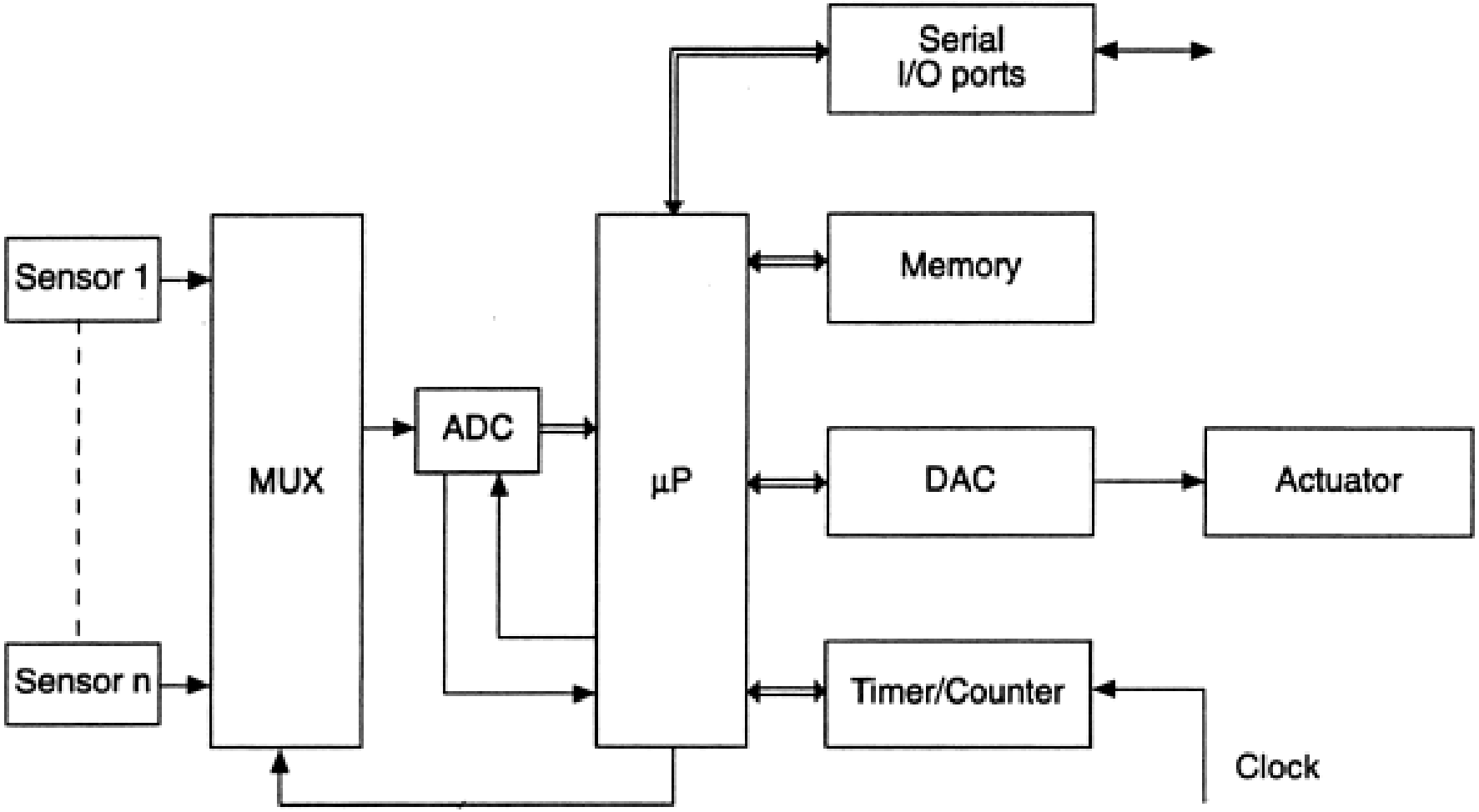
- Three major groups:
  - ✓ Direct Digital Control (DDC)
  - ✓ Supervisory Control
  - ✓ Distributed Control Systems

Direct Digital Control (DDC)

- directly interfaces to the process for data acquisition and control purpose.
- it has necessary hardware for directly interfacing (opto-isolator, signal conditioner, ADC, etc.)
- it should also have memory and arithmetic capability to execute required P, P+I, P+I+D control strategy.

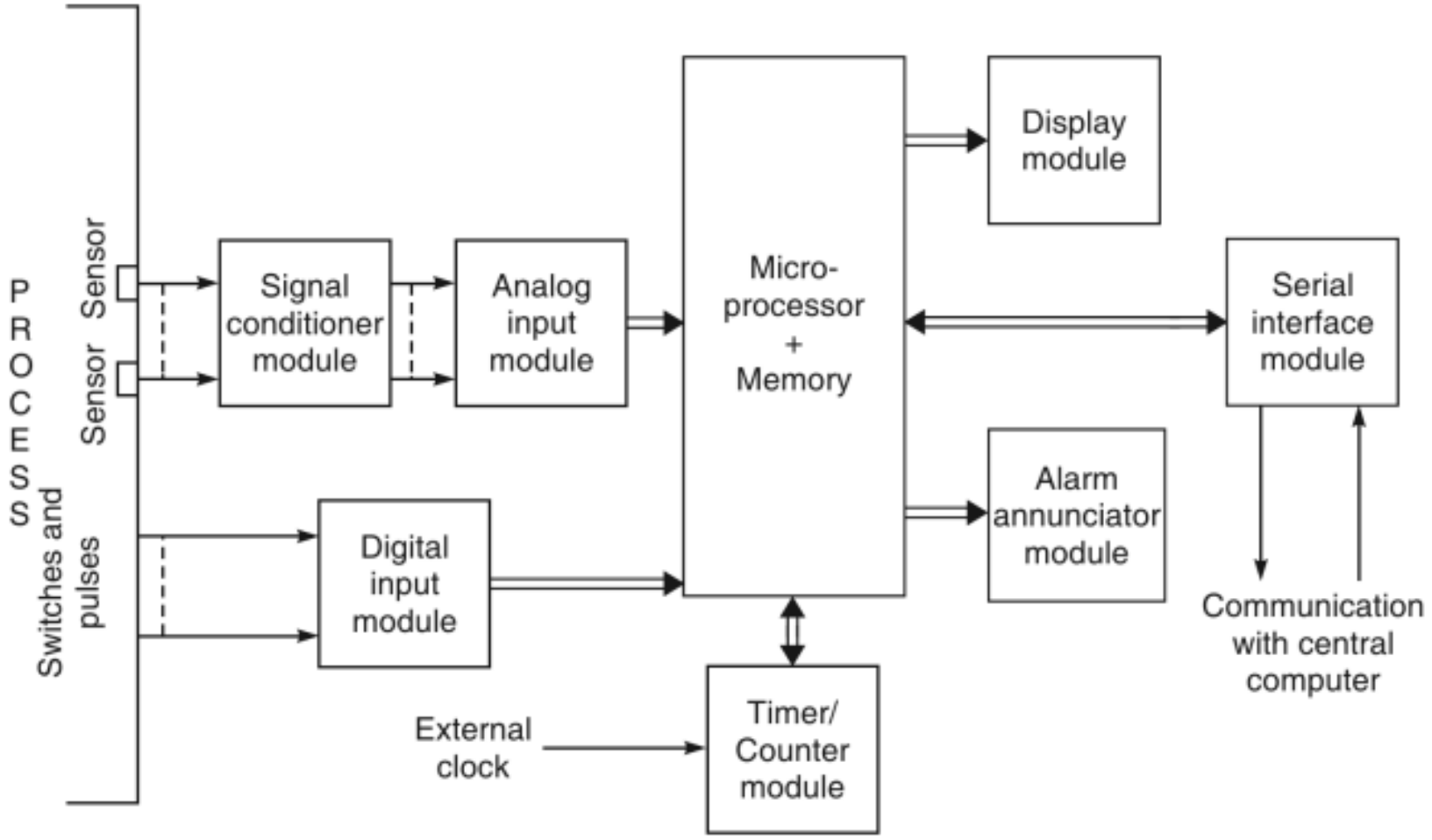
DAQ System

Direct Digital Control:



DAQ System

Supervisory Control:



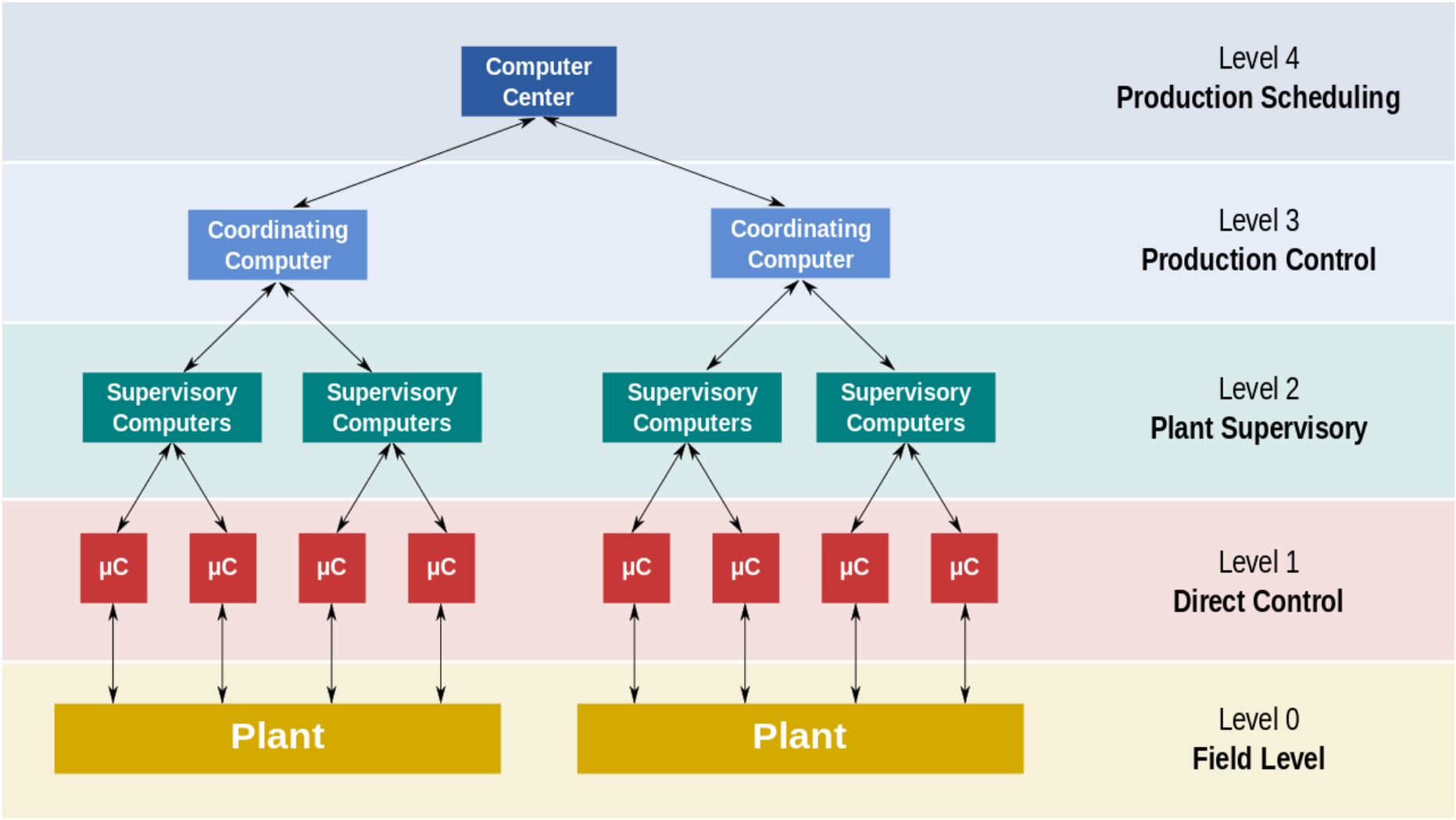
Supervisory control and data acquisition system

DAQ System

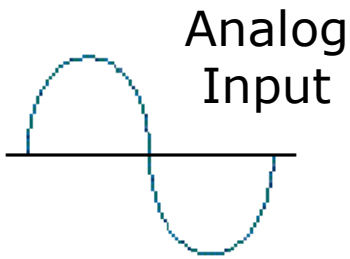
Distributed Control System:

- uses *custom designed processors* as controllers
- uses both proprietary interconnections and *standard communications protocol* for communication.
- *input and output modules* form component parts of the DCS.
- processor receives information from input modules and sends information to output modules.
- inputs and outputs can be either analog signal which are continuously changing or discrete signals
- buses connect the distributed controllers with the central controller and finally to the *Human–machine interface (HMI)* or control consoles

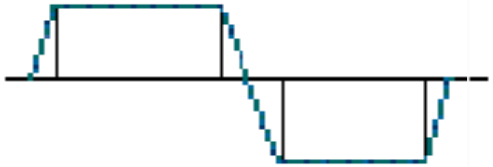
DAQ System

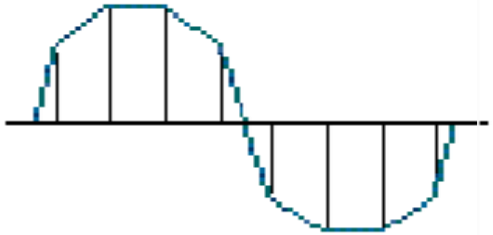

Computer Center
Coordinating Computer
Coordinating Computer
Supervisory Computers
Supervisory Computers
Supervisory Computers
Supervisory Computers
µC
µC
µC
µC
µC
µC
µC
µC
Plant
Plant
Level 4
Production Scheduling
Level 3
Production Control
Level 2
Plant Supervisory
Level 1
Direct Control
Level 0
Field Level

Sampling Rate



4 Samples/cycle





8 Samples/cycle

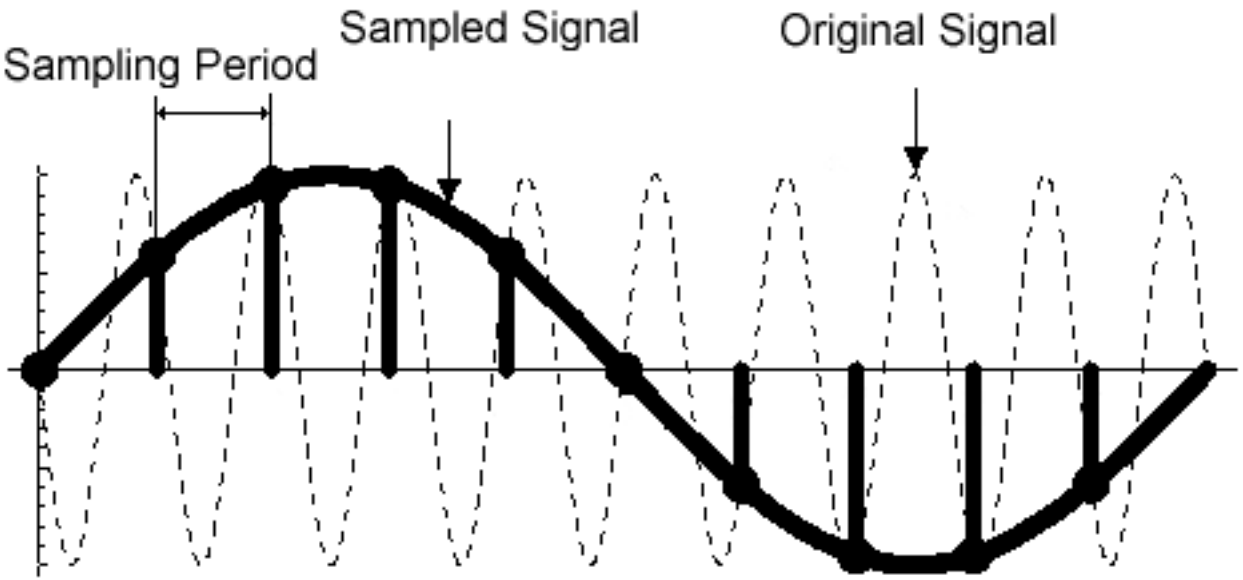
16 Samples/cycle

The higher the sampling rate, the better

Not obviously true

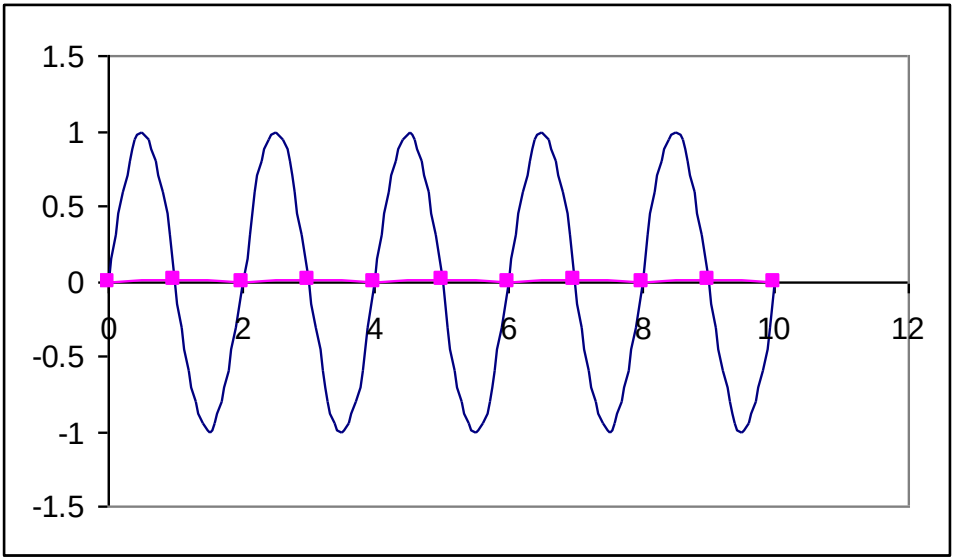
Aliasing

- Acquired signal gets distorted if sampling rate is too small.

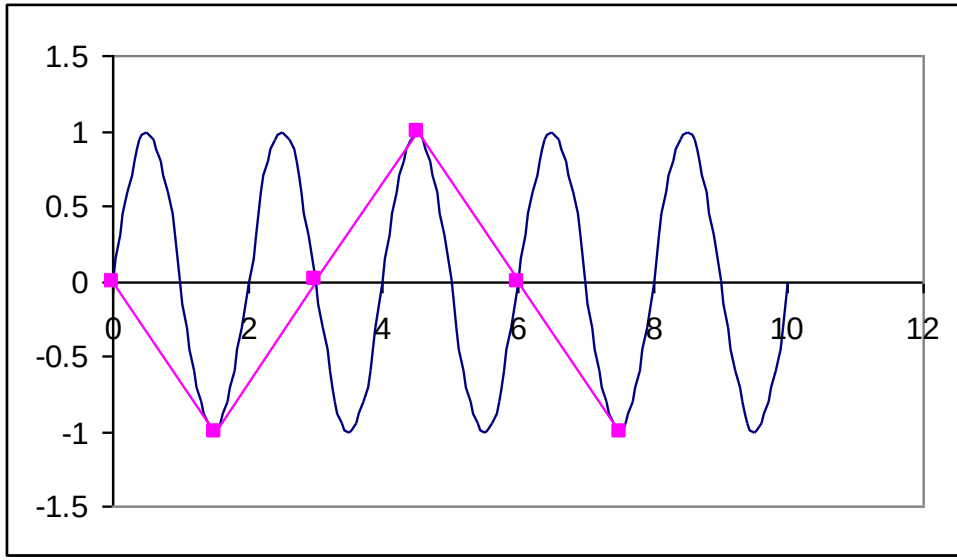


Sampling Theorem

- The highest frequency (The so-called Nyquist frequency) which can be accurately represented is one-half of the sampling rate.

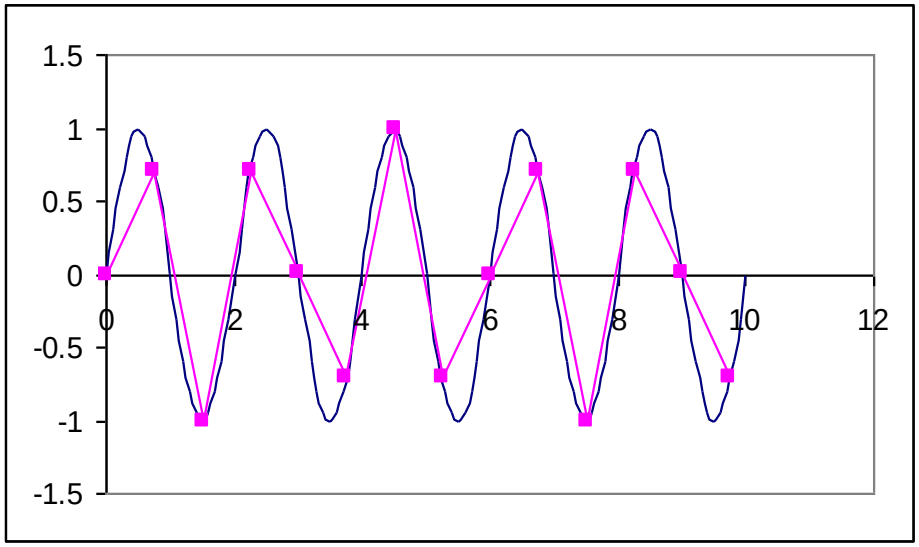


Sampling Frequency = 1/2 X Wave Frequency

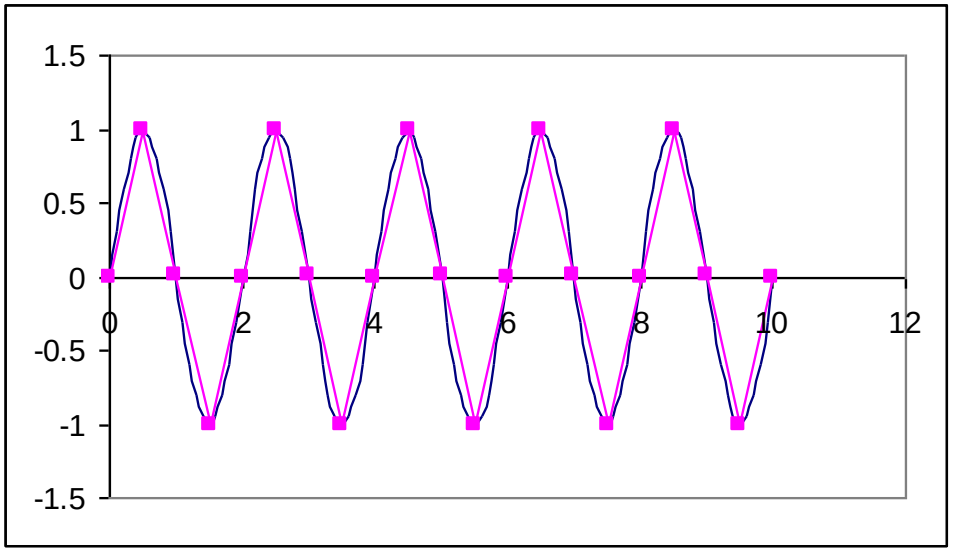


Sampling Frequency = 1/3 X Wave Frequency

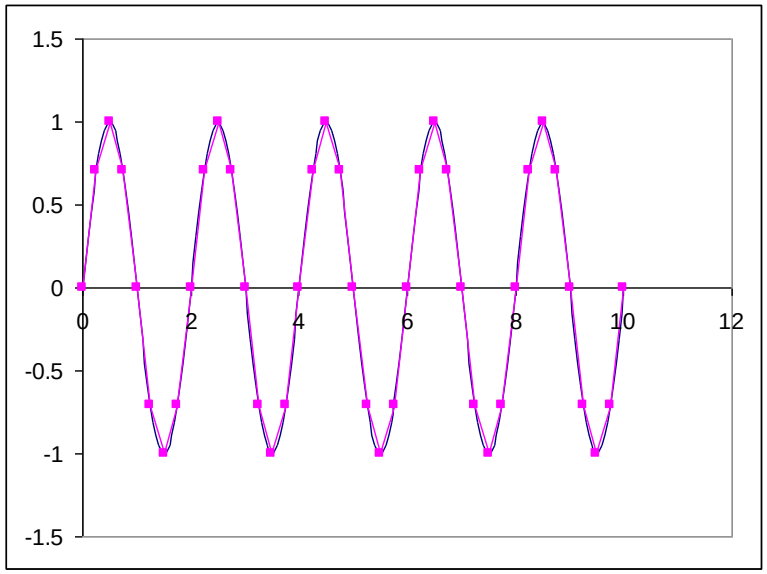
Sampling Theorem



Sampling Frequency = 2/3 X Wave Frequency



Sampling Frequency = Wave Frequency



Sampling Frequency = 2 X Wave Frequency

Throughput

- Effective rate of each individual channel is inversely proportional to the number of channels sampled.

- Example:
  - 100 KHz maximum.
  - 16 channels.

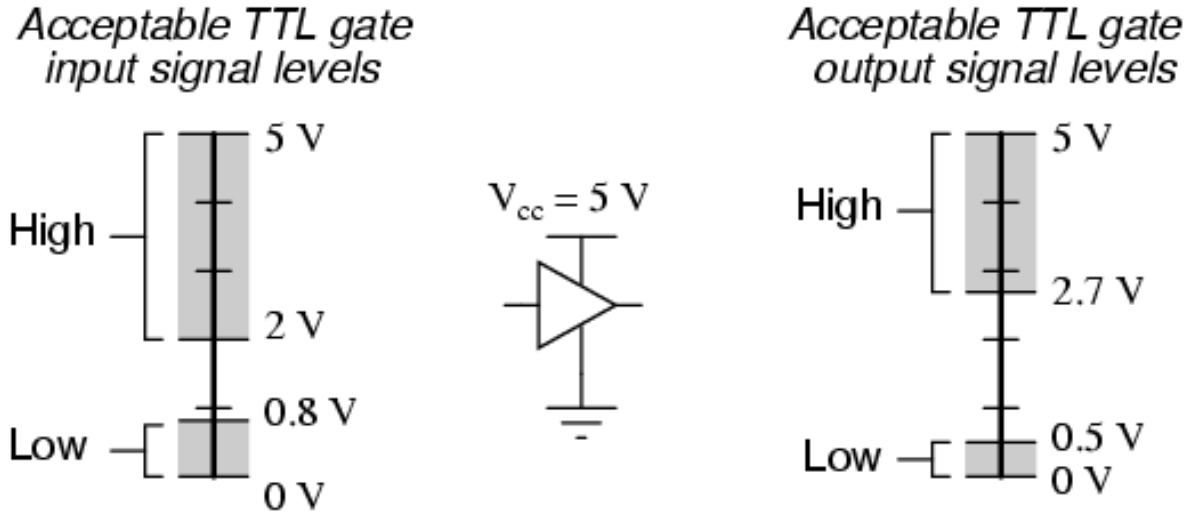
100 KHz/16 = 6.25 KHz per channel

Logic Level

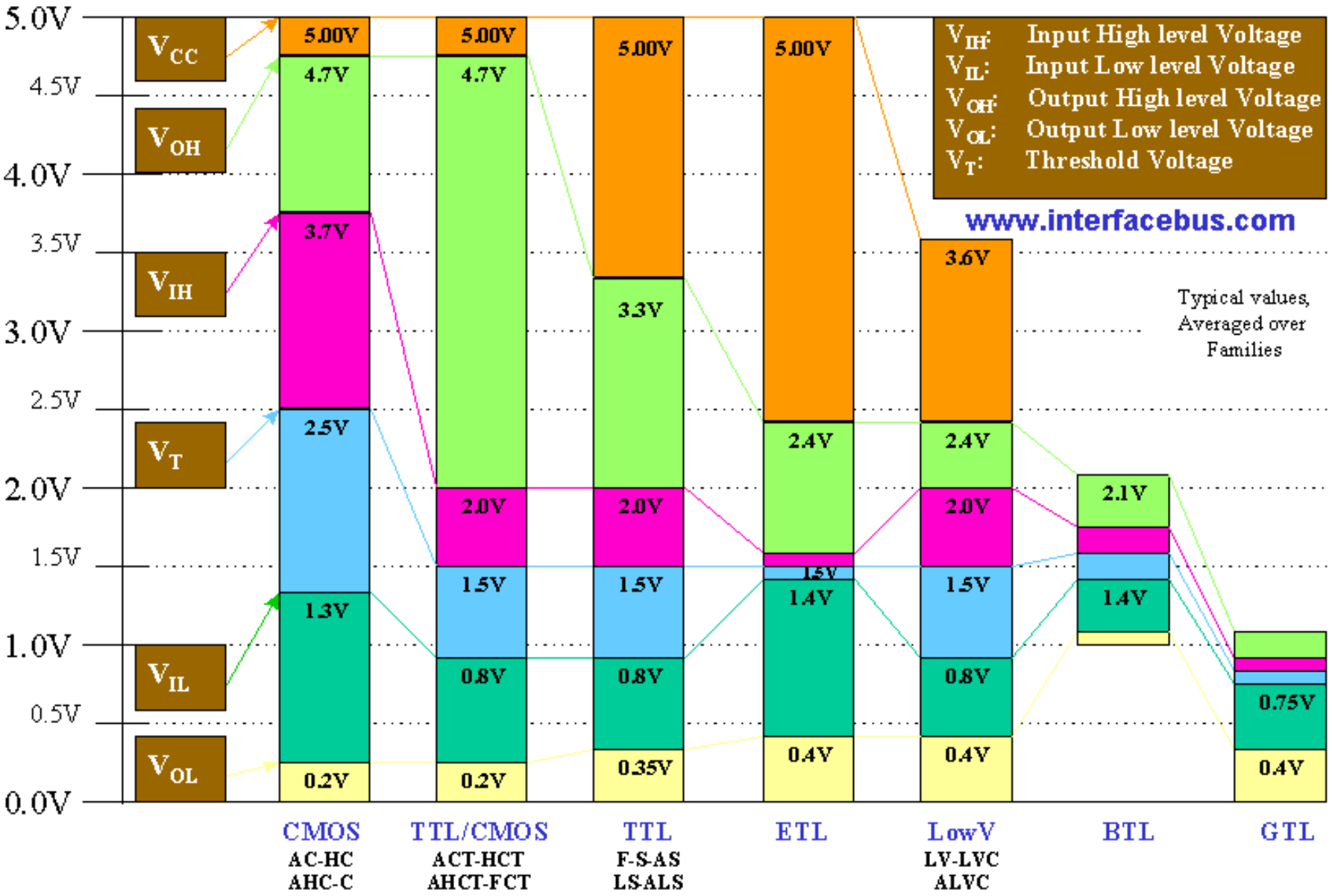
- Logic gate circuits are designed to input and output only two types of signals:
  - "high" (1) and "low" (0) as represented by a variable voltage: full power supply voltage for a "high" state and zero voltage for a "low" state.
- In a perfect world, all logic circuit signals would exist at these extreme voltage limits, and never deviate from them (i.e., less than full voltage for a "high," or more than zero voltage for a "low").
- However, in reality, logic signal voltage levels rarely attain these perfect limits due to stray voltage drops in the transistor circuitry.

Logic Level

- "Acceptable" input signal voltages - 0 to 0.8 volts for a "low" logic state, and 2 volts to 5 volts for a "high" logic state.
- "Acceptable" output signal voltages range from 0 volts to 0.5 volts for a "low" logic state, and 2.7 volts to 5 volts for a "high" logic state.



Logic Level


5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
V_{CC}
V_{OH}
V_{IH}
V_T
V_{IL}
V_{OL}
V_{IH}: Input High level Voltage
V_{IL}: Input Low level Voltage
V_{OH}: Output High level Voltage
V_{OL}: Output Low level Voltage
V_T: Threshold Voltage
www.interfacebus.com
Typical values, Averaged over Families
5.00V
4.7V
3.7V
2.5V
1.3V
0.2V
5.00V
4.7V
2.0V
1.5V
0.8V
0.2V
5.00V
3.3V
2.0V
1.5V
0.8V
0.35V
5.00V
2.4V
1.5V
1.4V
0.4V
3.6V
2.4V
2.0V
1.5V
0.8V
0.4V
2.1V
1.4V
0.75V
0.4V
CMOS
AC-HC
AHC-C
TTL/CMOS
ACT-HCT
AHCT-FCT
TTL
F-S-AS
LS-ALS
ETL
LowV
LV-LVC
ALVC
BTL
GTL

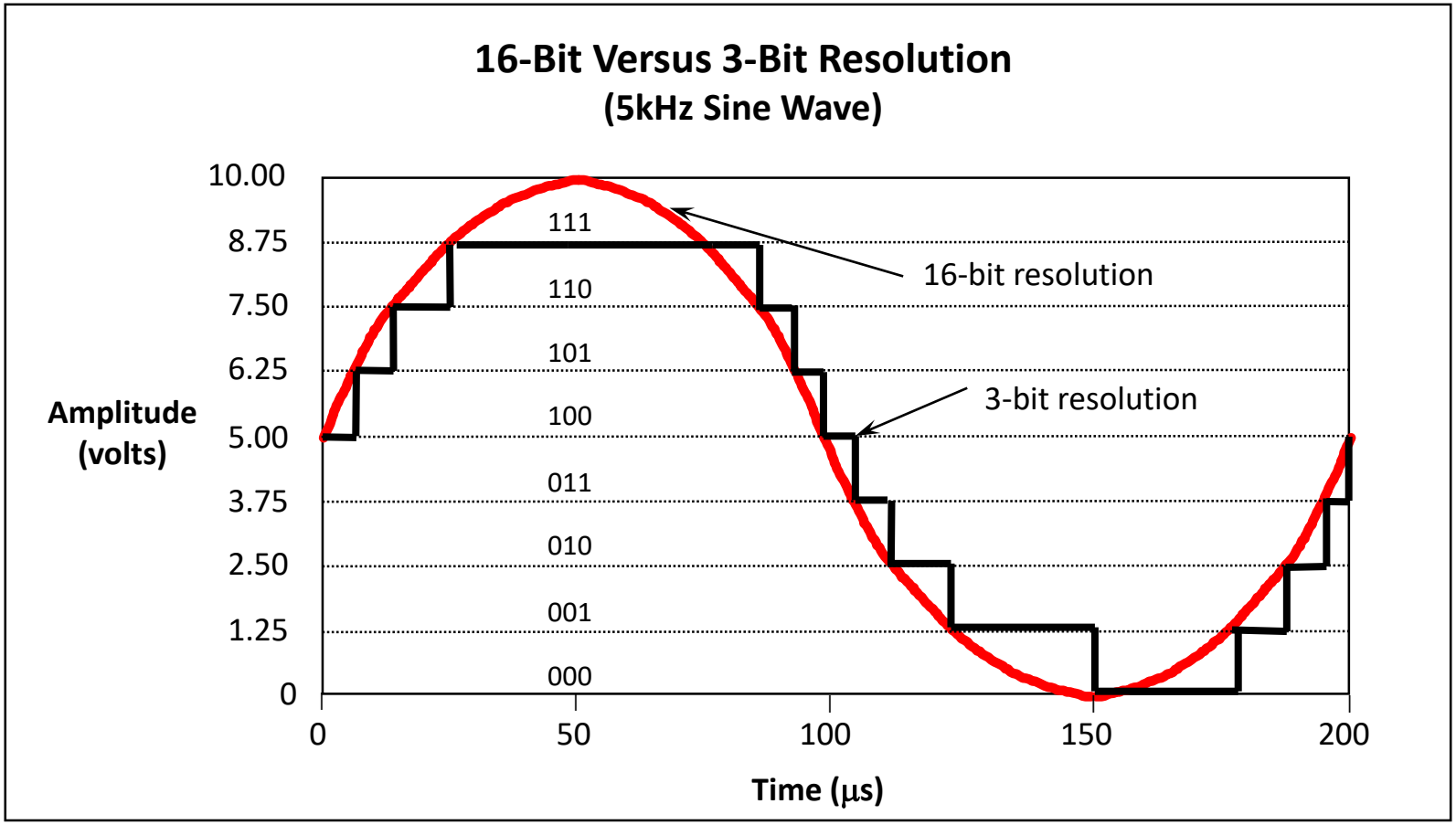
Resolution

- Number of bits the ADC uses to represent a signal
- Resolution determines how many different voltage changes can be measured
- Example: 12-bit resolution

  No. of levels = $2^{resolution}$ = 2^{12} = 4,096 levels

- Larger resolution = more precise representation of your signal

Resolution



– 3-bit resolution can represent 8 voltage levels
– 16-bit resolution can represent 65,536 voltage levels

Resolution

- Resolution = Amplitude / No. of Levels
- 3 Bit ADC with input amplitude of 10V can yield a resolution of

$$10V / 8 = 1.25V$$

- 16 Bit ADC with input amplitude of 10V can yield a resolution of

$$10V / 65536 = 152\ \mu V$$

- 12 Bit ADC with input amplitude of 10V can yield a resolution of

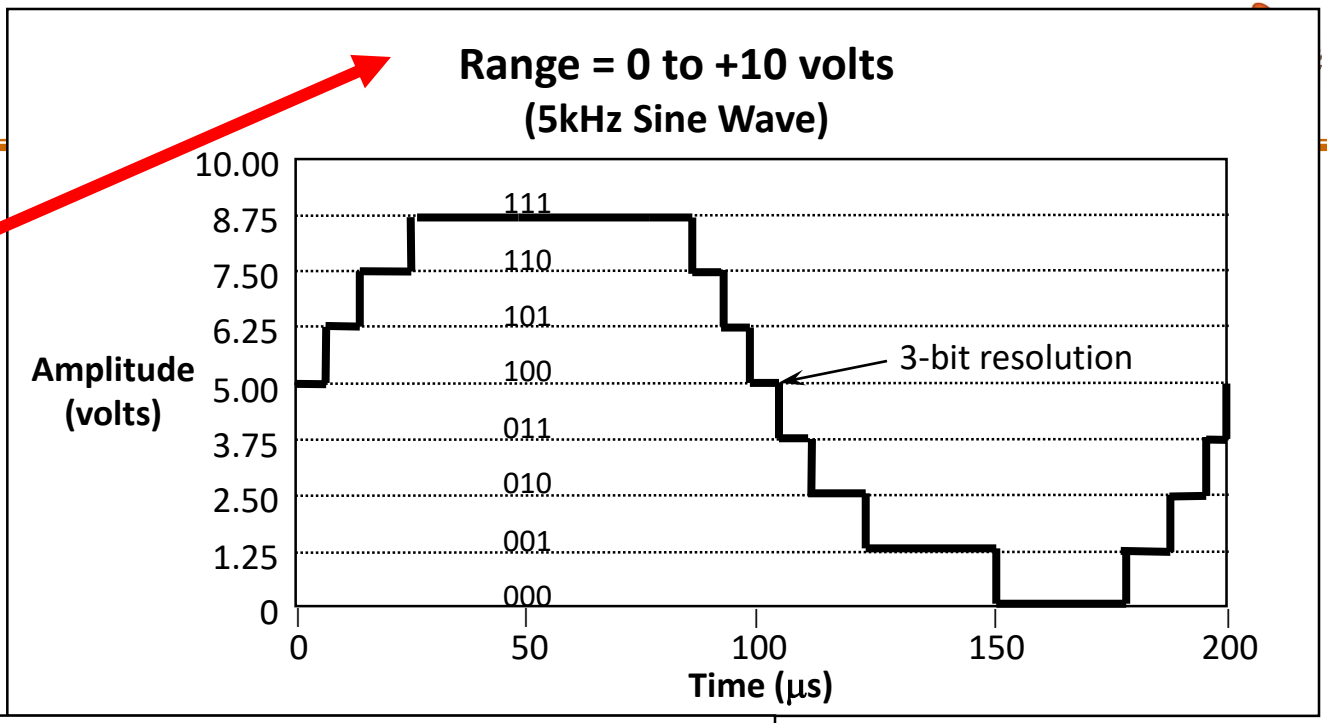
$$10V / 4096 = 2.44\ mV$$

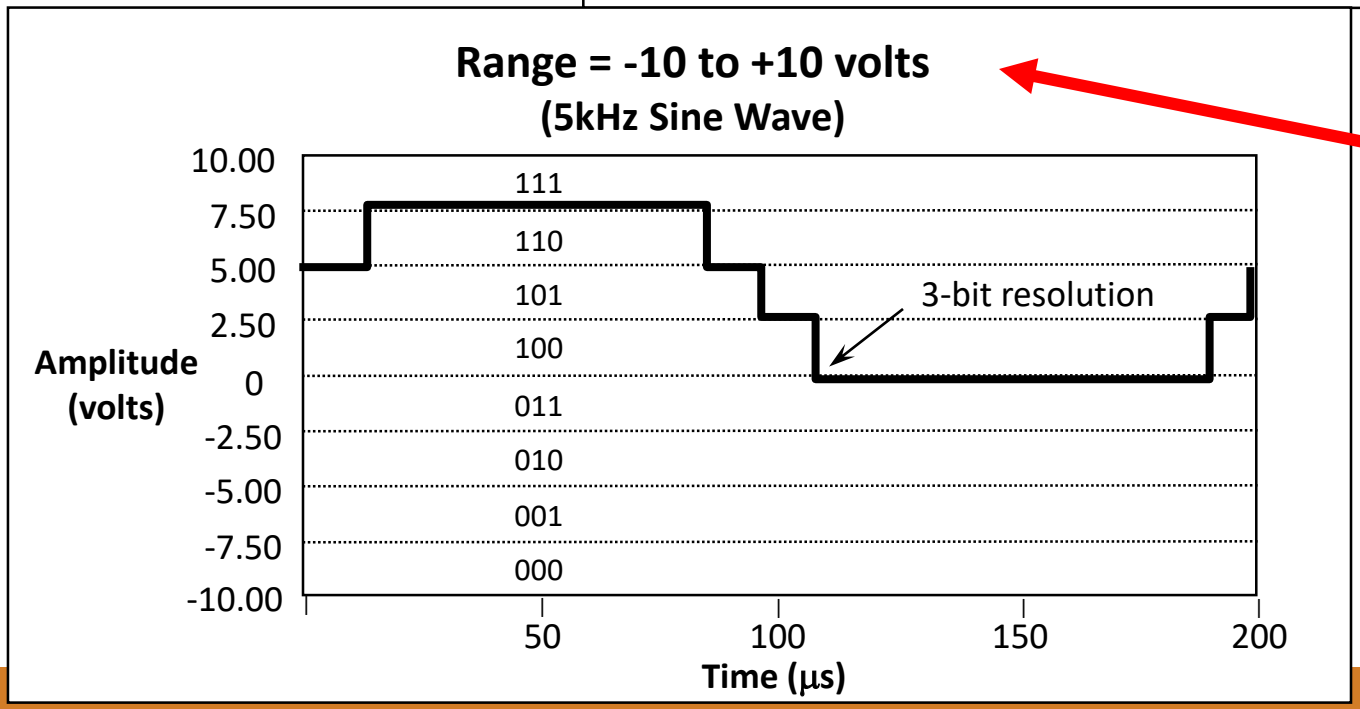
More than sufficient for process control applications

Range

- Minimum and maximum voltages the ADC can digitize DAQ devices often have different available ranges
  - 0 to + 5 volts
  - -5 to +5 Volts
  - 0 to +10 volts
  - -10 to +10 volts
- Pick a range that your signal fits in
- Smaller range = more precise representation of your signal
- Allows you to use all of your available resolution

- Proper Range
  - Using all 8 levels to represent your signal

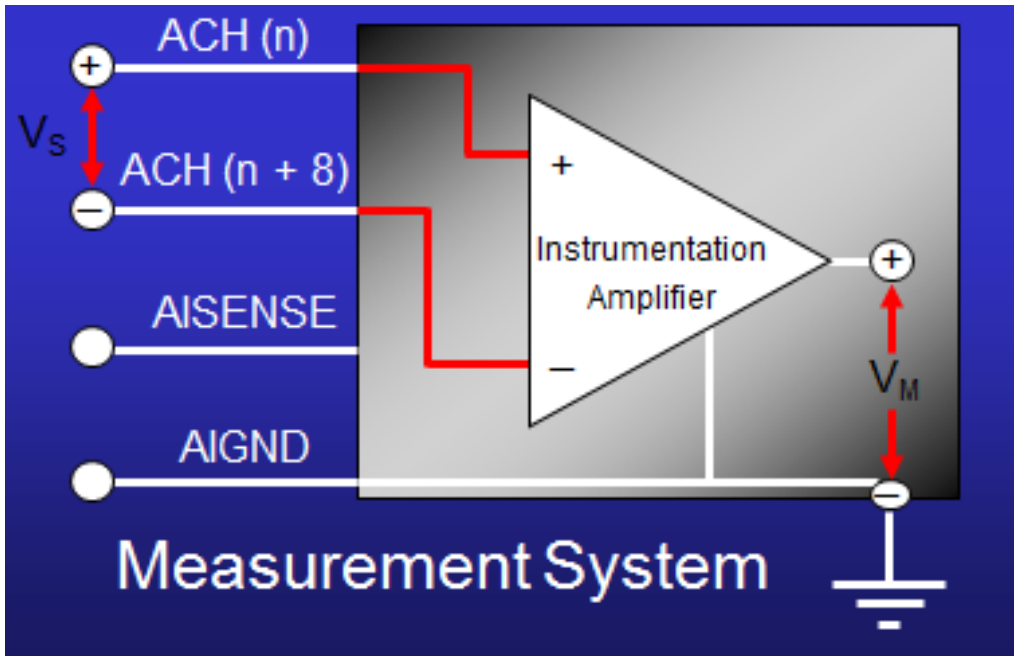




- Improper Range
  - Only using 4 levels to represent your signal

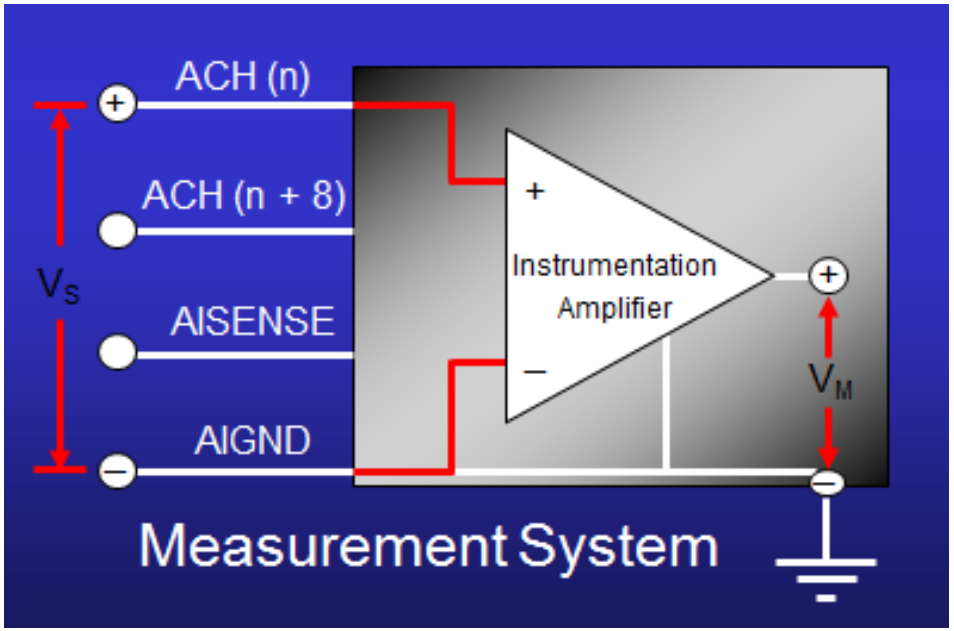
Mode - Differential, RSE or NRSE

- Differential Mode
  - Two channels used for each signal
  - ACH 0 is paired with ACH 8, ACH 1 is paired with ACH 9, etc.
  - Rejects common-mode voltage and common-mode noise



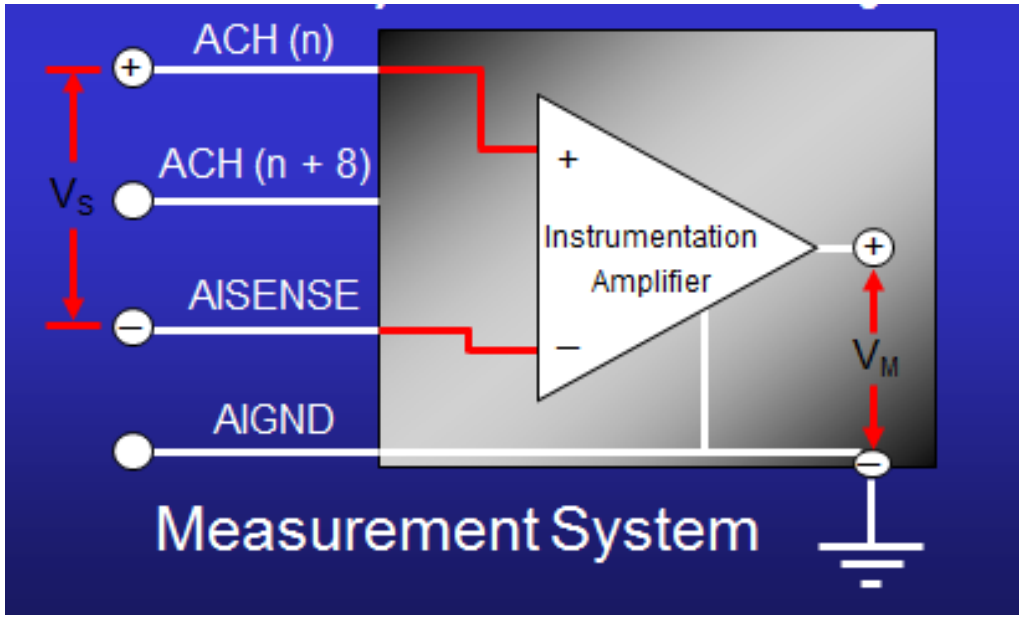
Mode - Differential, RSE or NRSE

- Referenced Single Ended (RSE) Mode
  - Measurement made with respect to system ground
  - One channel used for each signal
  - Doesn't reject common mode voltage



Mode - Differential, RSE or NRSE

- Non-Referenced Single Ended (NRSE) Mode
  - Variation on RSE
  - One channel used for each signal
  - Measurement made with respect to AISENSE not system ground
  - AISENSE is floating
  - Doesn't reject common mode voltage



Normalization

- Min-max normalization: to [new_minA, new_maxA]

$$v' = \frac{v - \min_A}{\max_A - \min_A}(new\_\max_A - new\_\min_A) + new\_\min_A$$

- Ex. Let temperature range of 30 to 300 °C is normalized to [0, 100%]. Then 160 °C is mapped to

$$\frac{160 - 30}{300 - 30}(100 - 0) + 0 = 48.148\%$$

- Z-score normalization (μ: mean, σ: standard deviation):

$$v' = \frac{v - \mu_A}{\sigma_A}$$

- Normalization by decimal scaling $v' = \frac{v}{10^j}$

Case Study

- Consider a level tank with a height of 0.5 m. A level transmitter is used and calibrated to give an output of 1 to 5V for 0 to 0.5m of level. A data acquisition card with a resolution of 12bit is used with a input range of 0 to 5V. If the level value is 0.3m, calculate the binary value that will be stored in the memory of the system.

Solution:

0 to 0.5m $\rightarrow$ 1 to 5 V

- 0.3m $\rightarrow$ $\frac{0.3-0}{0.5-0}(5-1)+1=3.4V$

Case Study

- ADC
  - 0V → 0 0 0 0 0 0 0 0 0 0 0 0 → 0 (Decimal Value)
  - 5V → 1 1 1 1 1 1 1 1 1 1 1 1 → 4095

- 3.4V → $\frac{3.4-0}{5-0}(4095-0)+0=2784.6\approx 2785$

- 2785 → 1 0 1 0 1 1 1 0 0 0 0 1