

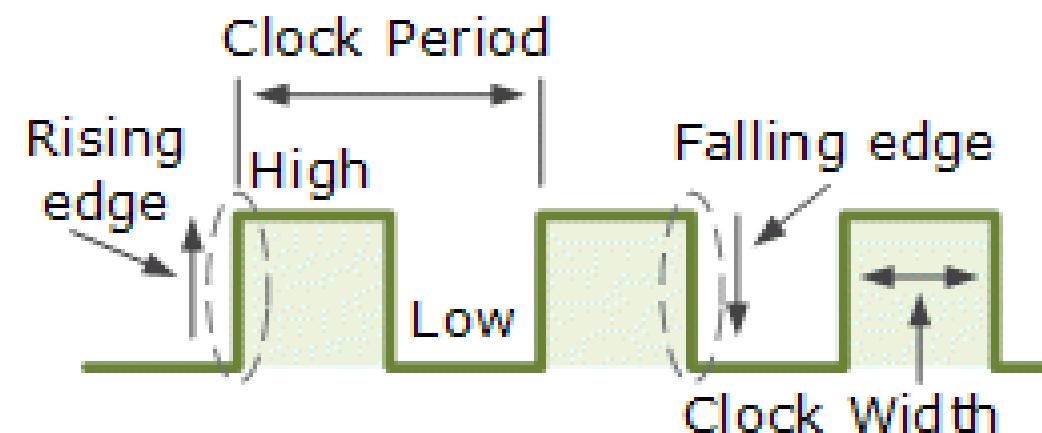
LIC: LECTURE

Signal Generators

- Multivibrator: Need and Different Types
 - Astable Multivibrator
 - Monostable Multivibrator
 - Bistable Multivibrator
- Astable Multivibrator
 - Working Principal
 - Calculation of Time Period
 - Design Example

Multivibrator

- The Multivibrator is the electronic circuit which is used to implement two state devices like oscillator, timer and flip-flops.
- Here, the two states refer to the two voltage levels of the Multivibrators.
- Depending upon the number of stages, the multivibrator can be divided into three types.

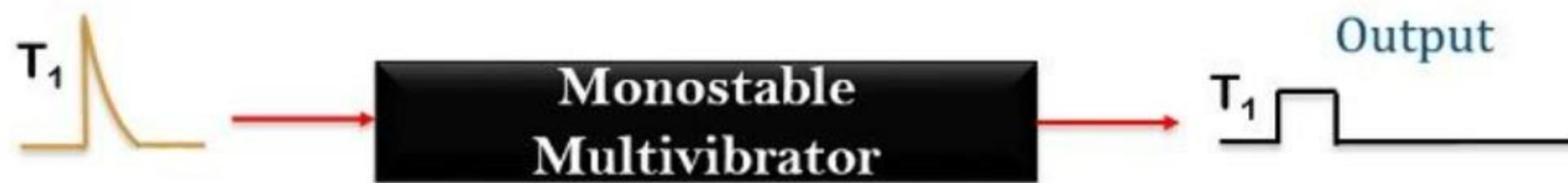


Multivibrator

Astable – A *free-running multivibrator* that has NO stable states but switches continuously between two states this action produces a train of square wave pulses at a fixed frequency. (Eg. Relaxation Oscillator)



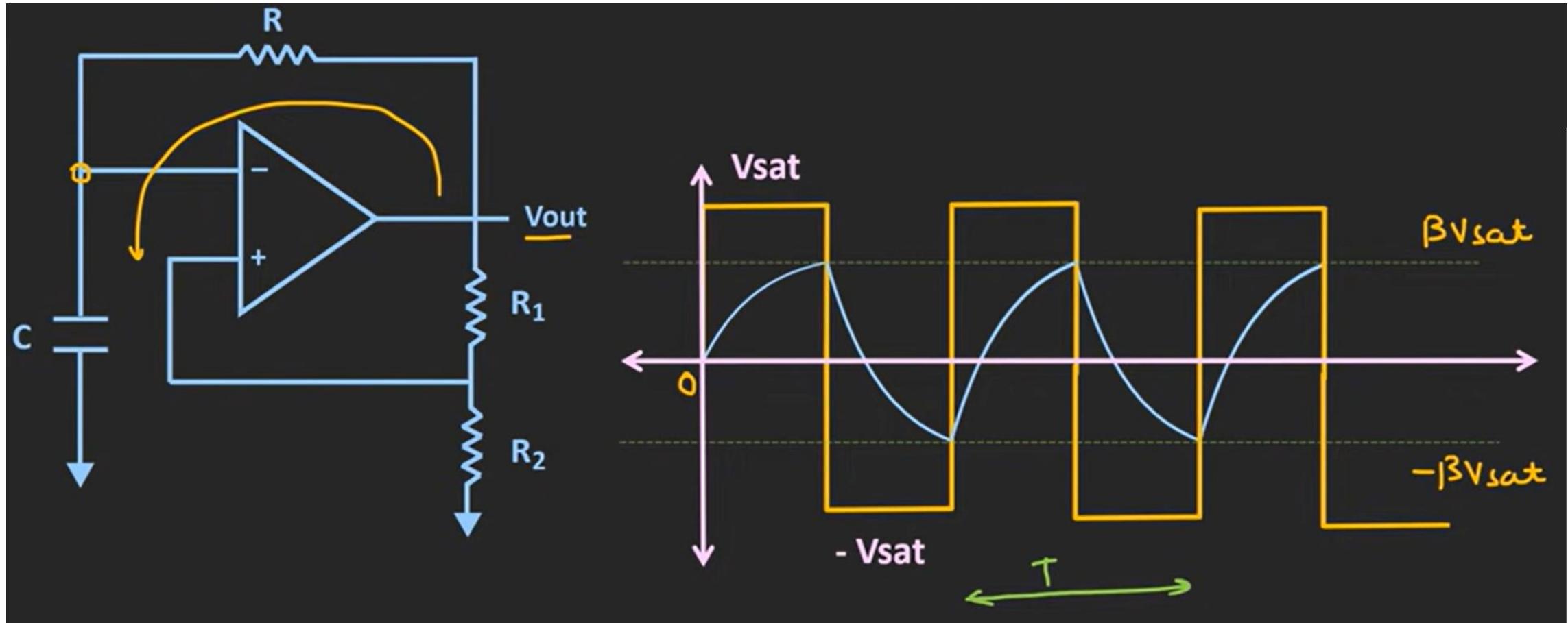
Monostable – A *one-shot multivibrator* that has only ONE stable state and is triggered externally with it returning back to its first stable state. (Eg. Timer applications)

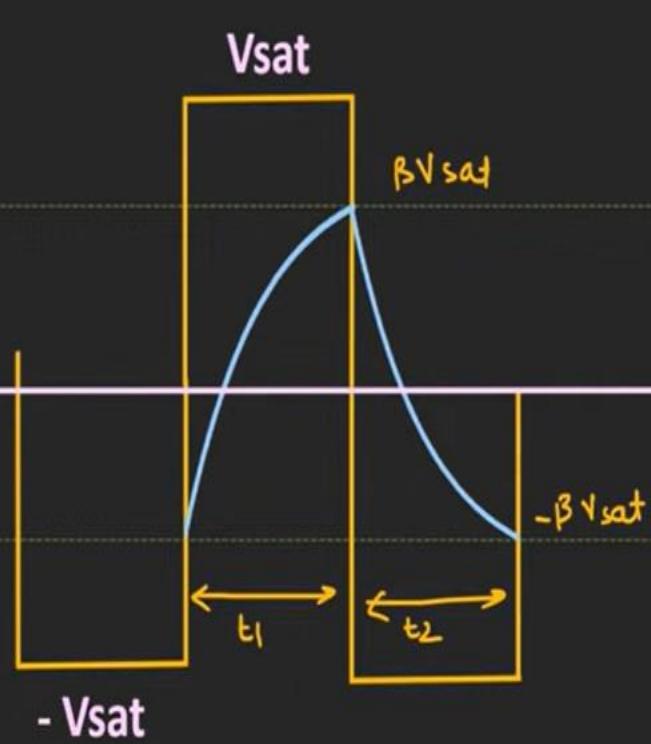


Bistable – A *flip-flop* that has TWO stable states that produces a single pulse either positive or negative in value. (Eg.-Sequential Circuits)



ASTABLE MULTIVIBRATOR (Free Running Multivibrator)





ASTABLE MULTIVIBRATOR

Derivation of Time Period
($T=t_1+t_2$)

Calculation of charging time- t_1

$$V_C(t) = V_{Final} + [V_{Initial} - V_{Final}] e^{-t/RC}$$

$$V_{Final} = V_{sat}$$

$$V_{in} = -\beta V_{sat}$$

$$V_C(t_1) = V_{sat} + [-\beta V_{sat} - V_{sat}] e^{-t_1/RC}$$

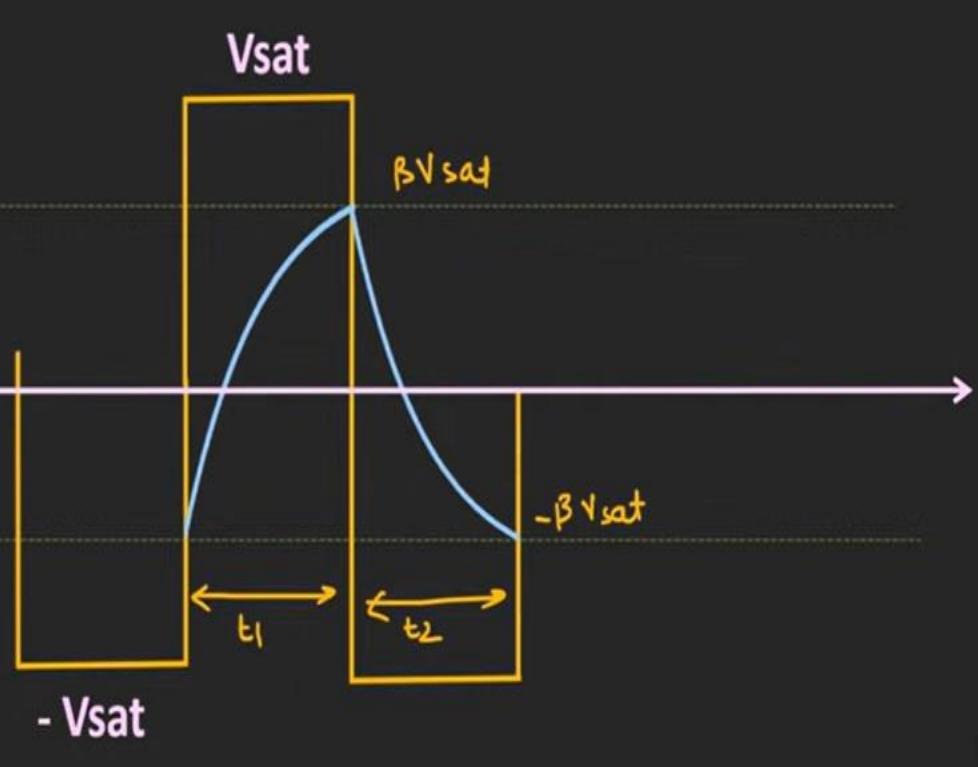
$$\beta V_{sat} = V_{sat} - [1 + \beta] V_{sat} e^{-t_1/RC}$$

$$\beta - 1 = -[1 + \beta] e^{-t_1/RC}.$$

$$\left[\frac{1 - \beta}{1 + \beta} \right] = e^{-t_1/RC}$$

$$\Rightarrow t_1 = -RC \ln \left[\frac{1 - \beta}{1 + \beta} \right]$$

$$t_1 = RC \ln \left[\frac{1 + \beta}{1 - \beta} \right]$$



$$V_C(t) = V_{Final} + [V_{Initial} - V_{Final}] e^{-t/RC}$$

$$V_{Initial} = \beta V_{sat} \rightarrow -\beta V_{sat}$$

$$V_{Final} = -V_{sat}$$

$$V_C(t_2) = -V_{sat} + [\beta V_{sat} - (-V_{sat})] e^{-t_2/RC}$$

$$-\beta V_{sat} = -V_{sat} + V_{sat} \times (1+\beta) \times e^{-t_2/RC}$$

$$\frac{1-\beta}{1+\beta} = e^{-t_2/RC}$$

$$\Rightarrow t_2 = RC \times \ln \left(\frac{1+\beta}{1-\beta} \right)$$

$$T = t_1 + t_2 = 2t_1 = 2RC \ln \left(\frac{1+\beta}{1-\beta} \right)$$

ASTABLE MULTIVIBRATOR

Derivation of Time Period
($T=t_1+t_2$)

Calculation of discharging time-t₂

Design Problem-1

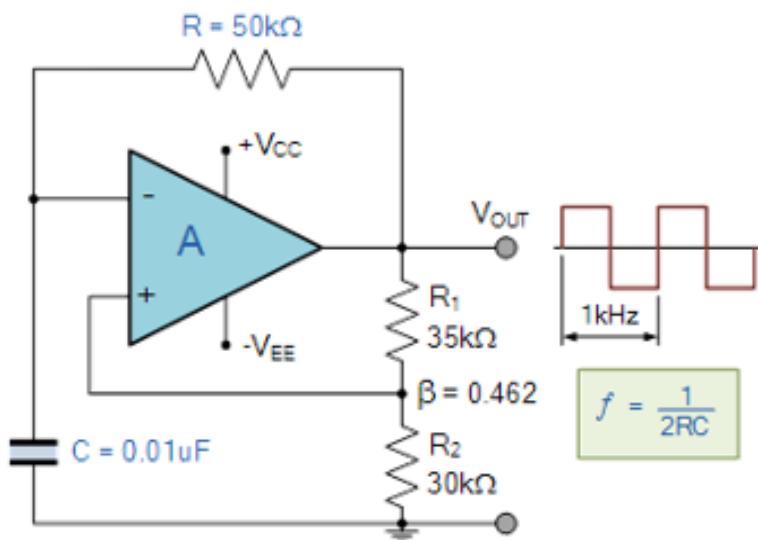
An op-amp multivibrator circuit is constructed using the following components.

$R_1 = 35 \text{ k}\Omega$, $R_2 = 30 \text{ k}\Omega$, $R = 50 \text{ k}\Omega$ and $C = 0.01 \mu\text{F}$ and powered with $V_{cc} = 11\text{V}$, $V_{EE} = -11\text{V}$ DC supply.

Calculate the circuits frequency of oscillation.

Design Problem-1

An op-amp multivibrator circuit is constructed using the following components. $R_1 = 35\text{k}\Omega$, $R_2 = 30\text{k}\Omega$, $R = 50\text{k}\Omega$ and $C = 0.01\mu\text{F}$ and powered with $V_{cc}=11\text{V}$, $V_{EE}=-11\text{V}$ DC supply. Calculate the circuits frequency of oscillation.



$$\beta = \frac{R_2}{R_1 + R_2} = \frac{30\text{k}\Omega}{35\text{k}\Omega + 30\text{k}\Omega} = 0.462$$

$$T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right) = 2RC \ln\left(\frac{1+0.462}{1-0.462}\right)$$

$$T = 2 \times (50\text{k}\Omega \times 0.01\mu\text{F}) \times \ln(2.717)$$

$$\therefore T = 0.001 \times 1 = 0.001\text{Sec or } 1\text{mS}$$

$$\therefore f = \frac{1}{T} = \frac{1}{0.001} = 1,000\text{Hz or } 1\text{kHz}$$

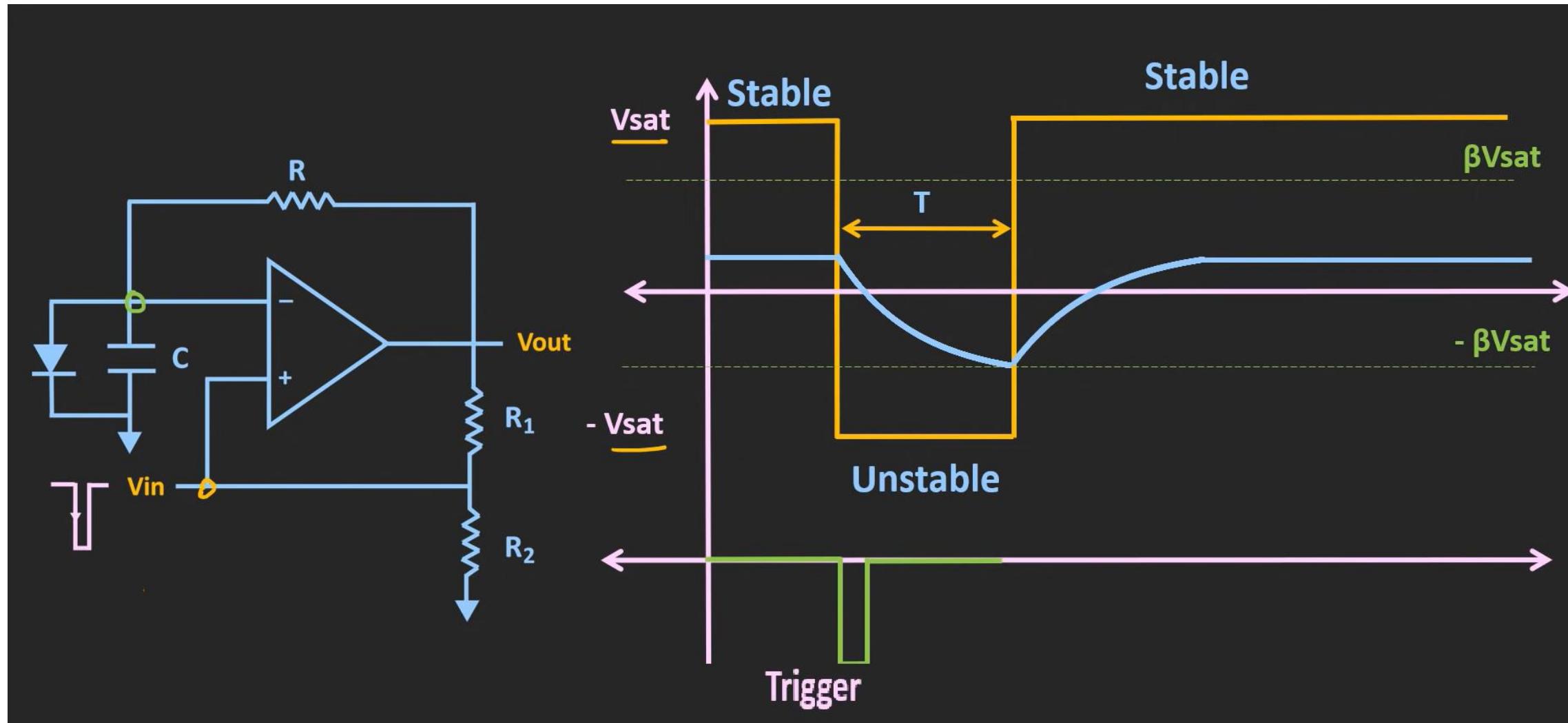
LIC: LECTURE

Signal Generators

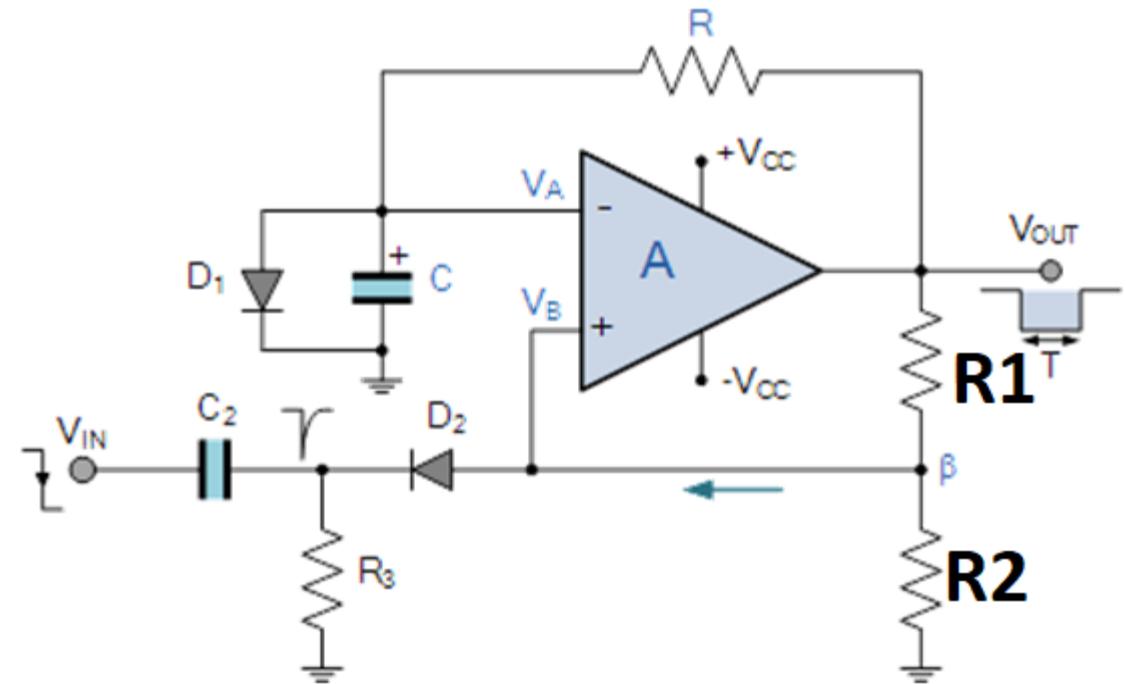
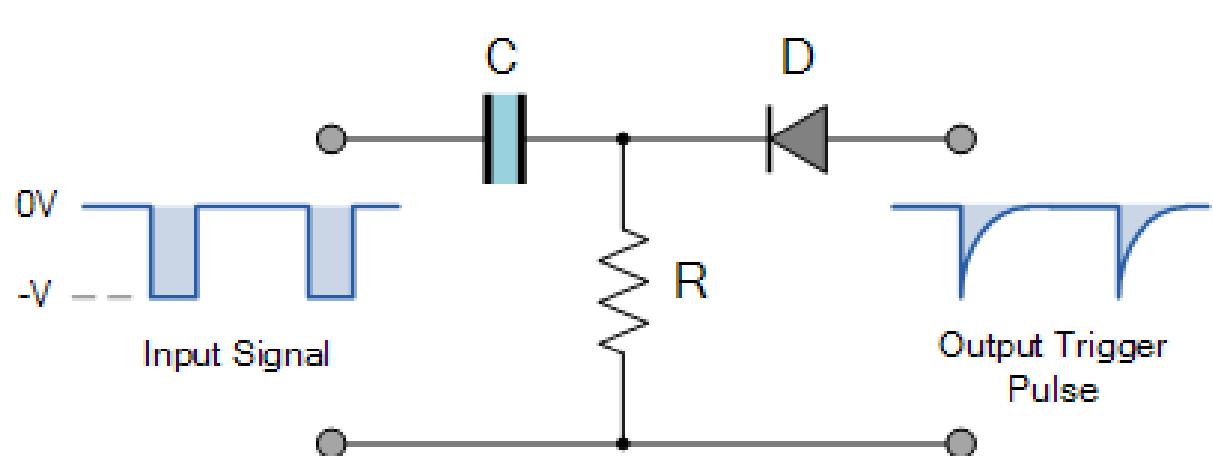
- ✓ **Astable Multivibrator**
 - ✓ **Working Principal**
 - ✓ **Calculation of Time Period**
 - ✓ **Design Example**
- **Monostable Multivibrator**
 - **Working Principal**
 - **Calculation of Time Period and Recovery Time**
 - **Design Example**

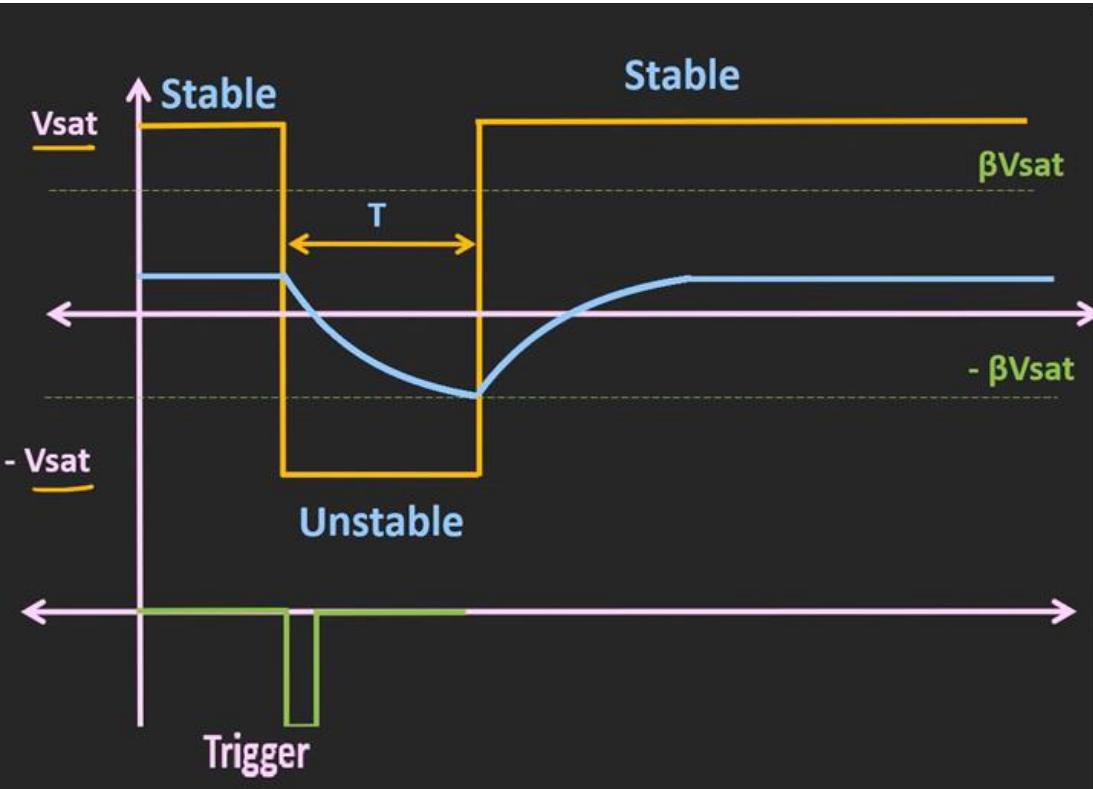
MONOSTABLE MULTIVIBRATOR

(1 STABLE & 1 QUASI-STABLE STATE-One Shot Multivibrator)



RC Differentiator Circuit





MONOSTABLE MULTIVIBRATOR

Derivation of Time Period (T) for unstable state (Pulse Width)

$$V_C(t) = V_{FINAL} + (V_{initial} - V_{FINAL}) e^{-t/RC}$$

$$\left. \begin{aligned} V_{FINAL} &= -V_{SAT} \\ V_{initial} &= V_D \\ V_C(t) &= -\beta V_{SAT} \end{aligned} \right\}$$

$$-\beta V_{SAT} = -V_{SAT} + (V_D - (-V_{SAT})) e^{-t/RC}$$

$$-\beta V_{SAT} = -V_{SAT} + (V_D + V_{SAT}) e^{-t/RC}$$

$$V_{SAT} - \beta V_{SAT} = (V_D + V_{SAT}) e^{-t/RC}$$

$$e^{-t/RC} = \frac{V_{SAT} [1 - \beta]}{V_{SAT} - \beta V_{SAT}}$$

$$e^{-t/RC} = \frac{V_{SAT} [1 - \beta]}{V_D + V_{SAT}} = \frac{V_{SAT}}{V_{SAT}} \left[\frac{1 - \beta}{1 + V_D/V_{SAT}} \right]$$

$$e^{-t/RC} = \frac{1 - \beta}{1 + \frac{V_D}{V_{SAT}}} \quad \text{taking natural log}$$

$$-\frac{t}{RC} = \ln \left(\frac{1 - \beta}{1 + V_D/V_{SAT}} \right)$$

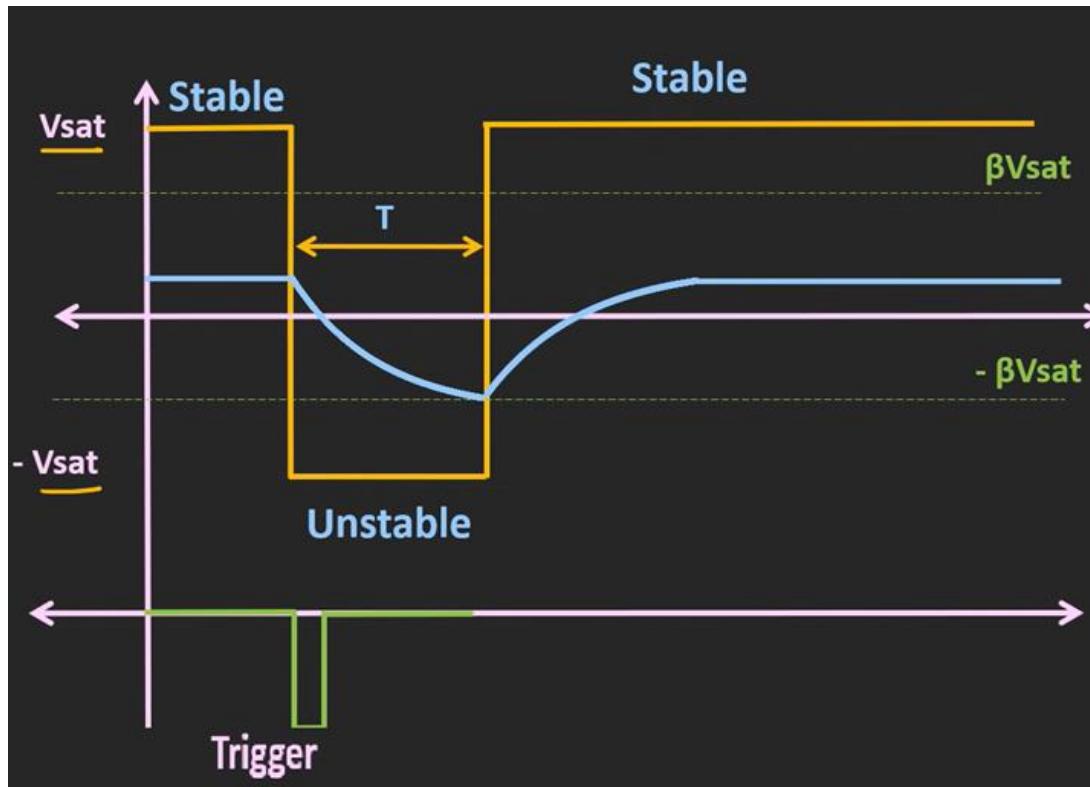
$$t = RC \ln \left(\frac{1 + V_D/V_{SAT}}{1 - \beta} \right)$$

$$t = RC \ln \left(\frac{1 + \frac{V_D}{V_{SAT}}}{1 - \frac{R_2}{R_1 + R_2}} \right)$$

DISCHARGING time
 $V_D \ll |V_{SAT}|$

If $V_D = 0$ & $\beta = R_2/R_1 + R_2$

$$t = RC \ln \left(1 + \frac{R_2}{R_1} \right)$$



MONOSTABLE MULTIVIBRATOR

Derivation of Charging
Time/Capacitor Recovery Time -
Stable State

$$V_C(t) = V_{final} + (V_{initial} - V_{final}) e^{-t/R_C}$$

$$V_{FINAL} = V_{SAT}$$

$$V_{initial} = -\beta V_{SAT}$$

$$V_C(t) = V_D$$

$$V_D = V_{SAT} + (-\beta V_{SAT} - V_{SAT}) e^{-t/R_C}$$

$$V_D - V_{SAT} = -V_{SAT}[1 + \beta] e^{-t/R_C}$$

$$e^{-t/R_C} = -\frac{(V_D - V_{SAT})}{V_{SAT}[1 + \beta]}$$

taking natural log

$$-\frac{t}{R_C} = \ln \frac{V_{SAT} - V_D}{V_{SAT}[1 + \beta]}$$

$$t = -R_C \ln \frac{1 - V_D/V_{SAT}}{1 + \beta}$$

$$t = R_C \ln \frac{1 + \beta}{1 - (V_D/V_{SAT})}$$

An op-amp monostable circuit is constructed using the following components. $R_1 = 30\text{k}\Omega$, $R_2 = 30\text{k}\Omega$, $R = 150\text{k}\Omega$ and $C = 1.0\mu\text{F}$. If the op-amp monostable is supplied from a $\pm 12\text{V}$ supply and the timing period is initiated with a 10ms pulse.

Calculate the circuits timing period, capacitor recovery time, total time between trigger pulses and the differentiator network values. Draw the completed circuit.

Data given: $R_1 = R_2 = 30\text{k}\Omega$, $R = 150\text{k}\Omega$, $C = 1.0\mu\text{F}$ and pulse width equals ten milliseconds, (10ms).

$$\beta = \frac{R_1}{R_1 + R_2} = \frac{30\text{k}\Omega}{30\text{k}\Omega + 30\text{k}\Omega} = 0.5$$

$$T = RC \ln \left(1 + \frac{R_1}{R_2} \right)$$

$$= RC \times \ln \left(1 + \frac{30\text{k}\Omega}{30\text{k}\Omega} \right)$$

$$= 150\text{k}\Omega \times 1.0\mu\text{F} \times 0.693$$

$$T = 0.104 \text{secs or } \underline{104\text{ms}}$$

$$T_{(\text{charging})} = RC \times \ln \left(\frac{1 + \beta}{1 - \frac{V_D}{V_{CC}}} \right)$$

$$T_{(\text{charging})} = RC \times \ln \left(\frac{1 + 0.5}{1 - \frac{0.7}{12}} \right)$$

$$\therefore T_{(\text{ch.})} = 150\text{k}\Omega \times 1.0\mu\text{F} \times 0.465 = \underline{70\text{ms}}$$

$$T_{(\text{total})} = T_{(\text{delay})} + T_{(\text{charging})}$$

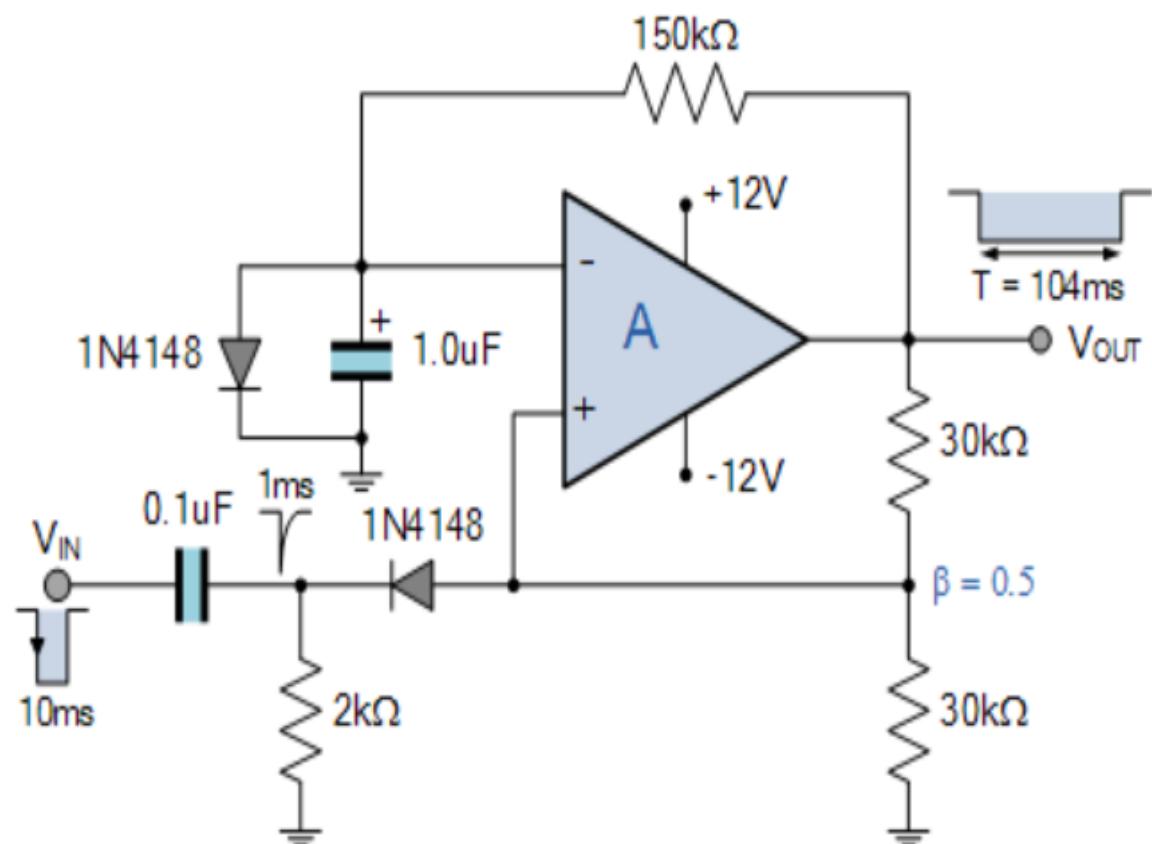
$$\therefore T_{(\text{total})} = 104\text{ms} + 70\text{ms} = 174\text{ms}$$

The input pulse is given as 10ms, therefore the negative spike duration will be 1ms (10%). If we assume a capacitance value of 0.1uF, then the differentiator RC values calculated as:

$$\text{Pulse width} = 1\text{ms} = 5RC$$

$$\text{If } C = 0.1\mu\text{F}$$

$$R = \frac{1\text{ms}}{5 \times 0.1\mu\text{F}} = 2000\Omega \text{ or } 2\text{k}\Omega$$

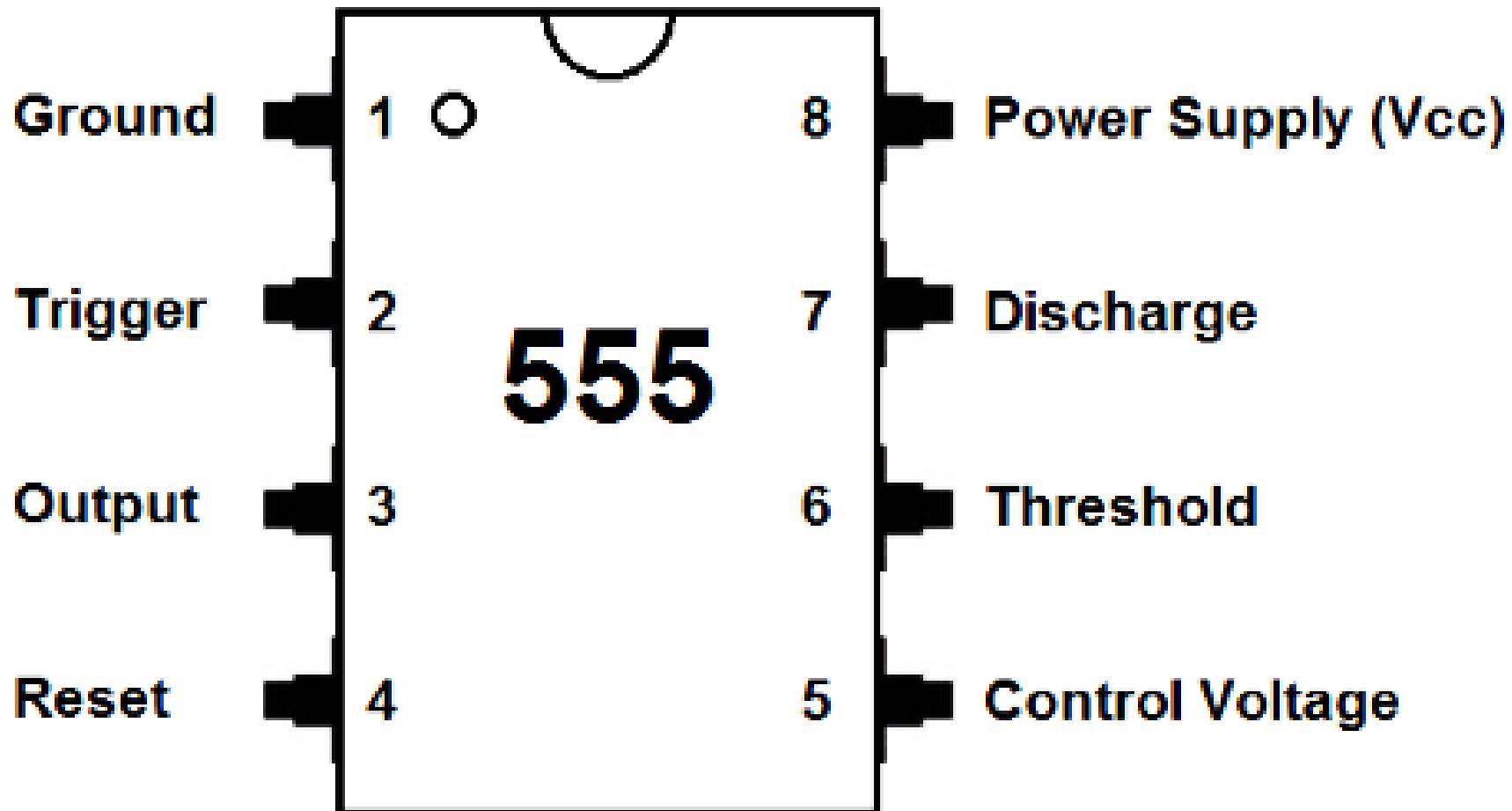


LIC: LECTURE

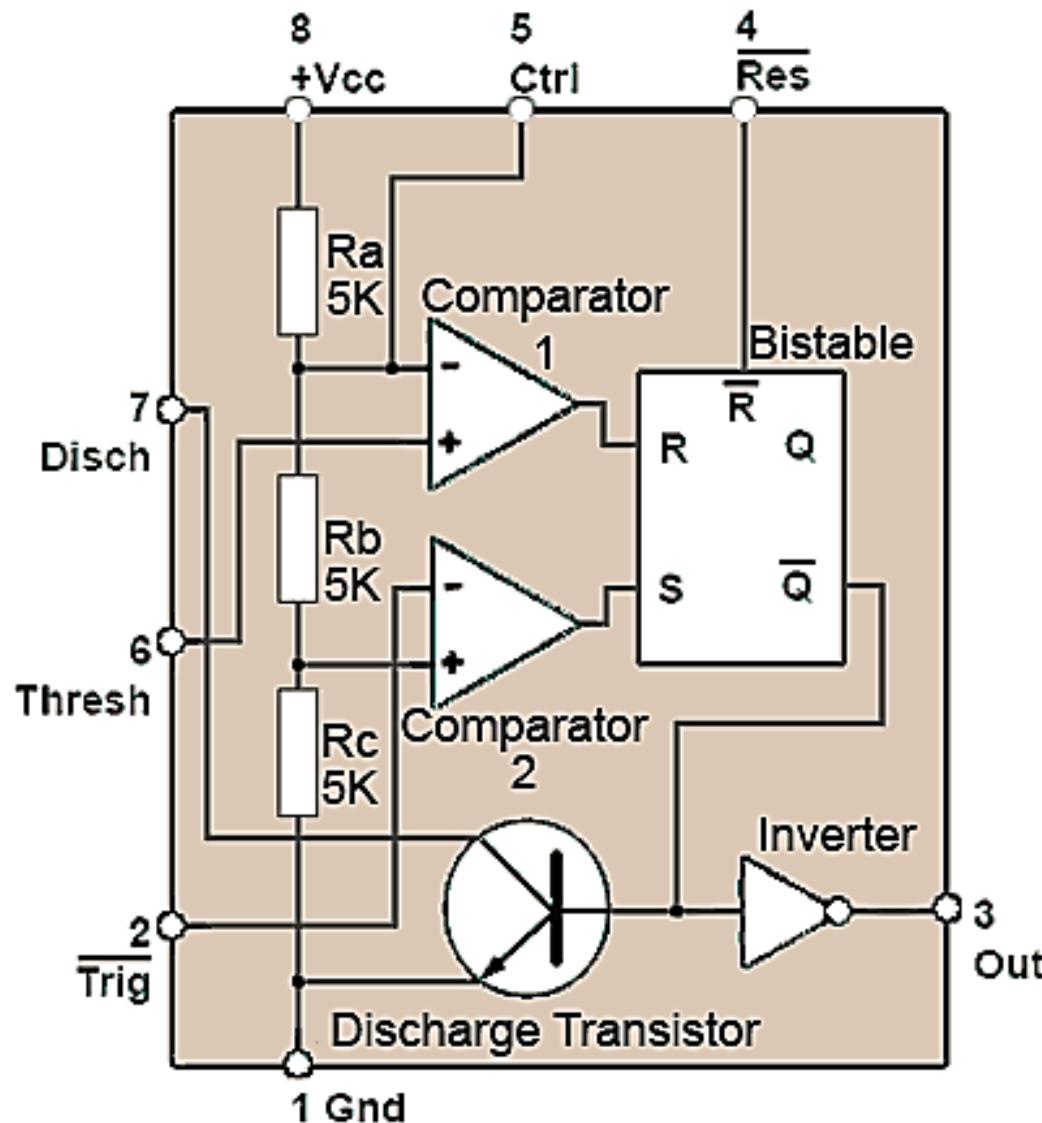
Signal Generators

- ✓ **Monostable Multivibrator using op-Amp**
 - ✓ Working Principal
 - ✓ Calculation of Time Period and Recovery Time
 - ✓ Design Example
- **555 Time IC**
 - Pin Configuration
 - Internal Block Diagram
- **Astable Multivibrator using Timer IC**

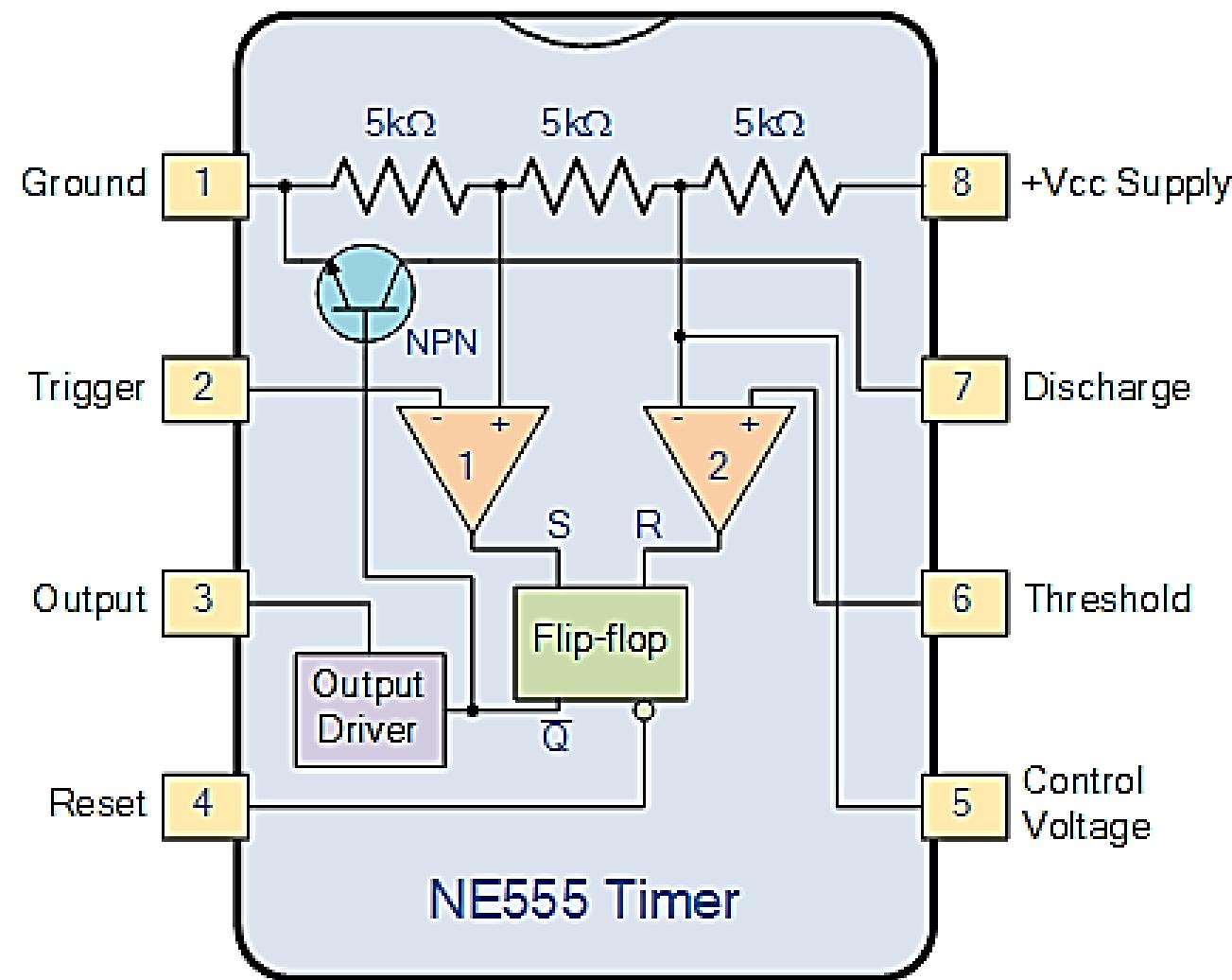
PIN DIAGRAM



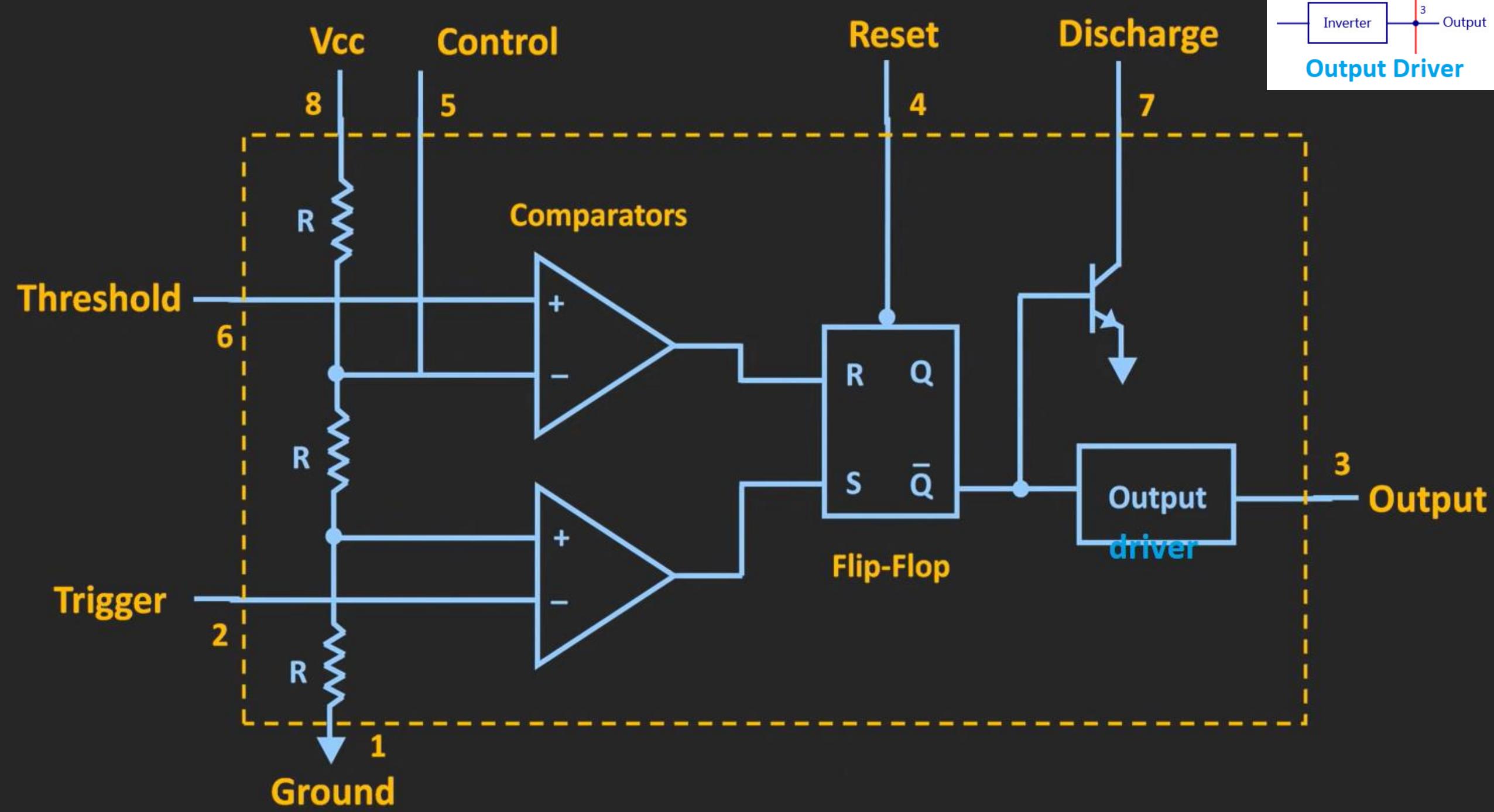
FUNCTIONAL BLOCK DIAGRAM OF 555 TIMER



FUNCTIONAL BLOCK DIAGRAM OF 555 TIMER

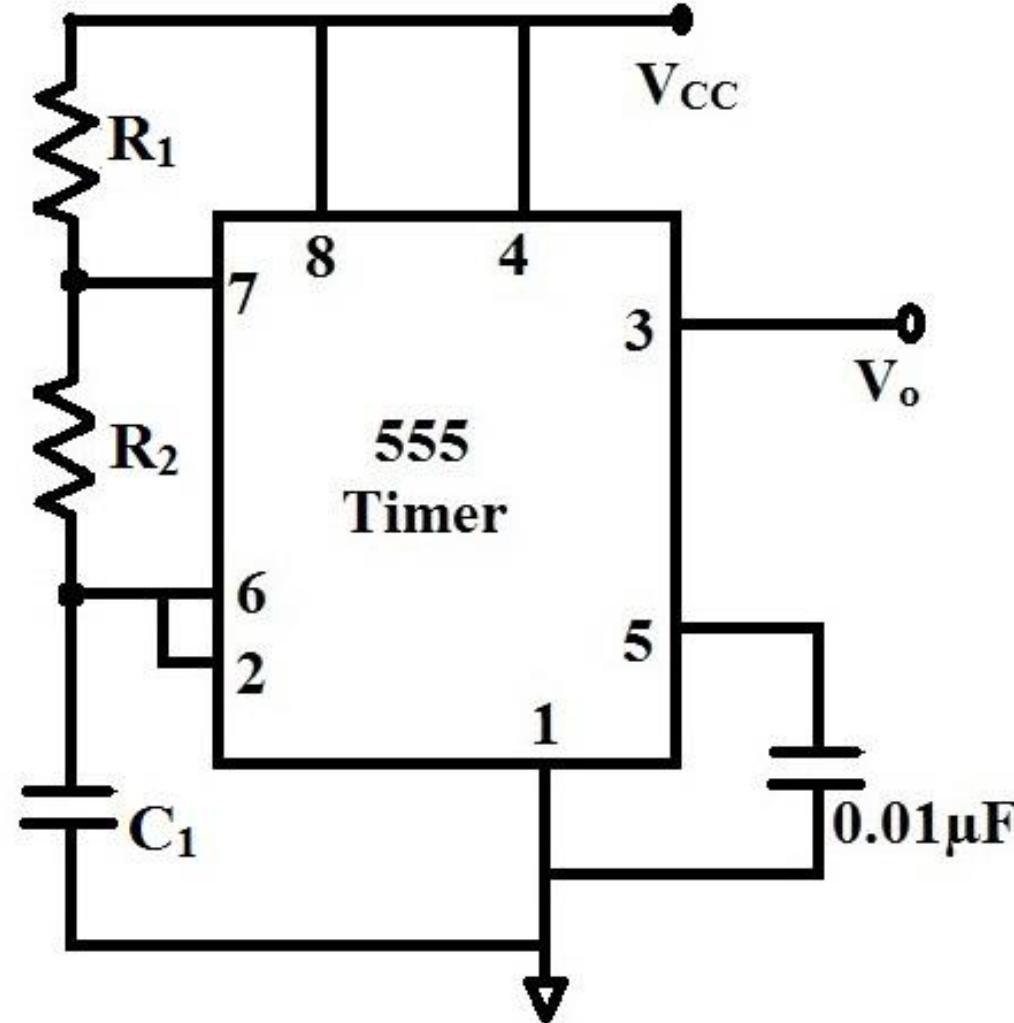


FUNCTIONAL BLOCK DIAGRAM OF 555 TIMER

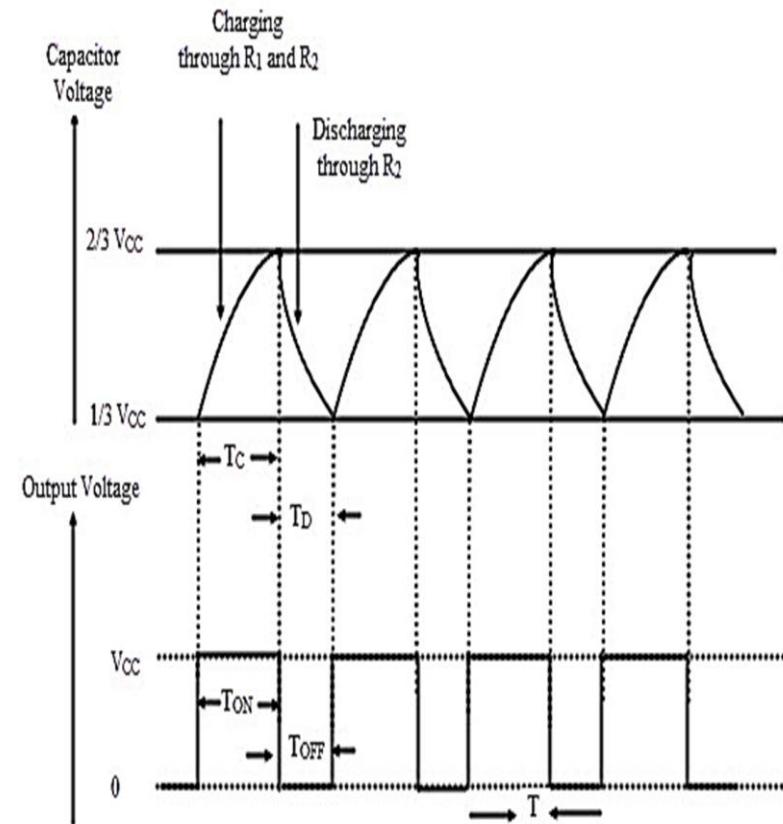
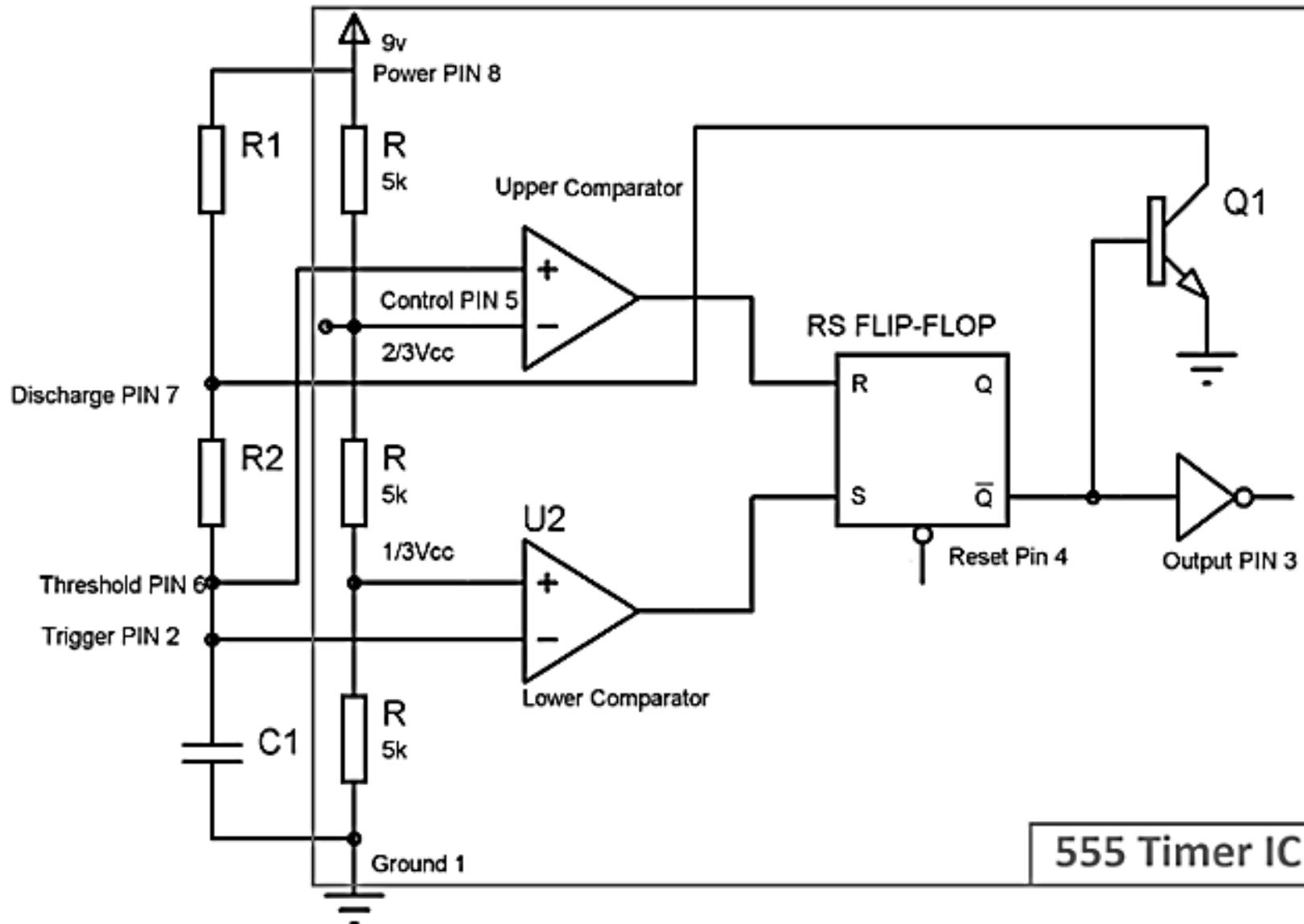


ASTABLE MULTIVIBRATOR USING 555 TIMER

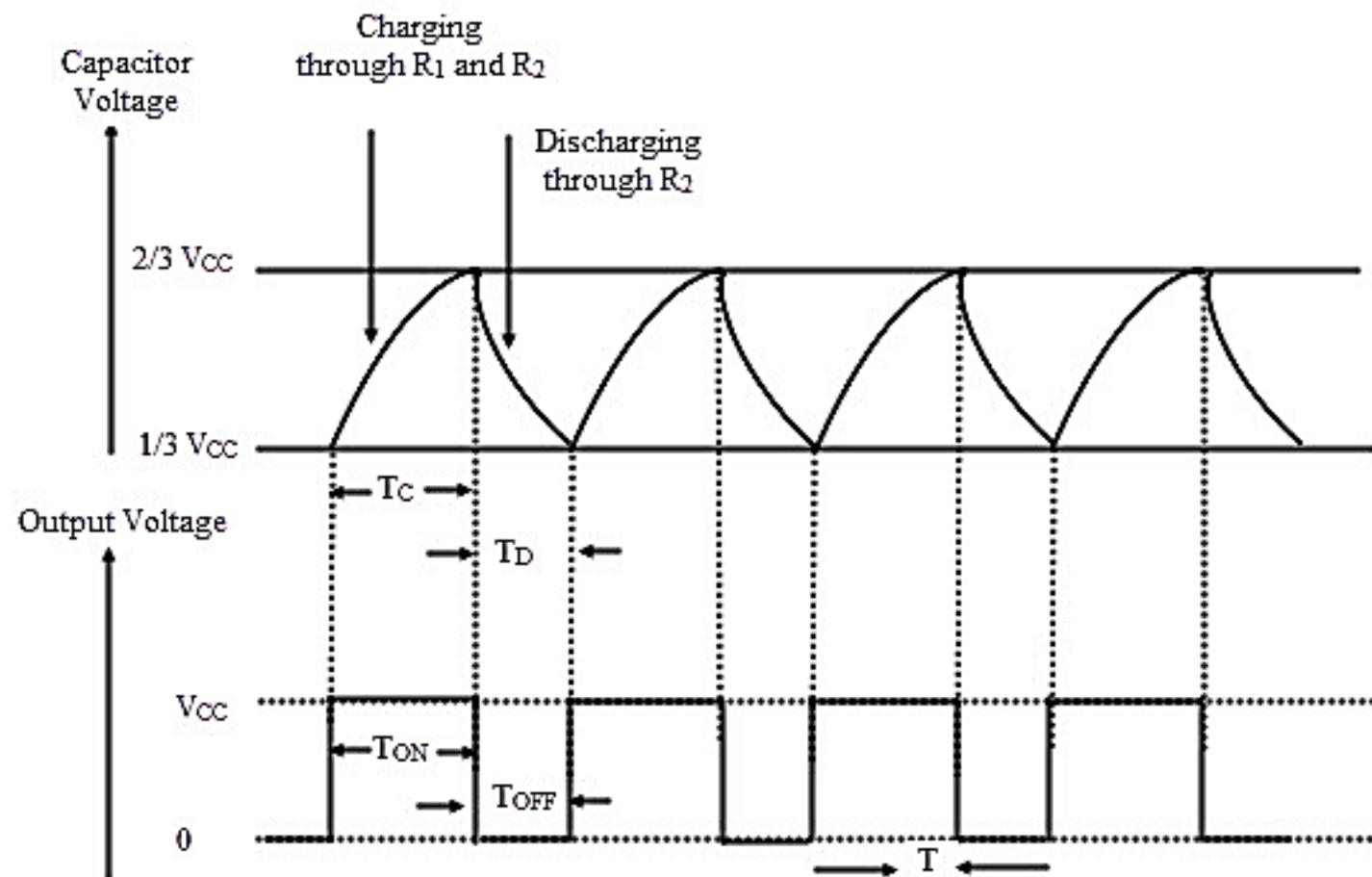
- 1 - Ground
- 2 - Trigger
- 3 - Output
- 4 - Reset
- 5 - Control
- 6 - Threshold
- 7 - Discharge
- 8 - Vcc



FUNCTIONAL BLOCK DIAGRAM OF ASTABLE MULTIVIBRATOR



TIMING PULSES



DERIVATION FOR THE EXPRESSION OF DUTY CYCLE

$$V_C = V_{CC} \left(1 - e^{-t/RC}\right)$$

- Time taken, t_1 by the circuit to charge from $0 - \frac{2}{3}V_{CC}$,

$$\frac{2}{3}V_{CC} = V_{CC} \left(1 - e^{-t_1/RC}\right)$$



$$t_1 = 1.099RC$$

- Time taken, t_2 by the circuit to charge from $0 - \frac{1}{3}V_{CC}$,

$$\frac{1}{3}V_{CC} = V_{CC}(1 - e^{-t_2/RC})$$

$$t_2 = 0.405RC$$

- Time to charge from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$,

$$T_C = t_1 - t_2$$

$$T_C = 0.69(R_1 + R_2)C$$

- Capacitor discharges from $\frac{2}{3}V_{CC}$ to $\frac{1}{3}V_{CC}$.

$$\frac{1}{3}V_{CC} = \frac{2}{3}V_{CC}e^{-t/RC}$$

- Solving the equation we get ,

$$t = 0.69 T_D = 0.69 R_2 C$$

- Total time,

$$T = T_C + T_D$$

$$T = 0.69 (R_1 + 2R_2)C$$

$$f = \frac{1.45}{(R_1+2R_2)C}$$

- Duty cycle,

$$D\% = \frac{T_C}{T} \times 100\%$$

$$\Rightarrow D\% = \left(\frac{R_1 + R_2}{R_1 + 2 R_2} \right) \times 100\%$$

$$T = 0.69 (R_1 + 2R_2)C$$

$$f = \frac{1.45}{(R_1 + 2R_2)C}$$

LIC: LECTURE

Signal Generators

- ✓ **555 Time IC**
 - ✓ Pin Configuration
 - ✓ Internal Block Diagram
- ✓ **Astable Multivibrator using Timer IC**
 - Design Example
- **Bistable Multivibrator using Timer IC**
 - Applications

EXAMPLE 10.3. In the circuit of Fig. 10.16 specify suitable components for $f_0 = 50 \text{ kHz}$ and $D(\%) = 75\%$.

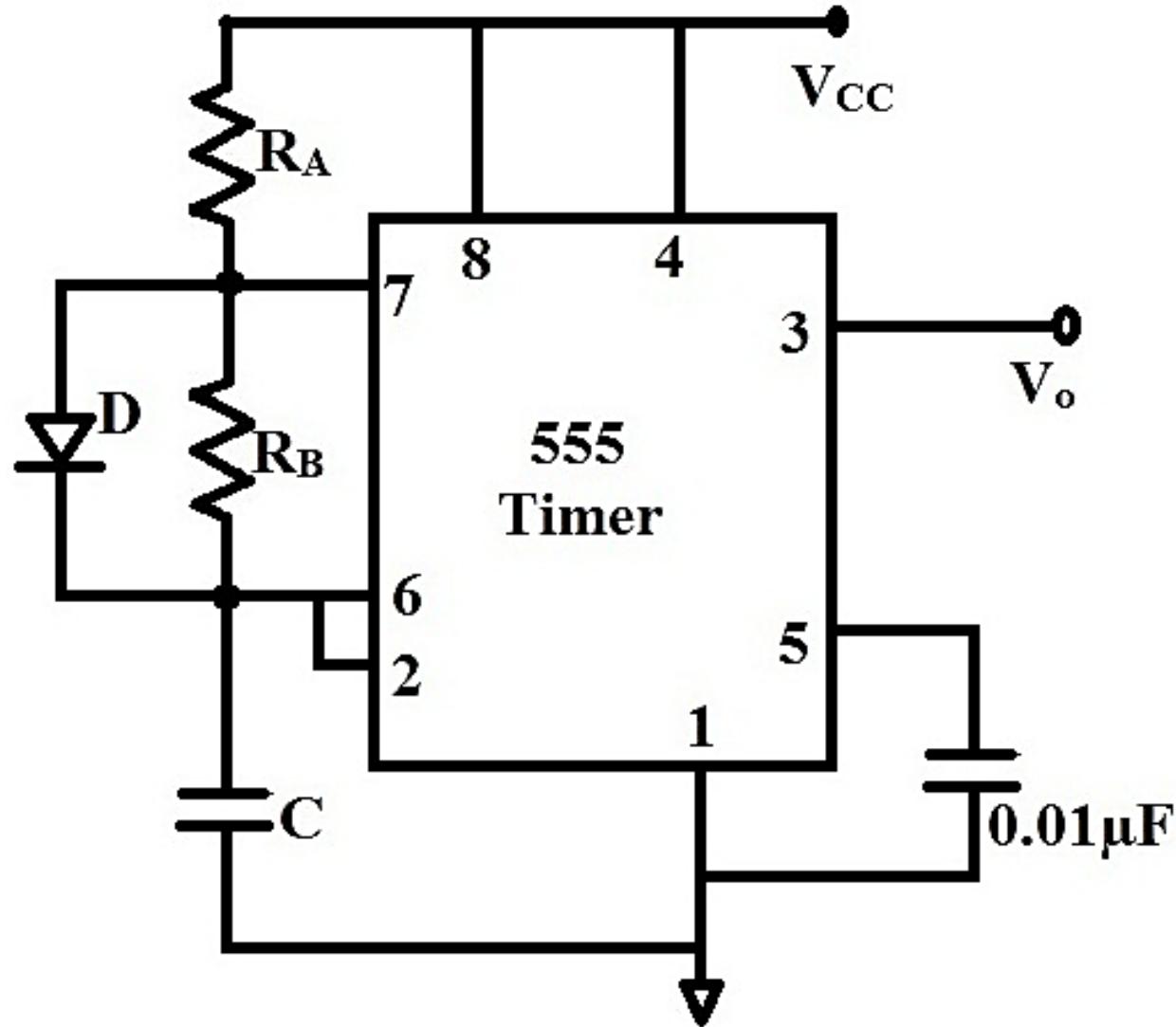
Solution. Let $C = 1 \text{ nF}$, so that $R_A + 2R_B = 1.44/(f_0C) = 28.85 \text{ k}\Omega$. Imposing $(R_A + R_B)/(R_A + 2R_B) = 0.75$ gives $R_A = 2R_B$. Solving gives $R_A = 14.4 \text{ k}\Omega$ (use $14.3 \text{ k}\Omega$) and $R_B = 7.21 \text{ k}\Omega$ (use $7.15 \text{ k}\Omega$).

Q1) For a astable multivibrator using 555 timer, $R_1 = 6.8\text{k}\Omega$, $R_2 = 3.3\text{k}\Omega$ and $C = 0.1\mu\text{F}$. Calculate (a) t_{HIGH} , (b) t_{LOW} , (c) free running frequency and (d) duty cycle, D.

Ans :-

- (a) $t_{\text{HIGH}} = 0.7\text{ms}$
- (b) $t_{\text{LOW}} = 0.23\text{ms}$
- (c) $f = 1.07\text{kHz}$
- (d) $D = 0.75 \text{ or } 75\%$

ADJUSTABLE DUTY CYCLE MULTIVIBRATOR



DUTY CYCLE DERIVATION

- During charging,

$$T_C = 0.69 R_A C$$

- During discharge,

$$T_D = 0.69 R_B C$$

- Therefore, total time period T is,

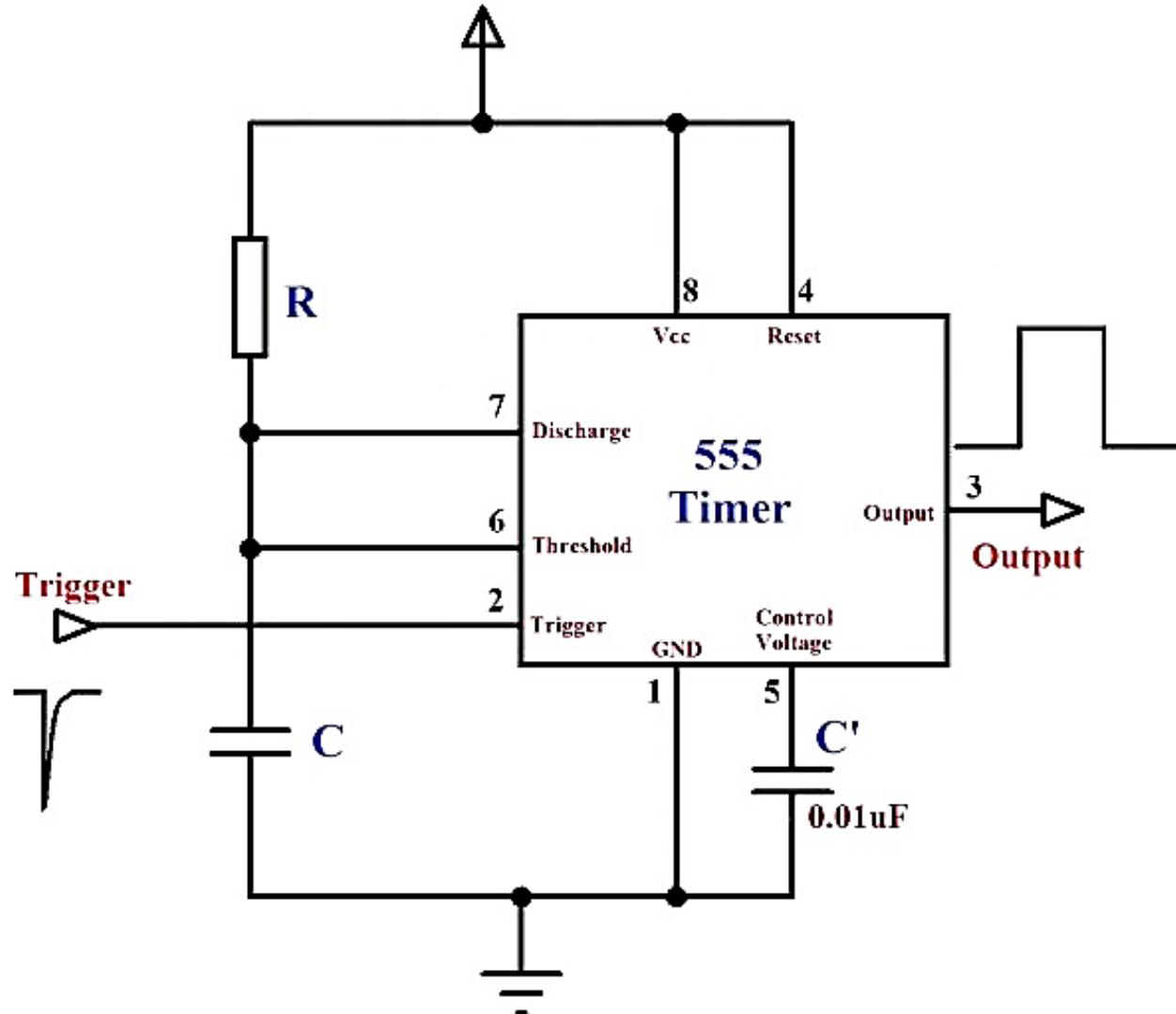
$$T = 0.69 (R_A + R_B)C$$

$$f = \frac{1.45}{(R_A + R_B)C}$$

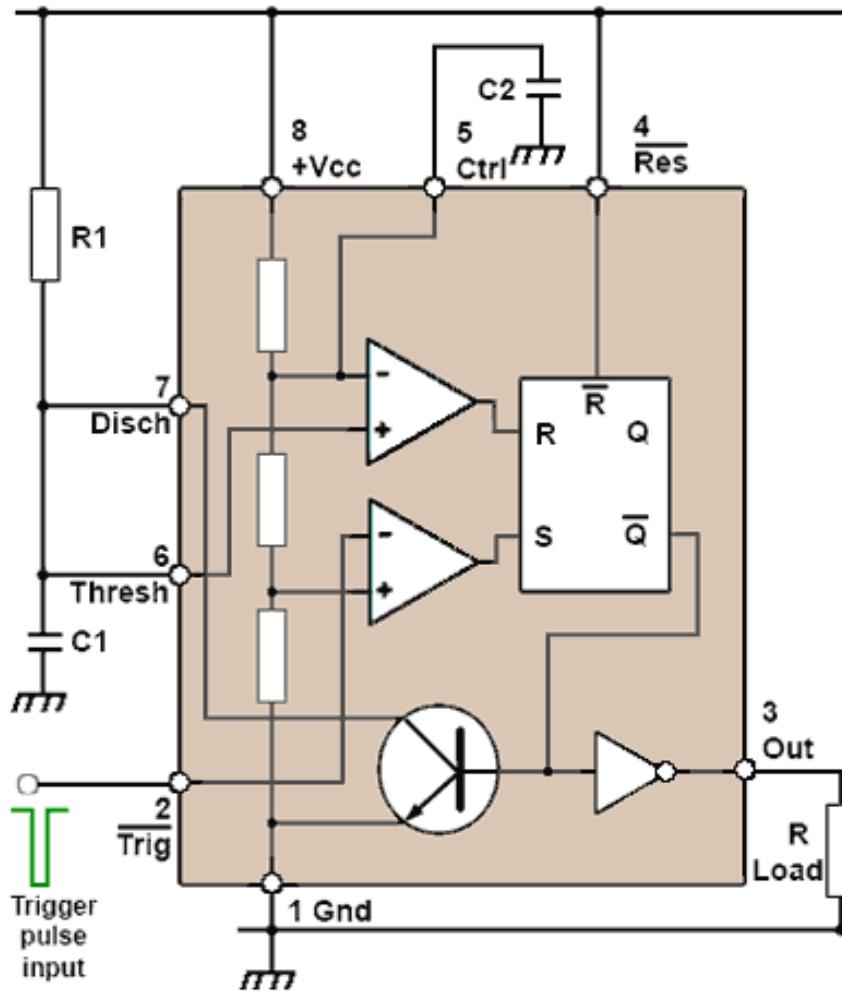
$$D = \frac{R_A}{R_A + R_B}$$

MONOSTABLE MULTIVIBRATOR USING 555 TIMER

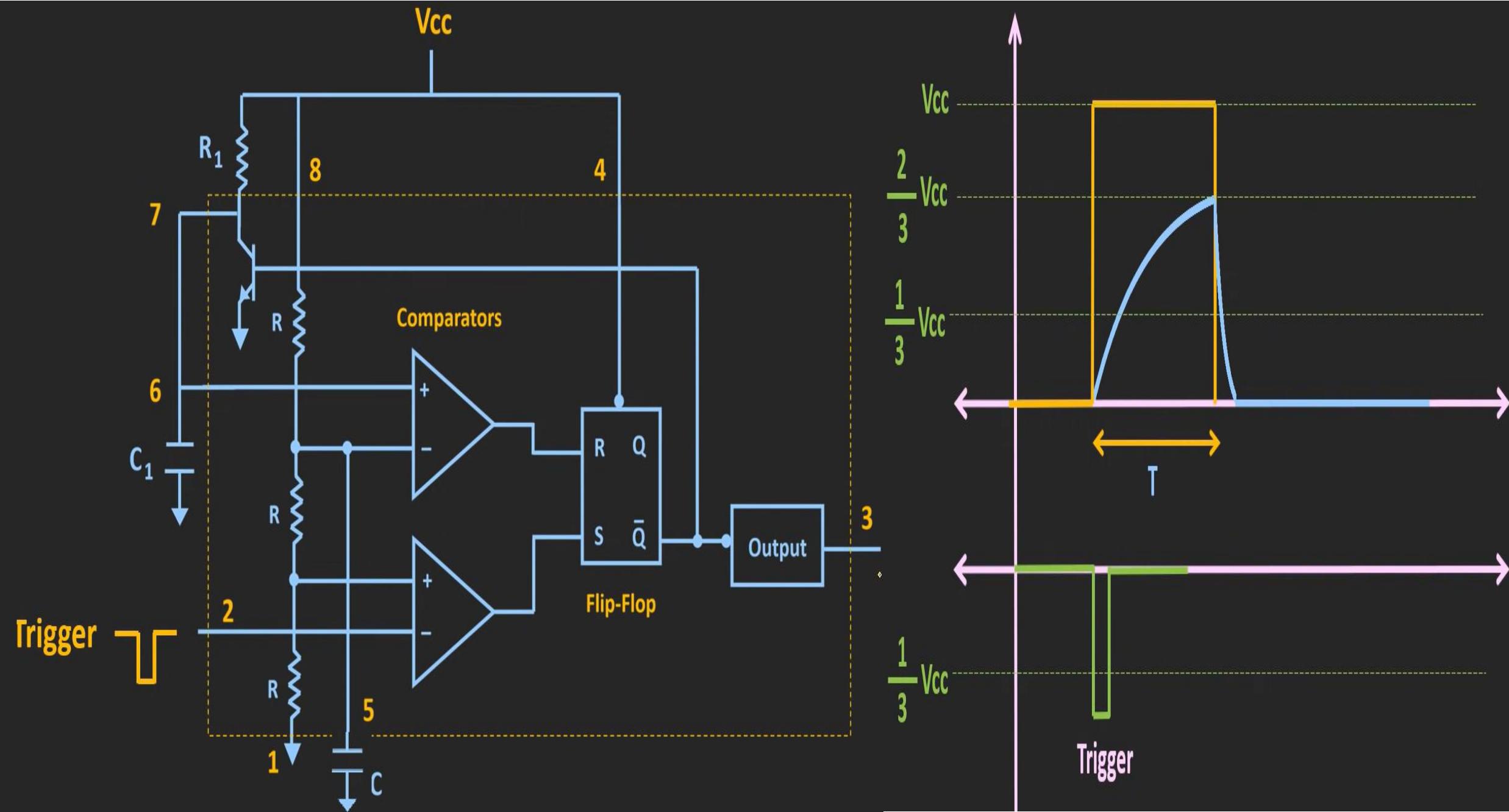
MONOSTABLE MULTIVIBRATOR USING 555 TIMER



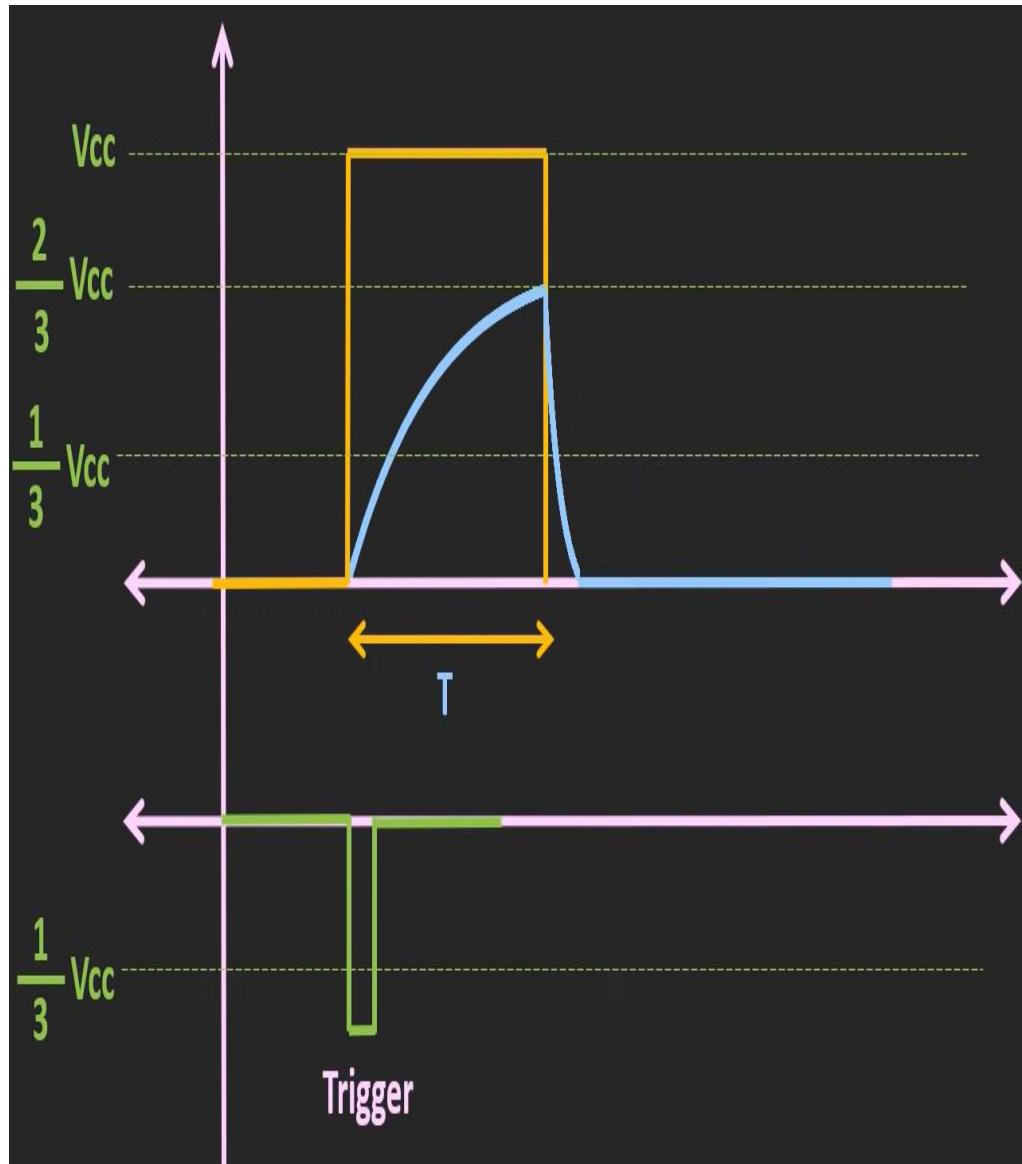
FUNCTIONAL BLOCK DIAGRAM OF MONOSTABLE MULTIVIBRATOR



FUNCTIONAL BLOCK DIAGRAM OF MONOSTABLE MULTIVIBRATOR



TIME PERIOD DERIVATION



$$V_c(t) = V_o (1 - e^{-t/RC})$$

$$\begin{aligned} V_c(t) &= V_F + C(V_I - V_F)e^{-t/RC} \\ &= V_{CC} + (0 - V_{CC})e^{-t/RC} \end{aligned}$$

$$\begin{aligned} V_c(t) &= V_{CC} \times C(1 - e^{-t/RC}) \\ \frac{1}{3} &= e^{-t_1/RC} \end{aligned}$$

$$\ln\left(\frac{1}{3}\right) = -\frac{t_1}{RC}$$

$$\Rightarrow t_1 = RC \times \ln(3)$$

$$t_1 \approx 1.1 RC$$

Q2) Design a monostable multivibrator using 555 timer to produce a pulse width of 100ms. Calculate the value of R by assuming the values of $C = 0.47\mu F$.

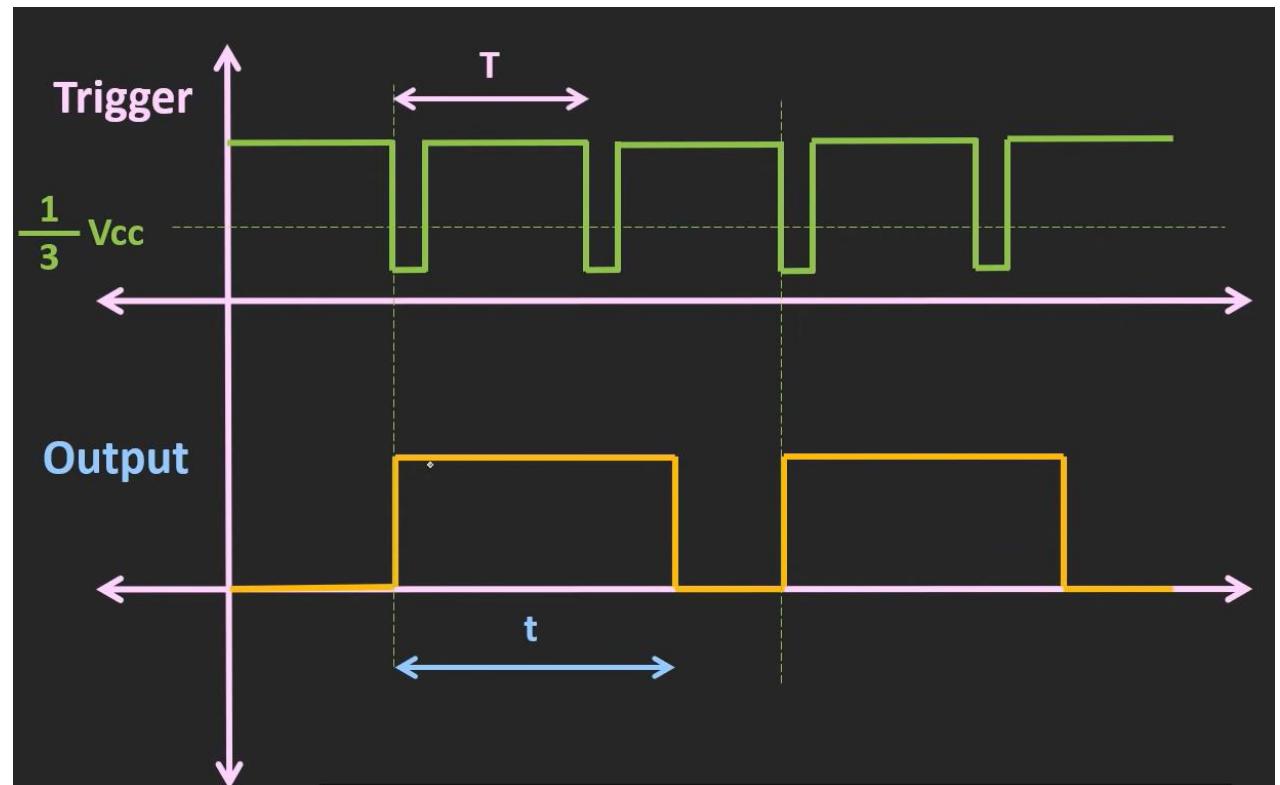
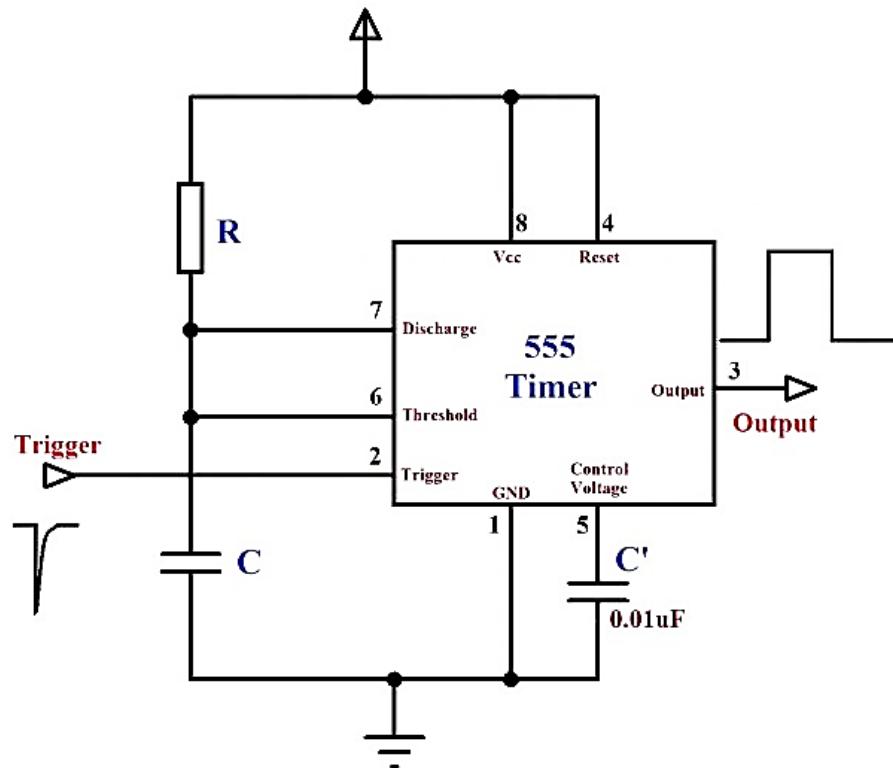
Ans: -

$$T = 1.1 RC$$

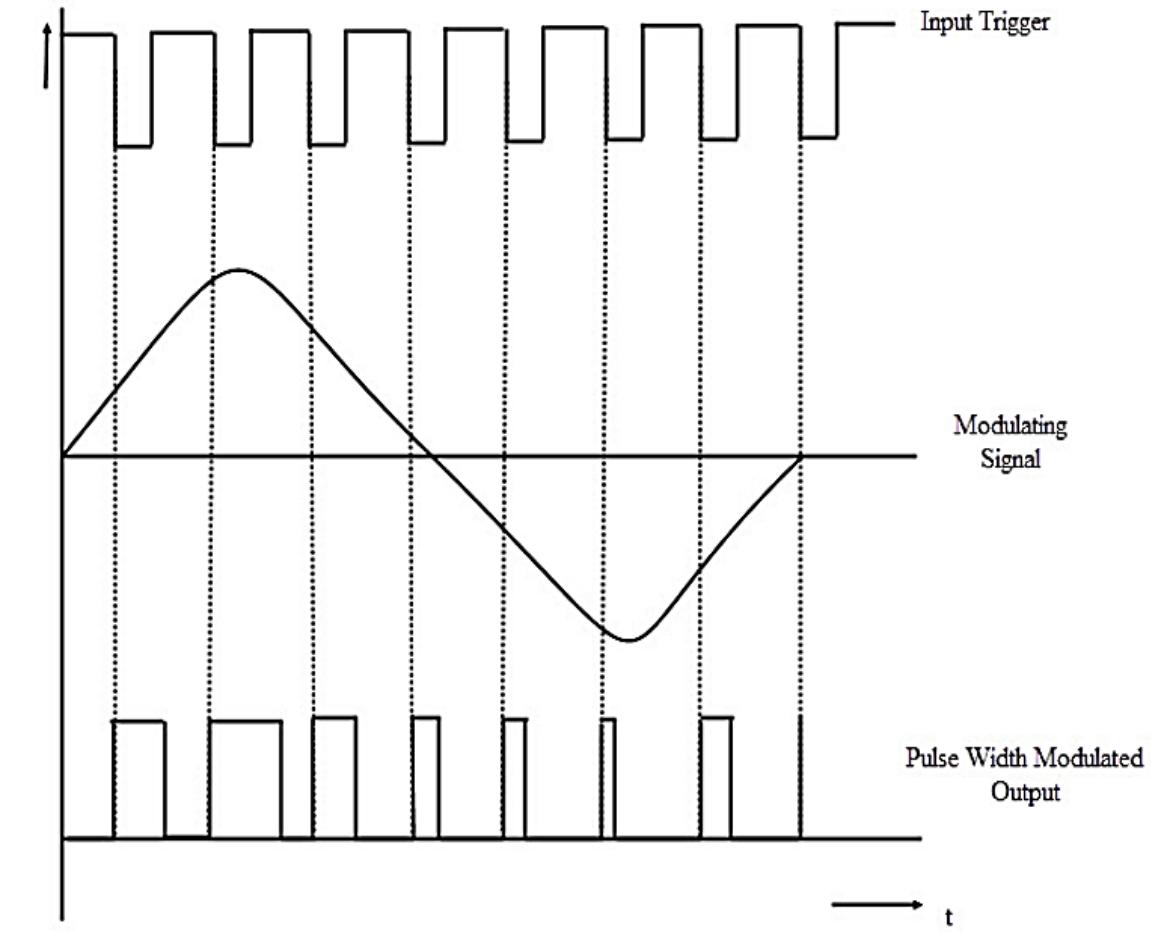
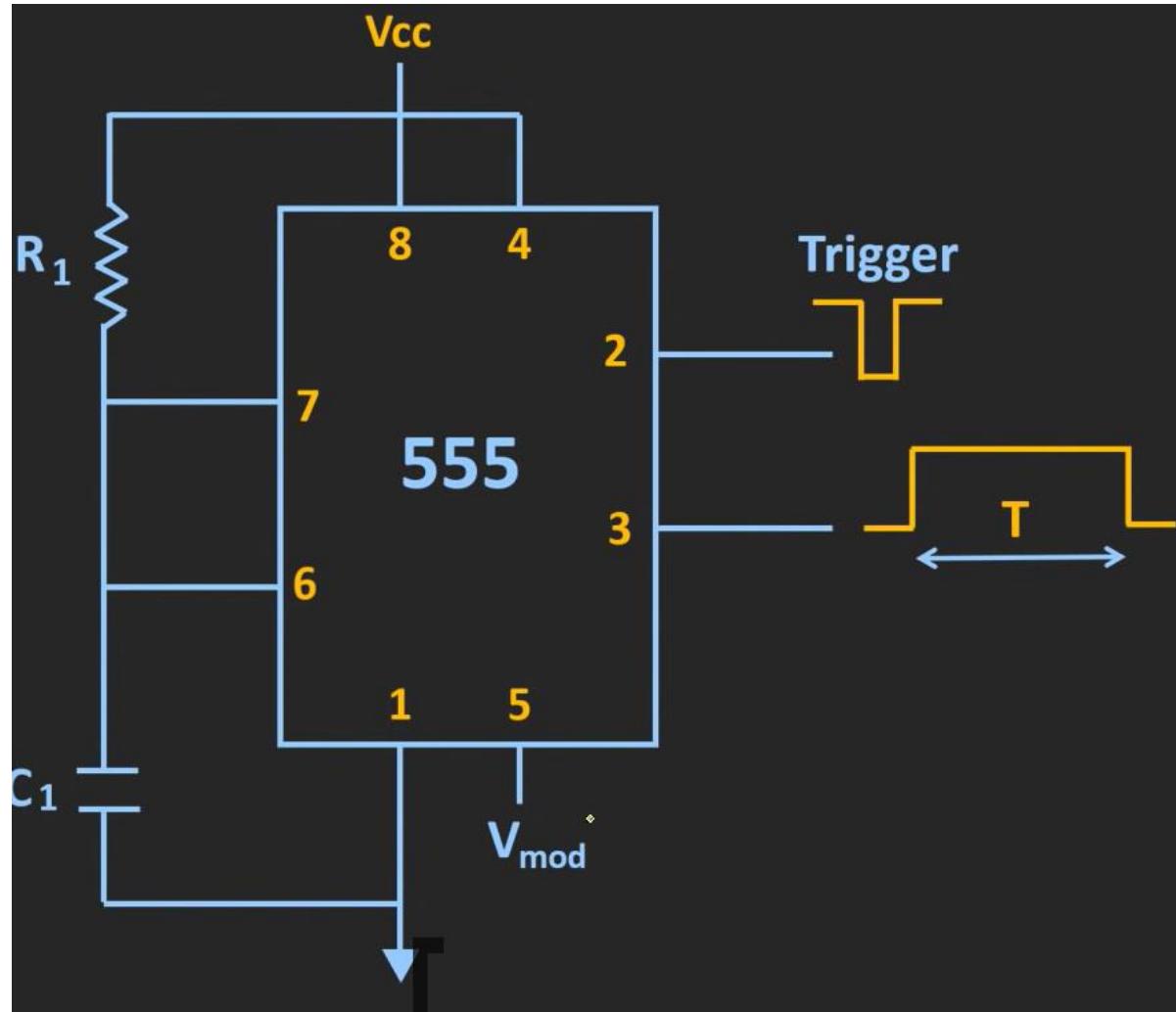
$$R = 193.423k\Omega$$

APPLICATION OF MONOSTABLE MULTIVIBRATOR

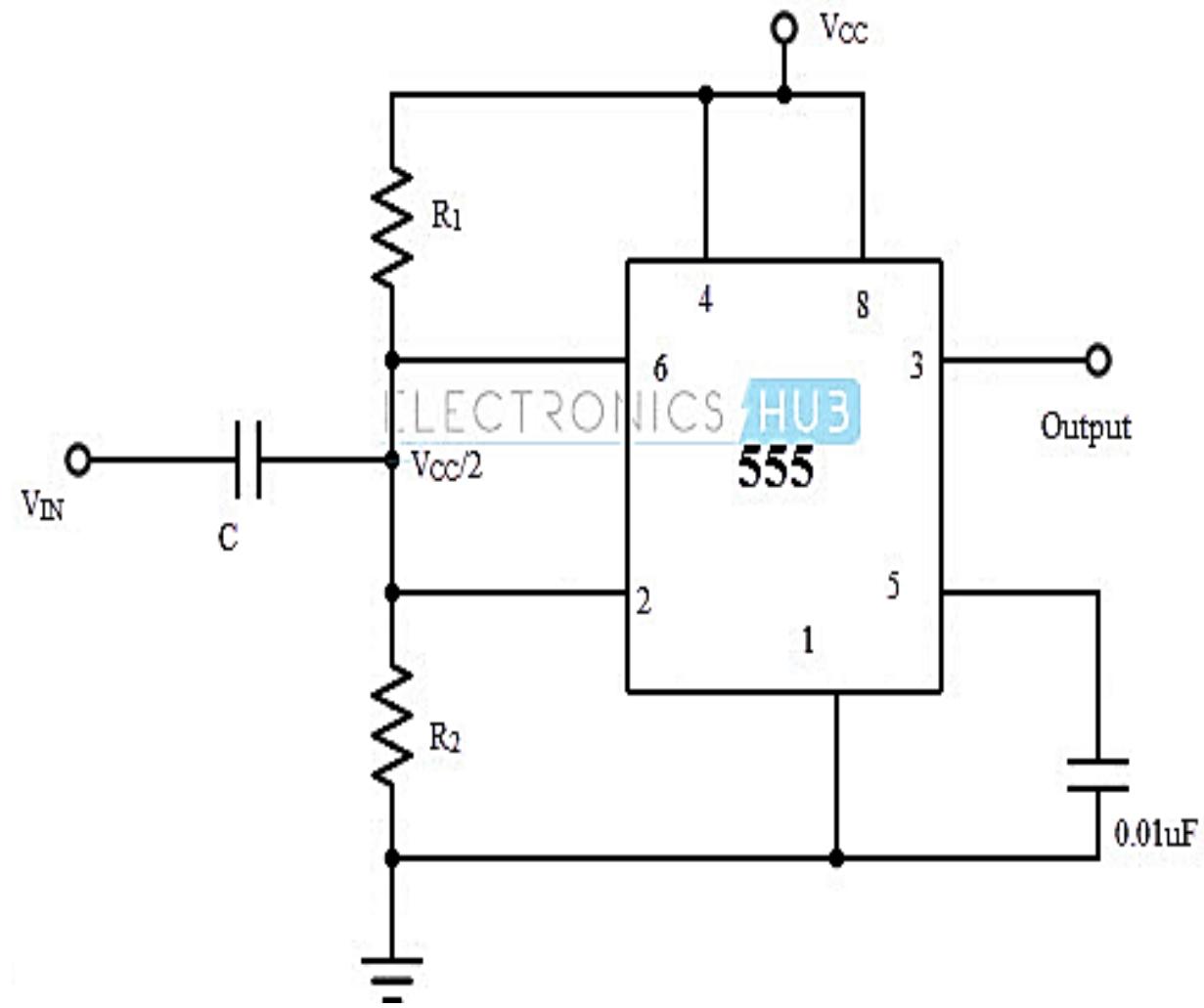
Frequency Divider



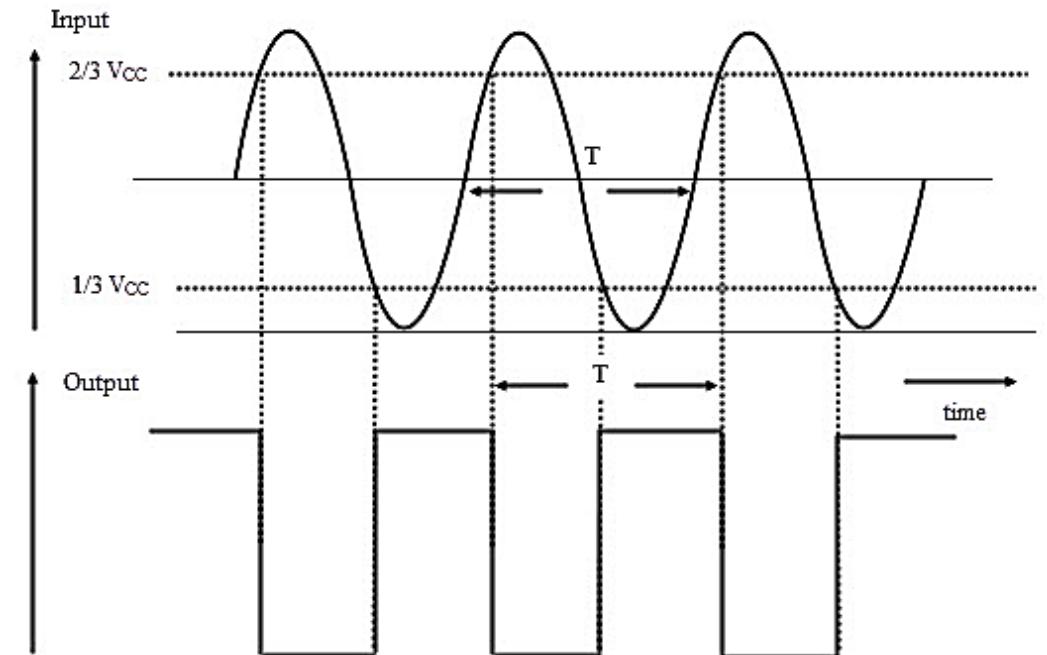
Pulse Width Modulation



SCHMITT TRIGGER



TIMING PULSES



LIC: LECTURE

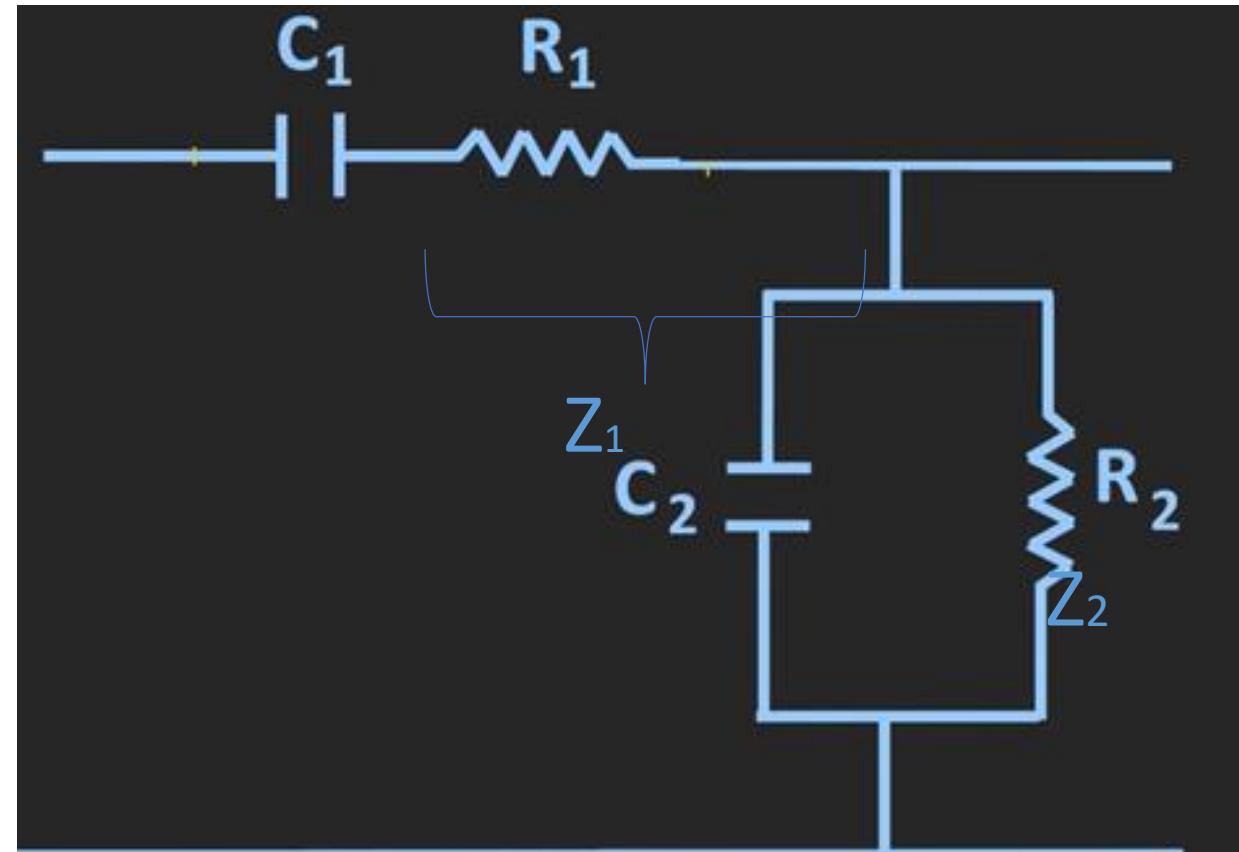
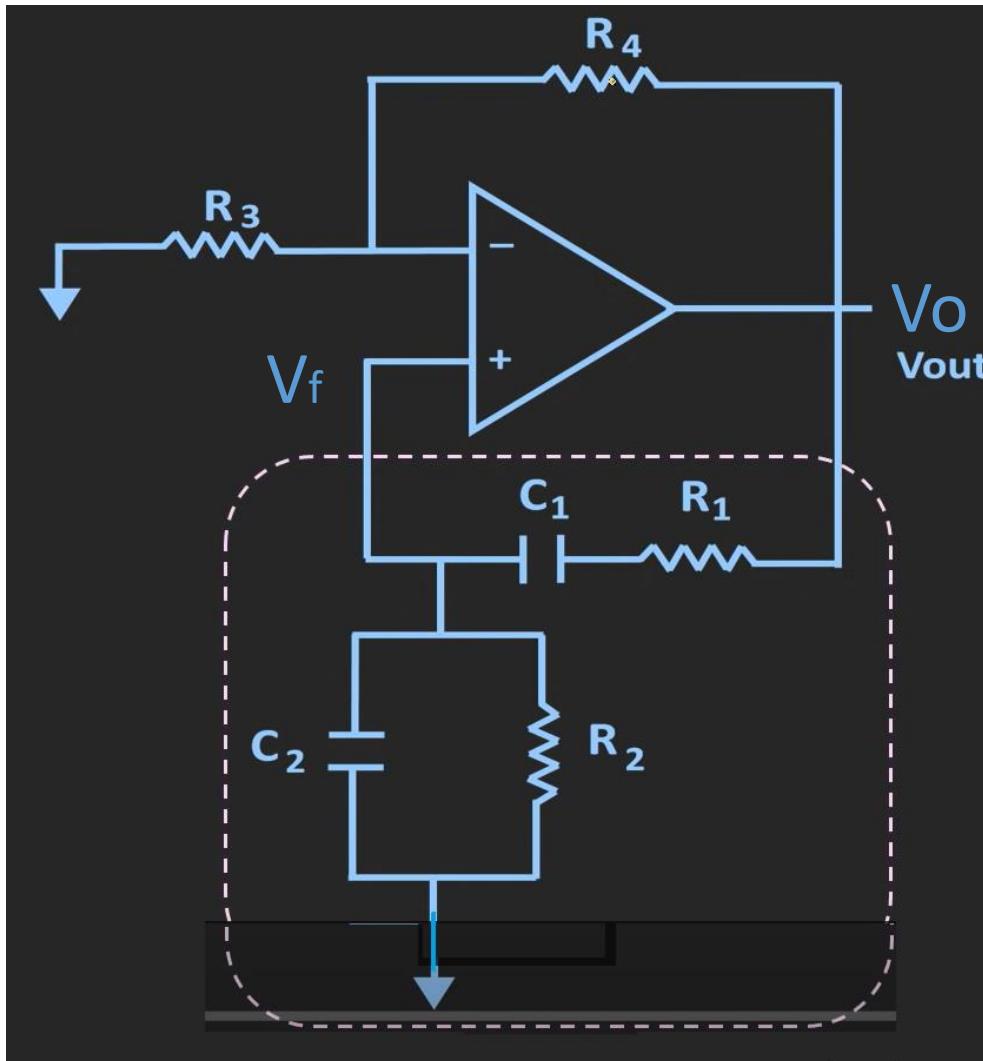
Signal Generators

- ✓ Design of Multivibrators using Timer IC
 - ✓ Different Applications
- Sine Wave Generation Using Op-Amp
 - Circuit
 - Derivation of frequency of operation
- Triangular Wave Generation Using Op-Amp
 - Circuit
 - Derivation of frequency of operation

Sine Wave Generation

- One of the simplest sine wave oscillators which uses a RC network in place of the conventional LC tuned tank circuit to produce a sinusoidal output waveform, is called a **Wien Bridge Oscillator**.
- The **Wien Bridge Oscillator** is so called because the circuit is based on a frequency-selective form of the Wheatstone bridge circuit.
- The Wien Bridge oscillator is a two-stage RC coupled amplifier circuit that has good stability at its resonant frequency, low distortion and is very easy to tune making it a popular circuit as an audio frequency oscillator but the phase shift of the output signal is considerably different from the previous phase shift **RC Oscillator**.

WEIN'S BRIDGE OSCILLATOR



$$\beta = V_f / V_o$$

The loop gain must be unity or greater. The feedback signal feeding back at the input must be phase-shifted by 360° (which is the same as zero degrees).

$$\beta = \frac{1}{3}$$

$$\frac{V_o}{V_{in}} = \frac{\frac{Z_2}{Z_1+Z_2}}{= \frac{R_2}{1+j\omega R_2 C_2}}$$

$$\frac{V_o}{V_{in}} = \frac{\frac{R_2}{1+j\omega R_2 C_2}}{R_1 + \frac{1}{j\omega C_1} + \frac{R_2}{1+j\omega C_2 R_2}}$$

$$\frac{V_o}{V_{in}} = \frac{\frac{R_2 C_1 j\omega C_1}{R_1 C_1 j\omega C_1 (1+j\omega C_2 R_2) + 1+j\omega C_2 R_2 + j\omega R_2 C_1}}{j\omega R_2 C_1}$$

$$\frac{V_o}{V_{in}} = \frac{j\omega R_2 C_1}{1 - \omega^2 R_1 R_2 C_1 C_2 + j\omega [R_1 C_1 + R_2 C_2 + R_2 C_1]}$$

$$\omega^2 R_1 R_2 C_1 C_2 = 1$$

$$\Rightarrow \omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \Rightarrow f = \frac{1}{2\pi \times \sqrt{R_1 R_2 C_1 C_2}} \Rightarrow f = \frac{1}{2\pi R C}$$

$$\frac{V_o}{V_{in}} = \frac{\frac{R_2 C_1}{R_1 C_1 + R_2 C_2 + R_2 C_1}}{= \beta}$$

$$A\beta = 1$$

$$A = \frac{1}{\beta} = \frac{R_1 C_1 + R_2 C_2 + R_2 C_1}{R_2 C_1} = \frac{R_1}{R_2} + \frac{C_2}{C_1} + 1$$

$$A = \frac{1}{\beta} = \frac{R_1 C_1 + R_2 C_2 + R_2 C_1}{R_2 C_1} = \frac{R_1}{R_2} + \frac{C_2}{C_1} + 1$$

$$A = 1 + \frac{R_1}{R_3} = \frac{R_1}{R_2} + \frac{C_2}{C_1} + 1$$

$$\Rightarrow \frac{R_1}{R_3} = \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

$$R_1 = R_2$$

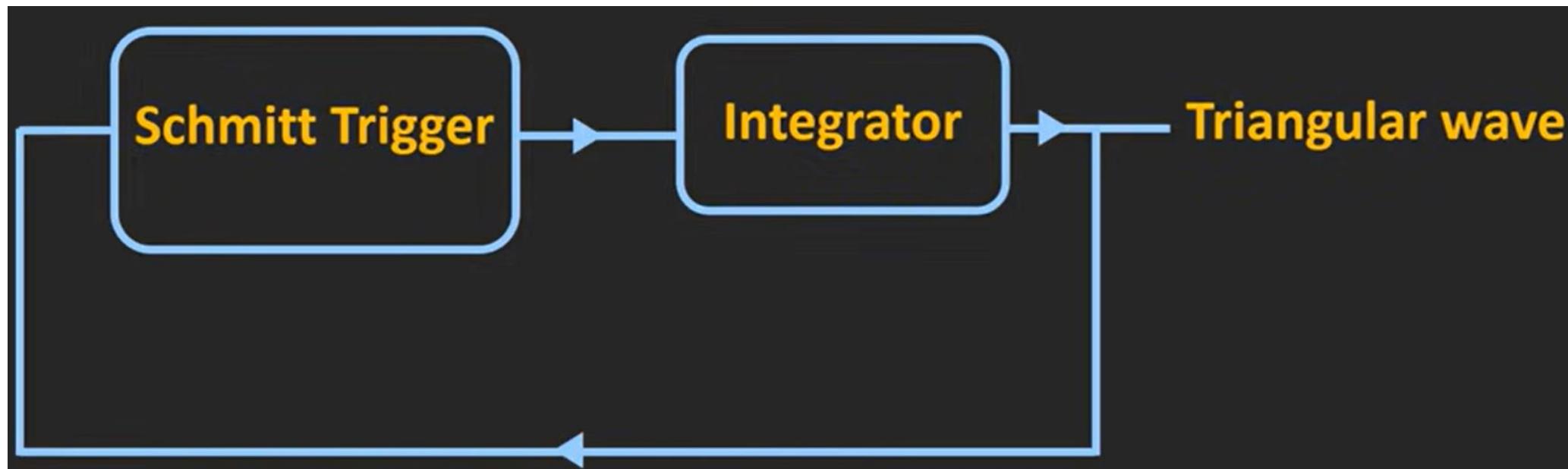
$$C_1 = C_2$$

$$\Rightarrow \frac{R_1}{R_3} = 2$$

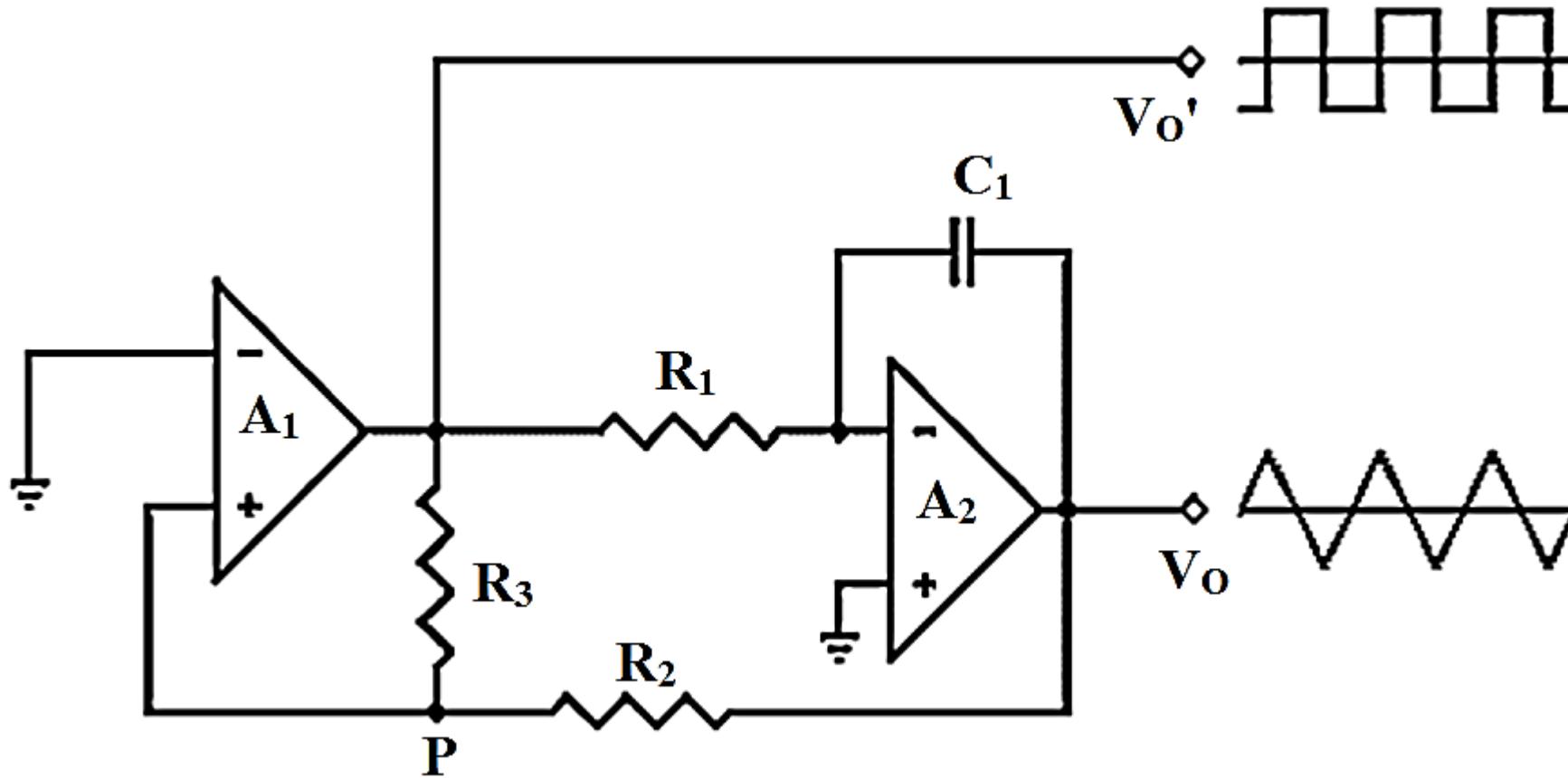
TRIANGULAR WAVE GENERATOR

????

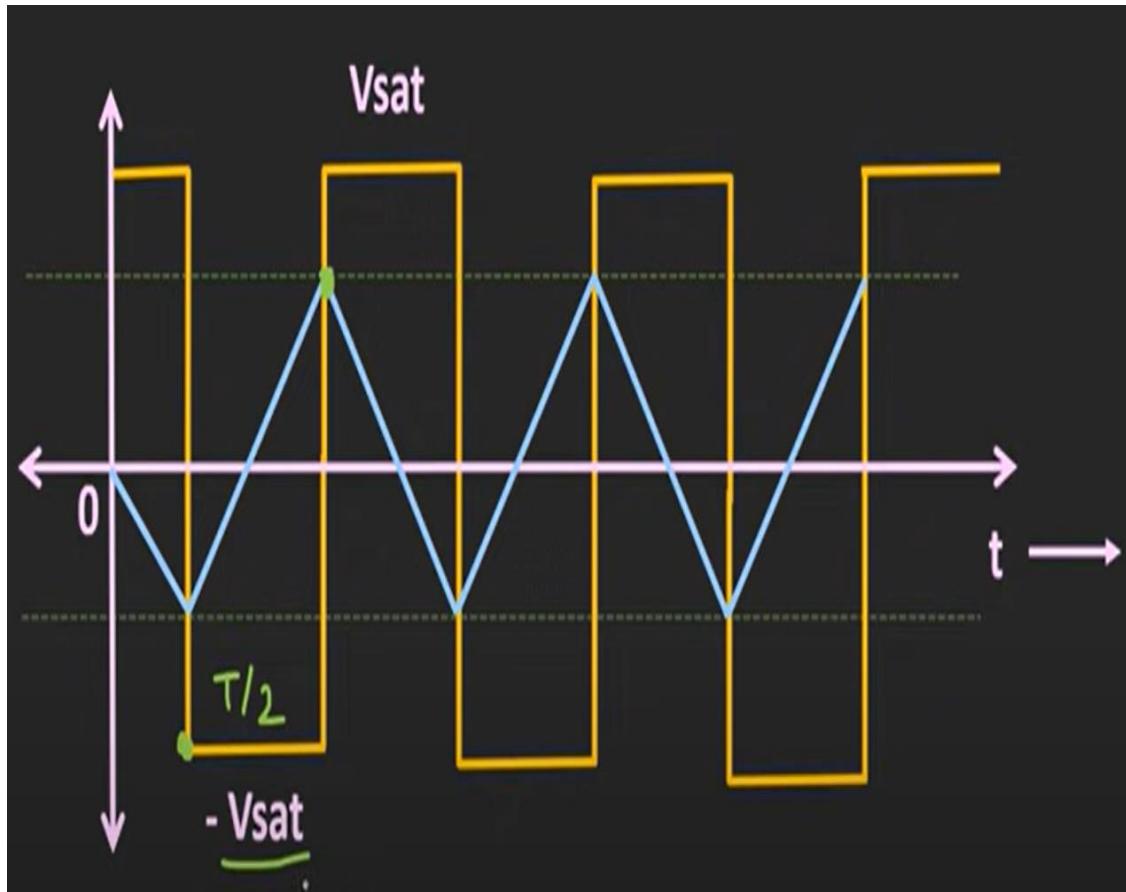
TRIANGULAR WAVE GENERATOR



TRIANGULAR WAVE GENERATOR using Schmitt Trigger

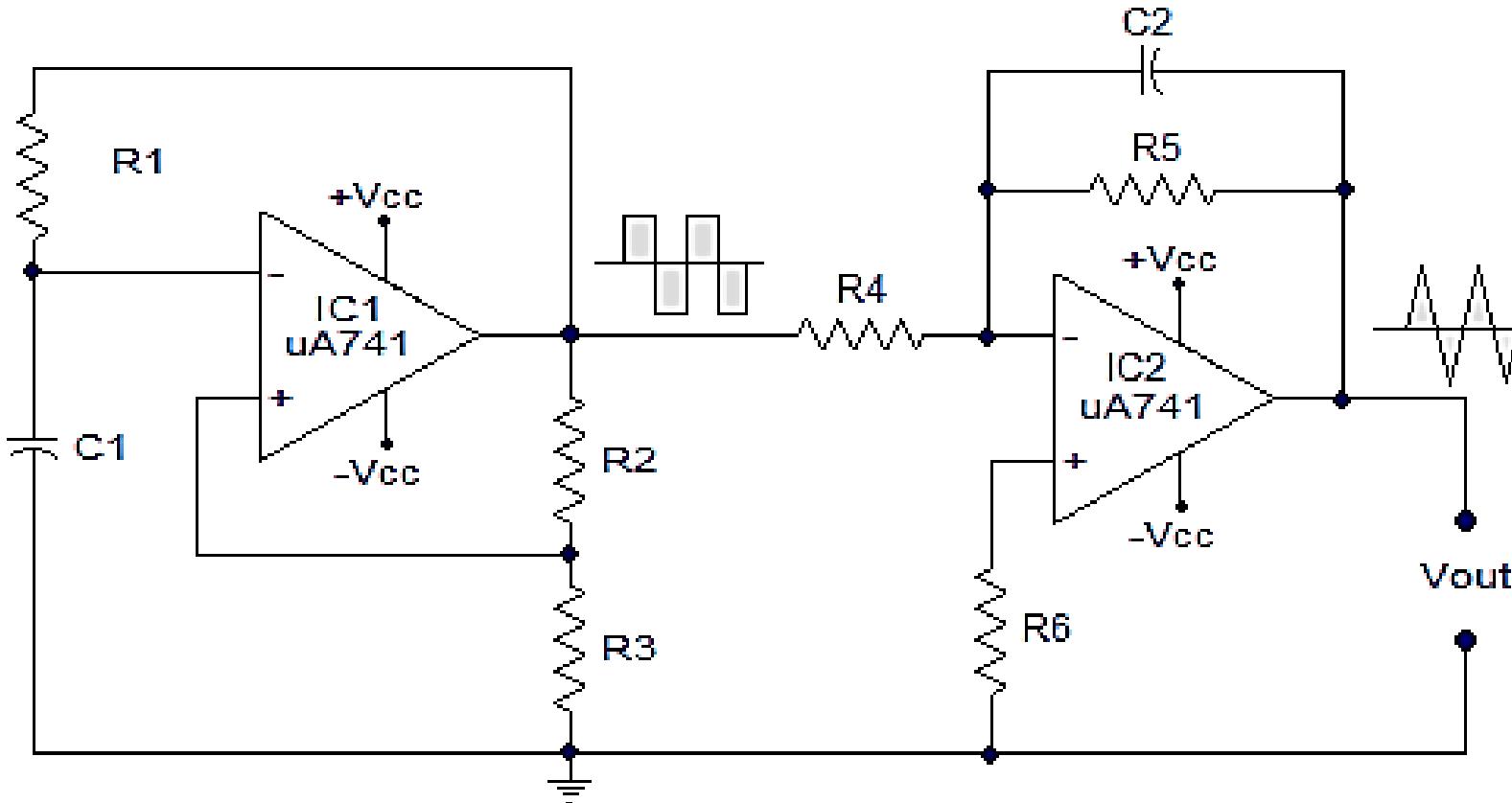


OUTPUT WAVEFORMS



$$V_O = - \frac{1}{R C} \int_0^t V_{in}(t) dt$$
$$V_{C(P-P)} = - \frac{1}{R_3 C_2} \times (-V_{sat}) \times \frac{T}{2}$$
$$V_{P-P} = \frac{V_{sat} \times T}{2 R_3 C_2}$$

TRIANGULAR WAVE GENERATOR using Astable Multivibrator



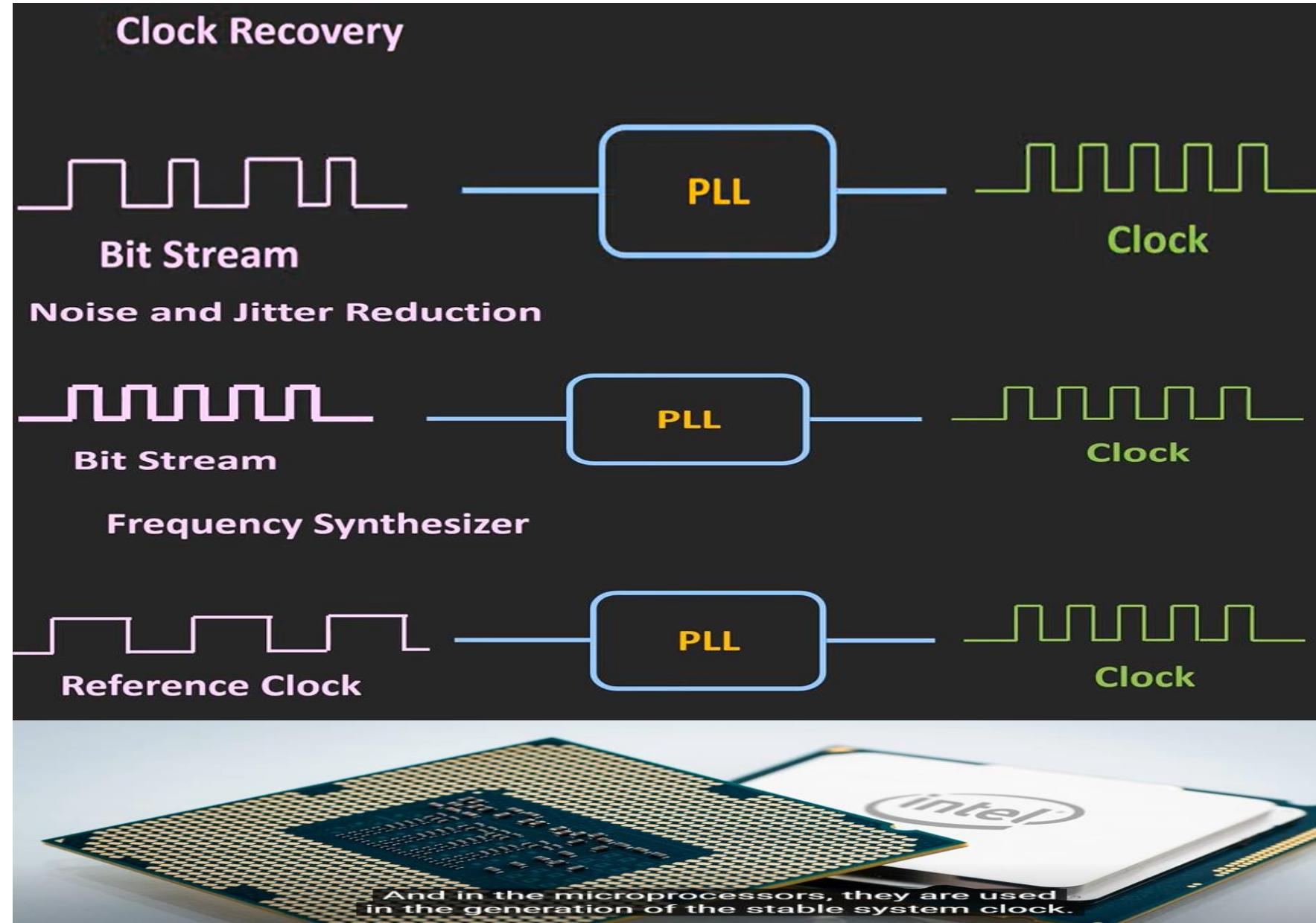
LIC: LECTURE

PHASE LOCKED LOOP (PLL)

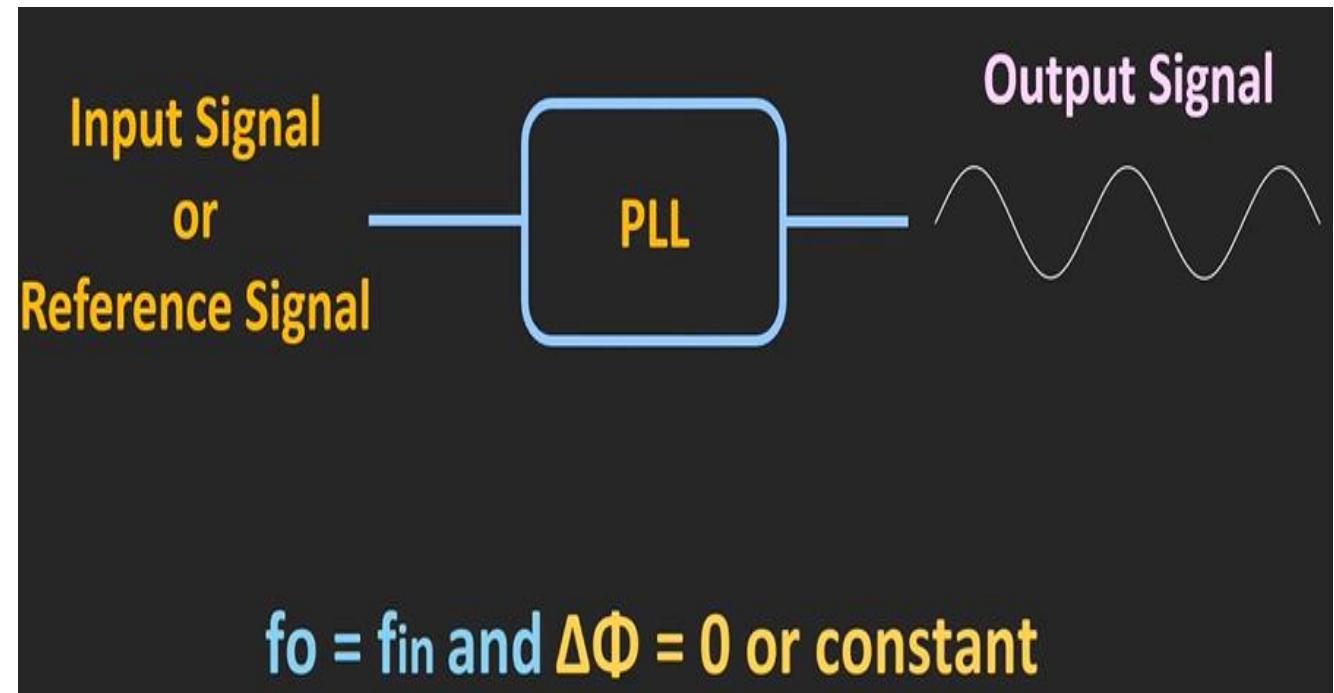
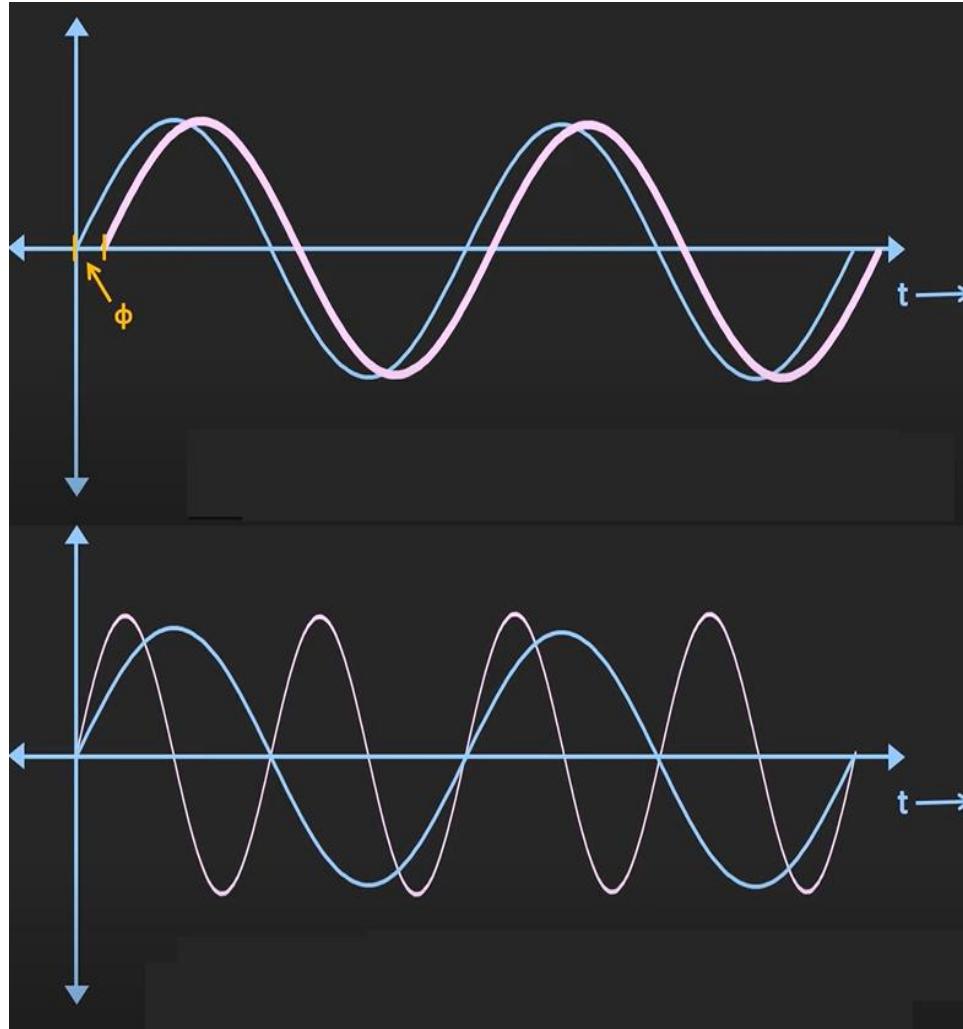
- **PLL Circuit**
 - Need and Requirements
 - Circuit
 - Working Principal
 - Phase Detector Design
 - Voltage Controlled Oscillator
 - Application as Frequency Synthesizer ($f.N$ or f/N)

PHASE LOCKED LOOP (PLL)

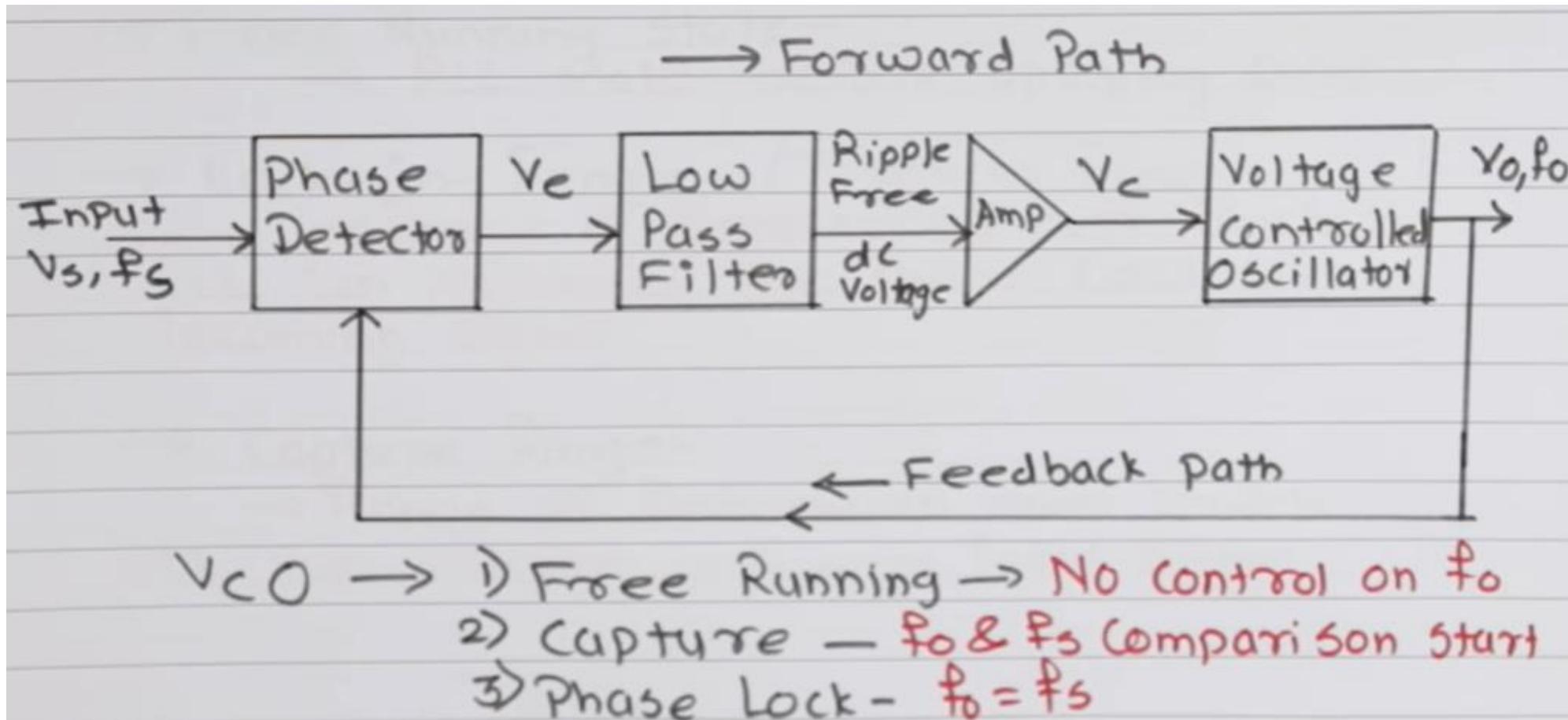
- Frequency Demodulation
- Clock Recovery
- Noise and Jitter Reduction
- Frequency Synthesizer
- Stable System Clock in Microprocessors



PHASE LOCKED LOOP (PLL)

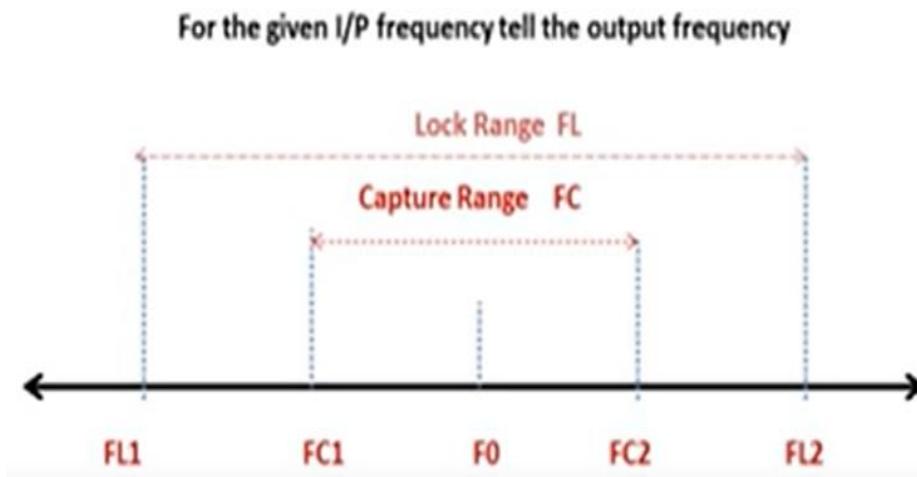


PLL Working Principal

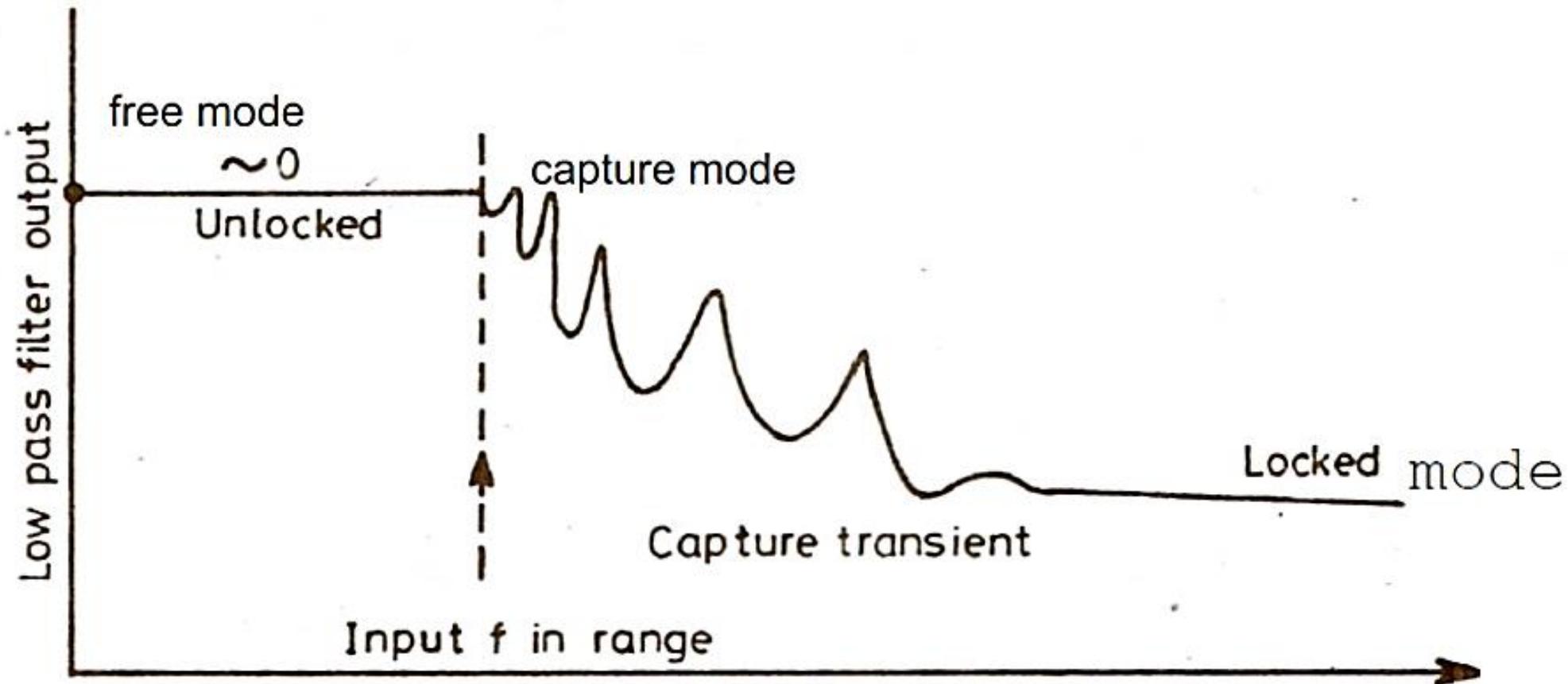


PLL Working Principal

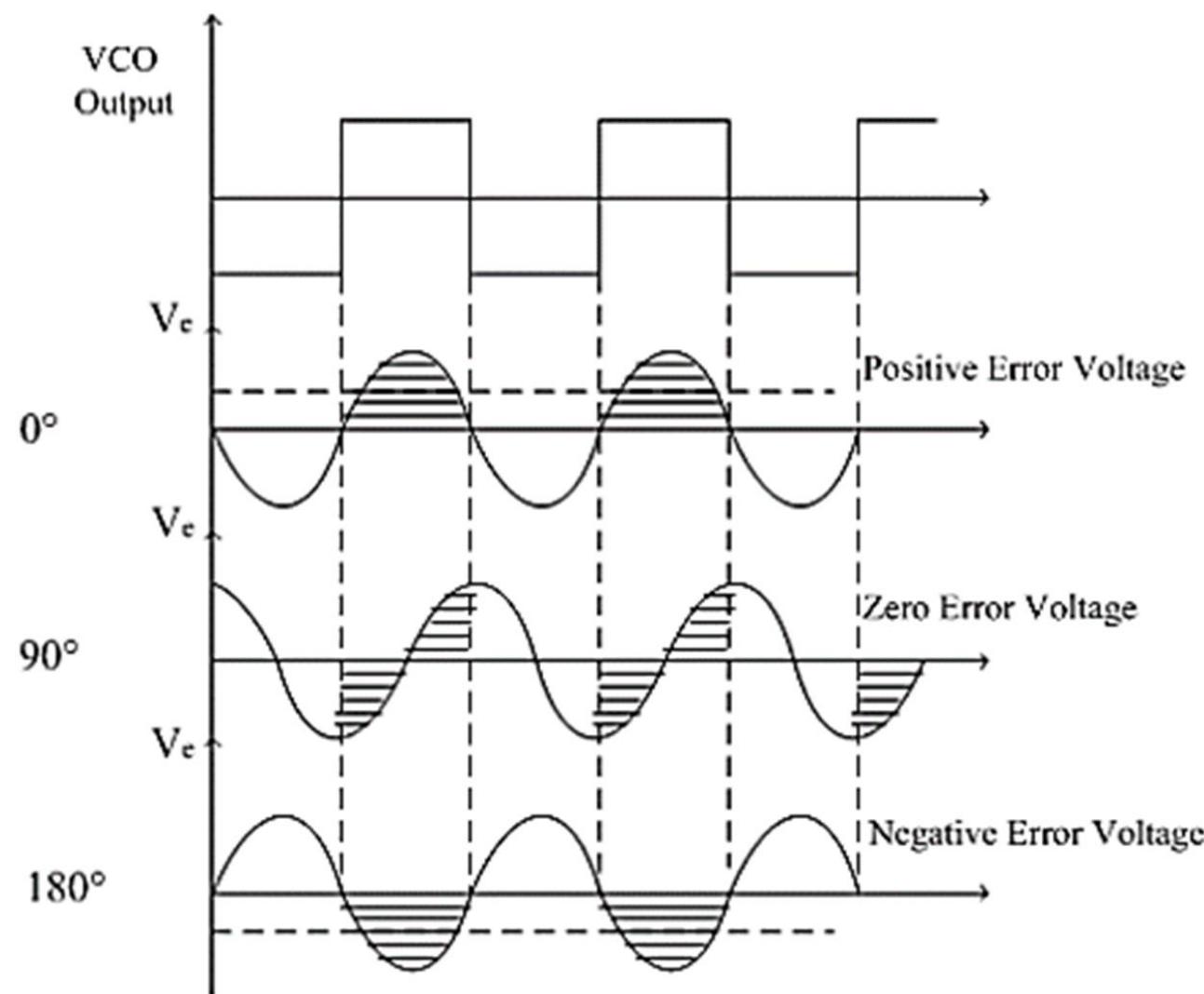
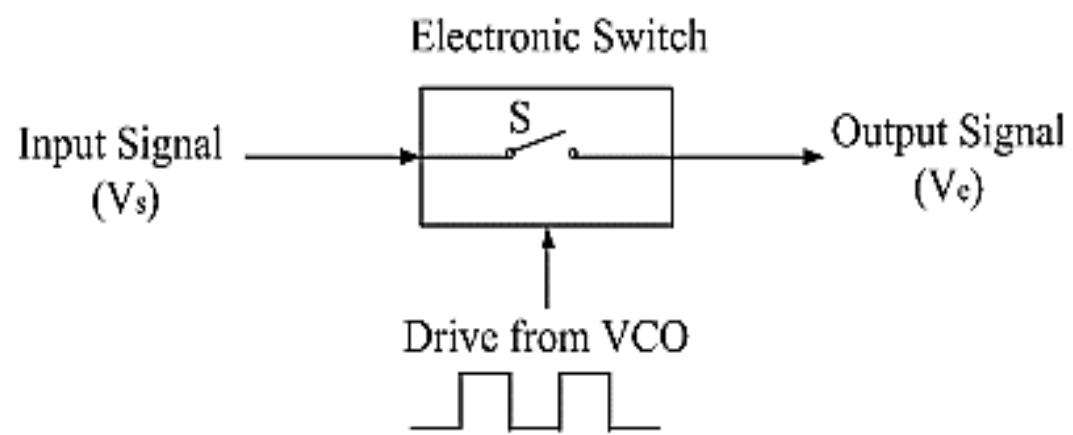
- **Lock range:** The range of frequencies over which the PLL maintains lock with the incoming signal is called the lock range of PLL.
- **Capture range:** The range of frequencies over which the PLL can acquire lock with an i/p signal is called the capture range.
- **PULL In Time:** The capture of an i/p signal does not take place as soon as the signal is applied, But it takes finite time. The total time taken by the PLL to establish lock is called pull-in time.



Capture transient



ANALOG PHASE DETECTOR



Analysis

- ❖ Phase detector is a multiplier which multiplies the input signal ($V_{in} = V_s \sin(2\pi f_{in}t)$) by the VCO signal ($V_{out} = V_o \sin(2\pi f_{out}t + \varphi)$)

- ❖ Therefore, Phase detector output,

$$V_e = kV_s V_o \sin(2\pi f_{in}t) \sin(2\pi f_{out}t + \varphi)$$

where $k \rightarrow$ phase comparator gain

$\varphi \rightarrow$ phase shift between the input signal and the VCO output.

$$\rightarrow V_e = \frac{kV_s V_o}{2} \left(\cos(2\pi f_{in}t - (2\pi f_{out}t + \varphi)) - \cos(2\pi f_{in}t + 2\pi f_{out}t + \varphi) \right)$$

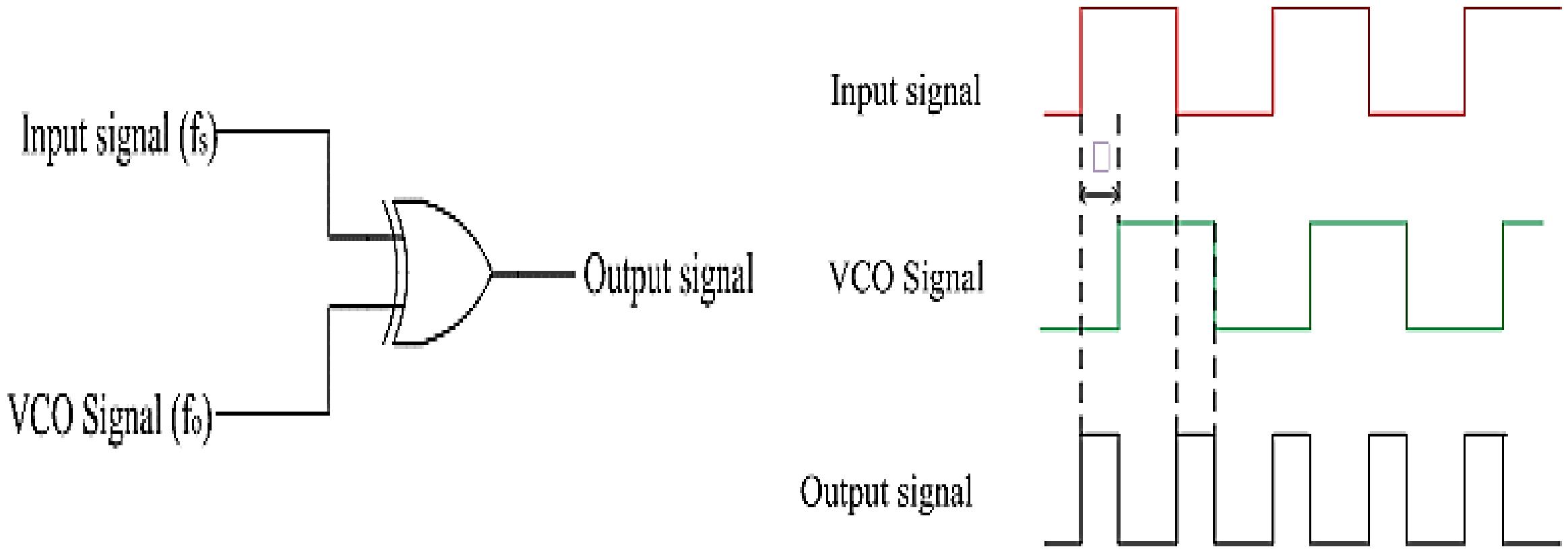
- ❖ Above expression indicates that output contains a double frequency term and a DC component.

- ❖ Double frequency term is eliminated by the LPF and the DC signal is applied to the modulating input signal of the VCO.
- ❖ When at lock, $f_{in} = f_{out}$,
$$\rightarrow V_e = \frac{kV_s V_o}{2} (\cos(-\varphi) - \cos(2\pi * 2f_{out}t + \varphi))$$
- ❖ For a perfect locked state, the phase shift should be 90° , in order to get zero error signal, i.e. $V_e = 0$.

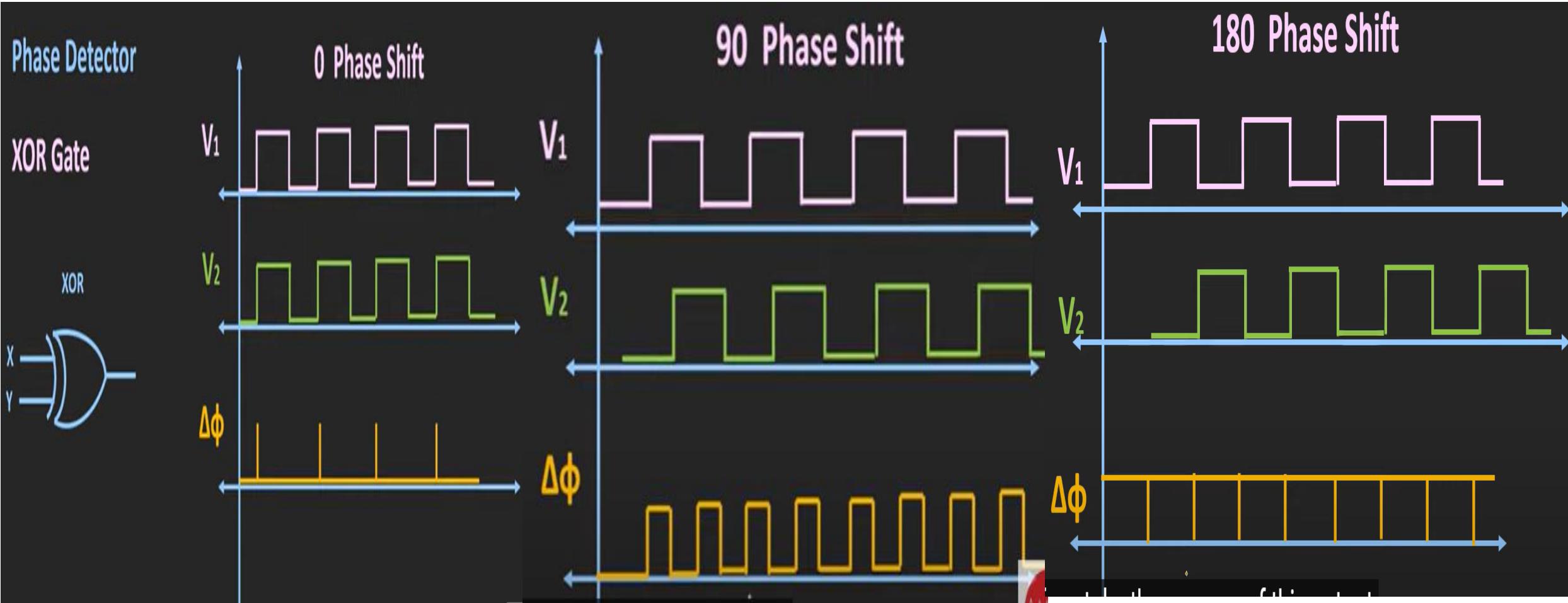
Drawbacks of Switch Type Phase Detector

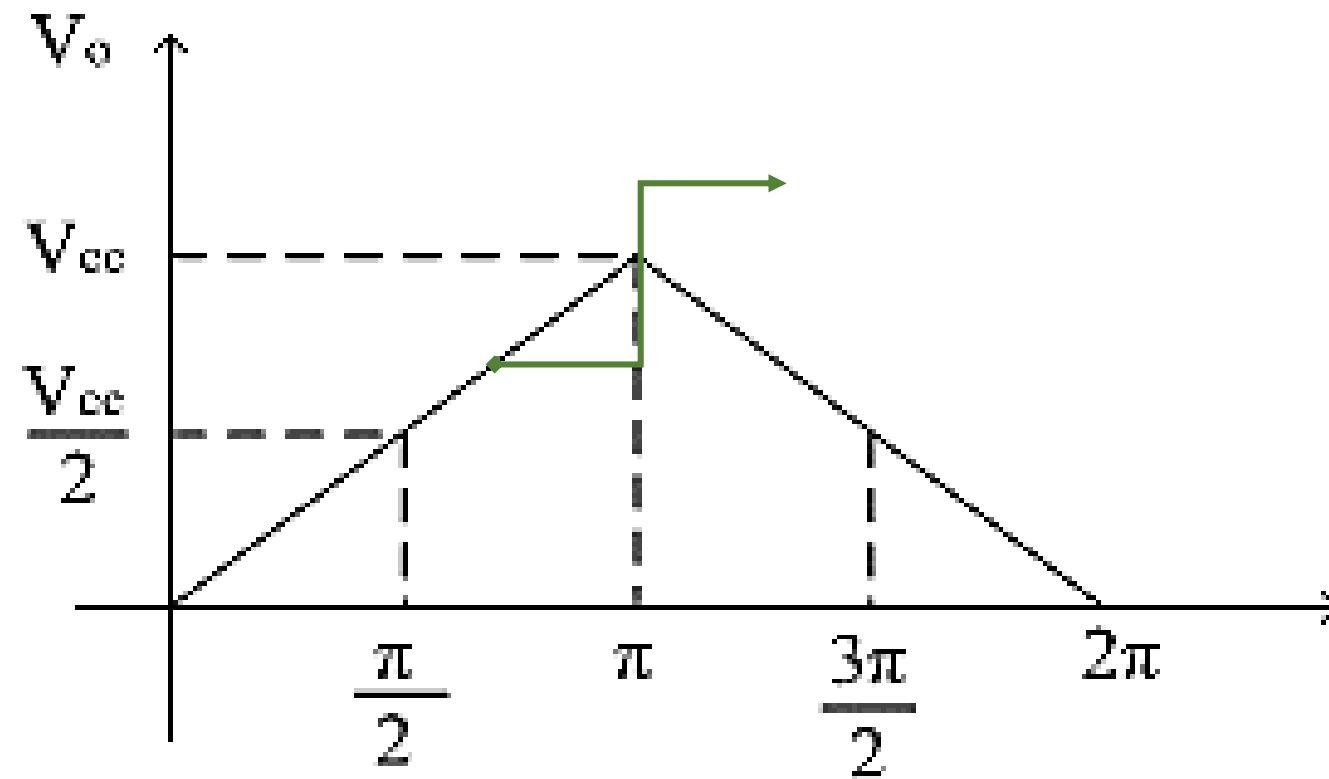
1. Output voltage V_e is proportional to the input signal amplitude making the phase detector gain and the loop gain dependent on the input signal amplitude.
 2. Output is proportional to $\cos \varphi$ and not φ making it non-linear.
- Both drawbacks can be eliminated by limiting the amplitude of the input signal i.e. converting the input to a constant amplitude square wave.

DIGITAL Phase Detector



DIGITAL Phase Detector





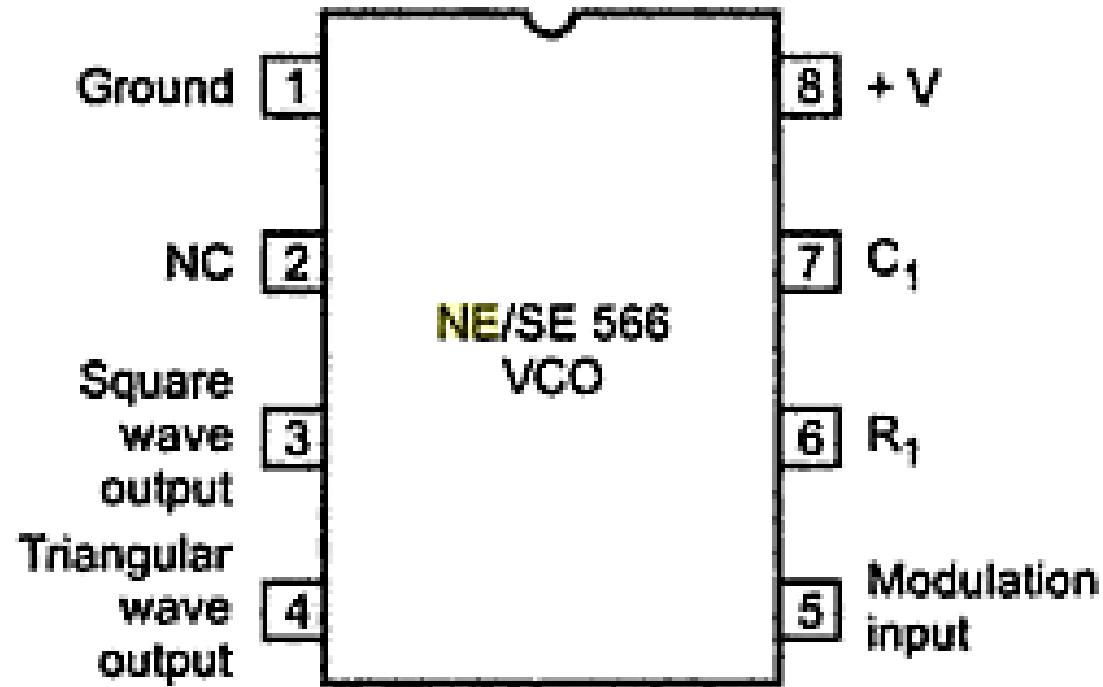
DC Output voltage Vs phase difference ϕ curve

LIC: LECTURE PHASE LOCKED LOOP (PLL)

✓ PLL Circuit

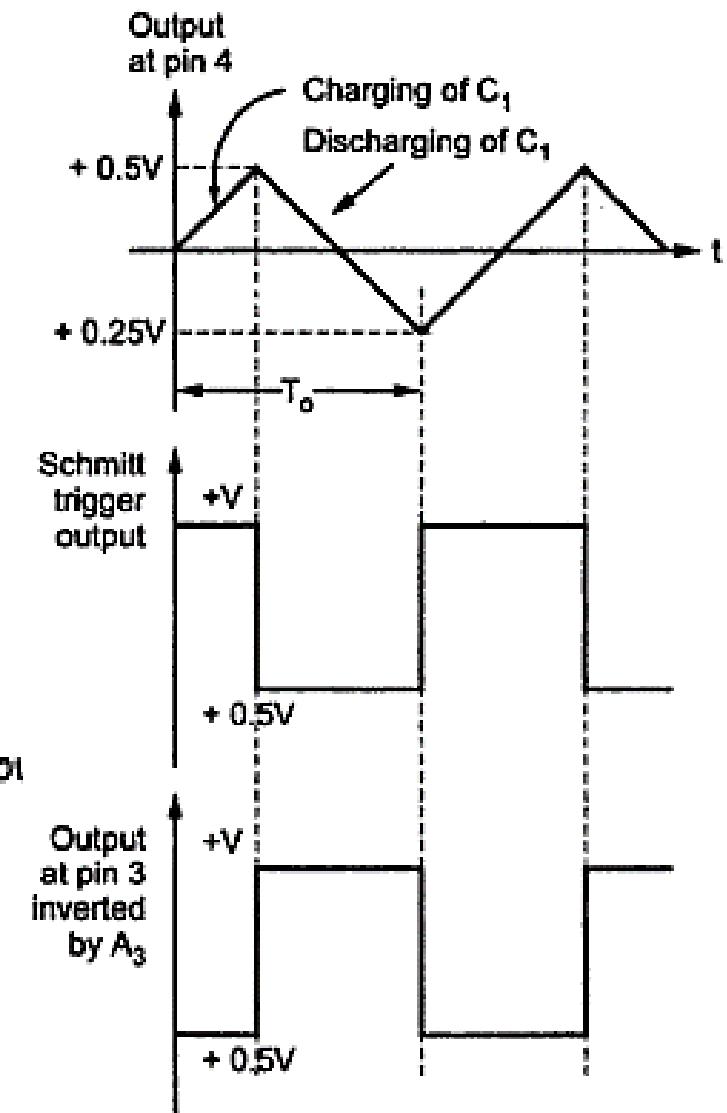
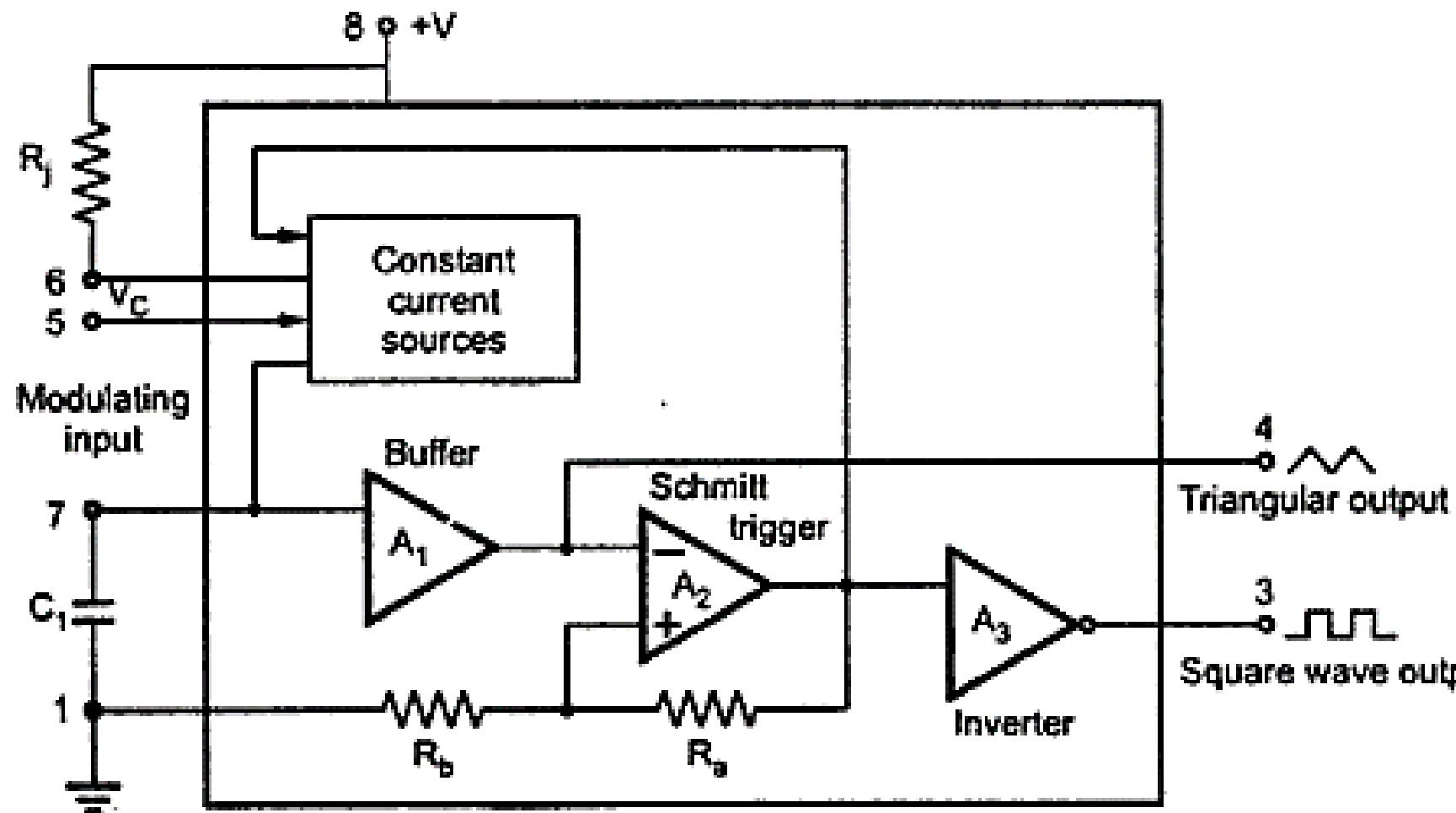
- ✓ Need and Requirements
- ✓ Circuit
- ✓ Working Principal
- ✓ Phase Detector Design
 - Voltage Controlled Oscillator
 - Application as Frequency Synthesizer ($f.N$ or f/N)

VOLTAGE Controlled Oscillator (VCO)



Pin Configuration

BLOCK DIAGRAM



Output Frequency Calculation

- Total voltage on the capacitor changes from $0.25 V_{CC}$ to $0.5 V_{CC}$.

$$\therefore \Delta V = 0.25 V_{CC}$$

- Capacitor charges with a constant current source.

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_1}$$
$$\Delta t = \frac{0.25 V_{CC} C_1}{i}$$

- Time period of triangular waveform = $2\Delta t$

- Frequency, f_o is

$$f_o = \frac{1}{T}$$

- But,

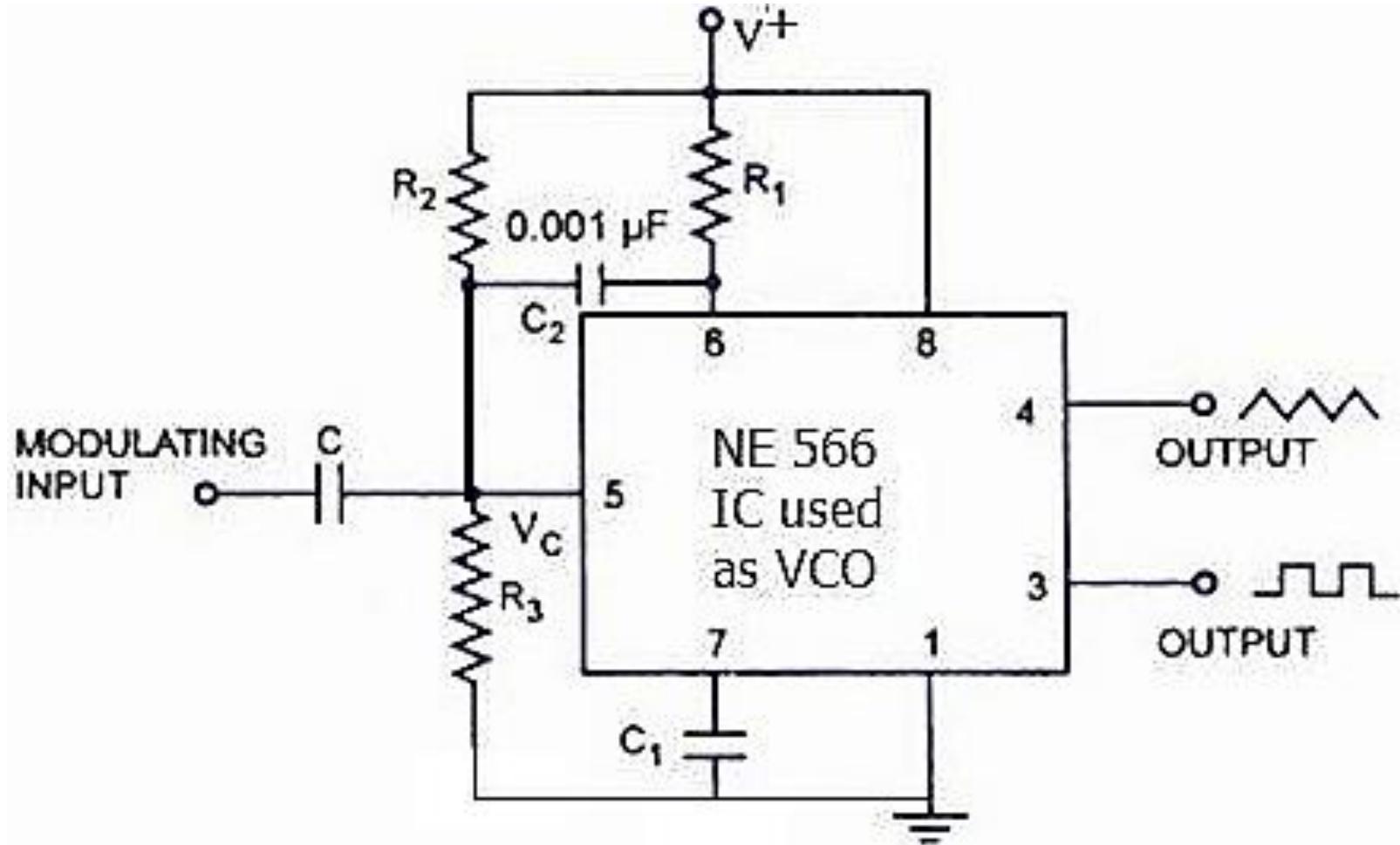
$$i = \frac{V_{CC} - V_C}{R_1}$$

- where V_C = voltage at pin 5.

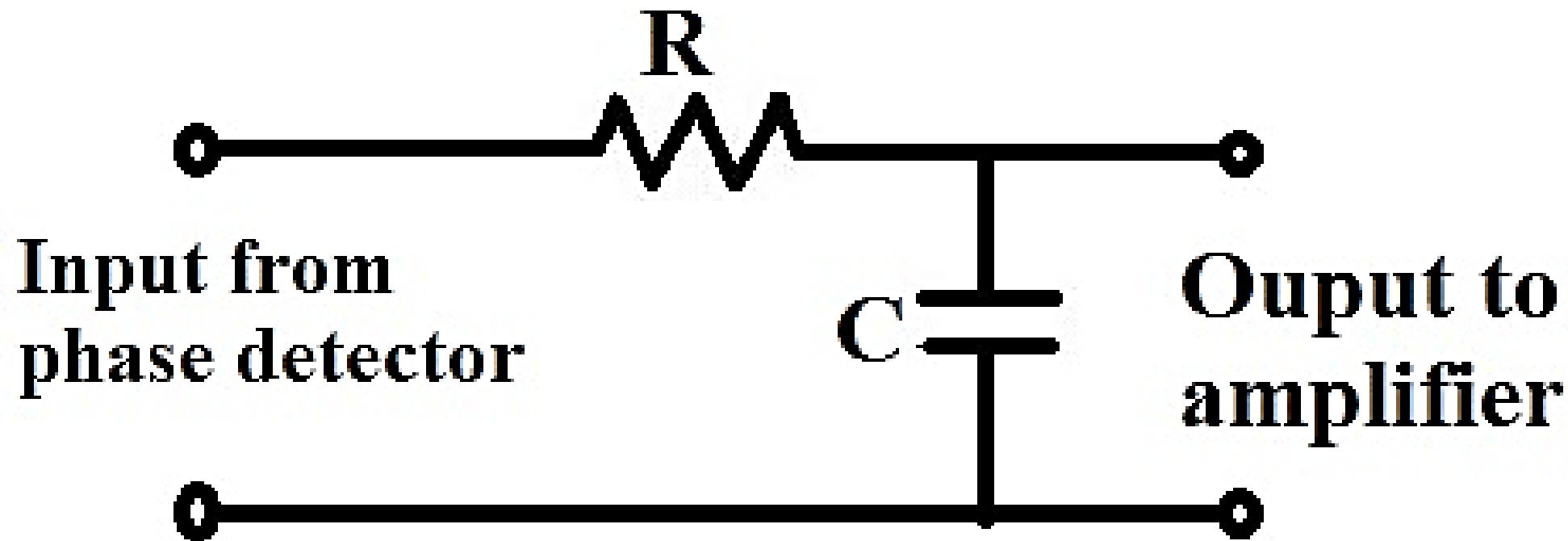
$$f_o = \frac{2(V_{CC} - V_C)}{C_1 R_1 V_{CC}}$$

Outcomes

- Output freq. of VCO can be changed by –
 - R_1
 - C_1
 - Modulating input V_C
- V_C can be varied by connecting a $R_2 - R_3$ circuit as shown in the circuit.



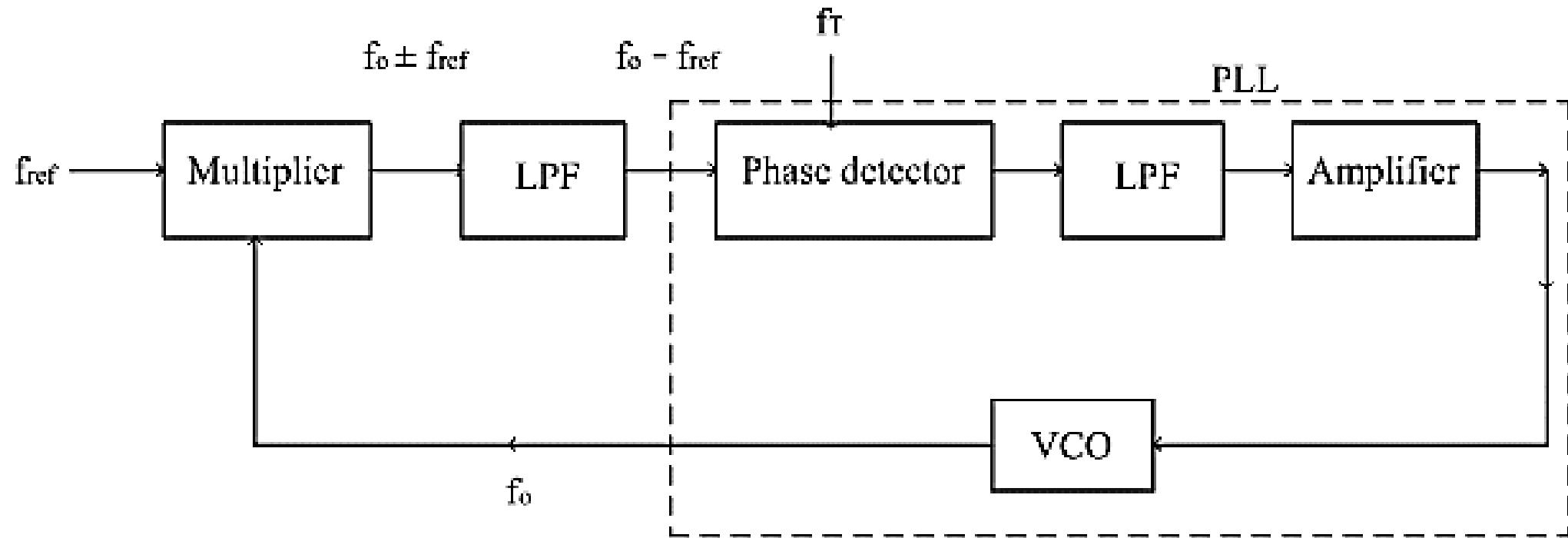
Low Pass Filter



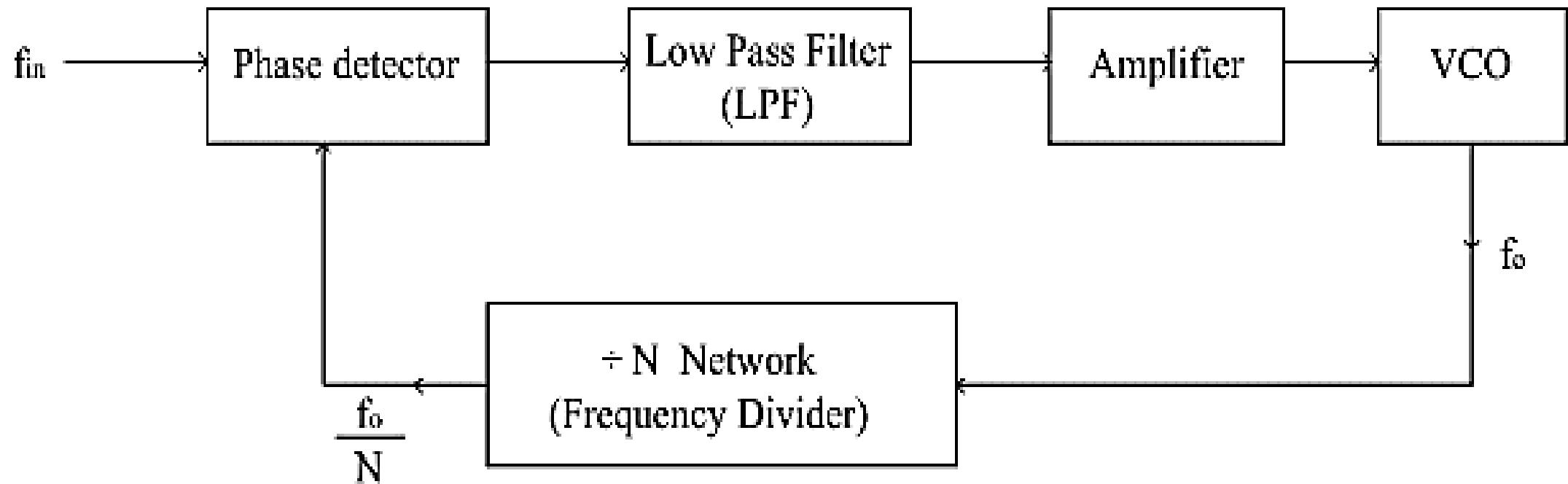
Applications of PLL

- ❖ Frequency Translation
- ❖ Frequency Multiplier/Divider
- ❖ Frequency Synthesizer

Frequency Translation

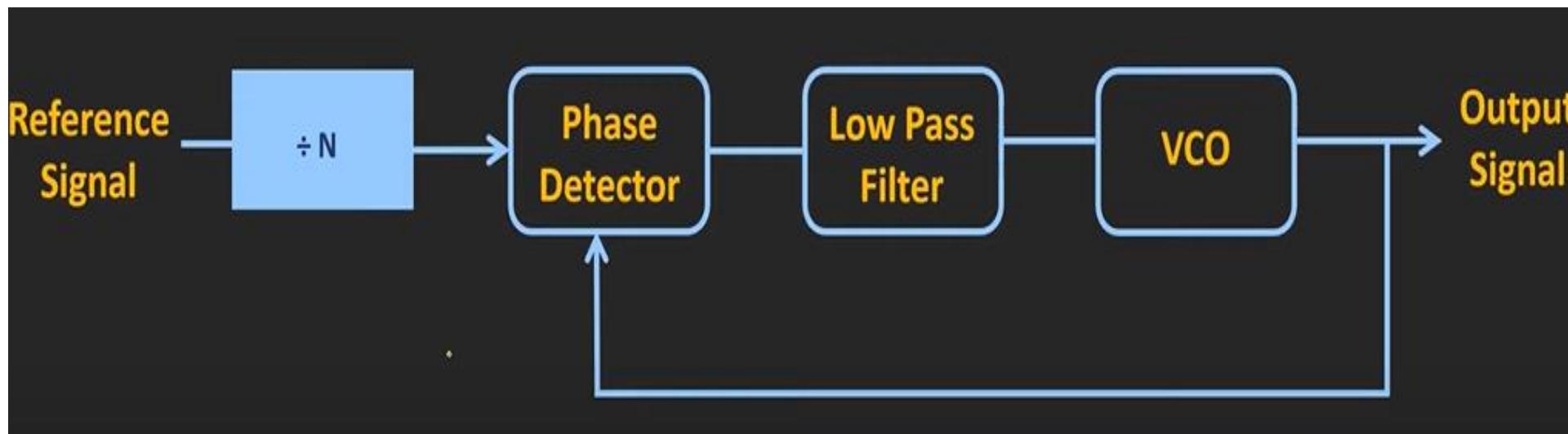
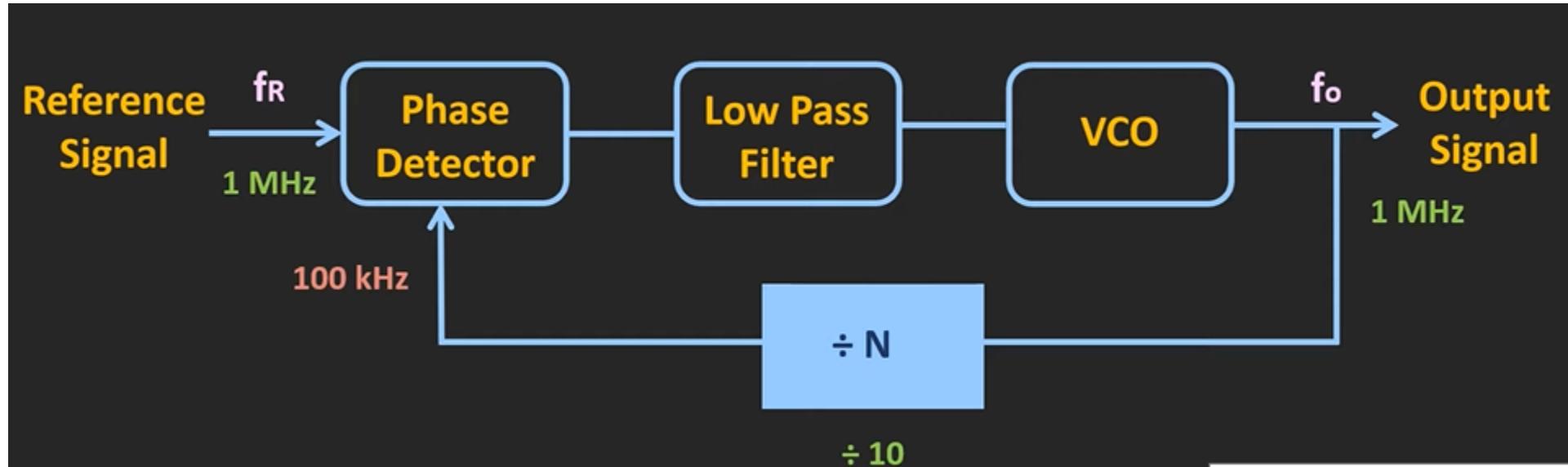


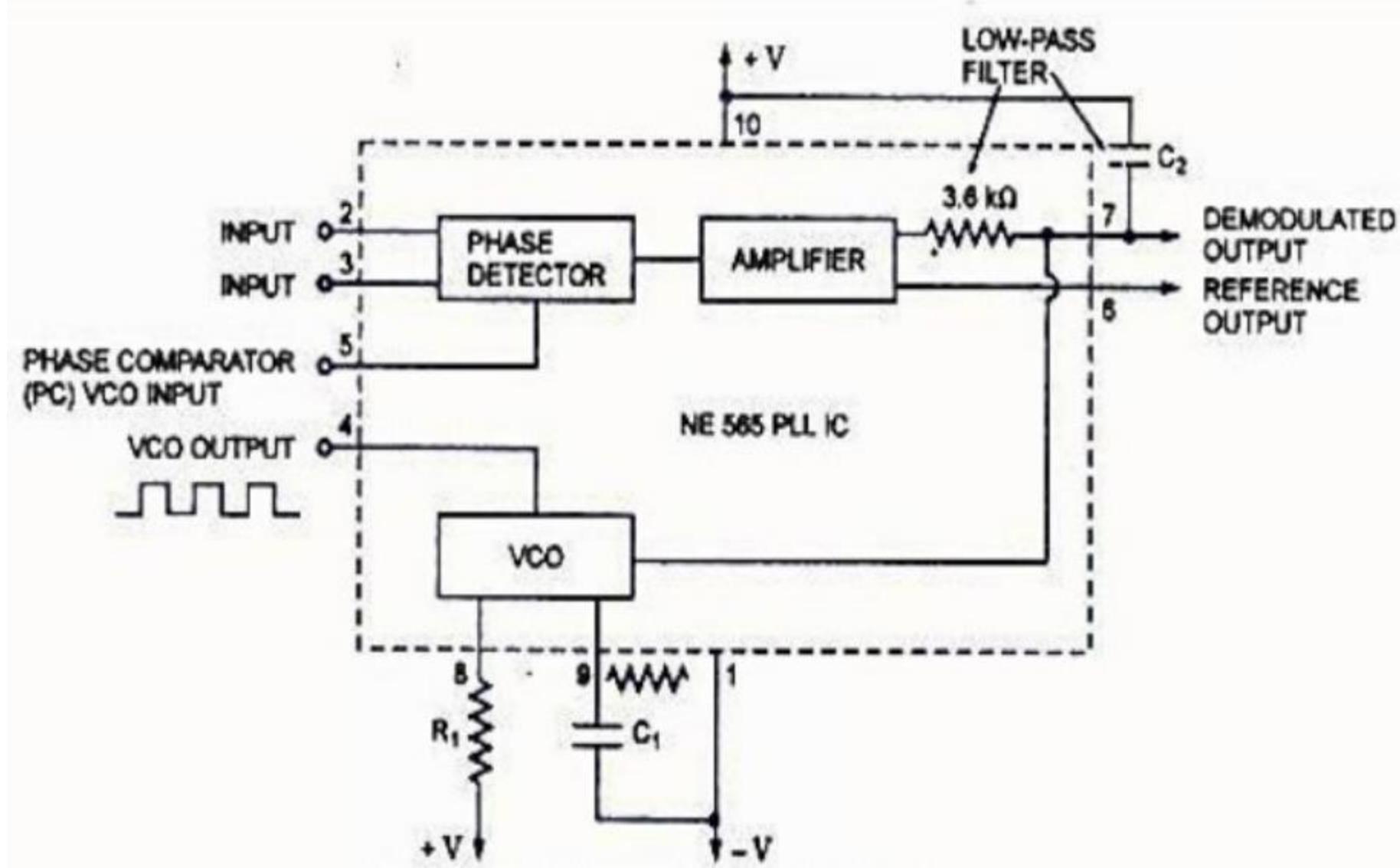
Frequency multiplier/ divider



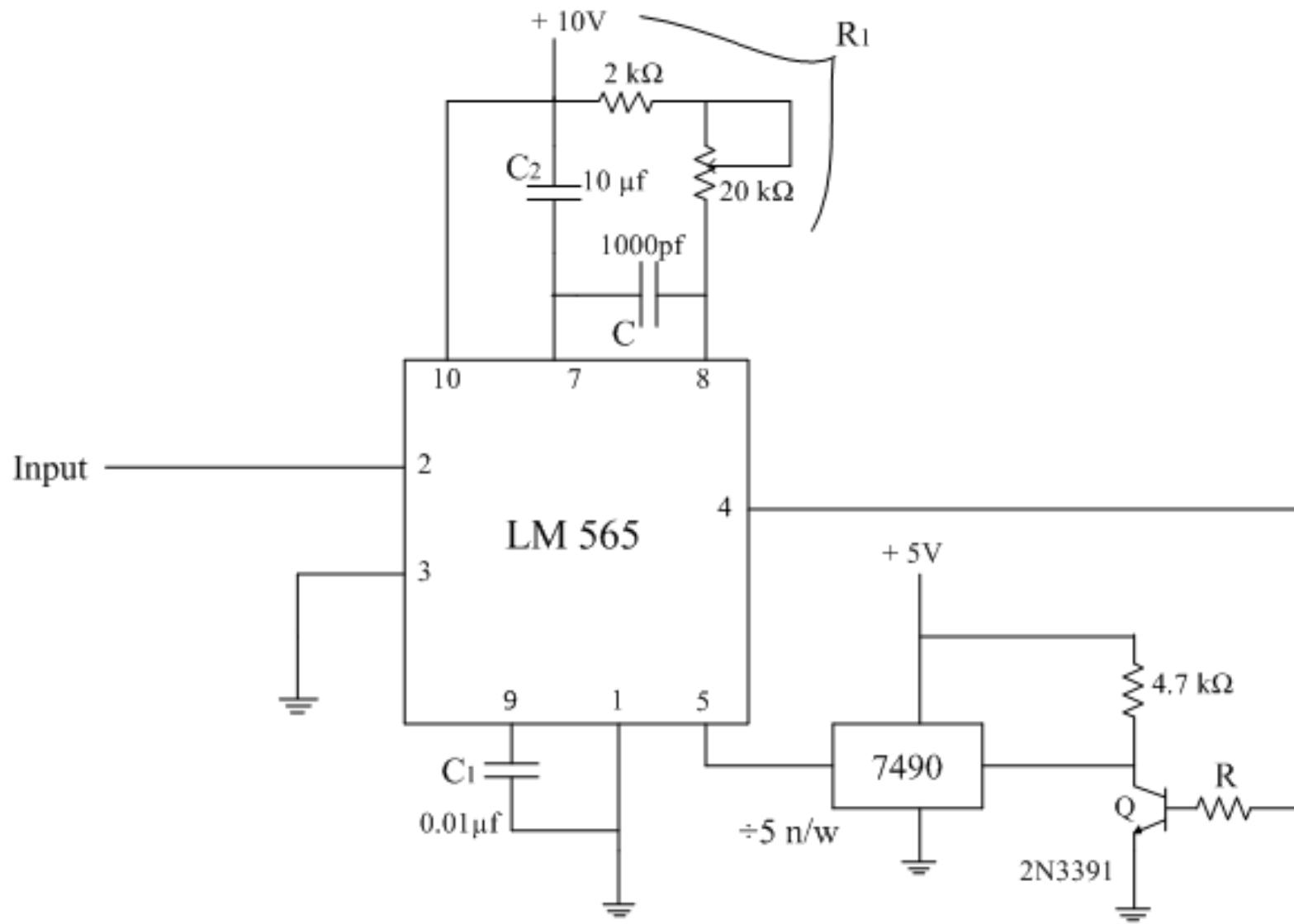
FREQUENCY MULTIPLIER

Frequency Synthesizer





Monolithic Phase Locked loop (NE/SE 565)



LIC: LECTURE

Voltage Reference and Regulators

- Introduction
- Performance Specifications
- Line and Load Regulations
- Thermal Coefficient
- Zener Diode as shunt Regulator

Performance Specifications

- The ability of a voltage reference or regulator to maintain a constant output under varying external conditions is characterized in terms of performance parameters such as:
 - ❖ line and load regulation
 - ❖ and the thermal coefficient.
- In the case of voltage references, output noise and long-term stability are also significant.

Line and Load Regulations

Voltage Regulator \rightarrow Maintain the o/p voltage constant.

conditions

- 1) Even though i/p changes
- 2) R_L changes.

Line Regulation \rightarrow change in o/p voltage to change in i/p voltage

$$\text{Line regulation} = \frac{\Delta V_o}{\Delta V_i} \quad \frac{5-5}{235-230} =$$

Line regulation = 0%. ΔV_o in μV

$230^{\text{i/p}} \rightarrow 5V$. $235 \rightarrow 5V$ ΔV_i in V
Line regulation in $\mu V/V$

Line and Load Regulations

$$\begin{aligned}\text{Load Regulation} &= \frac{\Delta V_o}{\Delta I_L} \\ &= \frac{V_{NL} - V_{FL}}{\Delta I_L}\end{aligned}$$

V_{NL} = No load voltage.

No load
No current
 $R = \infty$

V_{FL} = Full load voltage.

Load regulation = 0.1.

Line and Load Regulations

$$\text{Line regulation} = \frac{\Delta V_O}{\Delta V_I}$$

$$\text{Line regulation (\%)} = 100 \frac{\Delta V_O / V_O}{\Delta V_I}$$

$$\text{Load regulation} = \frac{\Delta V_O}{\Delta I_O}$$

$$\text{Load regulation (\%)} = 100 \frac{\Delta V_O / V_O}{\Delta I_O}$$

A related parameter is the *ripple rejection ratio* (RRR), expressed in decibels as

$$\text{RRR}_{\text{dB}} = 20 \log_{10} \frac{V_{ri}}{V_{ro}}$$

where V_{ro} is the output ripple resulting from a ripple V_{ri} at the input. The RRR is used especially in connection with voltage regulators to provide an indication of the amount of ripple (usually 120-Hz ripple) feeding through to the output.

Line and Load Regulations

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Numerical Problem

Problem: The data sheets of the μ A7805 5-V voltage regulator indicate that V_O typically changes by 3 mV when V_I is varied from 7 V to 25 V, and by 5 mV when I_O is varied from 0.25 A to 0.75 A. Moreover, $RRR_{dB} = 78$ dB at 120 Hz. (a) Estimate the typical line and load regulation of this device. What is the output impedance of the regulator? (b) Estimate the amount of output ripple V_{ro} for every volt of V_{ri} .

- (a) Line regulation = $\Delta V_O / \Delta V_I = 3 \times 10^{-3} / (25 - 7) = 0.17$ mV/V. Alternatively, line regulation = $100(0.17 \text{ mV/V}) / (5 \text{ V}) = 0.0033\%/\text{V}$. Load regulation = $\Delta V_O / \Delta I_O = 5 \times 10^{-3} / [(750 - 250)10^{-3}] = 10 \text{ mV/A}$. Alternatively, load regulation = $100(10 \text{ mV/A}) / (5 \text{ V}) = 0.2\%/\text{A}$. The output impedance is $\Delta V_O / \Delta I_O = 0.01 \Omega$.
- (b) $V_{ro} = V_{ri} / 10^{78/20} = 0.126 \times 10^{-3} \times V_{ri}$. Thus, a 1-V, 120-Hz ripple at the input will result in an output ripple of 0.126 mV.

Thermal Coefficient

- The thermal coefficient of VO , denoted as $TC(VO)$, gives a measure of the circuit's ability to maintain the prescribed output voltage V_o under varying thermal conditions. It is defined in two forms,

$$TC(V_O) = \frac{\Delta V_O}{\Delta T}$$

in which case it is expressed in millivolts or microvolts per degree Celsius, or

$$TC(V_O) (\%) = 100 \frac{\Delta V_O / V_O}{\Delta T}$$

in which case it is expressed in percent per degree Celsius. Replacing 100 by 10^6 gives the TC in parts per million per degree Celsius. Good **voltage references** have TCs on the order of a few parts per million per degree Celsius.

Numerical Problem

EXAMPLE The data sheets of the REF101KM 10-V precision voltage reference give a typical line regulation of 0.001%/V, a typical load regulation of 0.001%/mA, and a maximum TC of 1 ppm/°C. Find the variation in V_O brought about by: (a) a change of V_I from 13.5 V to 35 V; (b) a ±10-mA change in I_O ; (c) a temperature change from 0 °C to 70 °C.

$$(a) \text{ Line regulation (\%)} = 100 \frac{\Delta V_O / V_O}{\Delta V_I} \quad 0.001\%/\text{V} = 100(\Delta V_O / 10) / (35 - 13.5), \text{ or } \Delta V_O = 2.15 \text{ mV}$$

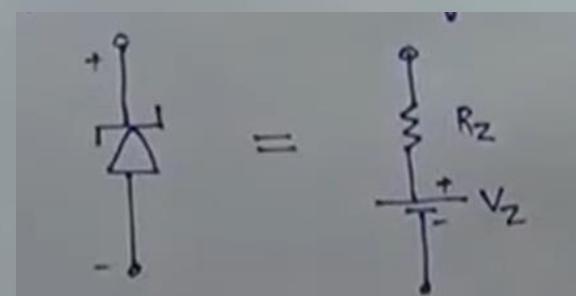
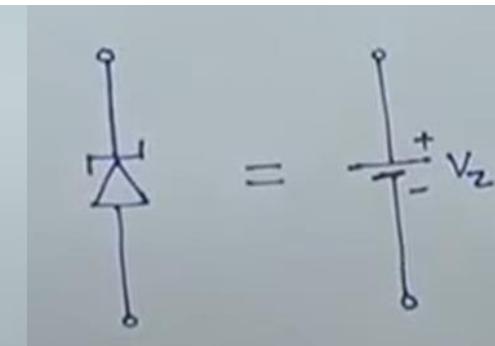
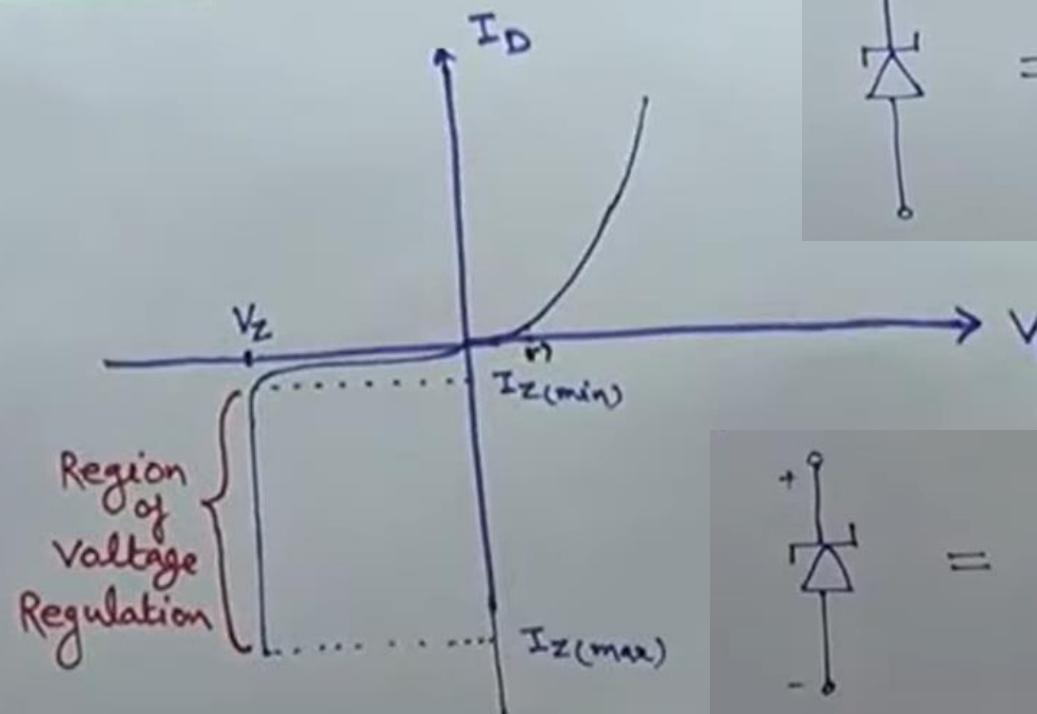
$$(b) \text{ Load regulation (\%)} = 100 \frac{\Delta V_O / V_O}{\Delta I_O} \quad 0.001\%/\text{mA} = 100(\Delta V_O / 10) / (\pm 10 \text{ mA}), \text{ or } \Delta V_O = \pm 1 \text{ mV}$$

$$(c) \text{ TC}(V_O) (\%) = 10^6 \frac{\Delta V_O / V_O}{\Delta T} \quad 1 \text{ ppm/}^\circ\text{C} = 10^6(\Delta V_O / 10) / (70 \text{ }^\circ\text{C}), \text{ or } \Delta V_O = 0.7 \text{ mV maximum.}$$

You will agree that these are rather small variations for a 10-V source!

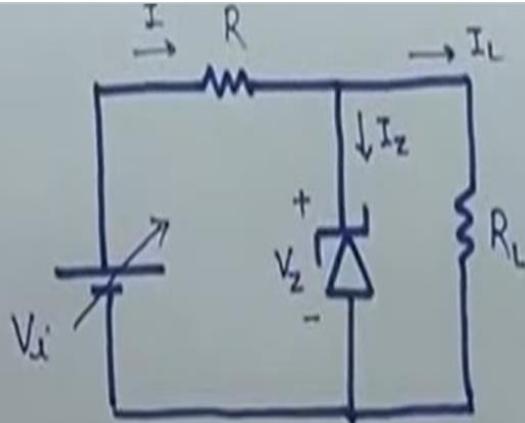
Zener Diode

V-I Characteristic :-



- A voltage regulator circuit keeps the load voltage constant irrespective of changes in input voltage or load resistance.

Zener Diode: Shunt Regulator

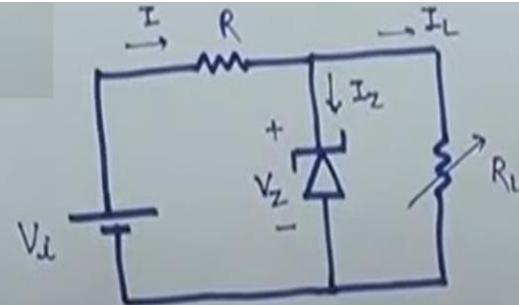


When V_i increasing:

$$V_o = V_z \text{ as long as } I_z < I_{z\max}$$

When V_i Decreasing: $V_o = V_z$ as long as $I_z > I_{z\min}$

$$I_z = I - I_L$$



i) when R_L increases

If $R_L \uparrow$, $I_L \downarrow$

but I remains constant

Since $I_L \downarrow$, $I_z \uparrow$

$$I = I_z + I_L$$

Therefore output voltage $V_o = V_z$ as long as $I_z < I_{z\max}$

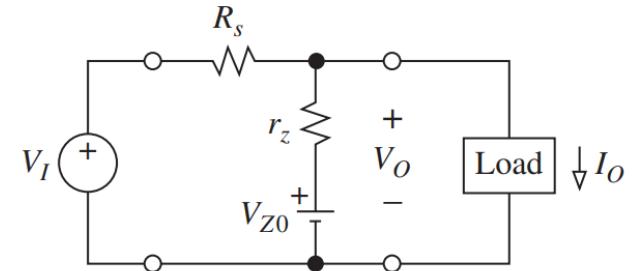
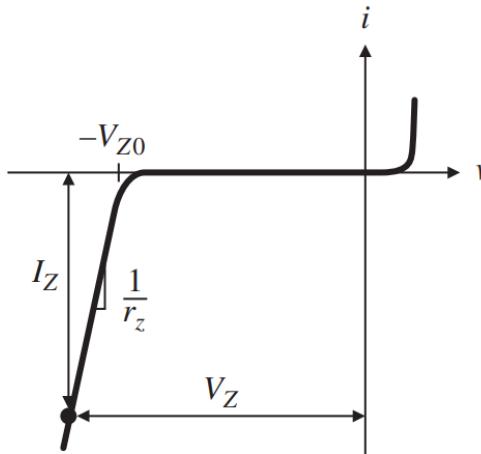
ii) when R_L Decreases

If $R_L \downarrow$, $I_L \uparrow$

Since $I_L \uparrow$, I_z decreases, $V_o = V_z$ as long as $I_z > I_{z\min}$

Zener Diode: Shunt Regulator

$$R_s \leq \frac{V_{I(\min)} - V_{Z0} - r_z I_{Z(\min)}}{I_{Z(\min)} + I_{O(\max)}}$$



$$V_O = \frac{r_z}{R_s + r_z} V_I + \frac{R_s}{R_s + r_z} V_{Z0} - (R_s \parallel r_z) I_O$$

Only the second term on the right-hand side is a desirable one. The other two indicate dependence on line and load as

$$\text{Line regulation} = \frac{r_z}{R_s + r_z}$$

$$\text{Load regulation} = -(R_s \parallel r_z)$$

Multiplying by 100/ V_O gives the regulations in percentage form.

Op-Amp based Shunt Regulator

The modest line and load regulation capabilities of a diode can be improved dramatically with the help of an op amp. The circuit of Fig. uses the artifice of powering the diode from V_O , that is, from the very voltage we are trying to regulate. The result is a far more stable voltage V_Z , which the op amp then amplifies to give

$$V_O = \left(1 + \frac{R_2}{R_1}\right) V_Z$$

This artifice, aptly referred to as *self-regulation*, shifts the burden of line and load regulation from the diode to the op amp. As an additional advantage, V_O is now adjustable, for instance, via R_2 . Moreover, R_3 can now be raised to avoid unnecessary power wastage and self-heating effects.

By inspection, we now have

$$\text{Load regulation} \cong -\frac{z_o}{1 + a\beta}$$

where a and z_o are the open-loop gain and output impedance, and $\beta = R_1/(R_1+R_2)$. To find the line regulation, we observe that because of single-supply operation, a 1-V change in V_I is perceived by the op amp both as a 1-V supply change and as a 0.5-V input common-mode change. This results in a worst-case input offset voltage change $\Delta V_{OS} = \Delta V_I(1/\text{PSRR} + 1/2\text{CMRR})$ appearing in series with V_Z . The op amp then gives $\Delta V_O = (1 + R_2/R_1)\Delta V_{OS}$, so

$$\text{Line regulation} = \left(1 + \frac{R_2}{R_1}\right) \times \left(\frac{1}{\text{PSRR}} + \frac{0.5}{\text{CMRR}}\right)$$

We observe that since z_o , a , PSRR, and CMRR are frequency-dependent, so are the line and load regulation. In general, both parameters tend to degrade with frequency.

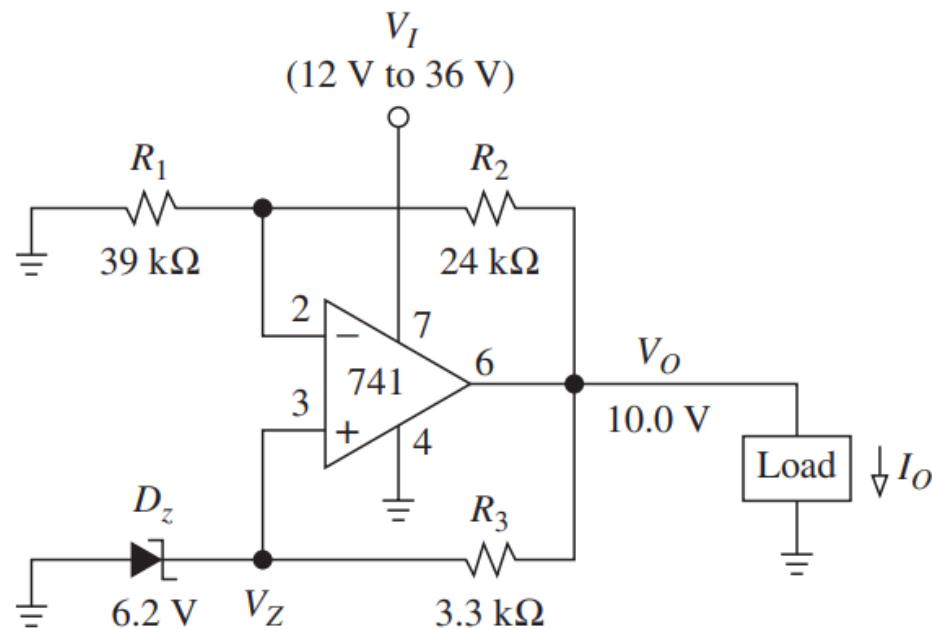
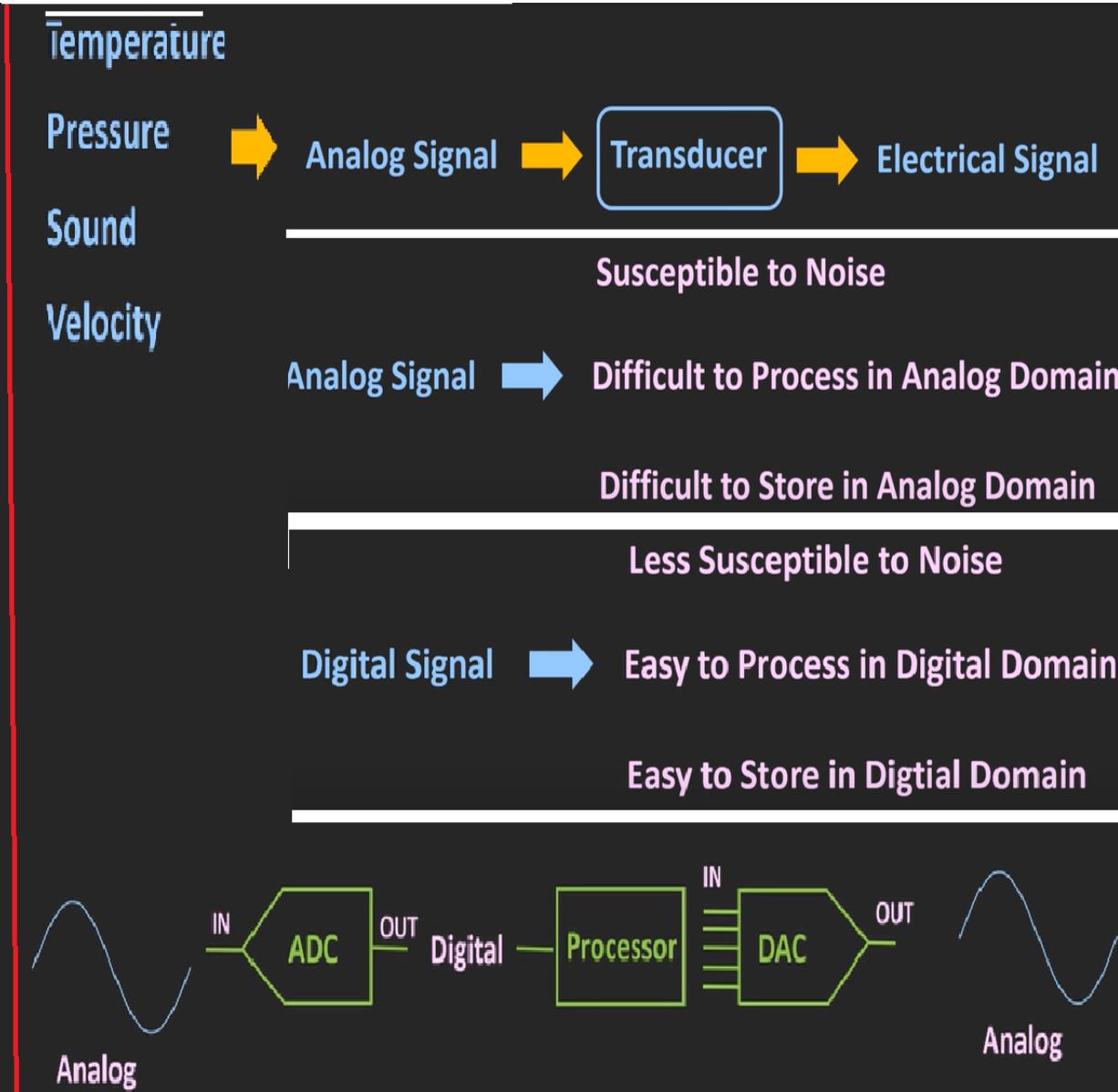
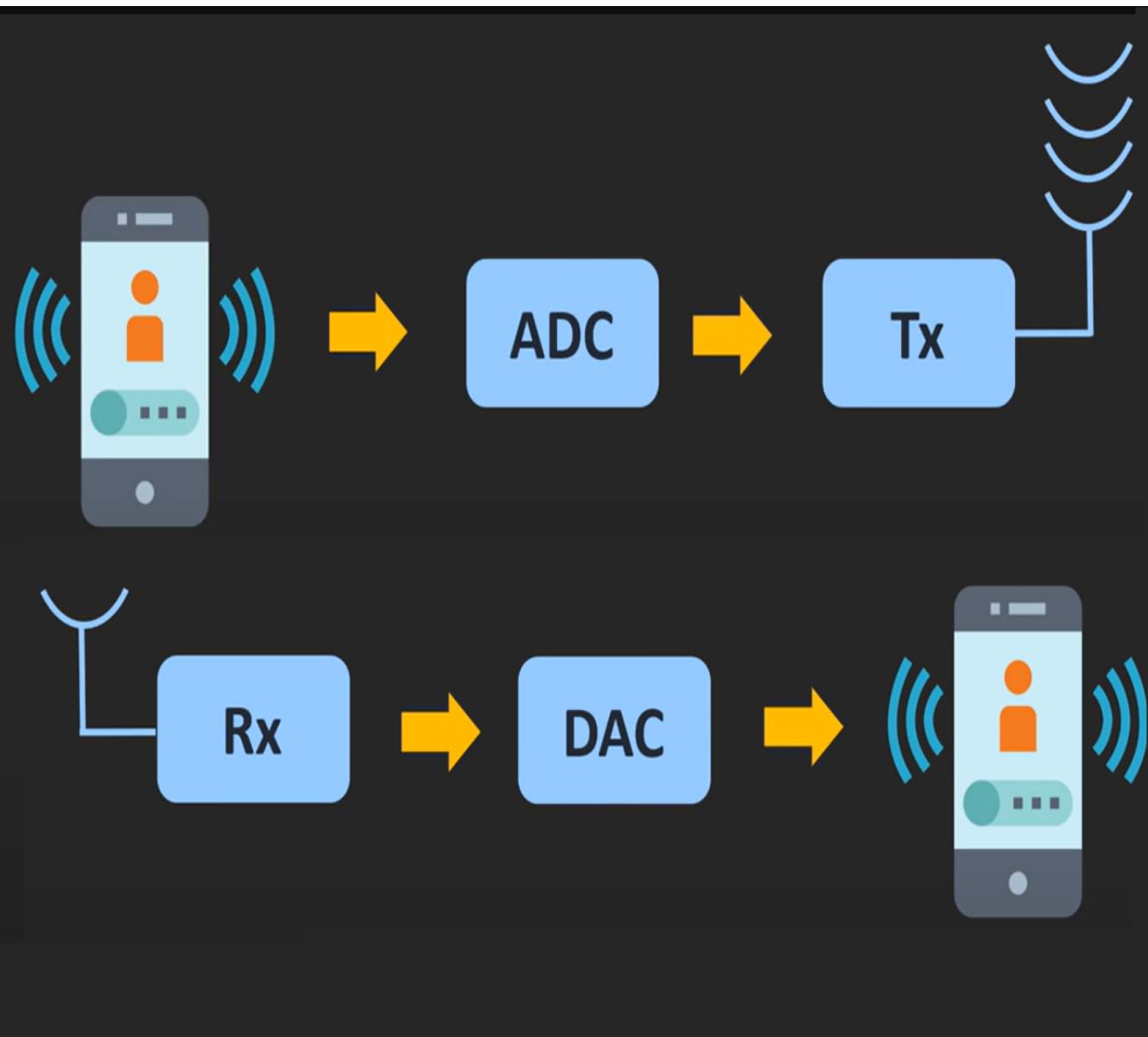


FIGURE
Self-regulated 10-V reference

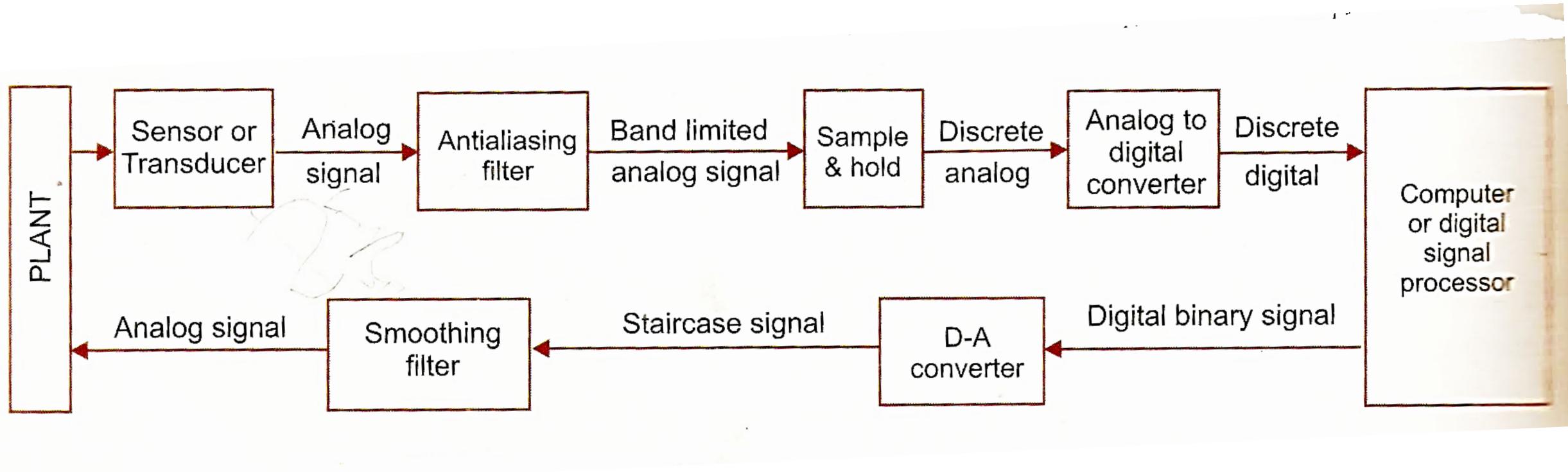
LIC: LECTURE D/A AND A/D CONVERTERS

- Introduction
- Digital to Analog Converters-DAC
 - ❖ 1. R-2R ladder Type DAC
 - ❖ 2. Weighted Resistor Type DAC

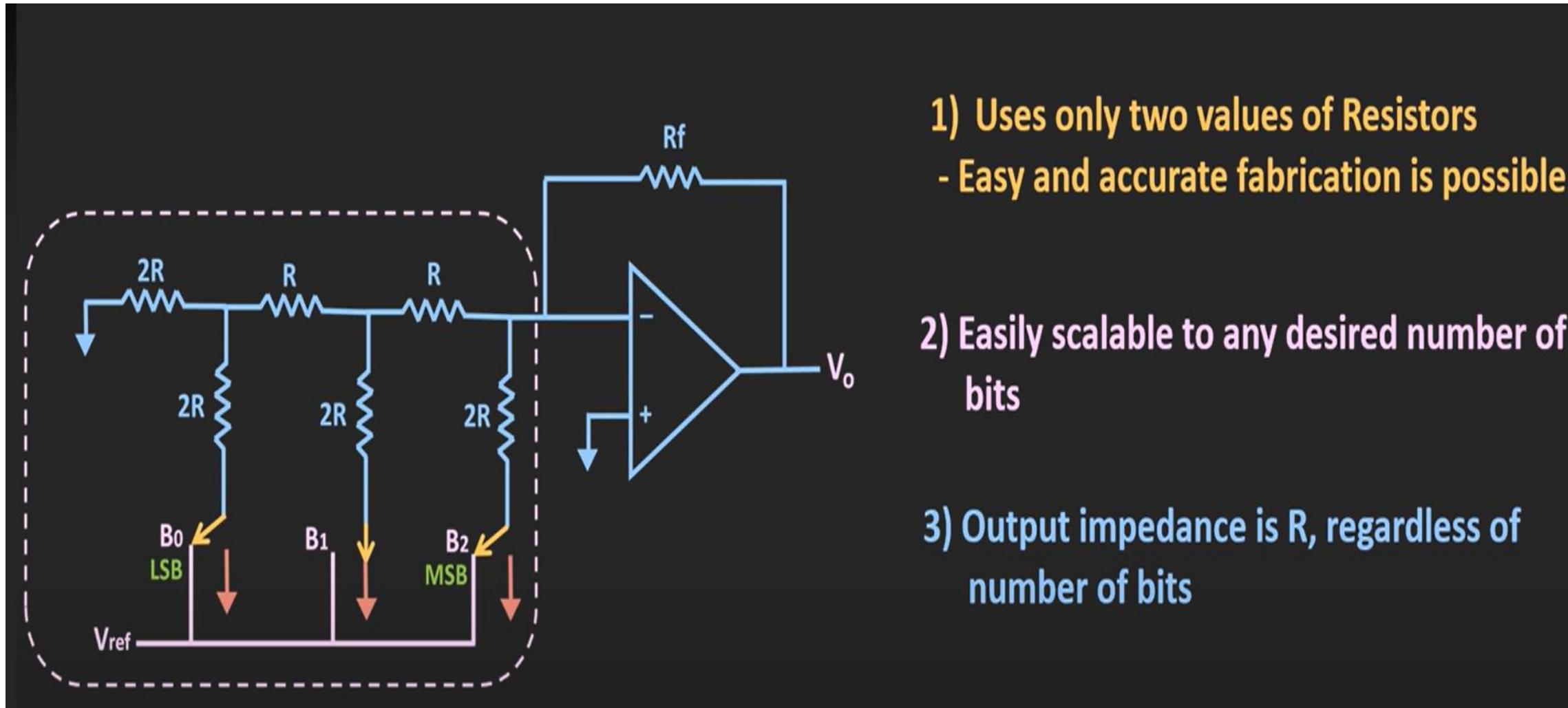
D/A AND A/D CONVERTERS: NEED



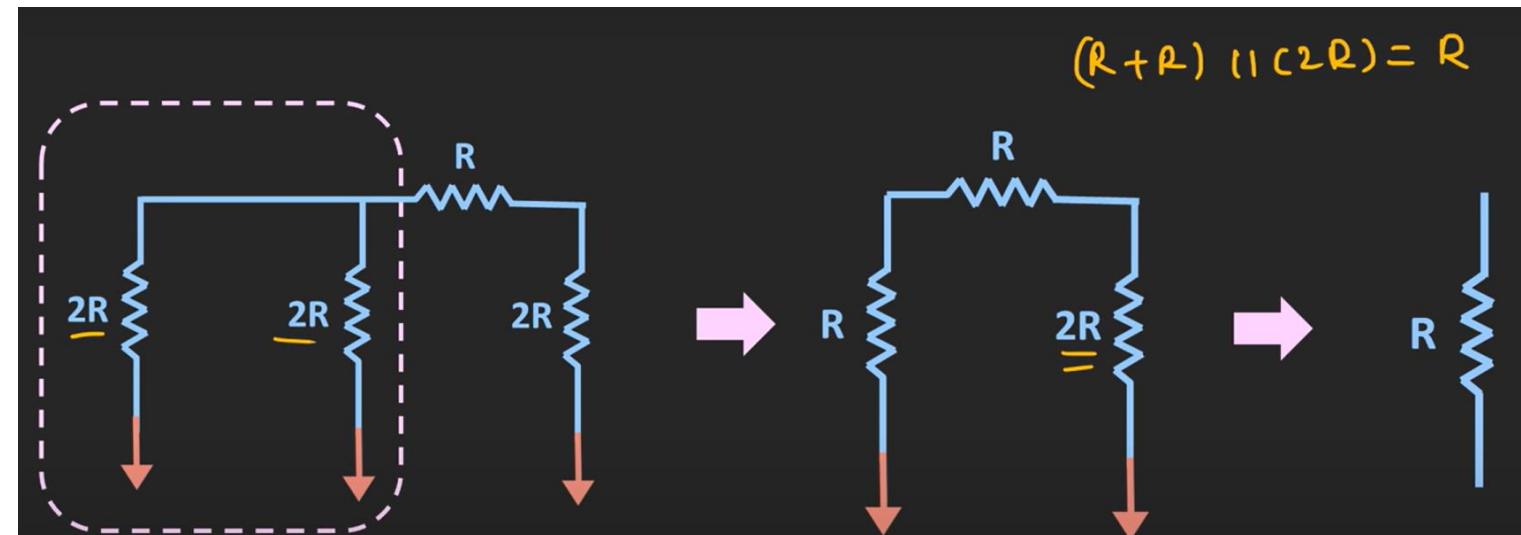
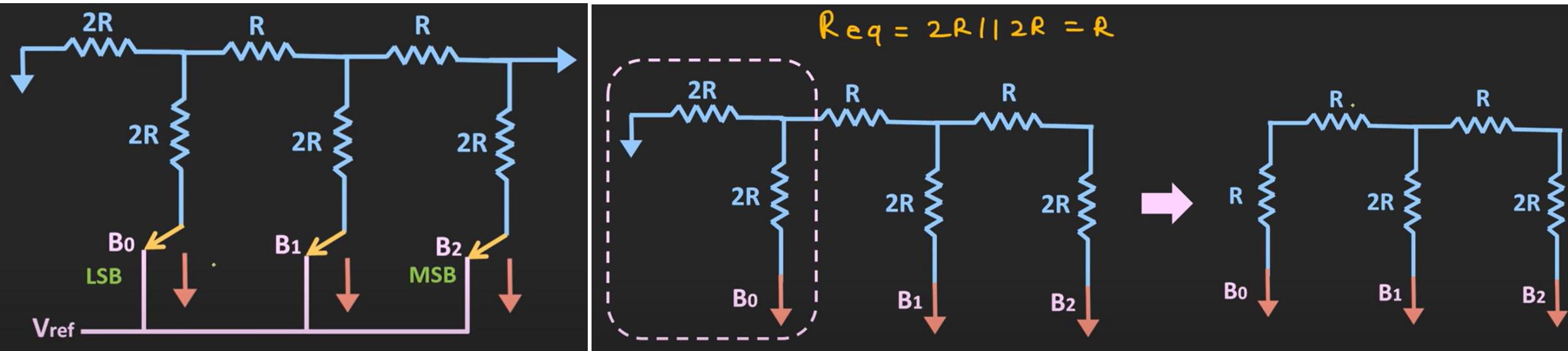
INTERFACING A DIGITAL COMPUTER TO THE ANALOG WORLD



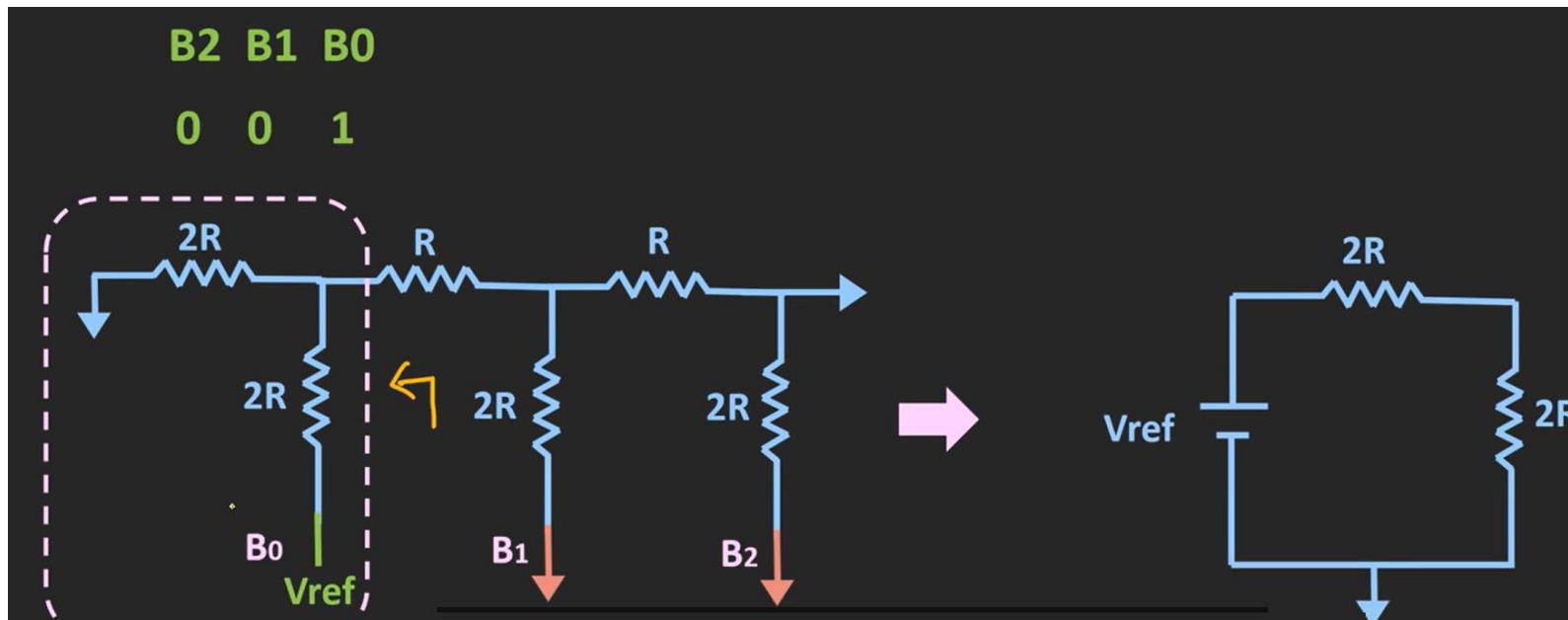
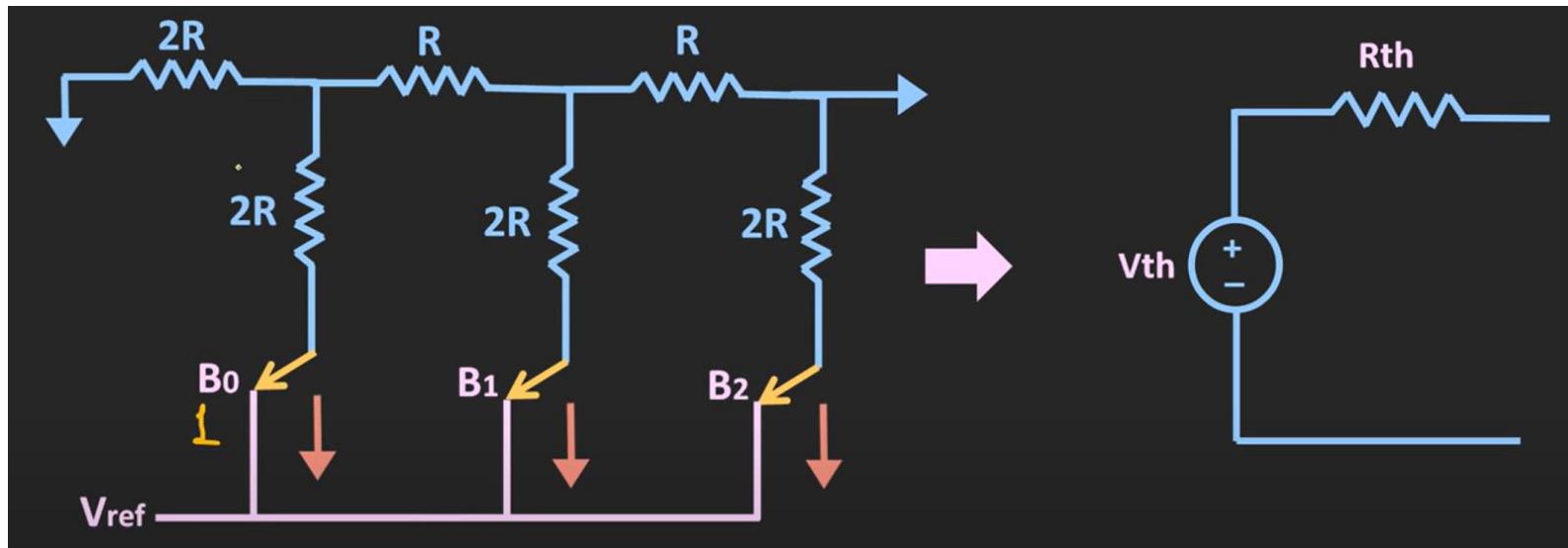
R-2R ladder Type DAC



OUTPUT IMPEDANCE OF R-2R LADDER TYPE DAC



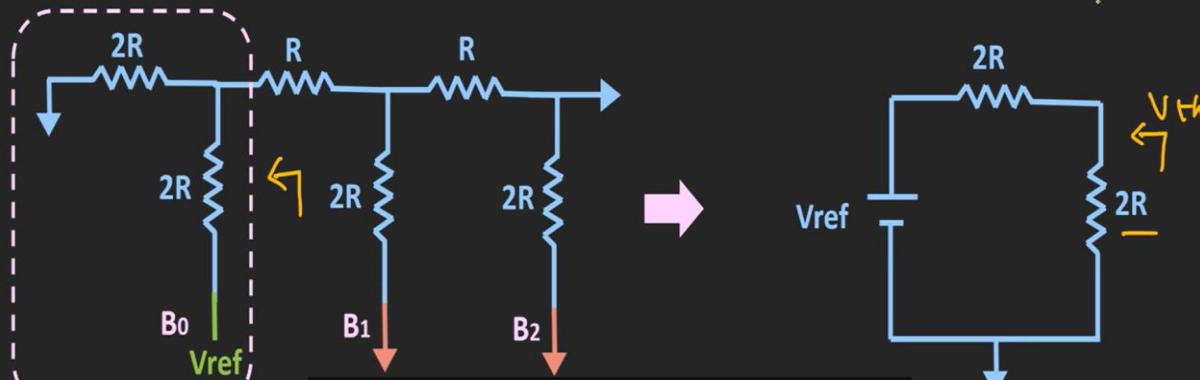
Equivalent Circuit of R-2R LADDER TYPE DAC



Thevenin's Equivalent if Binary Input is 001

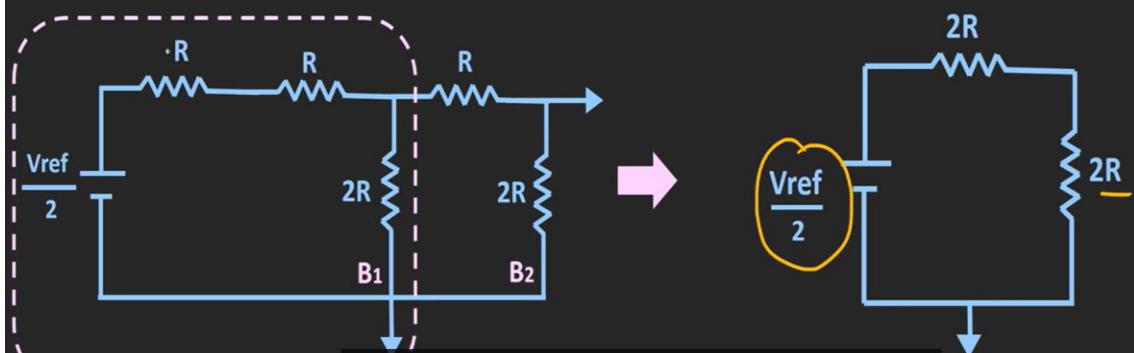
B2 B1 B0
0 0 1

$$V_{th} = \frac{2R \times V_{ref}}{2R + 2R} = \frac{V_{ref}}{2}$$
$$R_{th} = 2R \parallel 2R = R$$



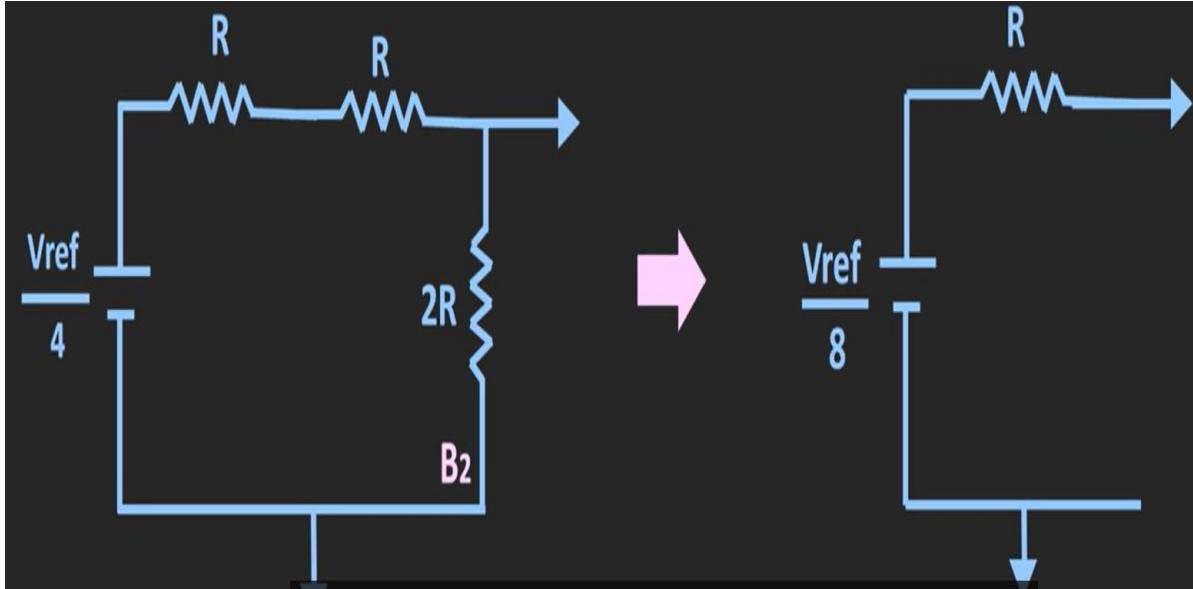
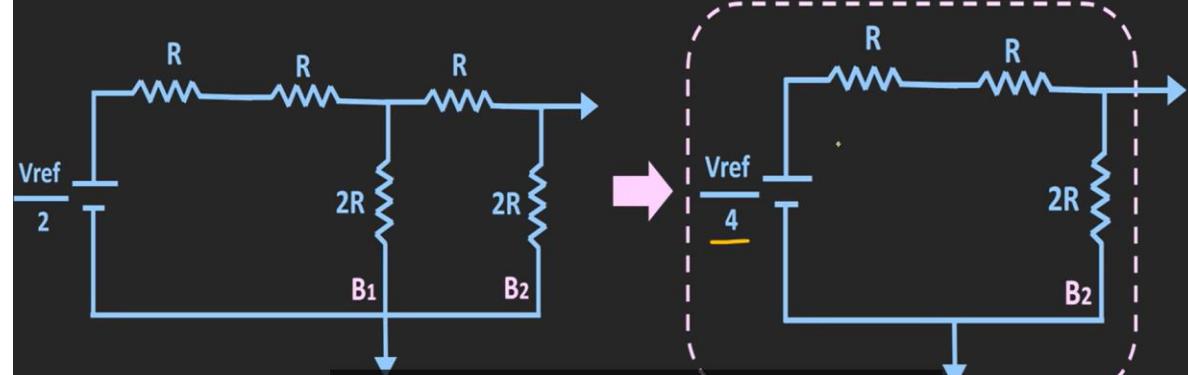
B2 B1 B0
0 0 1

$$V_{th} = \frac{2R \times (V_{ref}/2)}{2R + 2R} = \frac{V_{ref}}{4}$$
$$R_{th} = 2R \parallel 2R = R$$



B2 B1 B0
0 0 1

$$V_{th} = \frac{2R \times (V_{ref}/4)}{2R + 2R} = \frac{V_{ref}}{8}$$
$$R_{th} = 2R \parallel 2R = R$$



Output Voltage

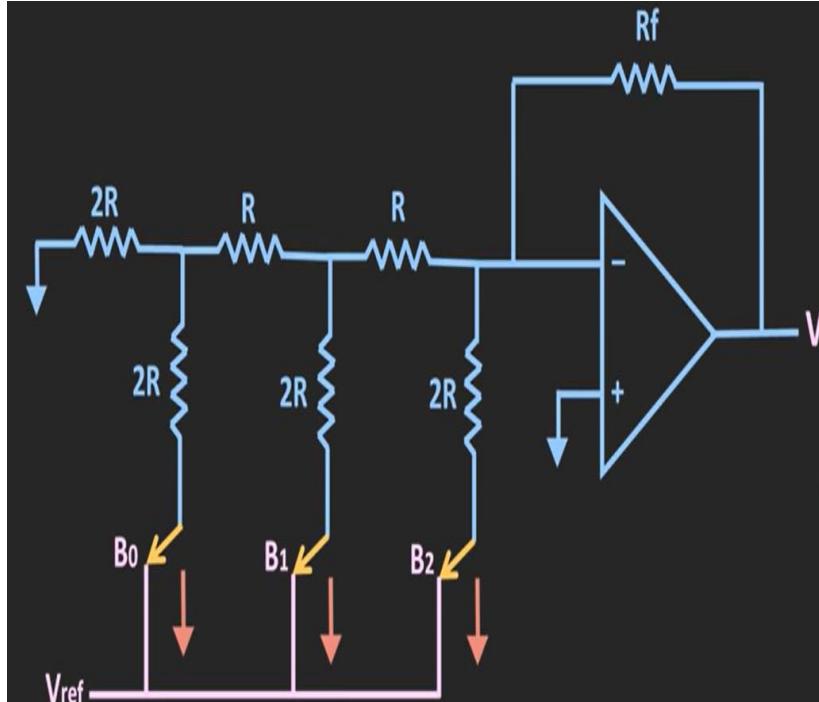
B2 B1 B0

$$1 \ 0 \ 0 \rightarrow \frac{V_{ref}}{2}$$

$$0 \ 1 \ 0 \rightarrow \frac{V_{ref}}{4}$$

$$0 \ 0 \ 1 \rightarrow \frac{V_{ref}}{8}$$

$$1 \ 1 \ 1 \rightarrow \frac{V_{ref}}{8} + \frac{V_{ref}}{4} + \frac{V_{ref}}{2} \rightarrow \frac{7 V_{ref}}{8}$$

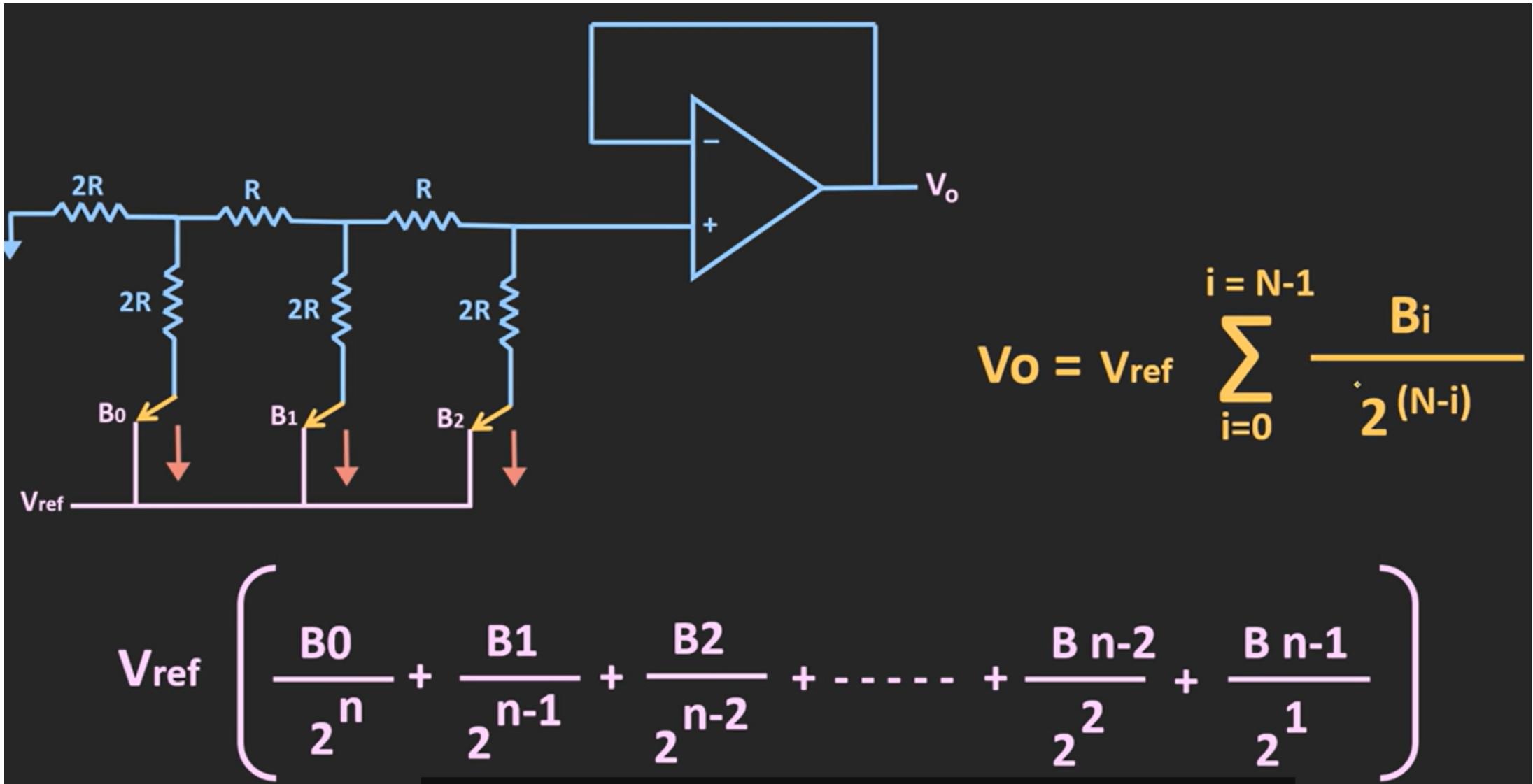


$$V_o = \left(-\frac{V_{ref} \times R_f}{R} \right) \sum_{i=0}^{i=N-1} \frac{B_i}{2^{(N-i)}}$$

$$V_{R-2R} = V_{ref} \left(\frac{B_0}{2^n} + \frac{B_1}{2^{n-1}} + \frac{B_2}{2^{n-2}} + \dots + \frac{B_{n-2}}{2^2} + \frac{B_{n-1}}{2^1} \right)$$

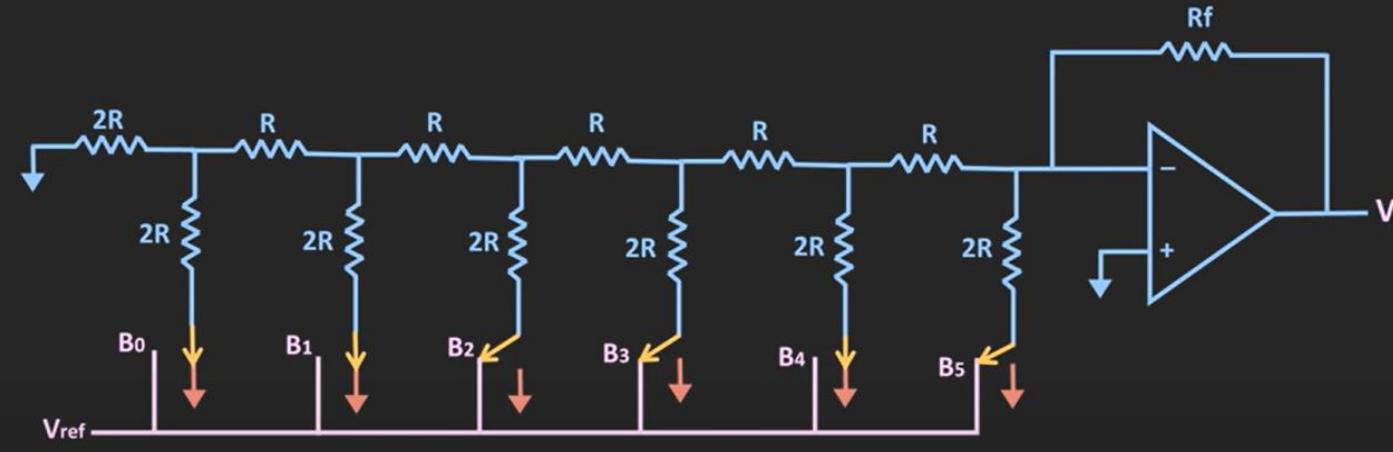
$$V_{ref} \left(\frac{-R_f}{R} \right) \left(\frac{B_0}{2^n} + \frac{B_1}{2^{n-1}} + \frac{B_2}{2^{n-2}} + \dots + \frac{B_{n-2}}{2^2} + \frac{B_{n-1}}{2^1} \right)$$

Unity Gain: R-2R ladder Type DAC



Problem-1

For the given DAC find the full scale output voltage if $R_f = 2 \text{ k}\Omega$ and $R = 1 \text{ k}\Omega$.
Also find the output voltage when the input is 101100. Assume $V_{ref} = 5\text{V}$



$$\begin{aligned} FSO &= 5\text{V} \left(\frac{-2}{1} \right) \left(\frac{1}{2^6} + \frac{1}{2^5} + \frac{1}{2^4} + \frac{1}{2^3} + \frac{1}{2^2} + \frac{1}{2^1} \right) \\ &= -10 \times \frac{63}{64} \\ &= -9.84375\text{V} \end{aligned}$$

$$V_o = \left[-\frac{V_{ref} \times R_f}{R} \right] \sum_{i=0}^{N-1} \frac{B_i}{2^{(N-i)}} = -5 \times \left(\frac{2}{1} \right) \times \left[\frac{1}{2^1} + \frac{1}{2^3} + \frac{1}{2^4} \right]$$

Problem-2

- What are the output voltage caused by logic 1 in each bit position in an R-2R ladder with input 11110001 if the input level for 0V and that for 1 is 10V.

$$\text{The voltage level caused by the } D_n \text{ bit} = \frac{E}{2^{n-n}}.$$

$$\begin{aligned}\text{The voltage level caused by } D_7 \text{ bit (MSB)} &= \frac{E}{2^{8-7}} = \frac{E}{2^1} \\ &= \frac{10}{2} = \underline{\underline{5V}}.\end{aligned}$$

$$D_6 \text{ bit} = \frac{E}{2^{8-6}} = \frac{10}{4} = \underline{\underline{2.5V}}.$$

$$D_5 \text{ bit} = \frac{10}{2^{8-5}} = \frac{10}{8} = \underline{\underline{1.25V}}.$$

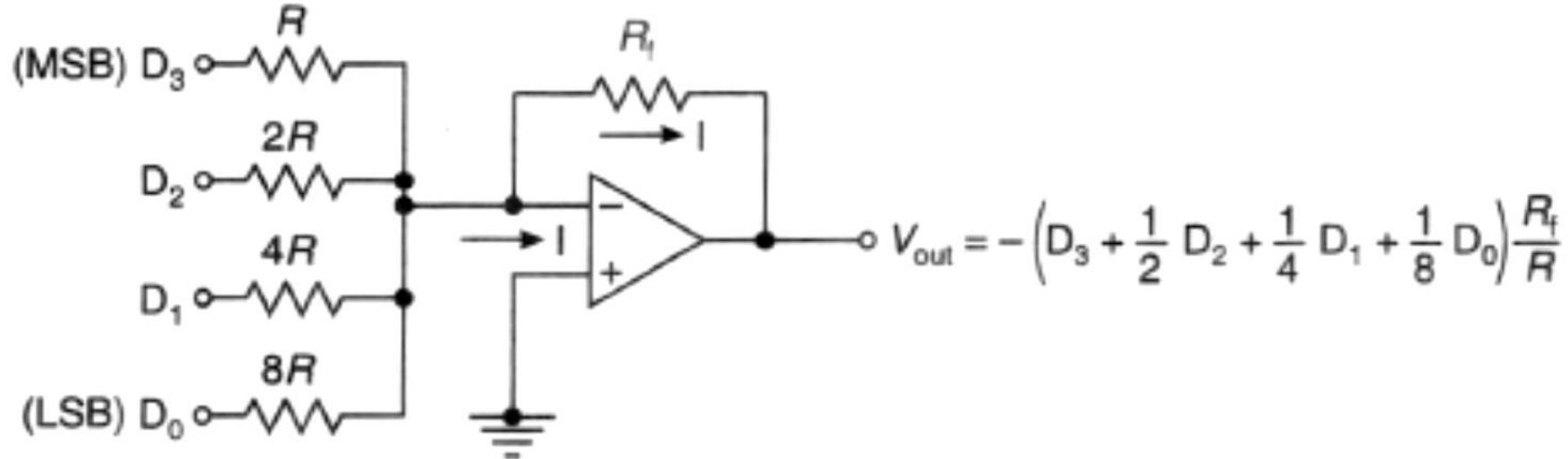
$$D_4 \text{ bit} = \frac{10}{2^{8-4}} = \frac{10}{16} = \underline{\underline{0.625V}}$$

$$D_0 \text{ bit} = \frac{10}{2^{8-0}} = \frac{10}{2^8} = \underline{\underline{0.03906V}}$$

LIC: LECTURE D/A AND A/D CONVERTERS

- Digital to Analog Converters-DAC
 - ✓ 1. R-2R ladder Type DAC
 - ❖ 2. Weighted Resistor Type DAC
- Analog to Digital Converters-DAC
 - ✓ Counter Type ADC

WEIGHTED RESISTOR TYPE DAC



See the derivation as per class notes

Q) For the 4 bit weighted resistor DAC, determine (a) the weight of each input bit if the inputs are 0V and 5V, (b) the full scale output, if $R_F = R = 1\text{k}\Omega$. Also, find the full scale output if R_F is changed to 500Ω .

Ans :-

(a) MSB \rightarrow Gain = 1 \rightarrow Weight = 5V

$D_2 \rightarrow$ Gain = $1/2 \rightarrow$ Weight = $5/2 = 2.5\text{V}$

$D_1 \rightarrow$ Gain = $1/4 \rightarrow$ Weight = $5/4 = 1.25\text{V}$

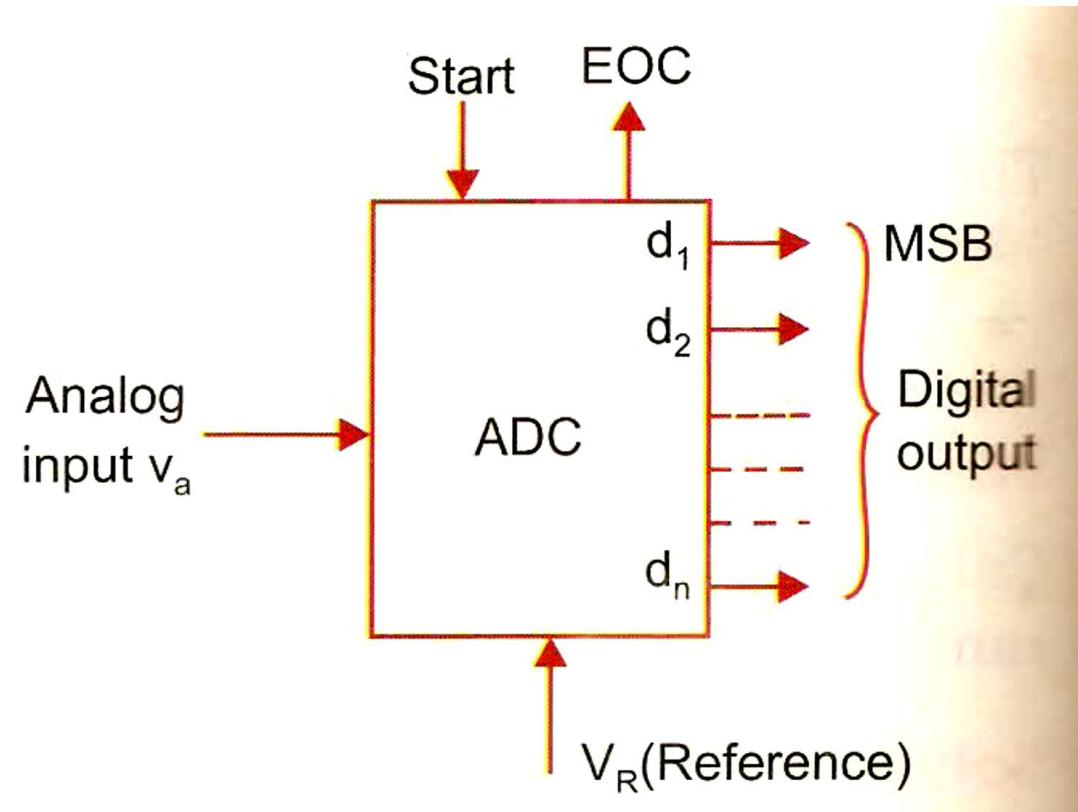
$D_0 \rightarrow$ Gain = $1/8 \rightarrow$ Weight = $5/8 = 0.625\text{V}$

(b) Full scale output,

$$V_{\text{out}} = - \left(1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} \right) \times 5 = -9.375\text{V}$$

(c) For $R_F = 500\Omega$, $V_{\text{out}} = -4.6875\text{V}$

SCHEMATIC OF ADC



CLASSIFICATION BASED ON THEIR CONVERSION TECHNIQUE

1) Direct type ADC

❑ Compare a given analog signal with the internally generated equivalent signal.

❑ Includes :-

- ✓ Flash (comparator) type converter
- ✓ Counter type converter
- ✓ Tracking or servo converter
- ✓ Successive approximation type converter

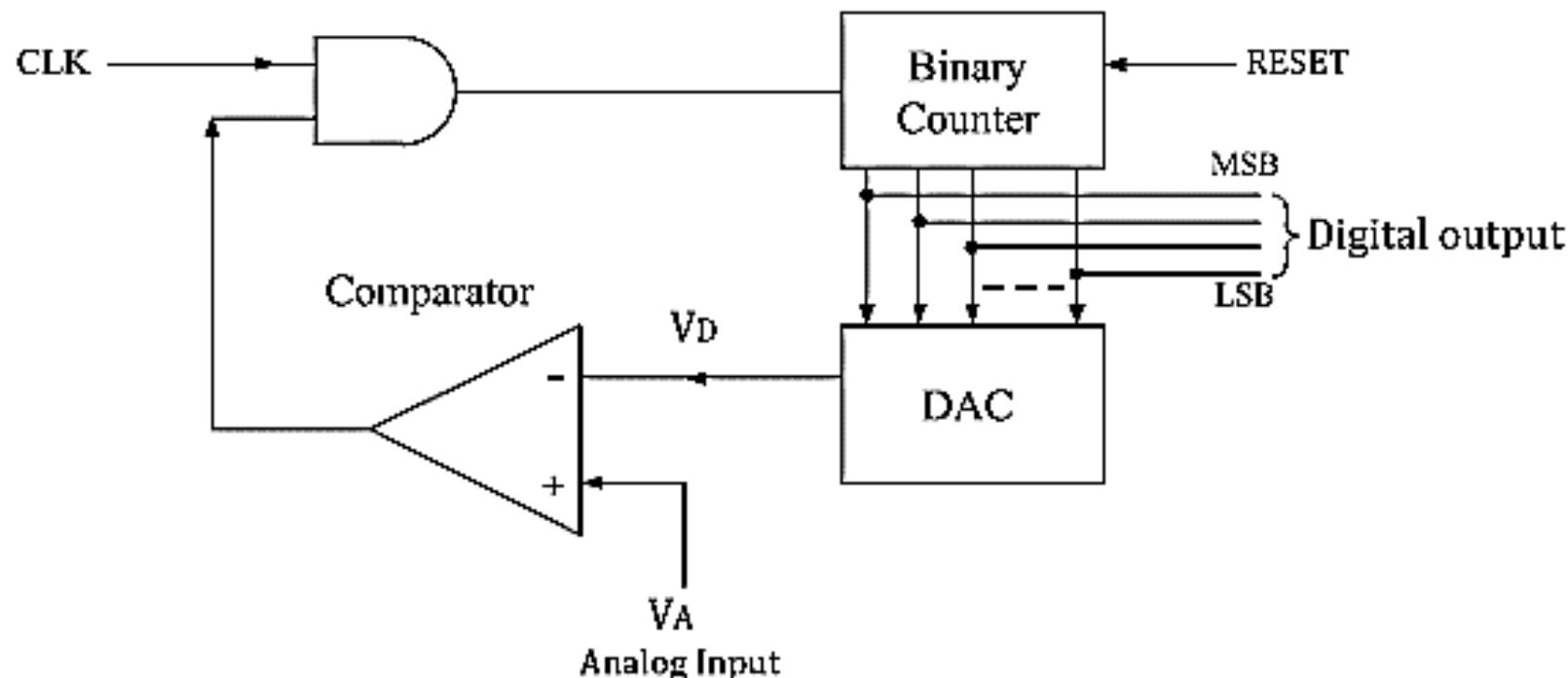
Faster but less accurate than
integrating type

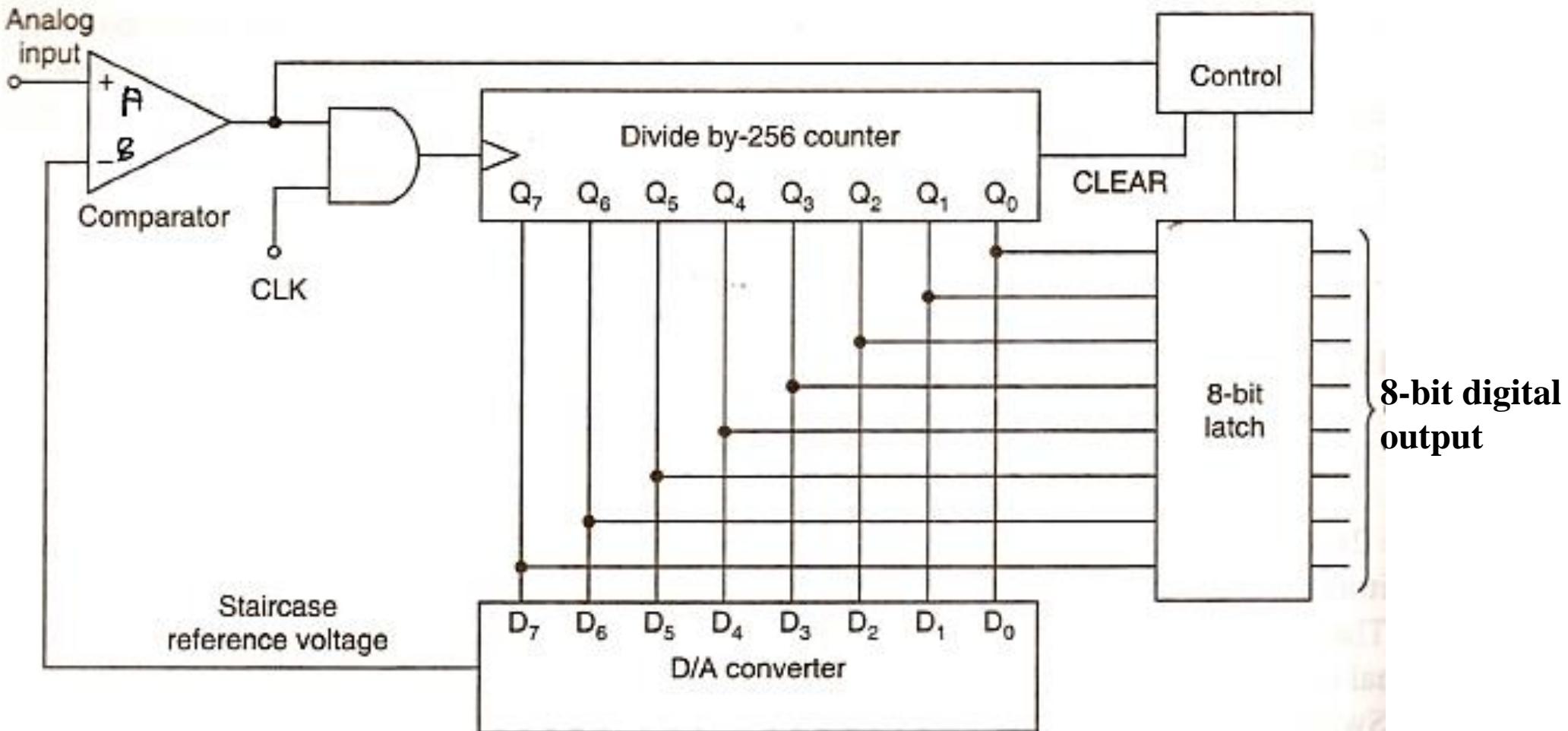
2) Integrating type ADC

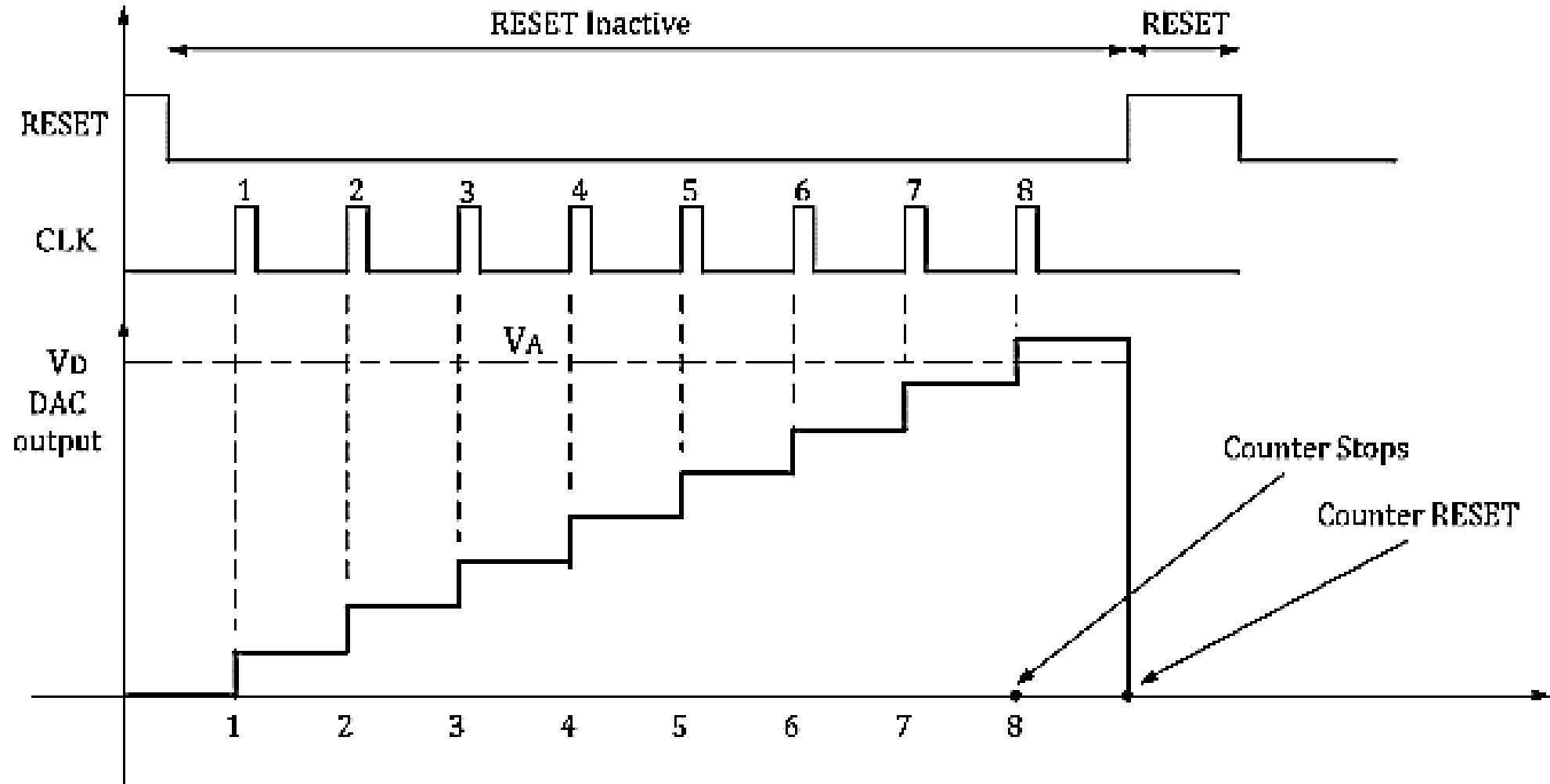
❑ Performs conversion in an indirect manner by 1st changing the analog input signal to a linear function of time or freq. and then to a digital code.

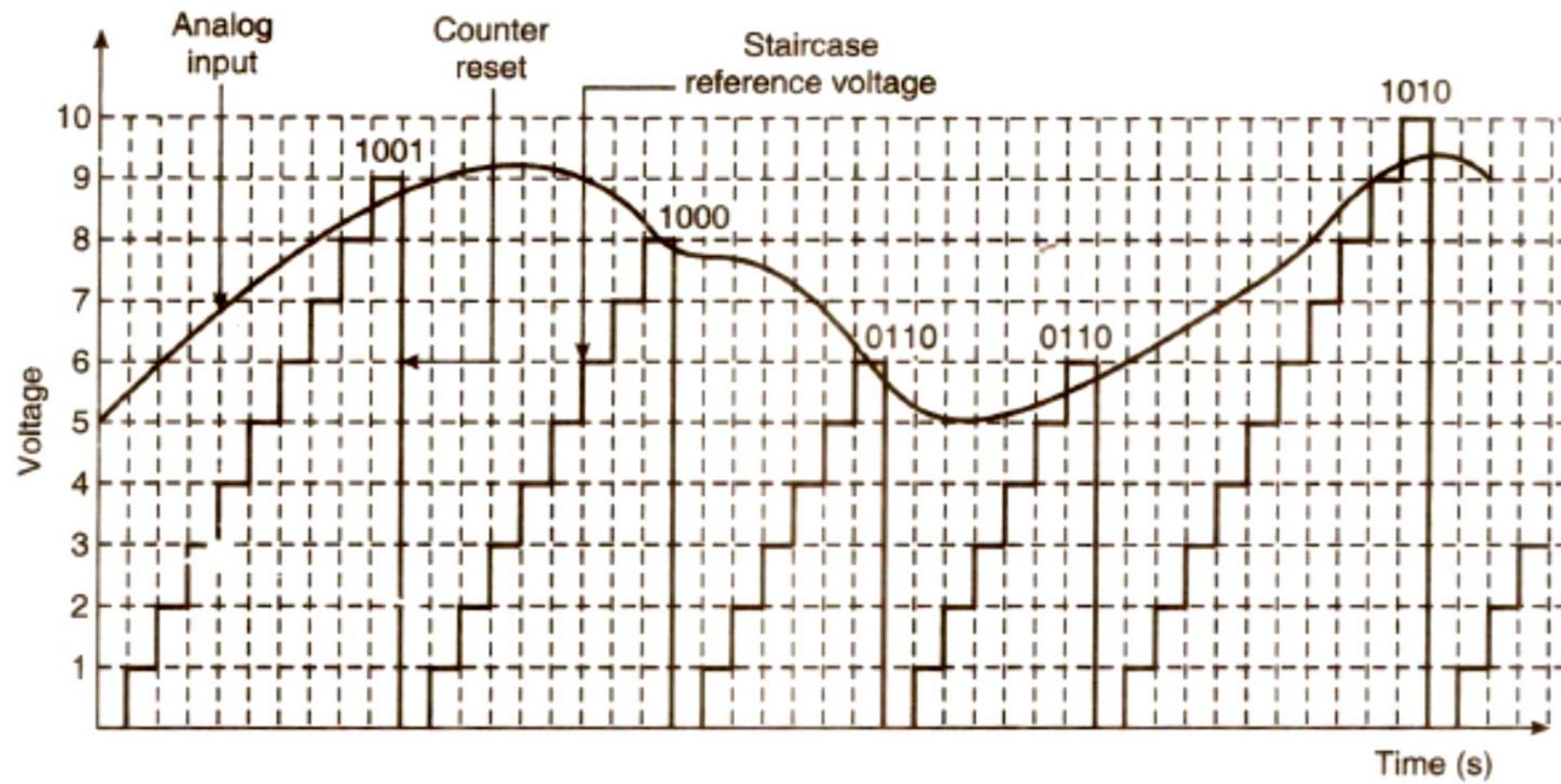
- ✓ Charge balancing ADC
- ✓ Dual slope ADC

COUNTER TYPE ADC







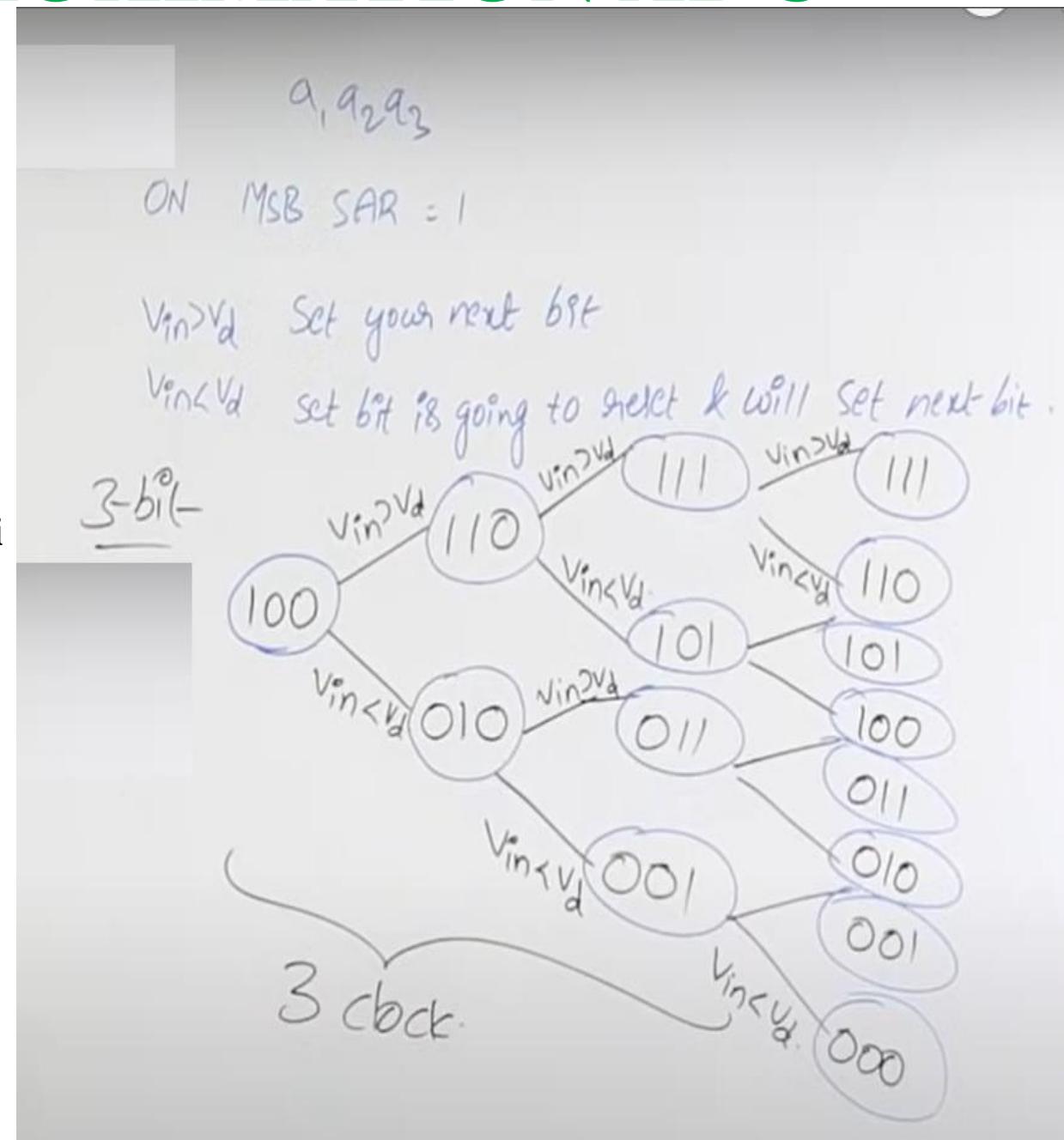
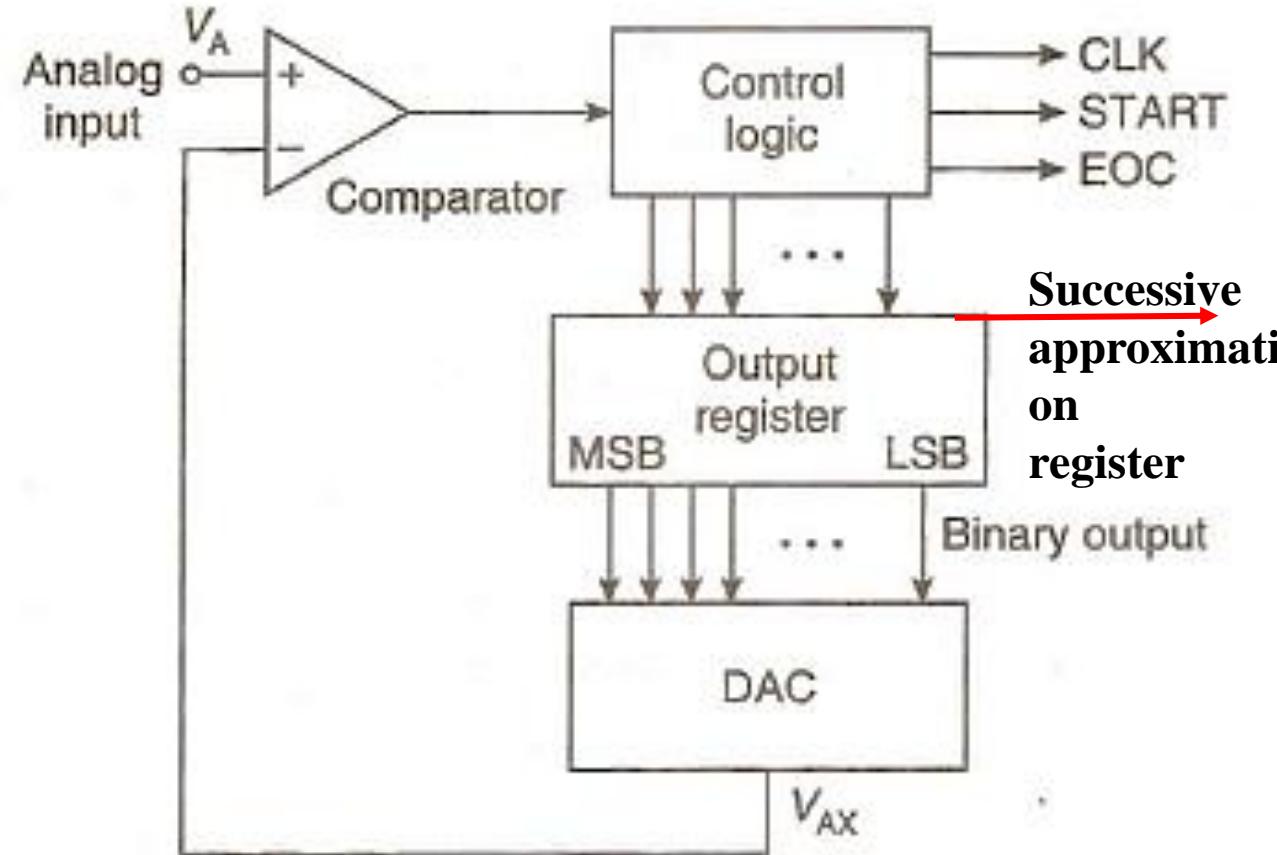


LIC: LECTURE

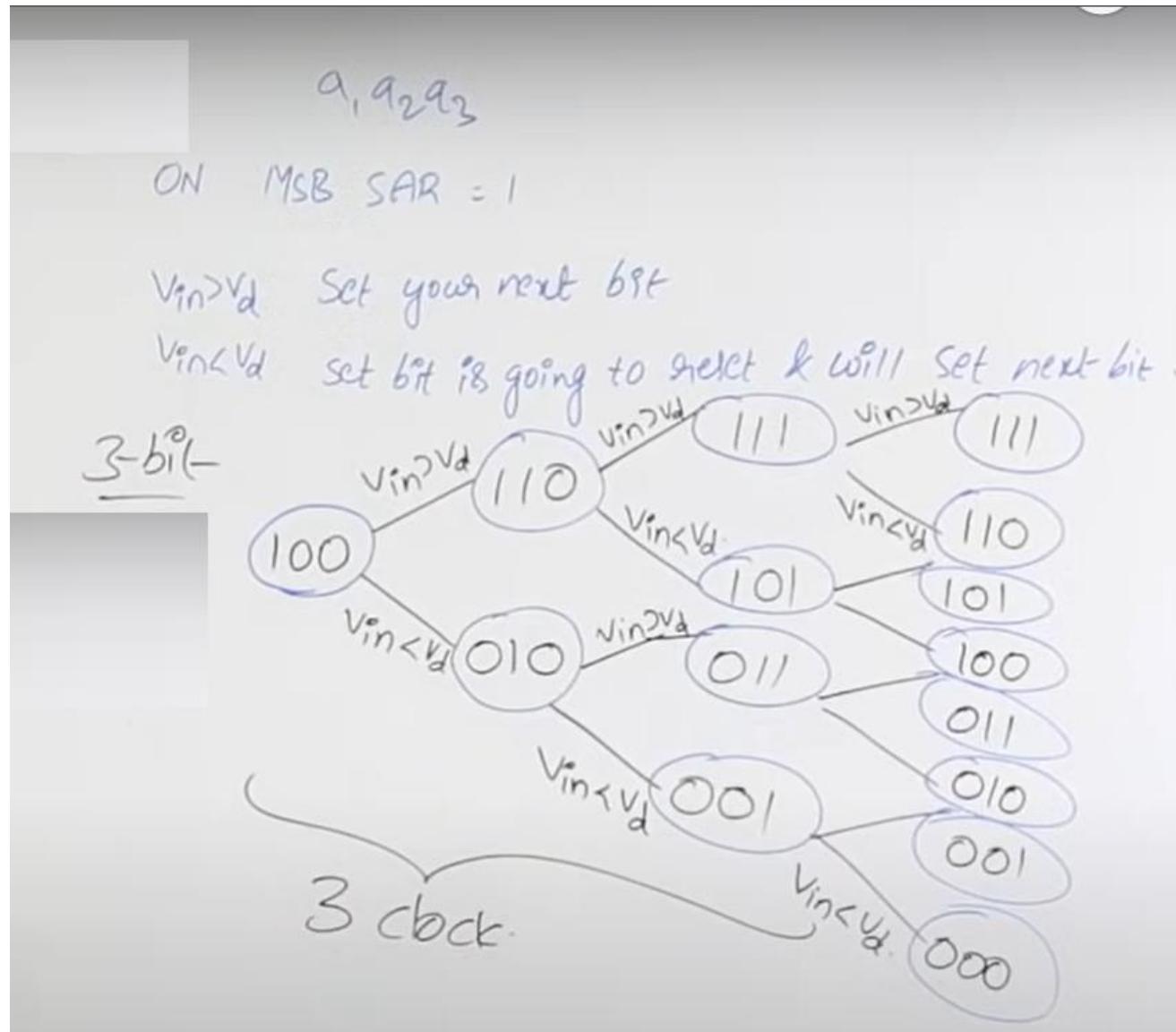
D/A AND A/D CONVERTERS

- Analog to Digital Converters-DAC
 - ✓ Counter Type ADC
 - Successive Approximation (SAR) Type ADC
 - DUAL Slope Type ADC

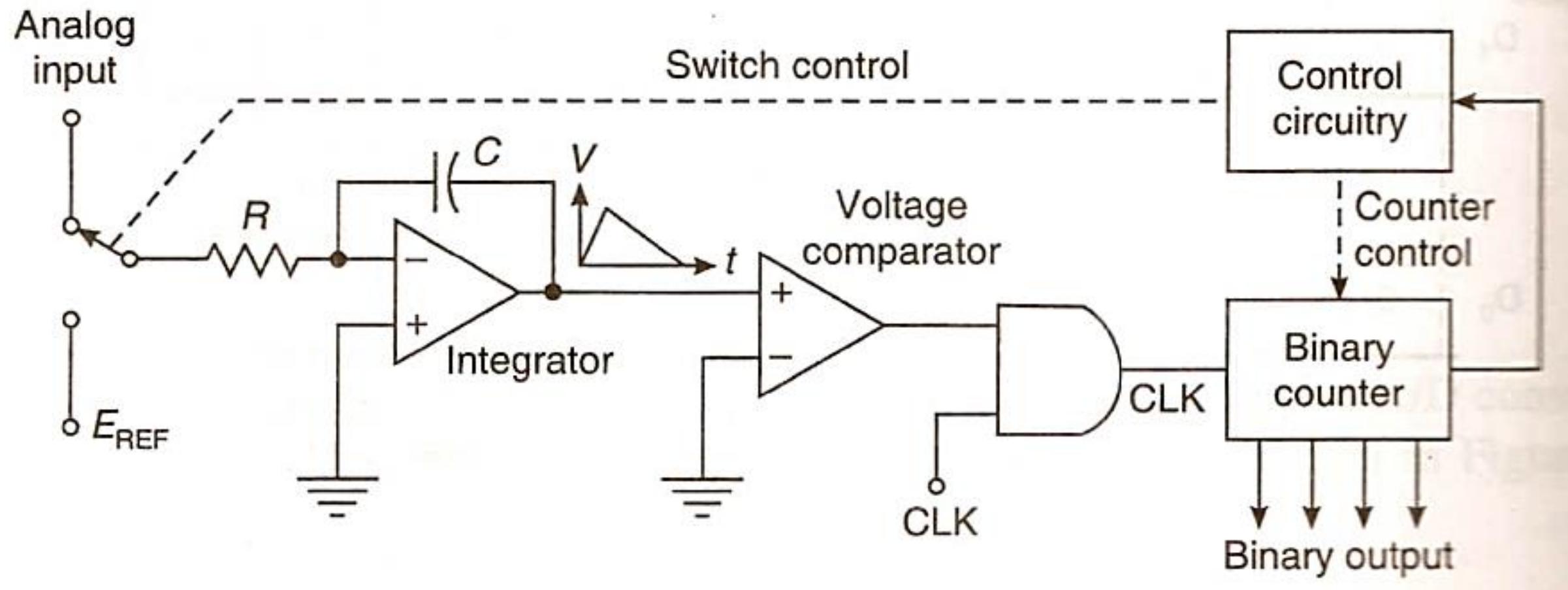
SUCCESSIVE APPROXIMATION ADC



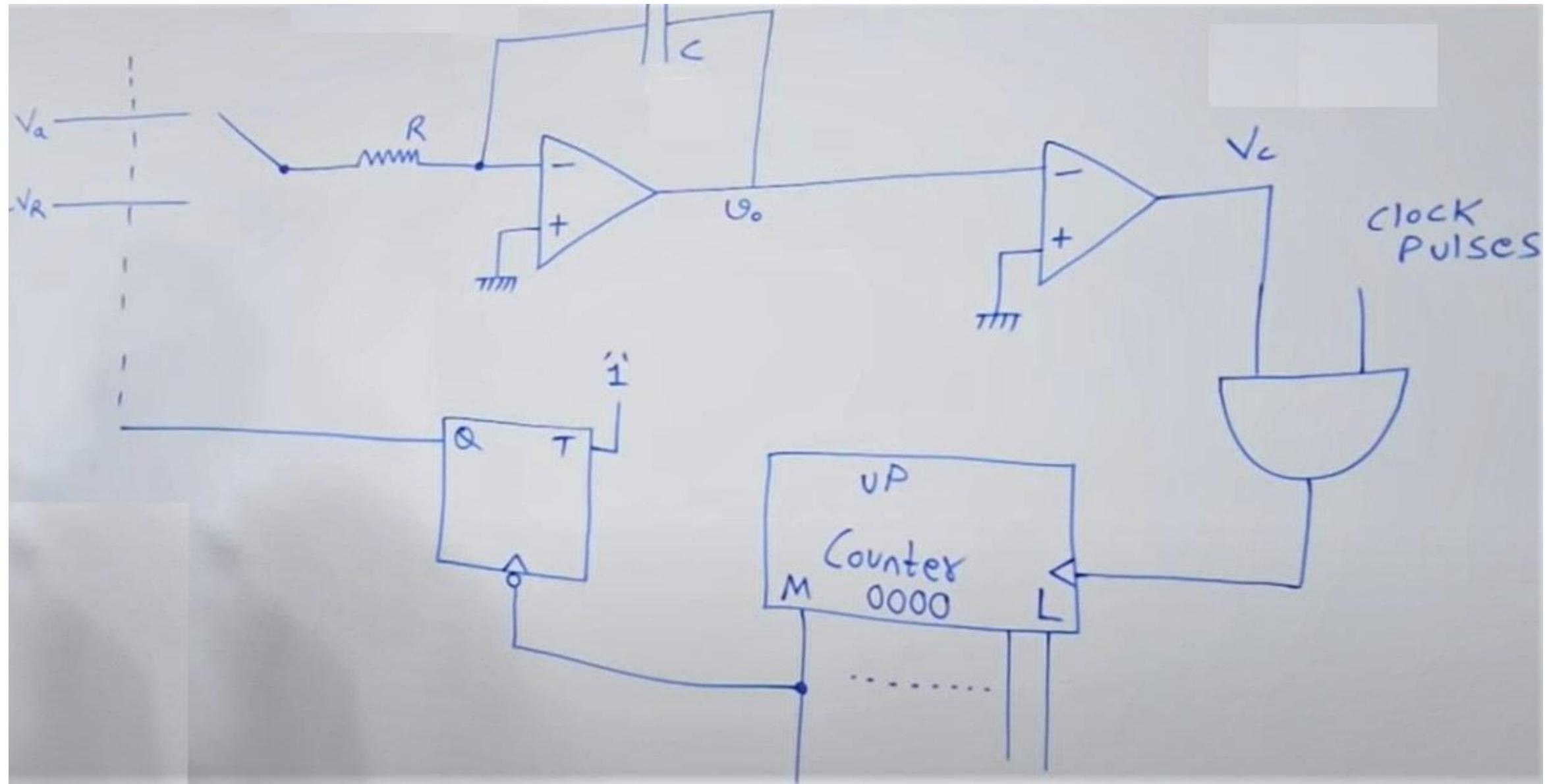
SUCCESSIVE APPROXIMATION ADC



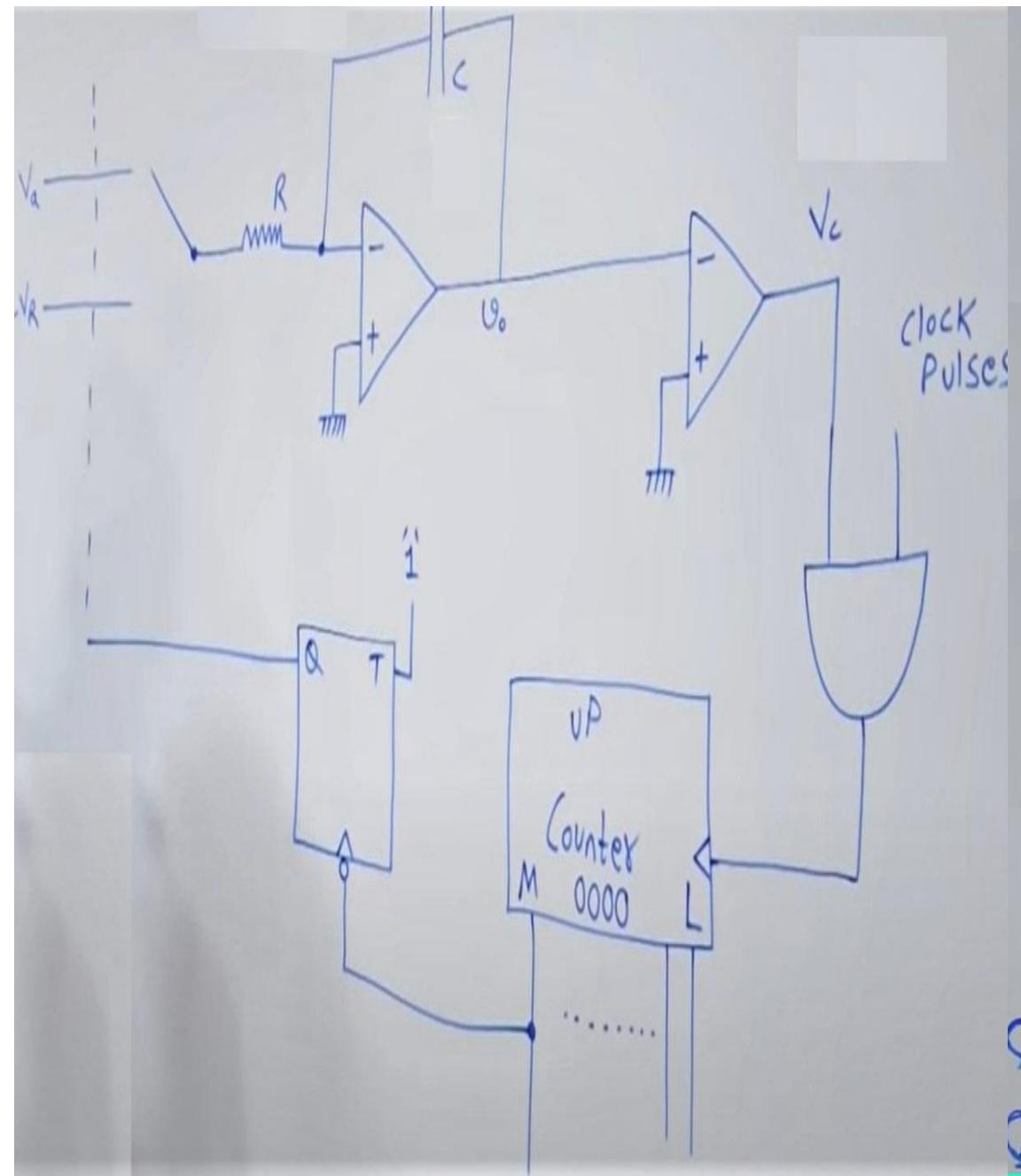
DUAL SLOPE ADC



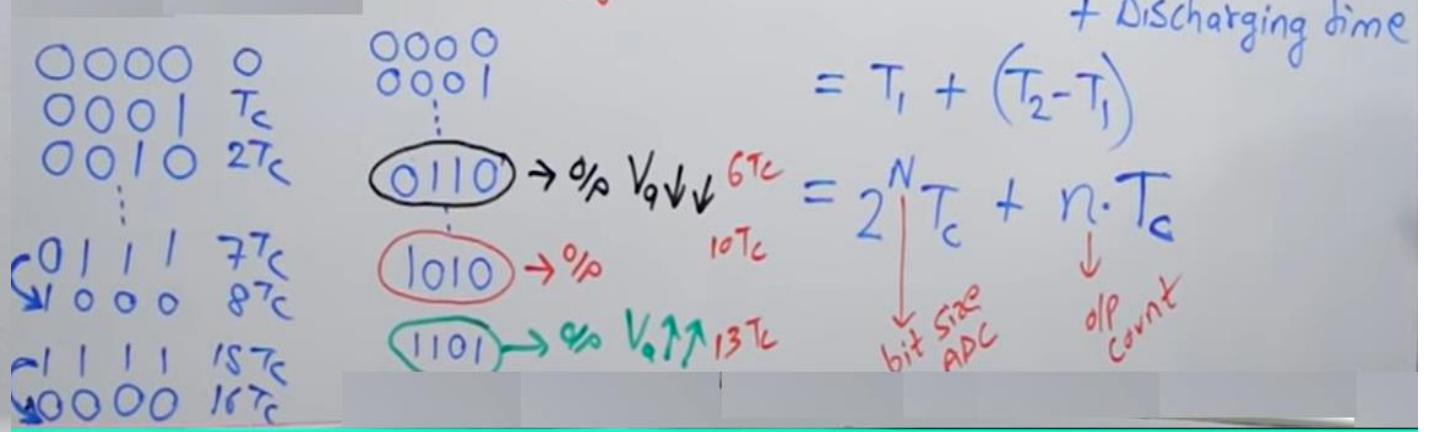
DUAL SLOPE ADC



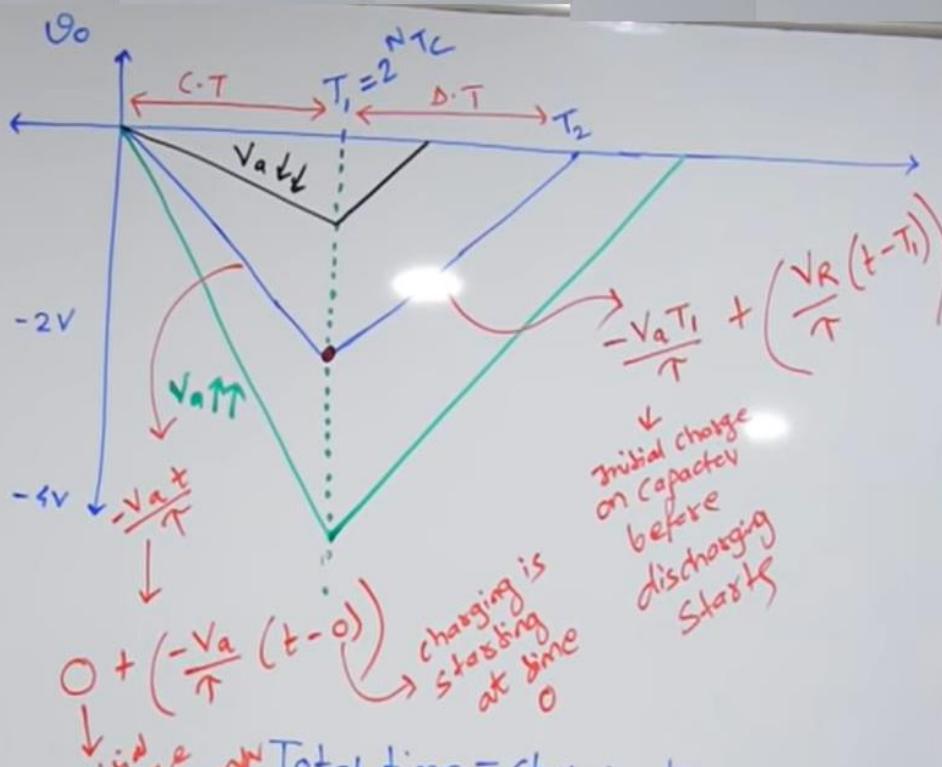
DUAL SLOPE ADC



0000	0
0001	T_C
0010	$2T_C$
.....
0111	$7T_C$
1000	$8T_C$
1111	$15T_C$
0000	$16T_C$



DUAL SLOPE ADC



0000	0
0001	T_C
0010	$2T_C$
⋮	⋮
0111	$7T_C$
1000	$8T_C$
1111	$15T_C$
00000	$16T_C$

0000
0001
⋮
0110

$$= T_1 + (T_2 - T_1)$$

$$\begin{aligned} 0110 &\rightarrow \% V_a \downarrow \downarrow 6T_C \\ 1010 &\rightarrow \% 10T_C \\ 1101 &\rightarrow \% V_a \uparrow \uparrow 13T_C \end{aligned}$$

bit size ADC
dP count

Discharging equation

$$V_o = -\frac{V_a T_1}{T} + \frac{V_R}{T} (t - T_1)$$

$$\text{at } t = T_2, V_o = 0$$

$$0 = -\frac{V_a T_1}{T} + \frac{V_R}{T} (T_2 - T_1)$$

$$\frac{V_a T_1}{T} = \frac{V_R}{T} (T_2 - T_1)$$

$$V_a T_1 = V_R (T_2 - T_1)$$

$$V_a \cdot 2^N T_C = V_R n T_C$$

$$n = \frac{V_a \cdot 2^N}{V_R}$$

$$n \propto V_a$$

Max. conversion time

$$= C \cdot T_{\text{fixed}} + \Delta T_{\text{max}}$$

$$= 2^N T_C + (2^N - 1) T_C$$

$$= (2^{N+1} - 1) T_C$$

ADC \rightarrow Slowest ADC

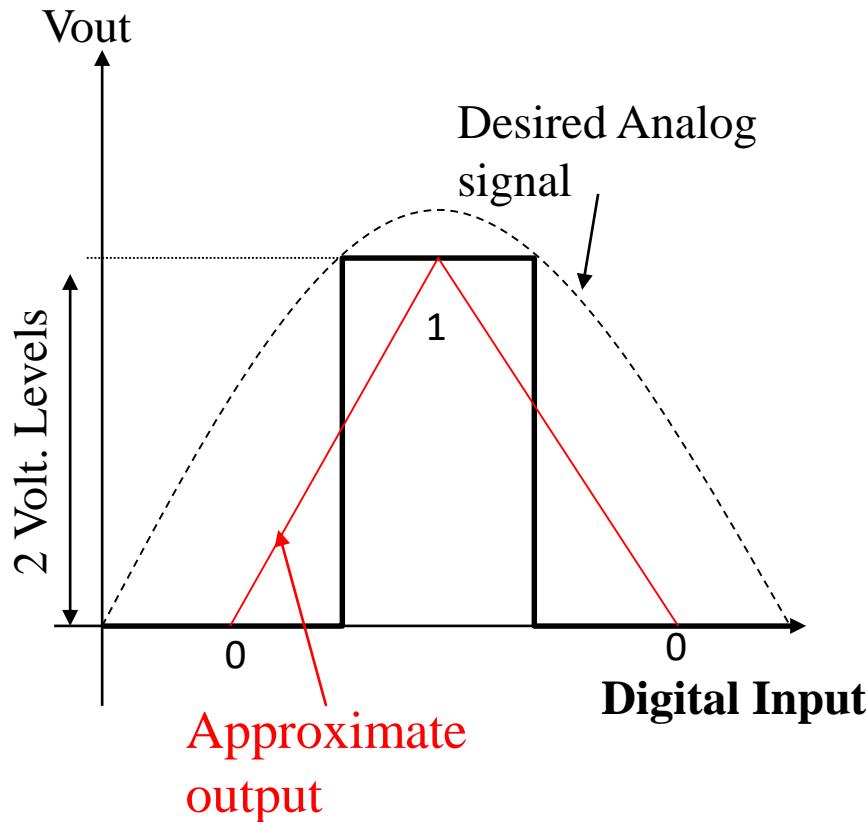
PERFORMANCE SPECIFICATIONS

- ❖ Resolution: is the smallest change in voltage which may be produced at the output of the converter.
- ❖ In short, the resolution is the value of the LSB.
- ❖ How closely can we approximate the desired output signal(Higher Res. = finer detail=smaller Voltage divisions).
- ❖ A common DAC has a 8 - 12 bit Resolution

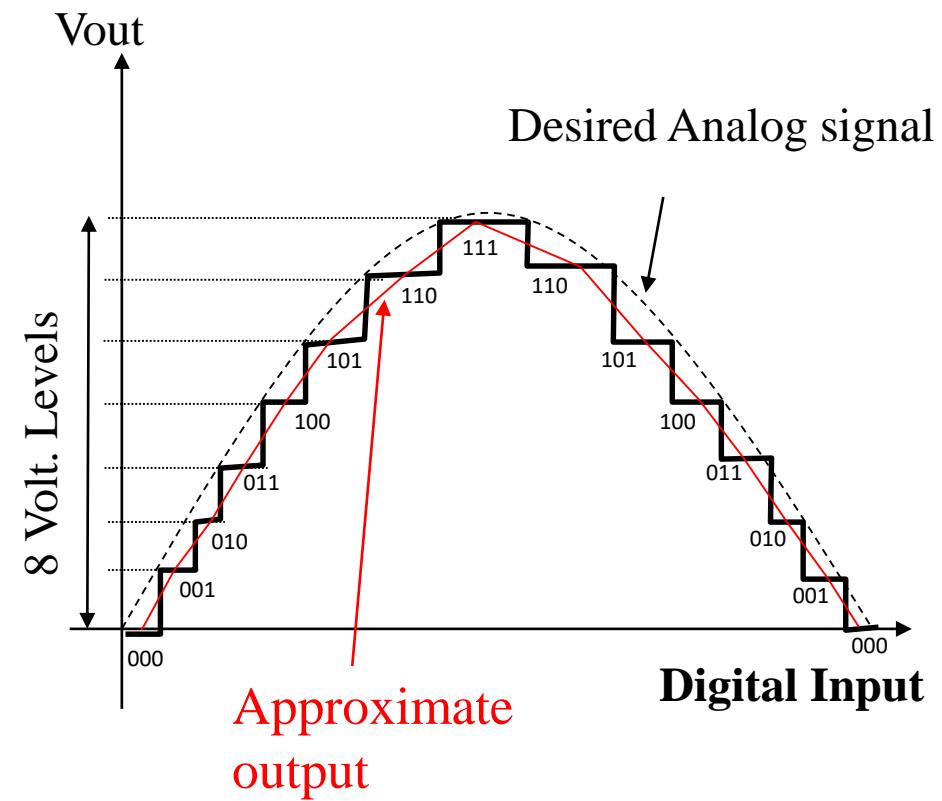
$$\text{Resolution (in volts)} = \frac{1}{2^n - 1}$$

PERFORMANCE SPECIFICATIONS

Poor Resolution(1 bit)



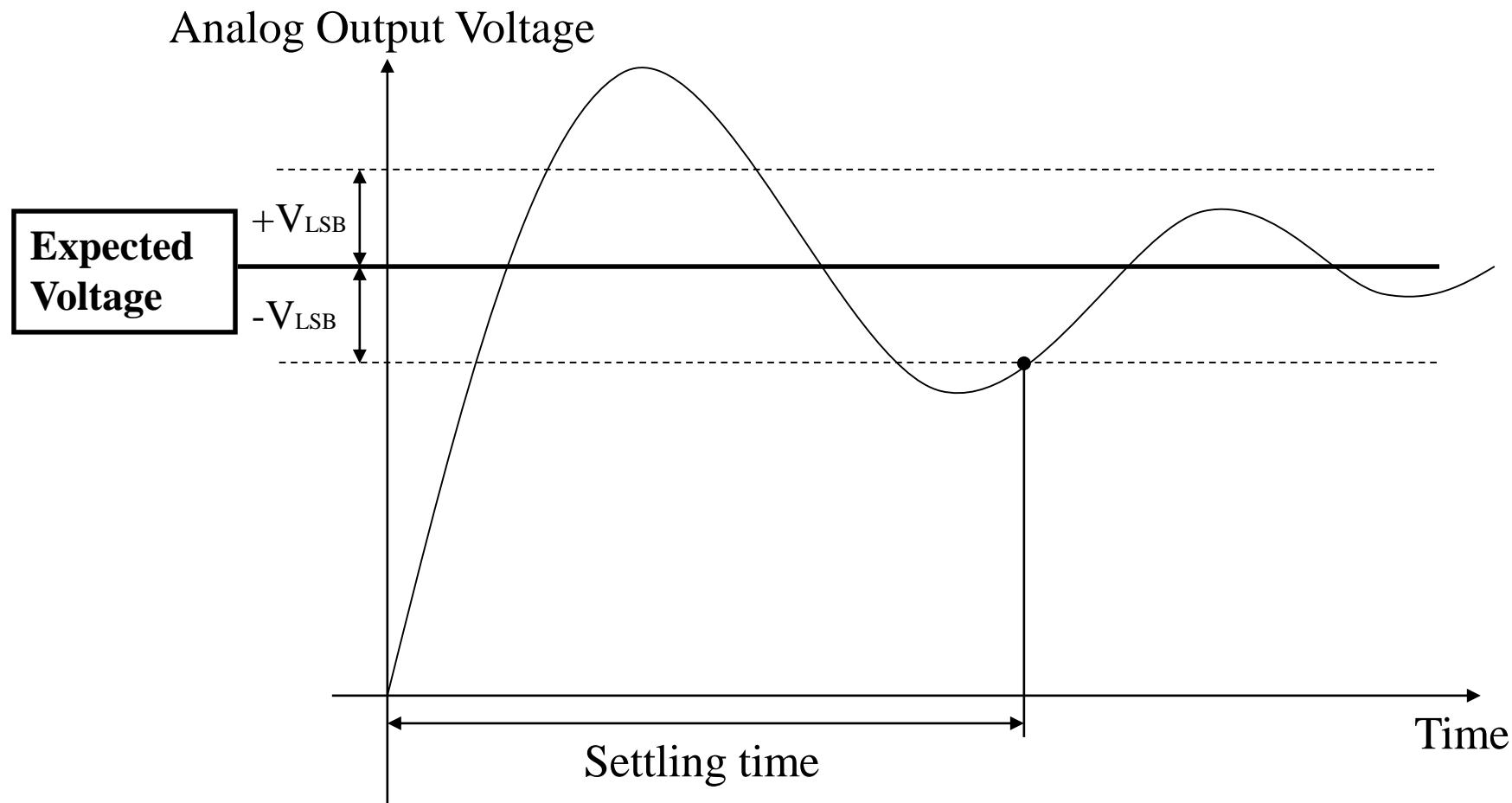
Better Resolution(3 bit)



SETTLING TIME

- ❖ The time required for the input signal voltage to settle to the expected output voltage (within $\pm \frac{1}{2}$ LSB).
- ❖ Any change in the input state will not be reflected in the output state immediately. There is a time lag, between the two events.
- ❖ Settling time ranges from about 100ns to 10 μ s depending on type of circuit used and the length of the word.

SETTLING TIME

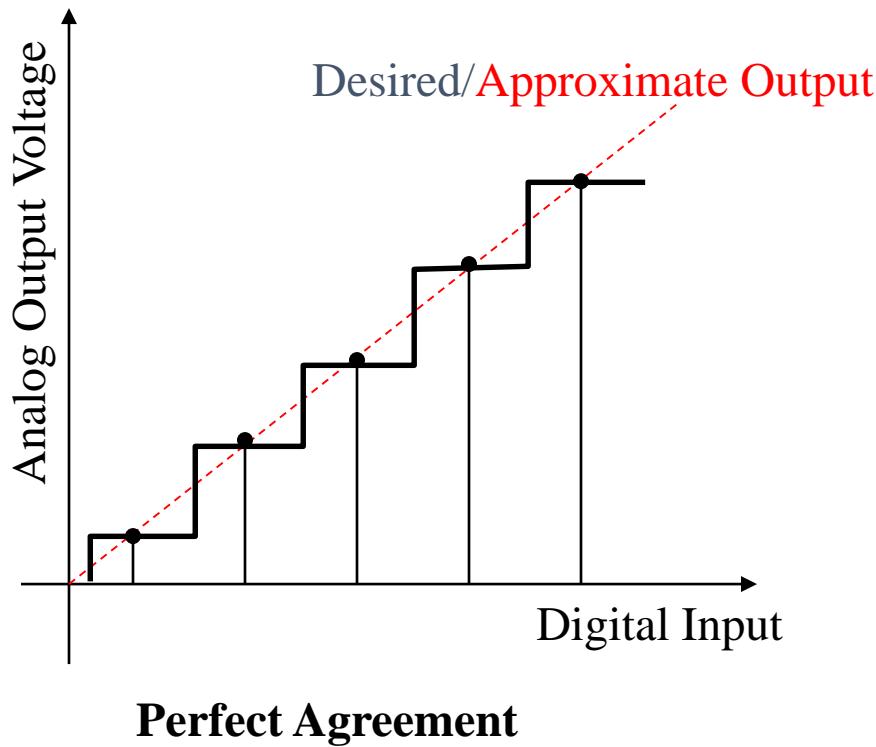


LINEARITY

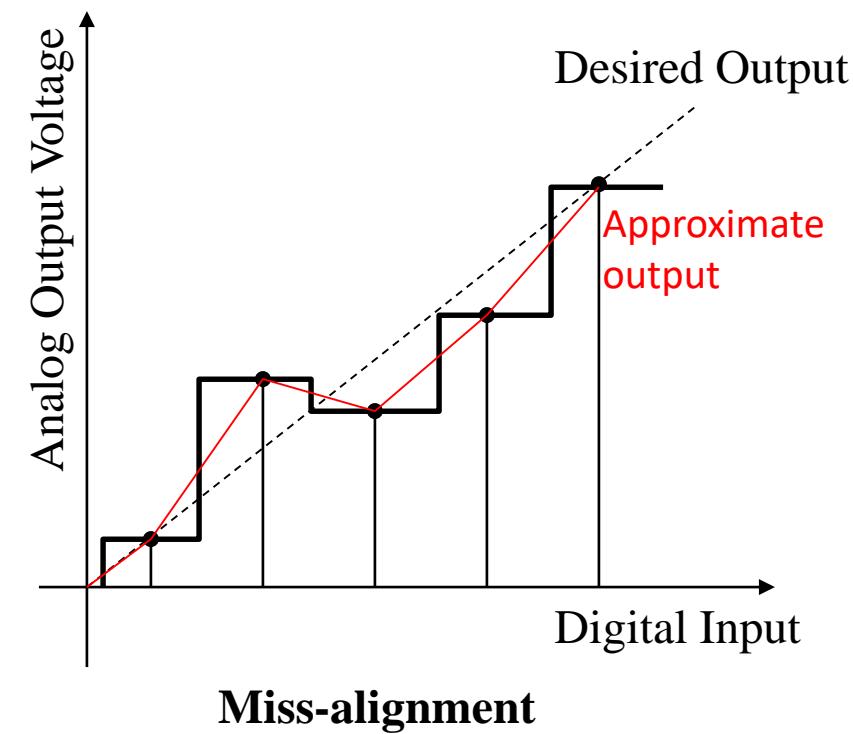
- ❖ The difference between the desired analog output and the actual output over the full range of expected values.
- ❖ Ideally, a DAC should produce a linear relationship between a digital input and the analog output, this is not always that case.

LINEARITY

Linearity(Ideal Case)



NON-Linearity(Real World)



SPEED

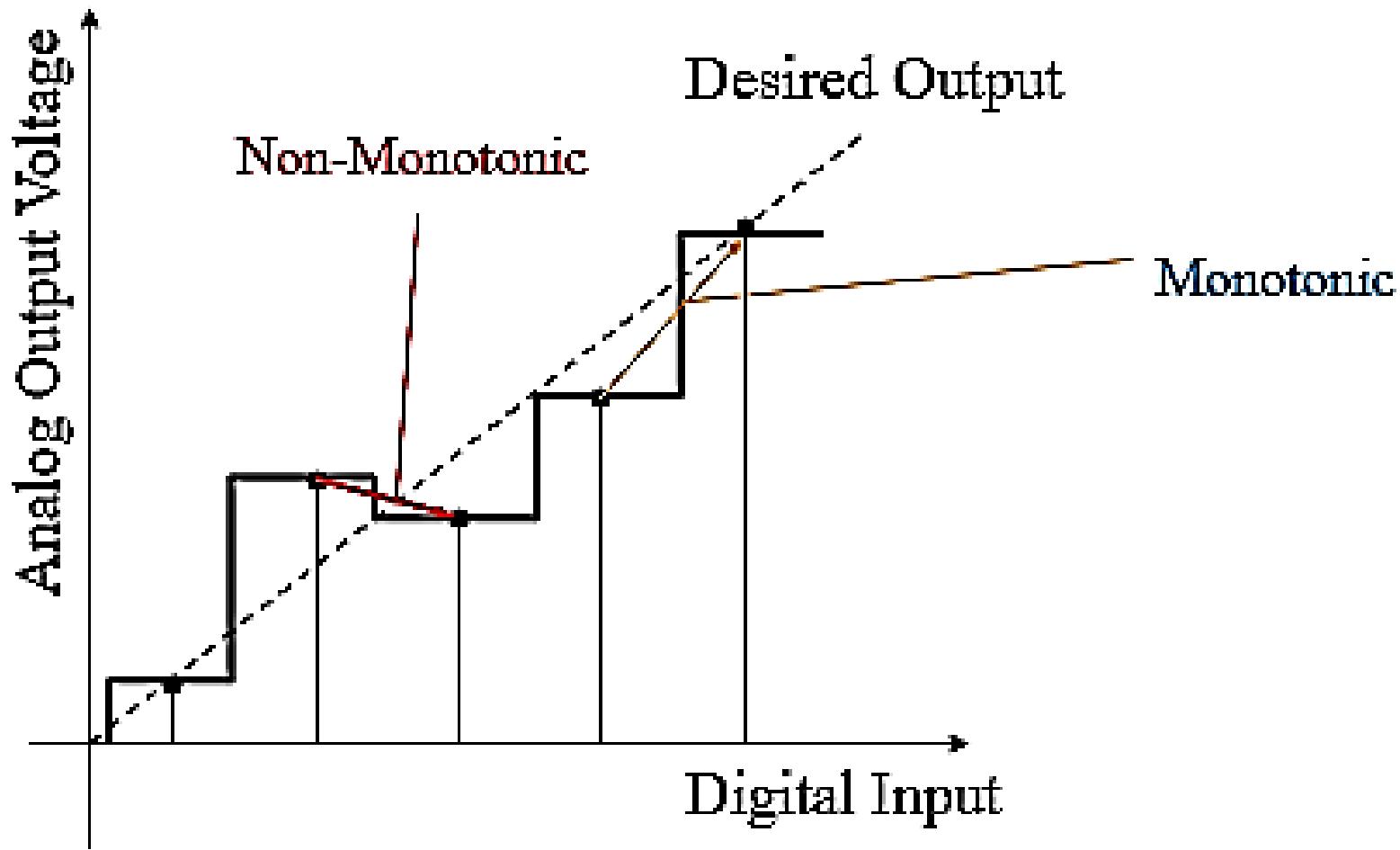
- ❖ Rate of conversion of a single digital input to its analog equivalent
- ❖ Conversion Rate depends on:
 - ❖ Clock speed of input signal
 - ❖ Settling time of converter

ACCURACY

- ❖ The maximum deviation between the actual converter output and the ideal converter output.
- ❖ The accuracy of a converter is also specified in terms of LSB increments or percentage of full scale voltage.

MONOTONICITY

- ❖ A monotonic DAC is the one whose analog output increases for an increase in digital input.
- ❖ A monotonic characteristic is essential in control applications, otherwise oscillations can result.
- ❖ In SAR, a non – monotonic characteristic may lead to missing codes.



Thank You !

All the best!