





setting time: time, reg for ip signal voltage to settle to the expected of voltage within ± 1/2 LSB nech may try change in apput state will not be reflected in the op state gnal ne). of bits VLSB - VLSB settling time linearity.
The diff b/w the desired avalog output and the actual output over the full range of expected values. Ideal

speed ! Accuracy" The max deviation by the actual convertex output & the ideal convexter output. Monotonocity, A monotonic DAC is the one whose analog of Encreases for an increase in digital input.