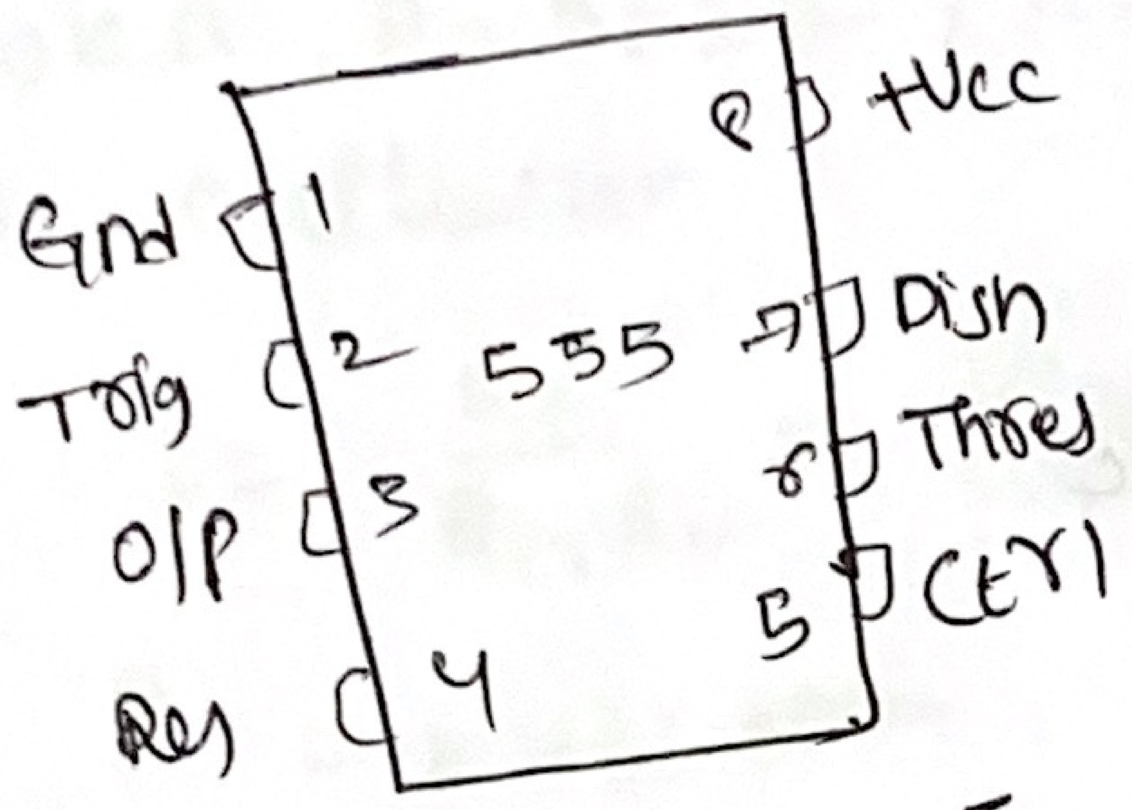
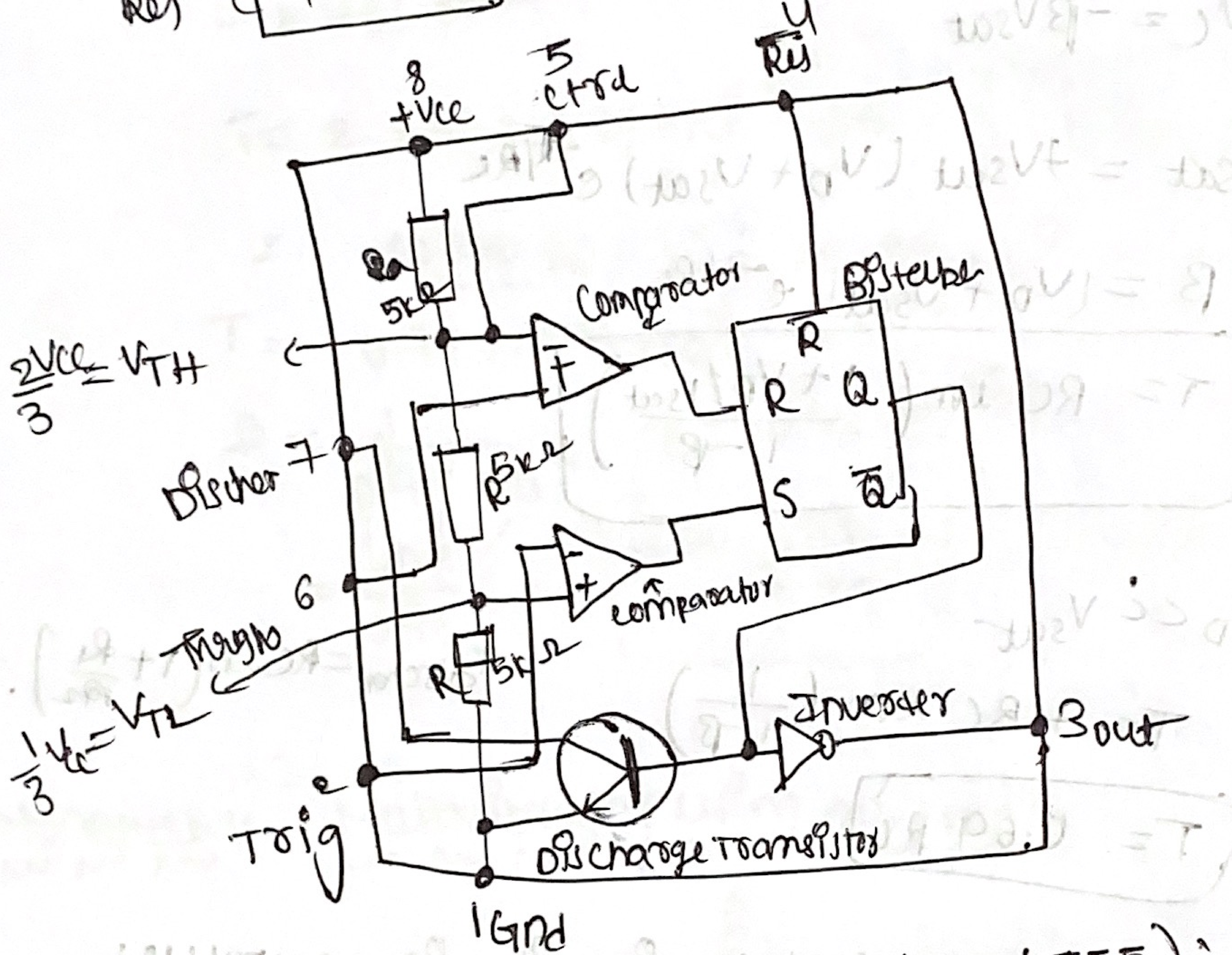
555 timer:

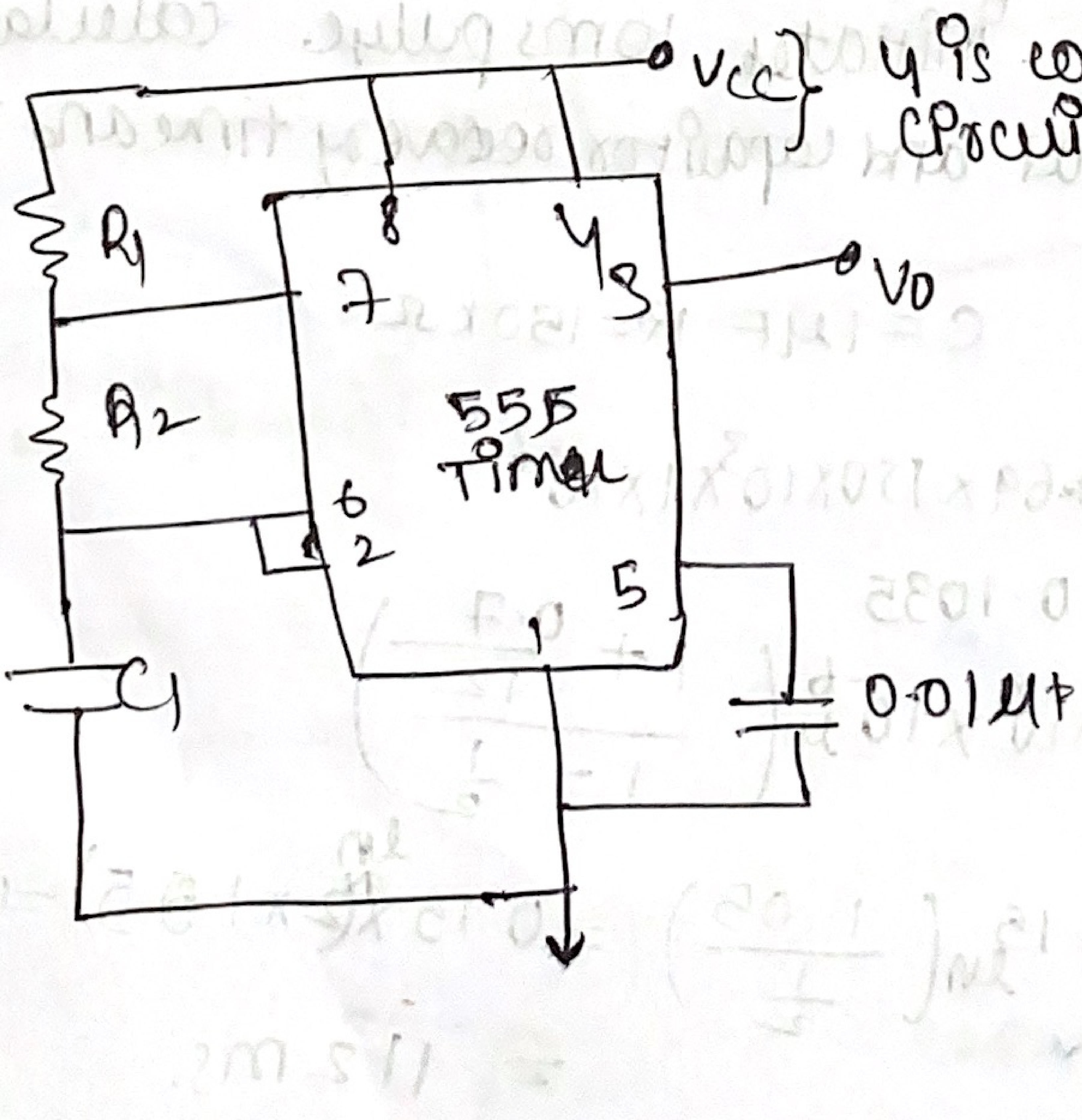
pin diagram





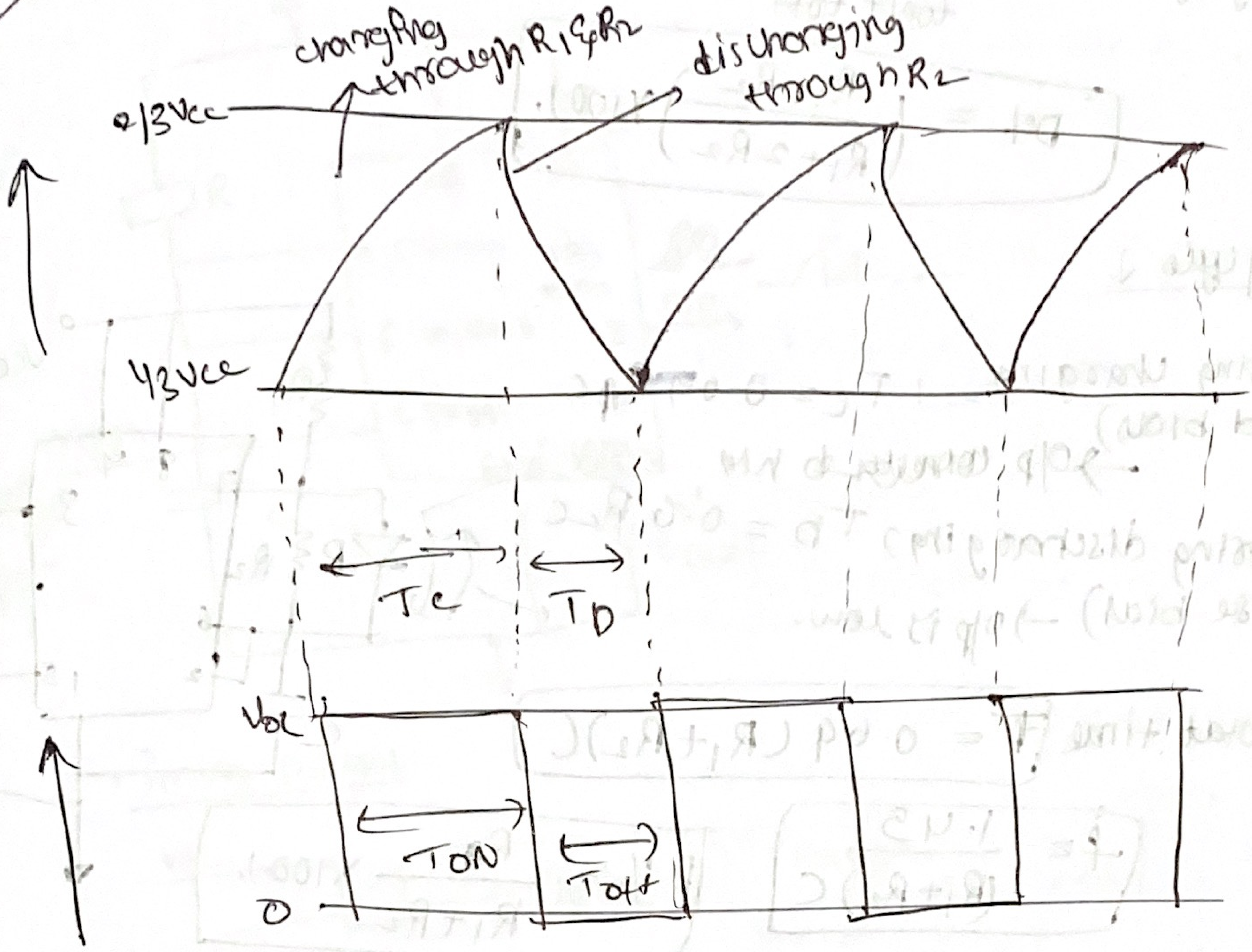
Block diagram of timer (555):

A stable Multivibrator using 555 timer:



4 is connected to make circuit astable Multivibrator

23/4/22



Derivation for expression of duty cycle:

$V_c = V_{cc}(1 - e^{-t/RC})$

→ t_1 taken by the circuit to charge from $0 \rightarrow \frac{2}{3}V_{cc}$ ($0 \rightarrow V_{TH}$)

$V_C = \frac{2}{3}V_{cc} = V_{cc}(1 - e^{t_1/RC})$

$1 - \frac{2}{3} = e^{t_1/RC}$

$t_1 = RC \ln 3$

$t_1 = 1.09\,RC$.

$t_{ON} = t_1 - t_2$

$t_{ON} = 0.69\,RC$

$\boxed{t_{ON} = 0.69(R_1 + R_2)C.}$ (charging time)

→ t_2 to charge from $0 \rightarrow 1/3\,V_{cc}$

$V_C = \frac{1}{3}V_{cc} = V_{cc}(1 - e^{-t_2/RC})$

$\frac{2}{3} = \frac{RC}{t_2} \ln\left(\frac{3}{2}\right)$

$t_2 = 0.40\,RC$.

→ Discharging time,

$\frac{1}{3}V_{cc} = \frac{2}{3}V_{cc}\, e^{-t/RC}$

$\boxed{t_{off} = 0.69\,R_2C}$

$T = t_{ON} + t_{off}$

$\boxed{T = 0.69(R_1 + 2R_2)C.}$ Total time

$\boxed{f = \frac{1.45}{(R_1 + 2R_2)C}}$ frequency.

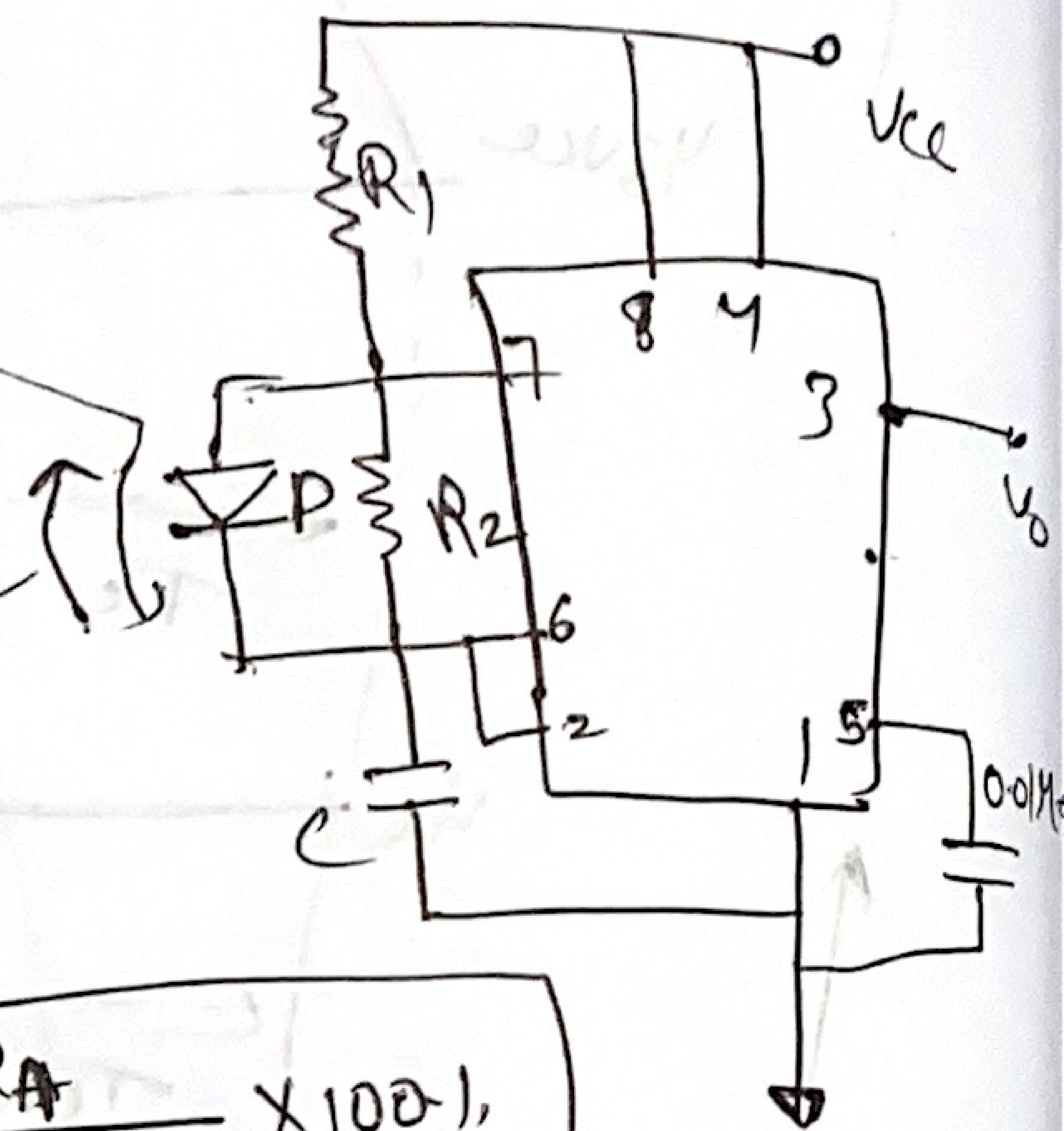
Duty cycle (D) % = $\frac{t_{ON}}{t_{ON} + t_{OFF}} \times 100\%$

$$\boxed{D\% = \left(\frac{R_1 + R_2}{R_1 + 2R_2}\right) \times 100\%}$$

Duty cycle ↓

During charging (forward bias) $T_C = 0.69 R_A C$
→ o/p connected to high

During discharging (Reverse bias) $T_D = 0.69 R_2 C$ → o/p is low.



Total time $\boxed{T = 0.69(R_1 + R_2)C}$

$$\boxed{f = \frac{1.45}{(R_1 + R_2)C}} \qquad \boxed{D\% = \frac{R_A}{R_1 + R_2} \times 100\%}$$

Q1) For stable multi vibrator using 555 timer, $R_1 = 6.8k\Omega$ $R_2 = 3.3k\Omega$ and $C = 0.1\mu F$. (a) t_{HIGH} (b) t_{LOW} (c) free running frequency and (d) Duty cycle (D).

A)

(a) $t_{ON} = 0.69(R_1 + R_2)C$

$= 0.69(3.3 + 6.8) \times 10^3 \times 0.01 \times 10^{-6}$

$= 6.969 \times 10^{-4} = 0.7ms$

(b) $t_{OFF} = 0.69 R_2 C$

$= 2.277 \times 10^{-4} = 0.23ms$

(c) $T = (6.969 + 2.277) \times 10^{-4}$

$= (9.246) \times 10^{-4}$

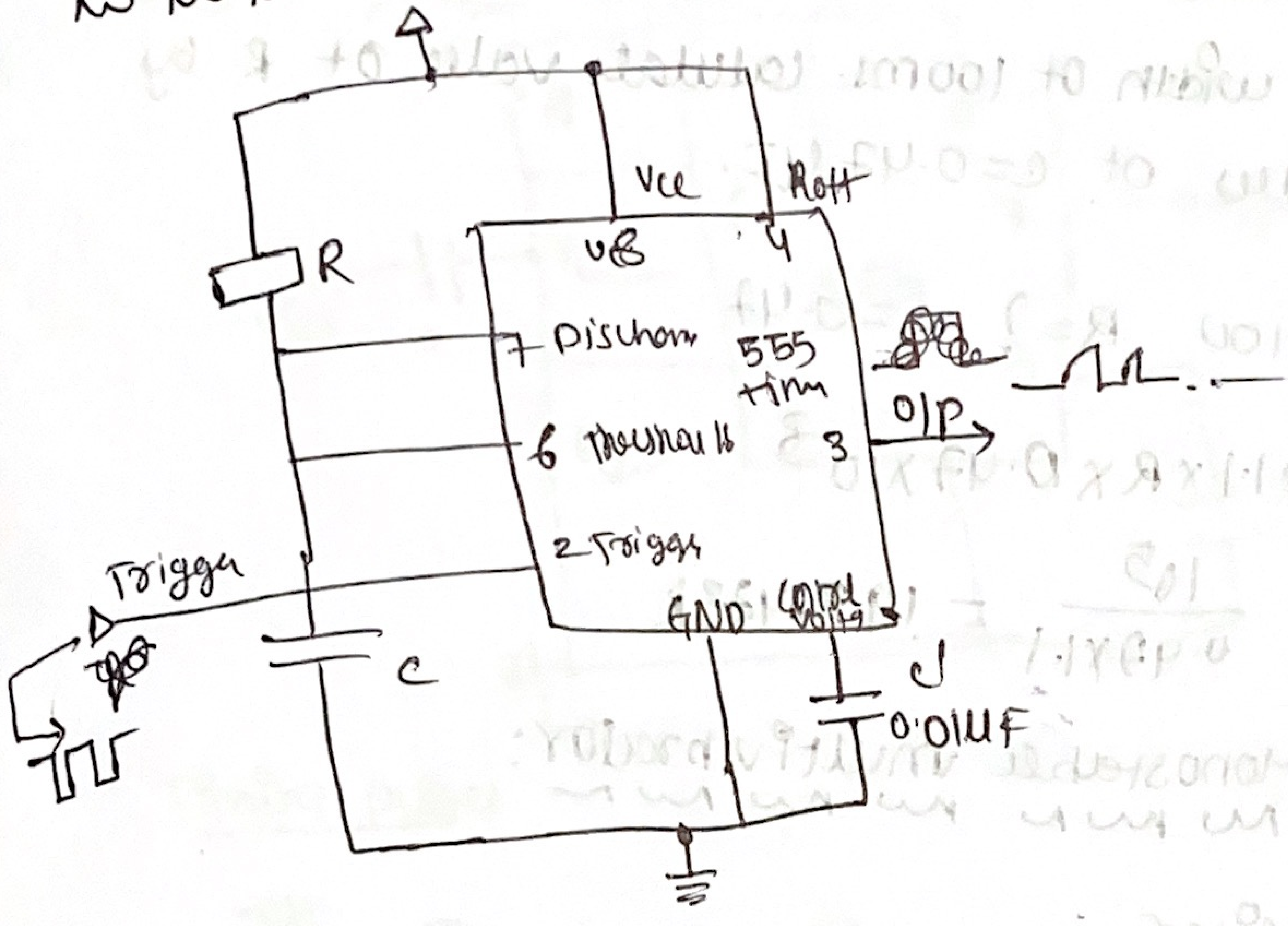
$f = \frac{1}{9.246 \times 10^{-4}} = 1081.5 Hz = 1.07KH$

(d) $D\% = \frac{6.969 \times 10^{-4}}{9.246 \times 10^{-4}} \times 100\%$

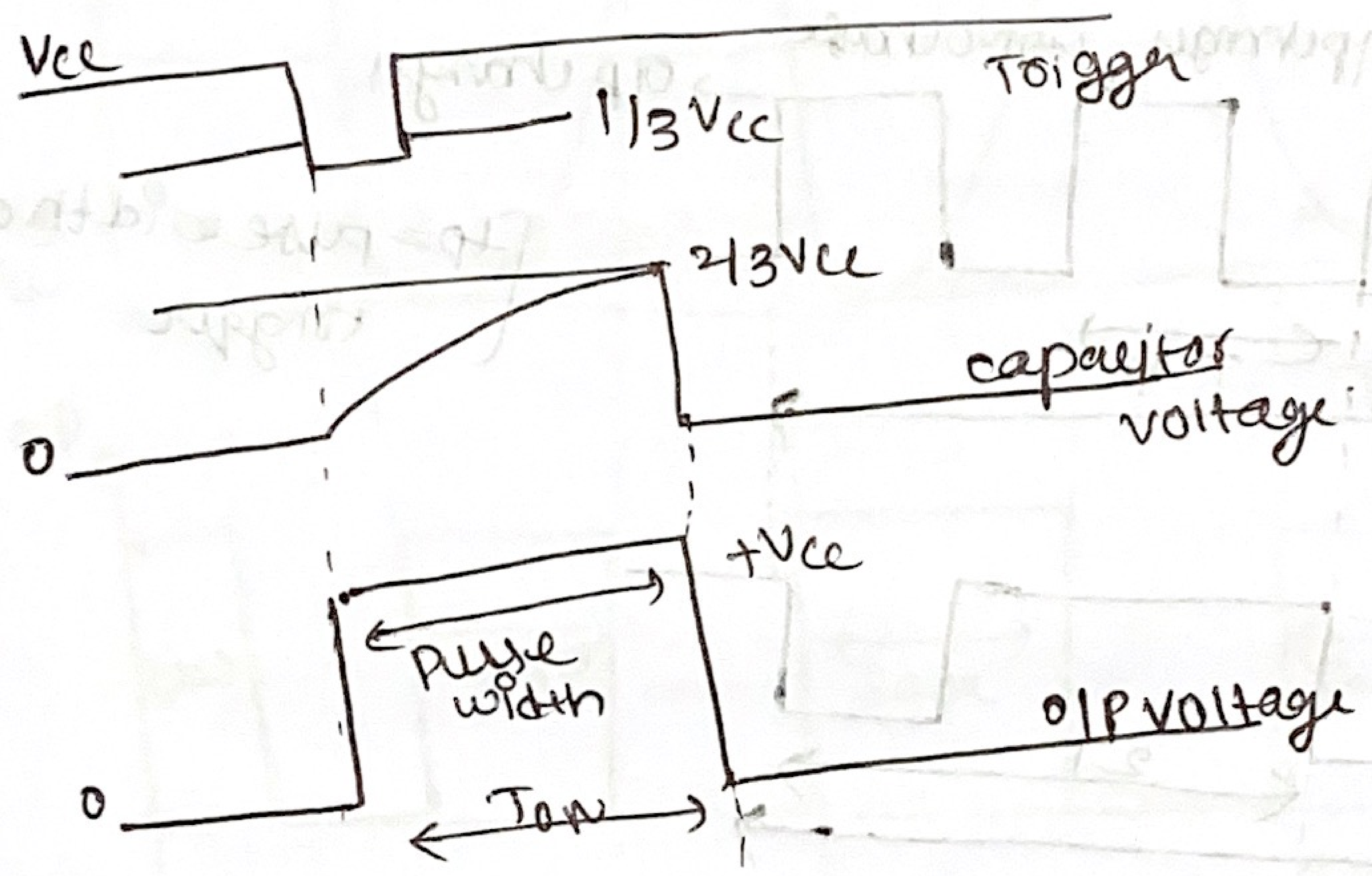
$= 0.75 \times 100\%$

$= 75\%$

Monostable Multivibrator:



Timing pulses.



25/4/22

Total time period:

$$V_c = V_{cc}(1-e^{-t/RC}).$$

At $t=T$, $V_c = \frac{2}{3}V_{cc}$

$$\frac{2}{3}V_{cc} = V_{cc}(1-e^{-T/RC})$$

$$\frac{2}{3}-1 = -e^{-T/RC}$$

$$T = RC\ln 3$$

$$T = 1.09\,RC$$

(Pulse width) $\boxed{T = 1.1RC}$

Q2) Design a monostable multivibrator using 555 timer to produce a pulse width of 100ms. Calculate value of R by assuming the value of C=0.47µF.

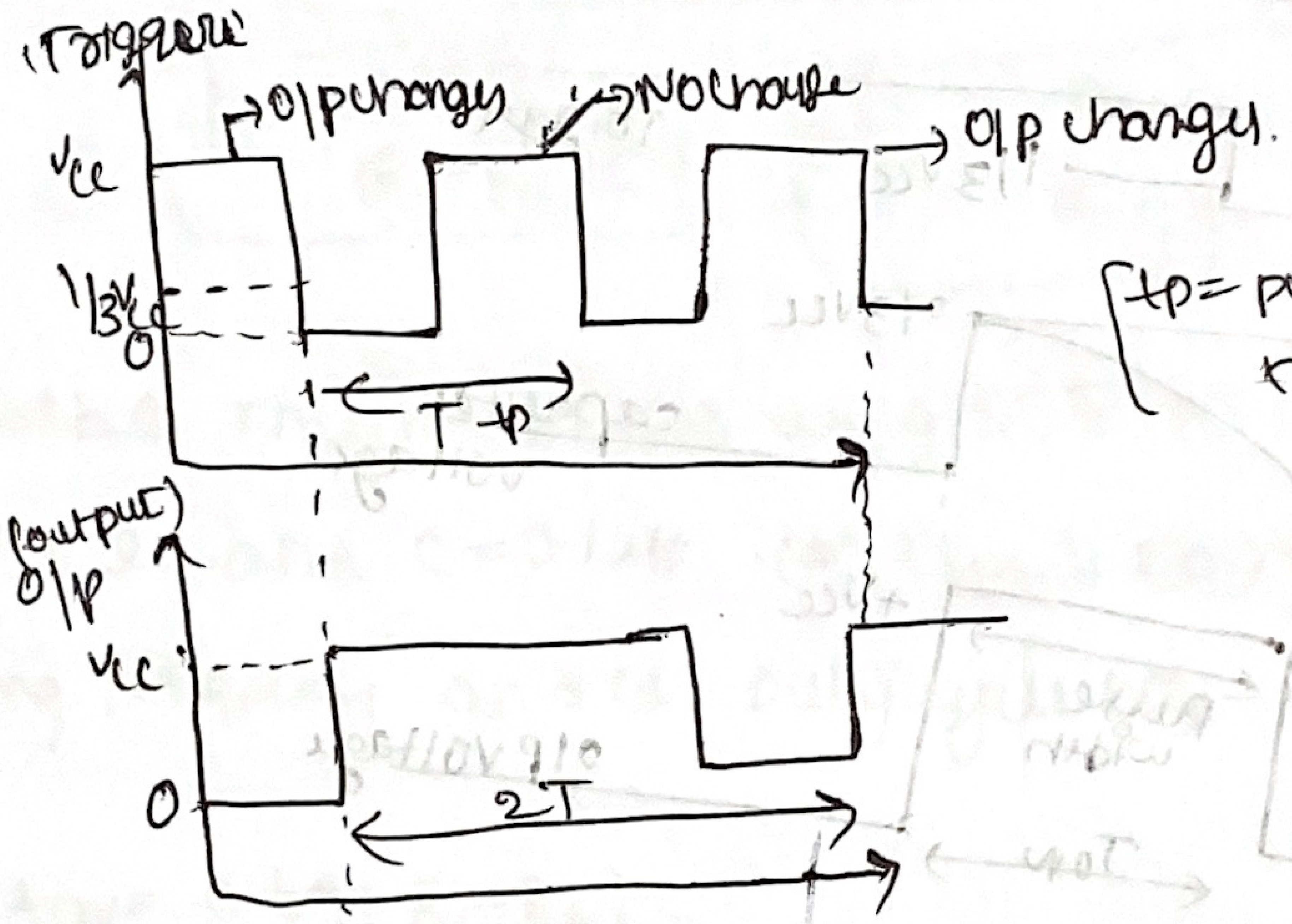
A) Pulse width = 100   R = ?   C = 0.47

$100 = 1.1 \times R \times 0.47 \times 10^{-3}$

$R = \frac{10^5}{0.47 \times 1.1} = 193.423k$

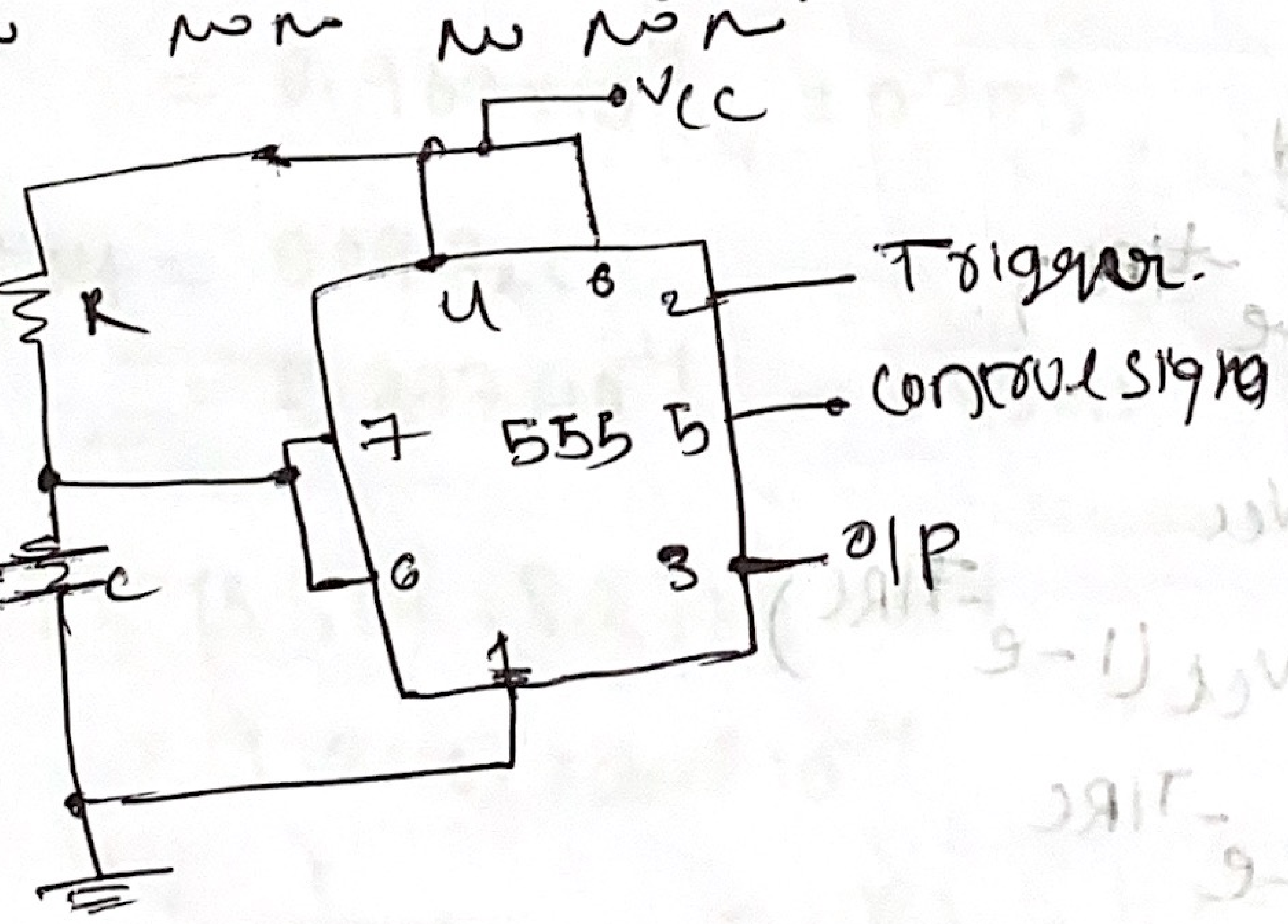
Application of Monostable multivibrator:

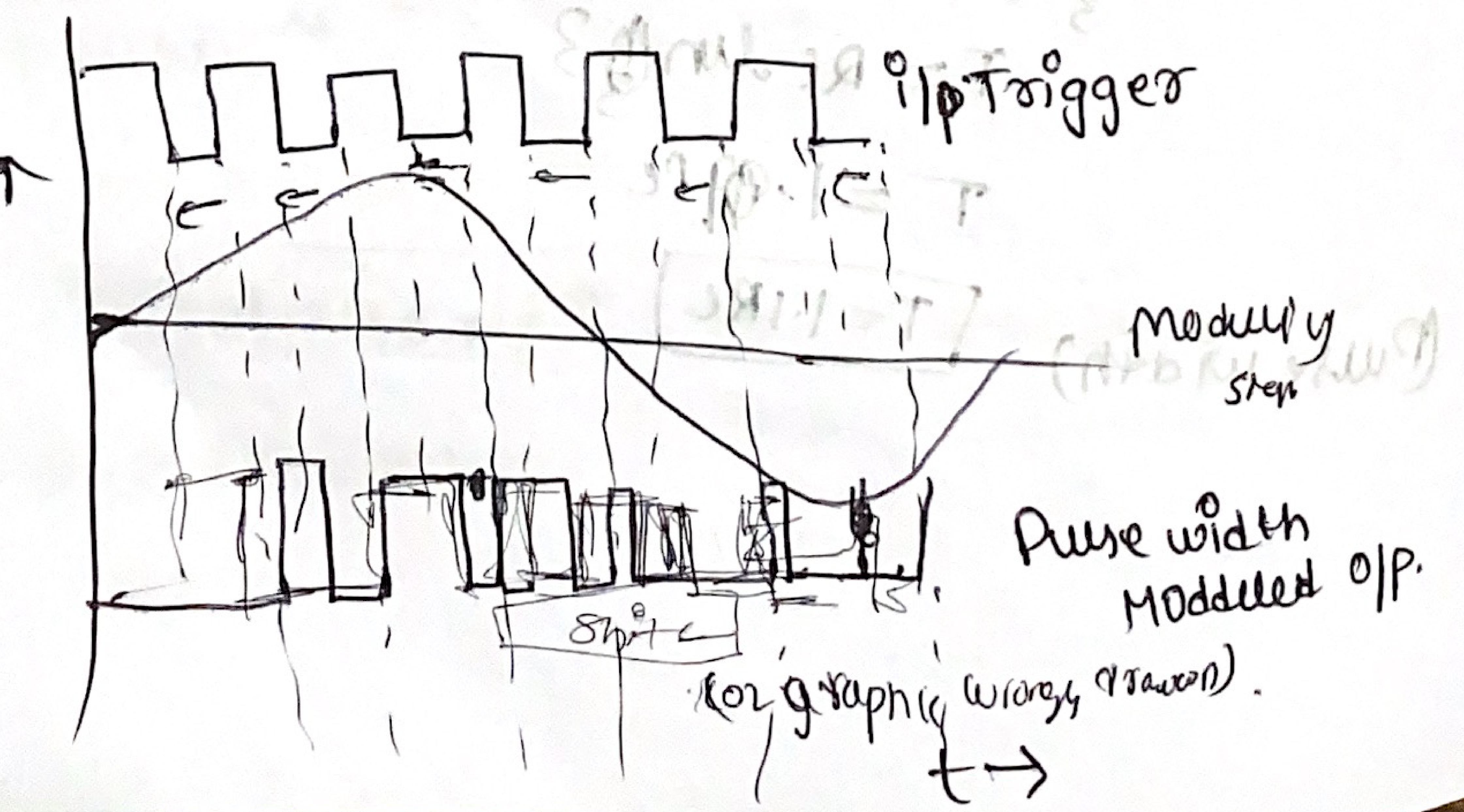
(i) Frequency Divider



[tp = pulse width of input trigger]

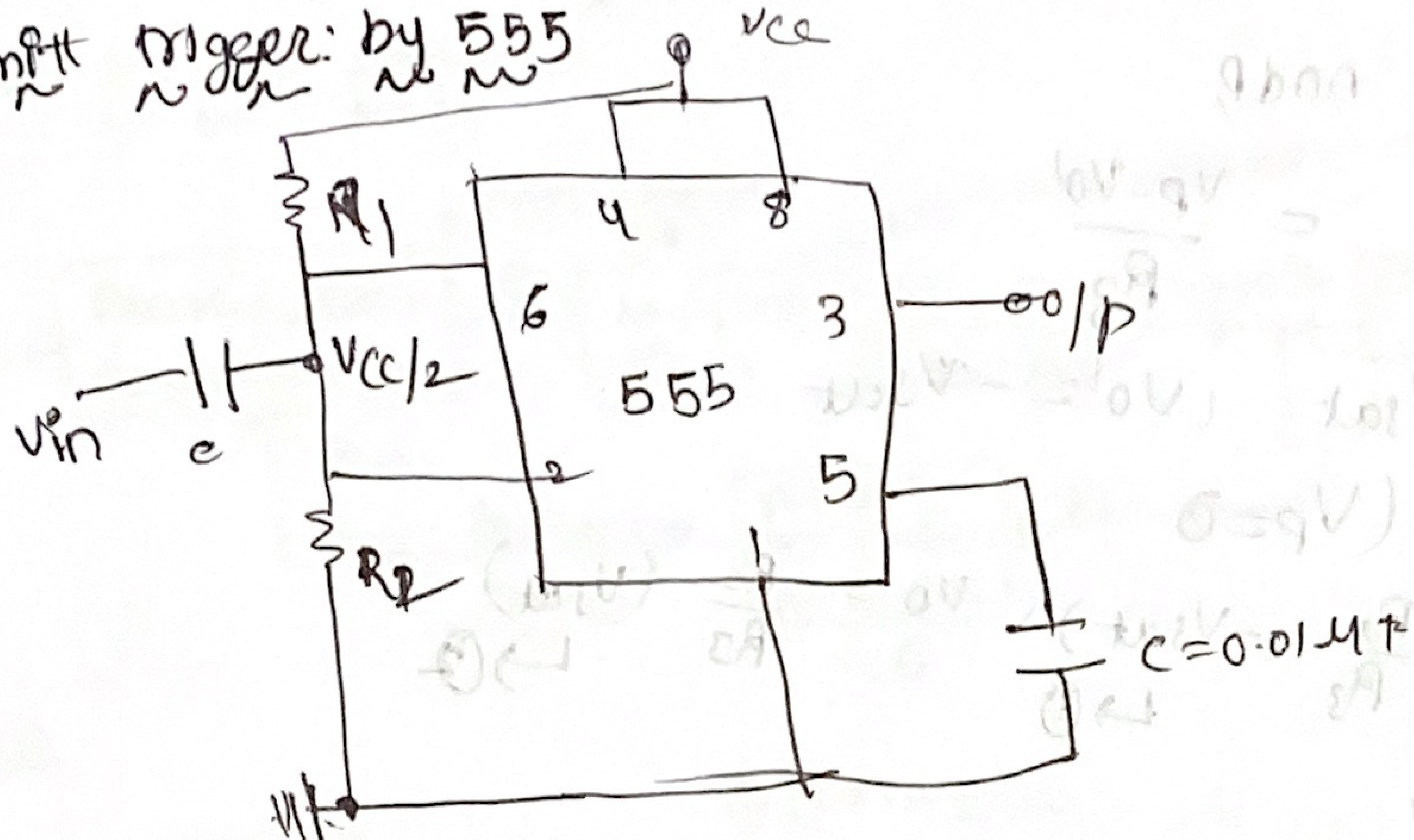
(ii) Pulse width Modulation



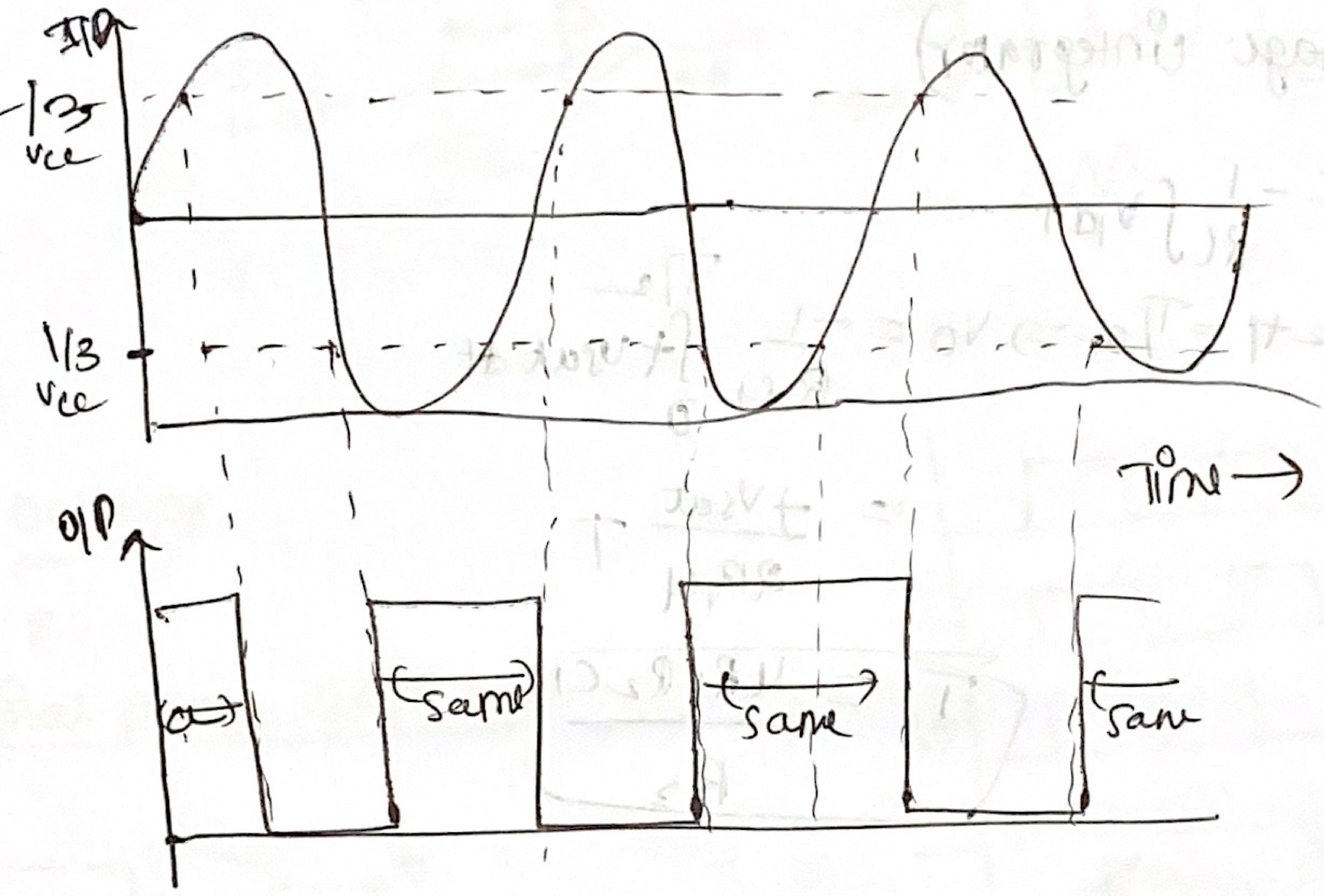


(or graphic wrongly drawn).

(iii) Schmitt trigger: by 555

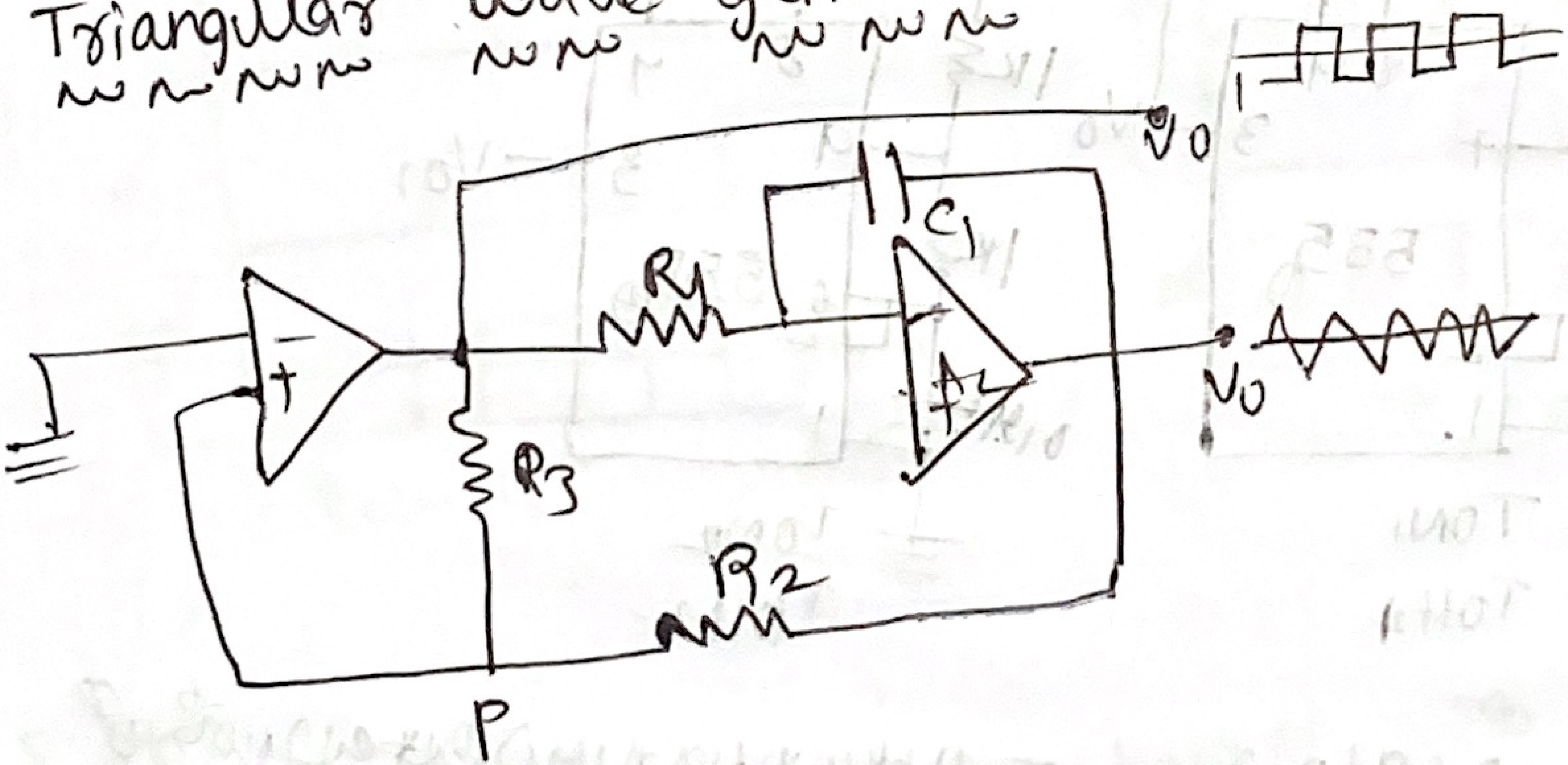


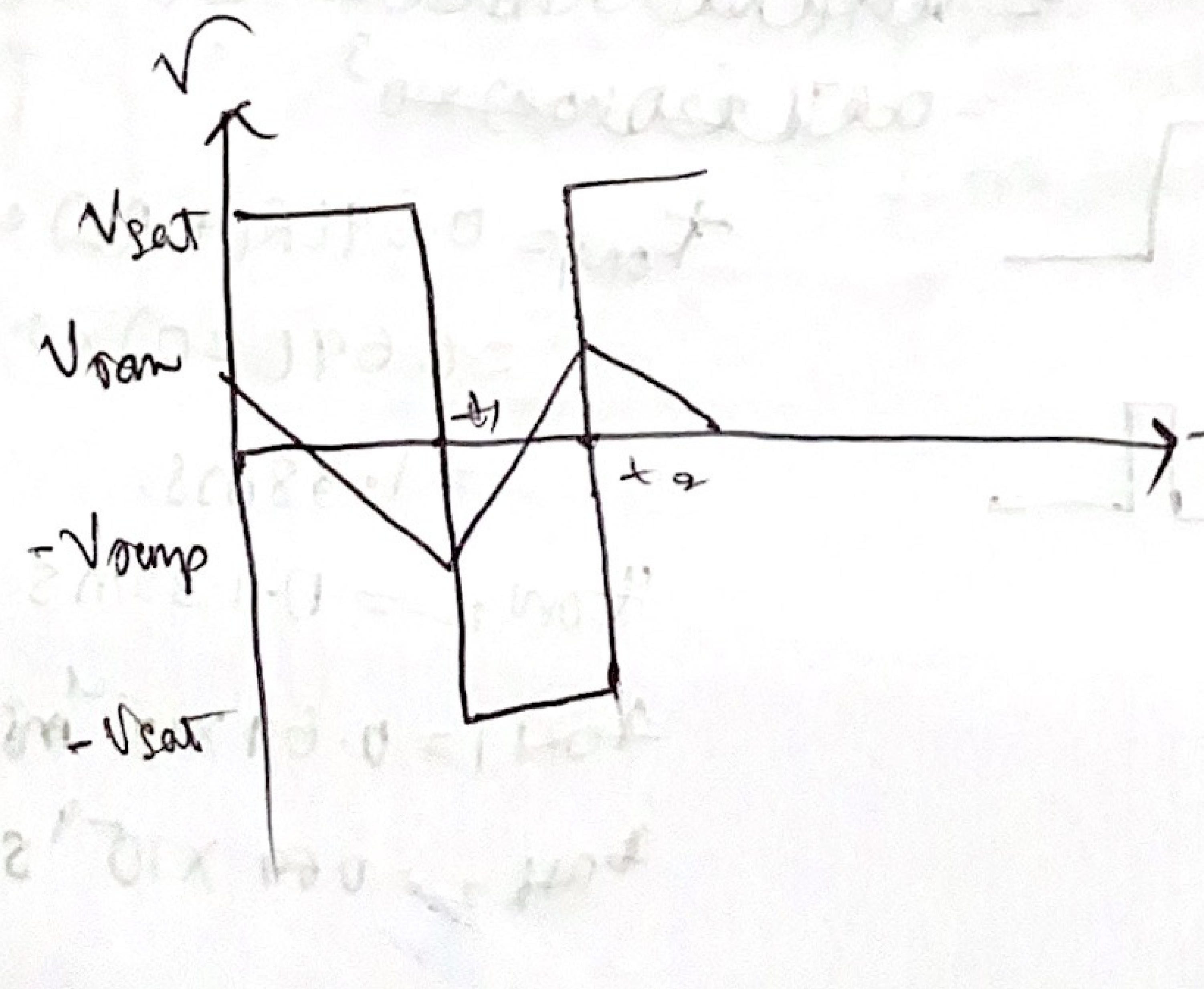
Timing pulses



27/04/22

Triangular wave generator:





kcl at node P,

$$\frac{V_0 - V_P}{R_2} = \frac{V_P - V_0'}{R_3}$$

$V_0' = V_{sat}$, $V_0' = -V_{sat}$

$(V_P = 0)$

$V_0 = \frac{R_2}{R_3}(-V_{sat}) \rightarrow ①$ $\quad V_0 = \frac{R_2}{R_3}(V_{sat}) \rightarrow ②$

② - ①

$$V_{0(PP)} = \frac{2R_2}{R_3}(V_{sat}).$$

2nd stage: integrator

$$V_0 = -\frac{1}{RC}\int V_i\,dt$$

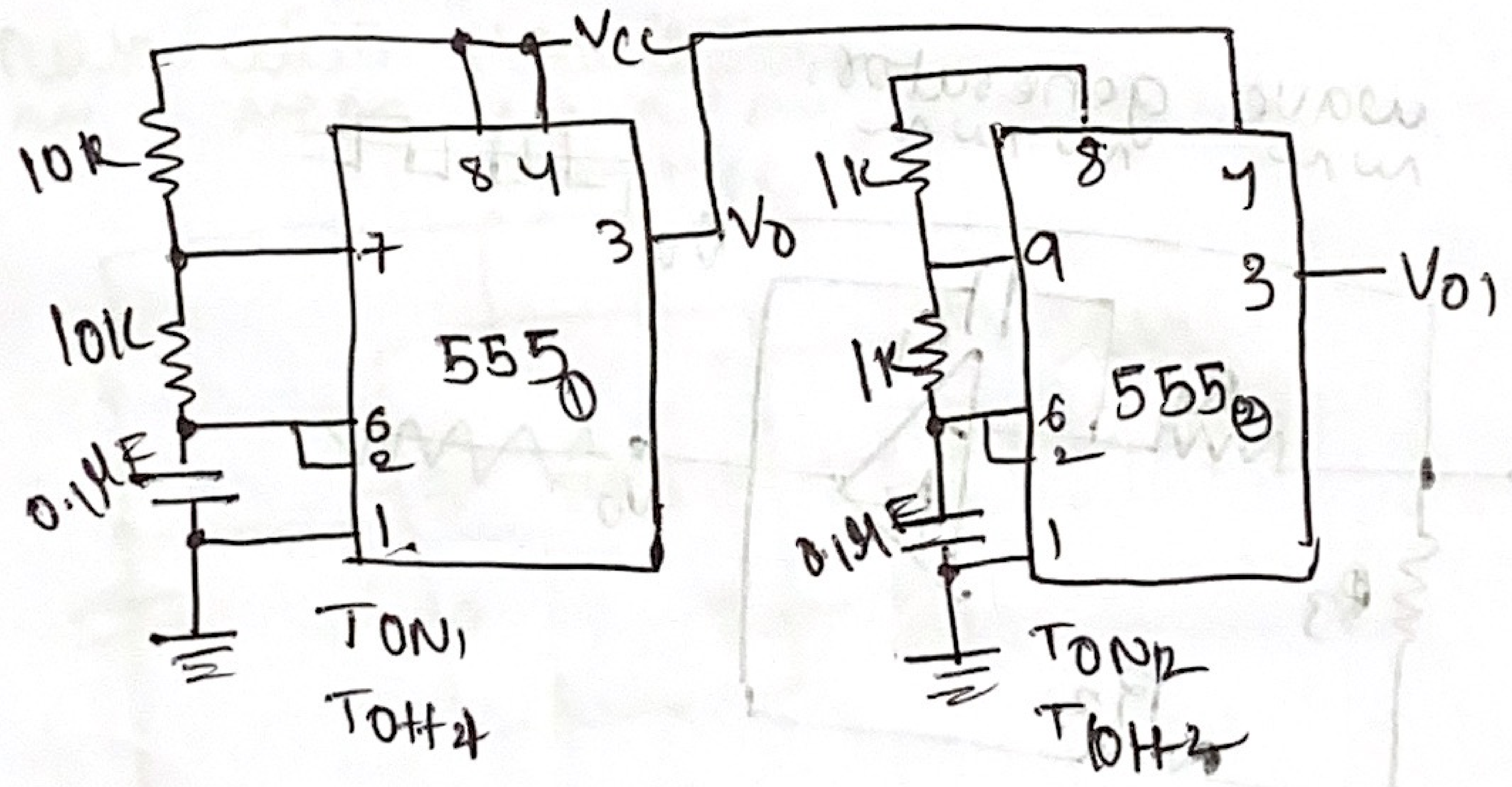
At $t = T/2 \Rightarrow V_0 = -\frac{1}{R_1C_1}\int_0^{T/2} \pm V_{sat}\,dt$

$$= \frac{\pm V_{sat}}{2R_1C_1}T$$

$$\boxed{T = \frac{4R_1R_2C_1}{R_3}}$$

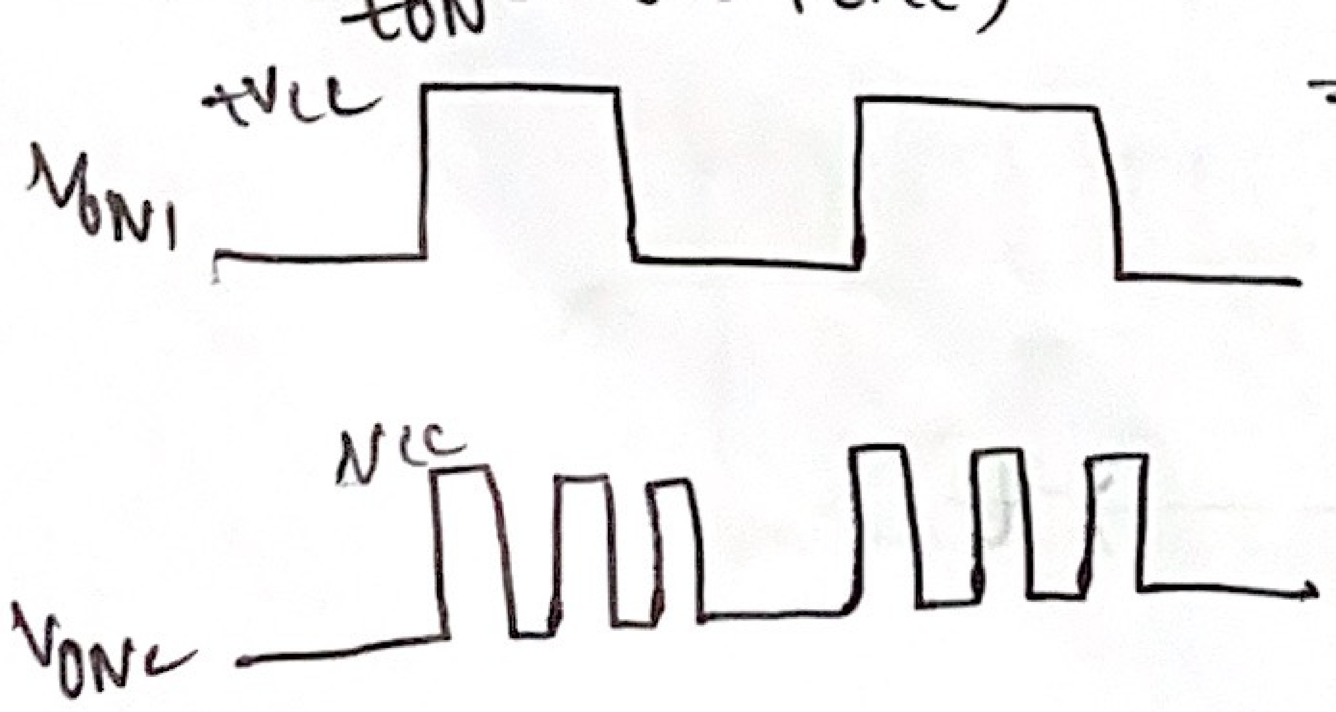
30/4/22

Q1)



$t_{ON} = 0.69(RC)$ $\quad = ~~0.69(\ldots)\times10^{-6}~~$

$= ~~0.69(220\times0.1)\times10^{-3}~~$



$t_{ON_1} = 0.69(R_1 + R_2)C$

$= 0.69(20)\times0.1\times10^{-3}$

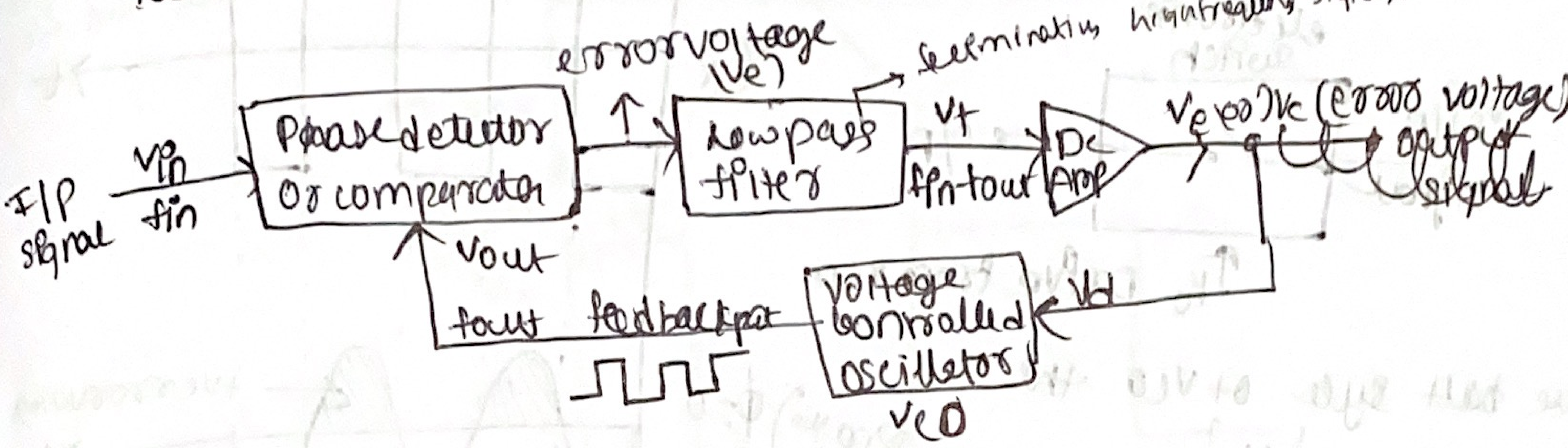
$= 1.38\,ms.$

$t_{ON_2} = 0.138\,ms.$

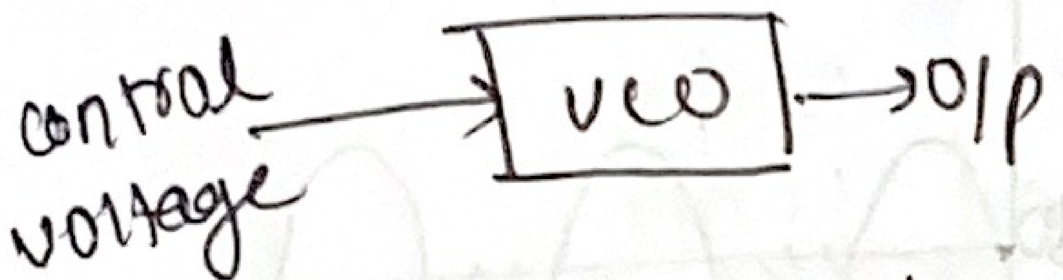
$t_{OFF_1} = 0.69\times10^{-4}\,s$

$t_{OFF_2} = 0.69\times10^{-4}\,s$

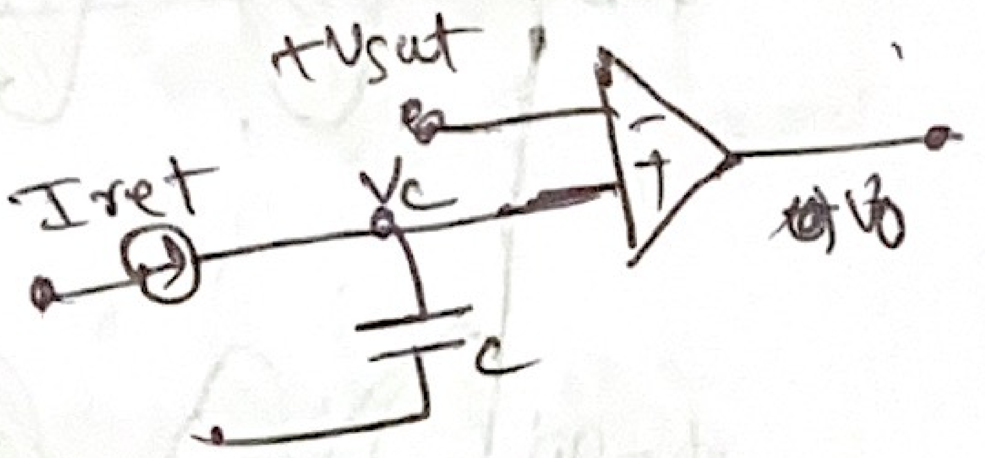
Phase locked loop:

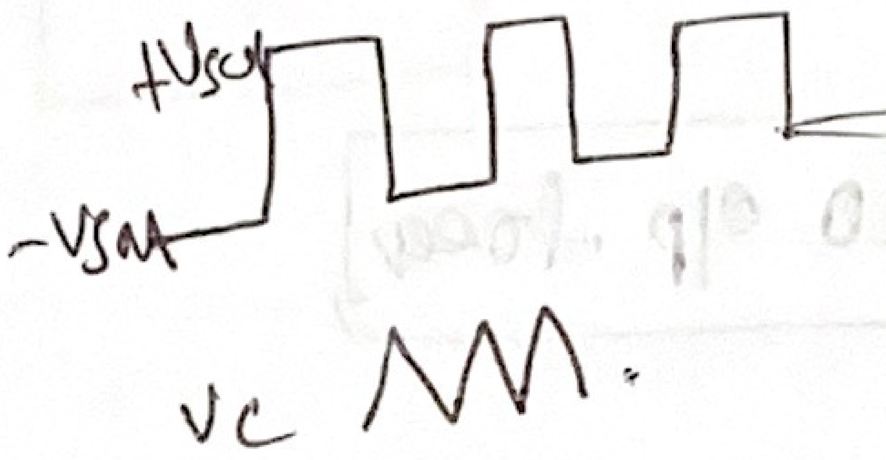


VCO



① Harmonic
② Relaxation.



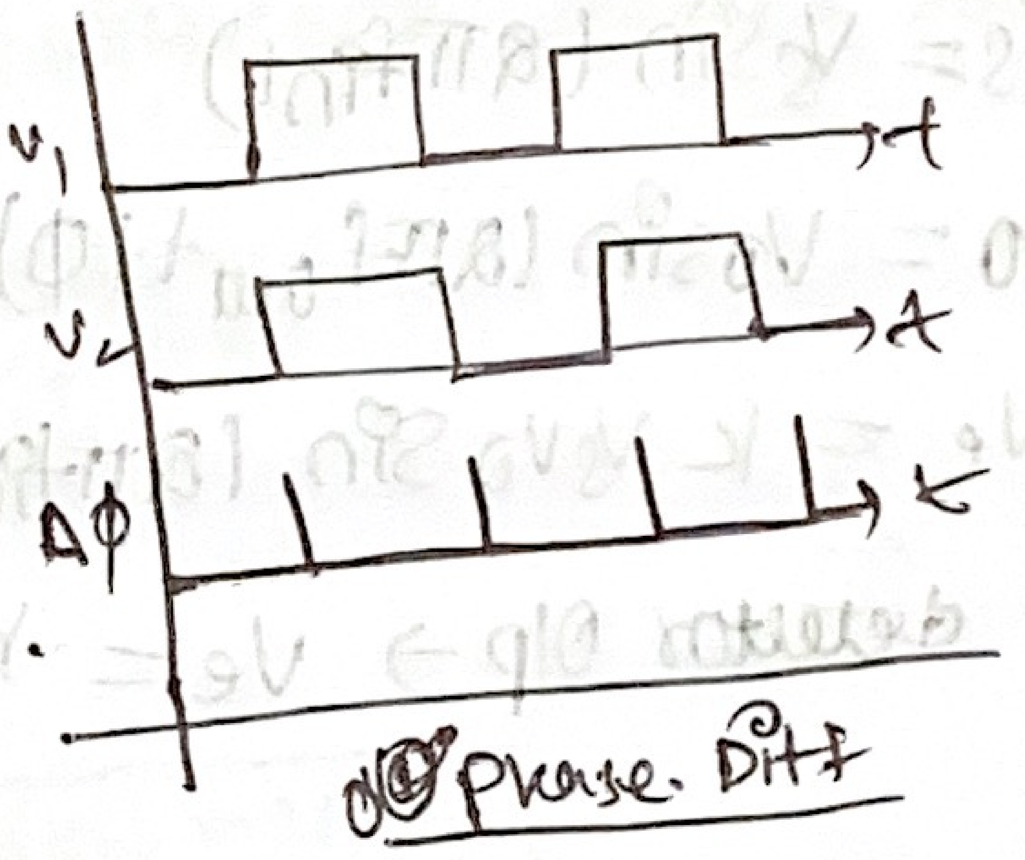


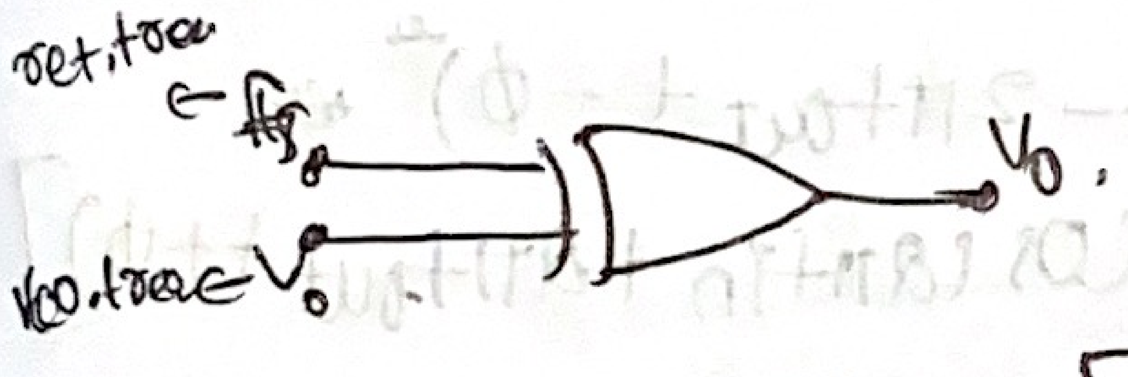
2/5/22

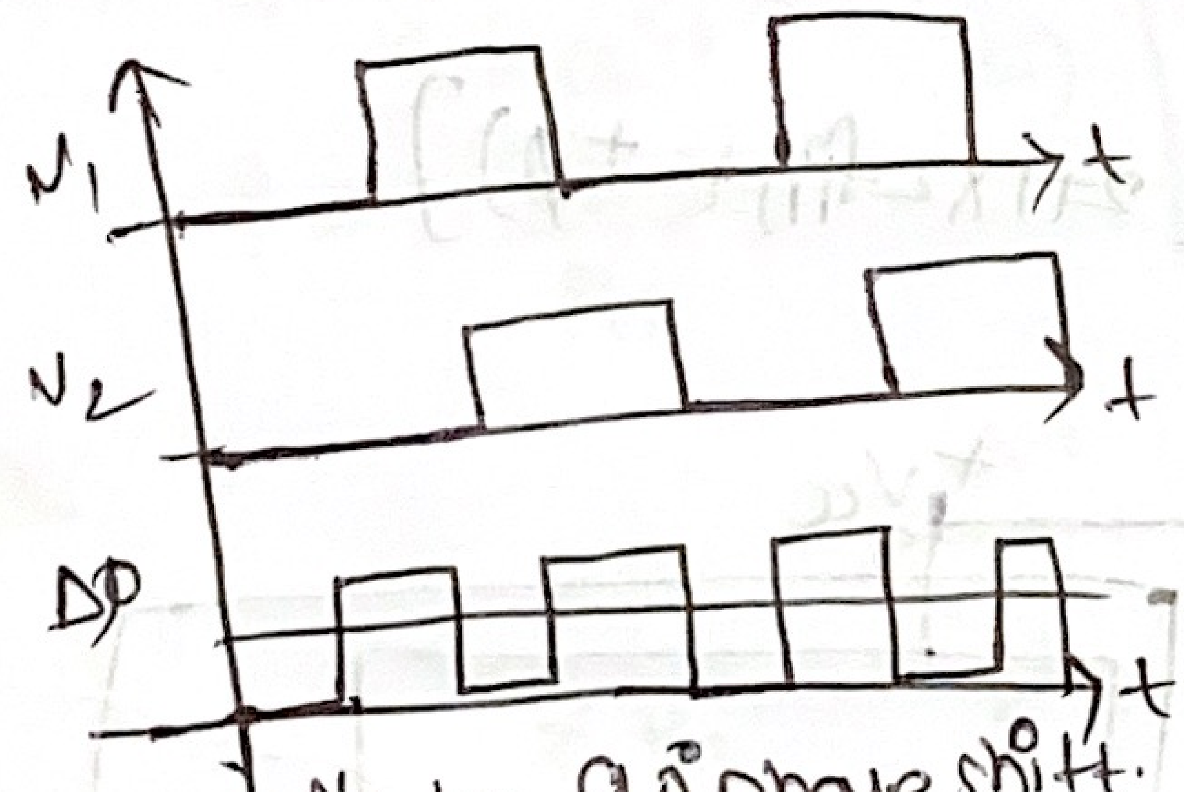
Phase Detector:

α→ β→

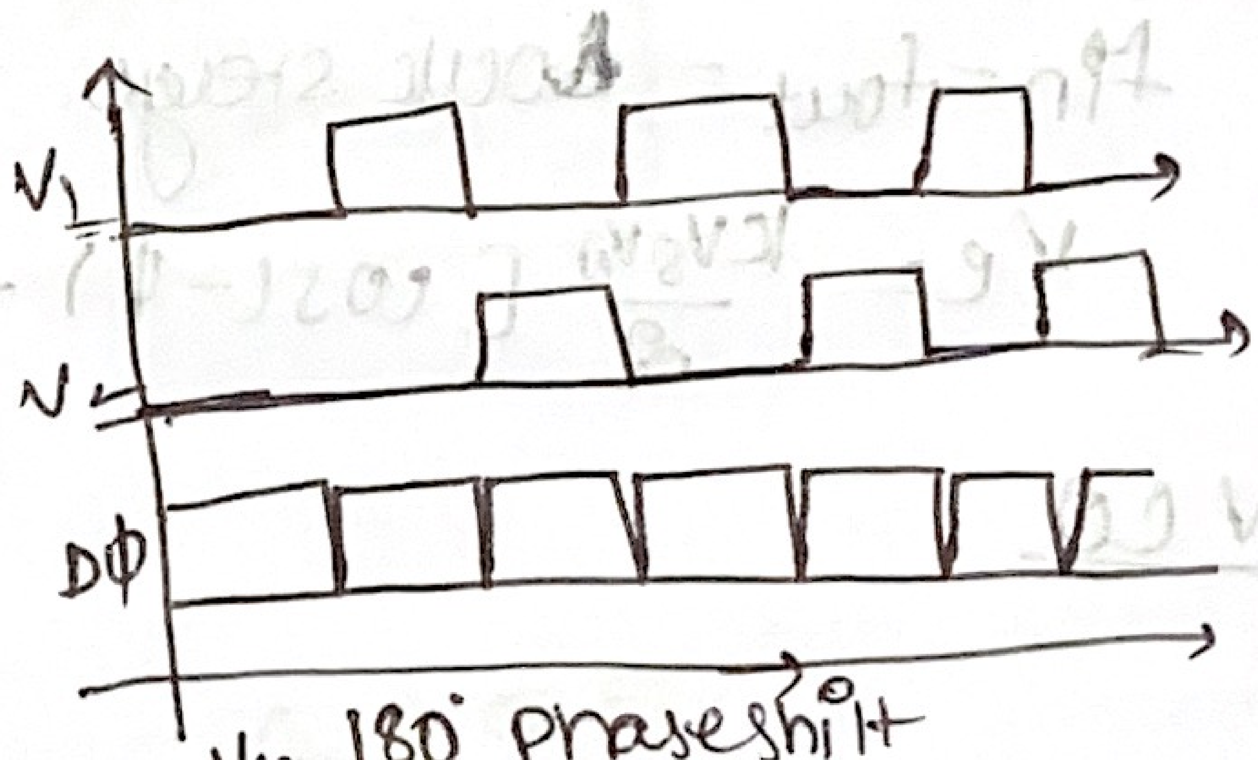
① Digital phase detector:



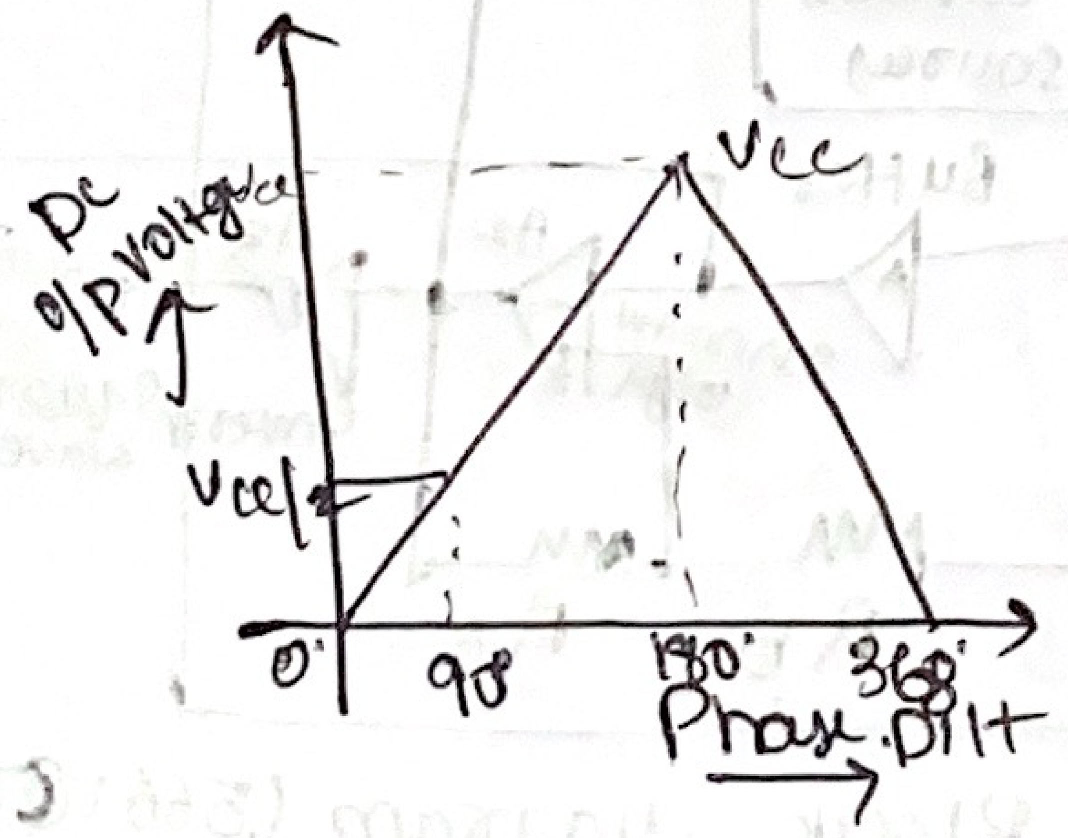




90° phase shift.

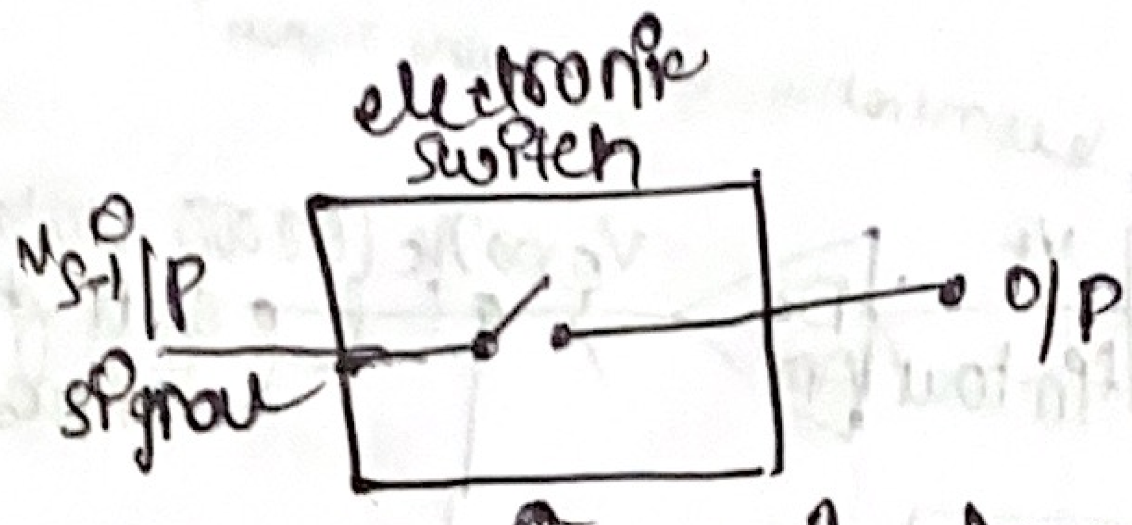


180° phase shift

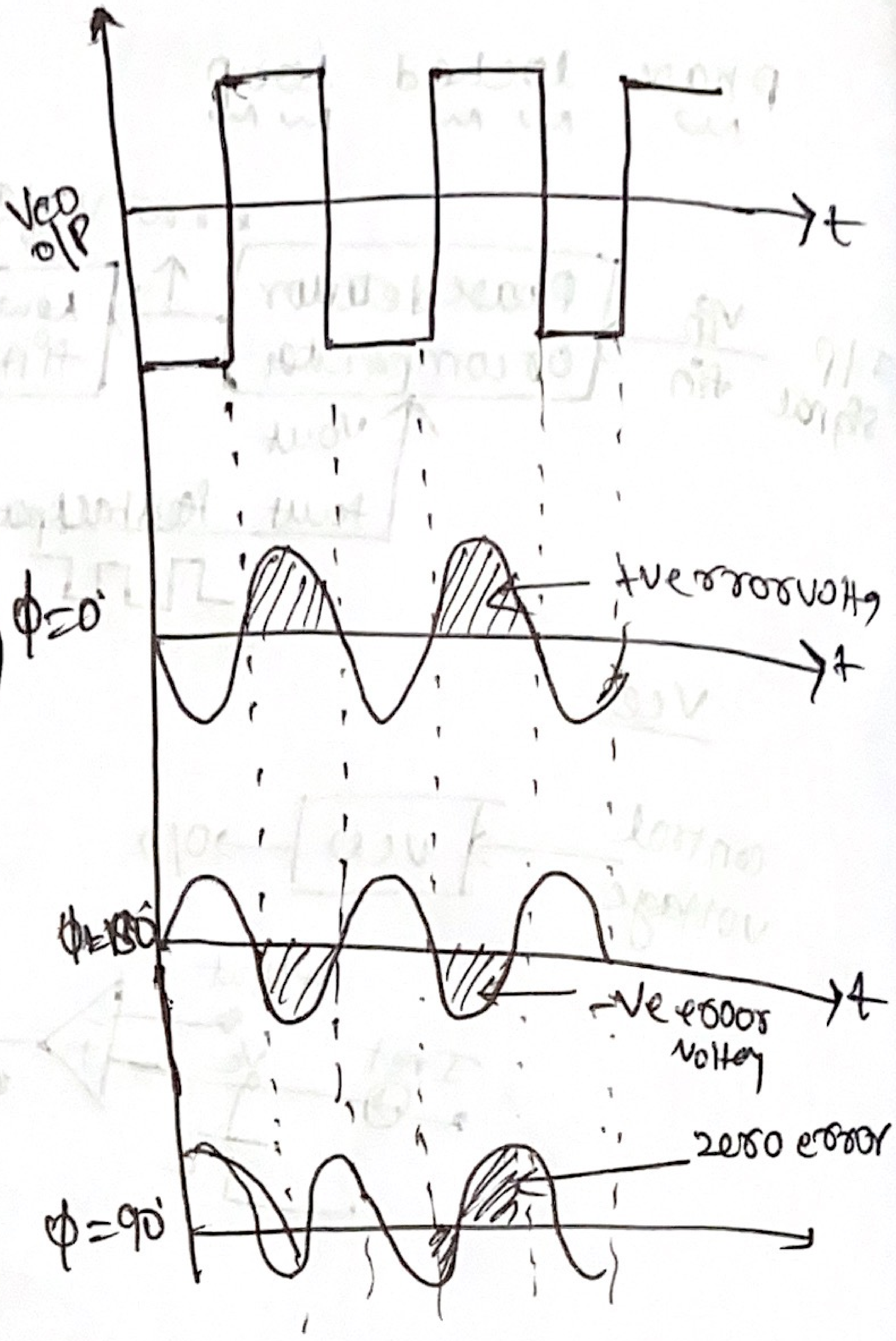


Draw back of XOR gate as not following wave, So XOR is not used alone.

② Analog phase Detector:



$\frac{1}{V_0}$ drive from VCO:



→ +ve half cycle of VCO the switch will be off.

→ -ve half cycle the VCO switch will be on.

$\boxed{f_{out} = \text{VCO o/p freq}}$

4/5/22

$V_S = V_S \sin(2\pi f_{in} t)$

$V_0 = V_0 \sin(2\pi f_{out} t + \phi)$

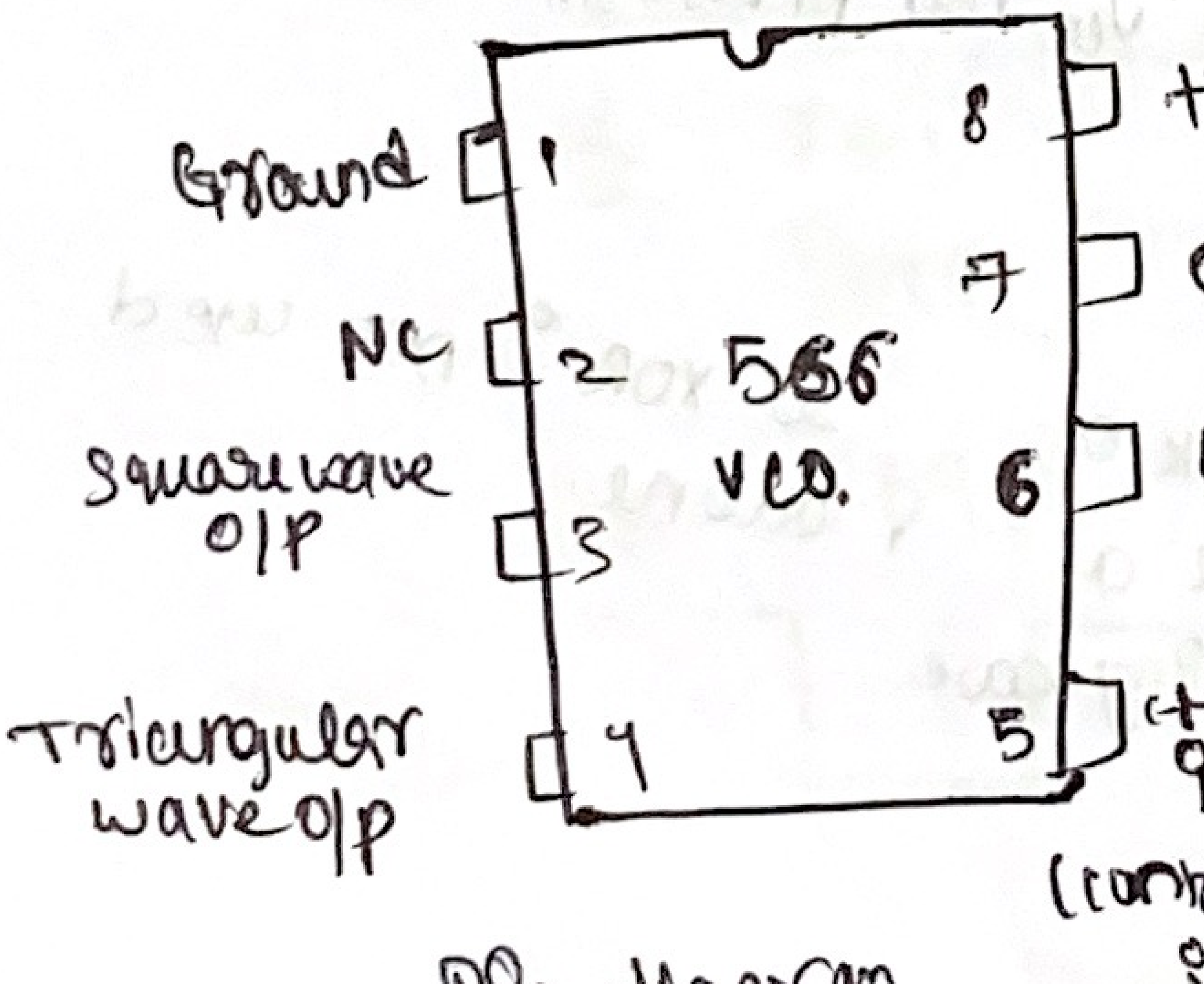
$V_e = K V_S V_0 \sin(2\pi f_{in} t) \times \sin(2\pi f_{out} t + \phi)$

Phase detector O/p → $V_e = \frac{K V_S V_0}{2} [\cos(2\pi f_{in} - 2\pi f_{out} t - \phi) - \cos(2\pi f_{in} + 2\pi f_{out} t + \phi)]$

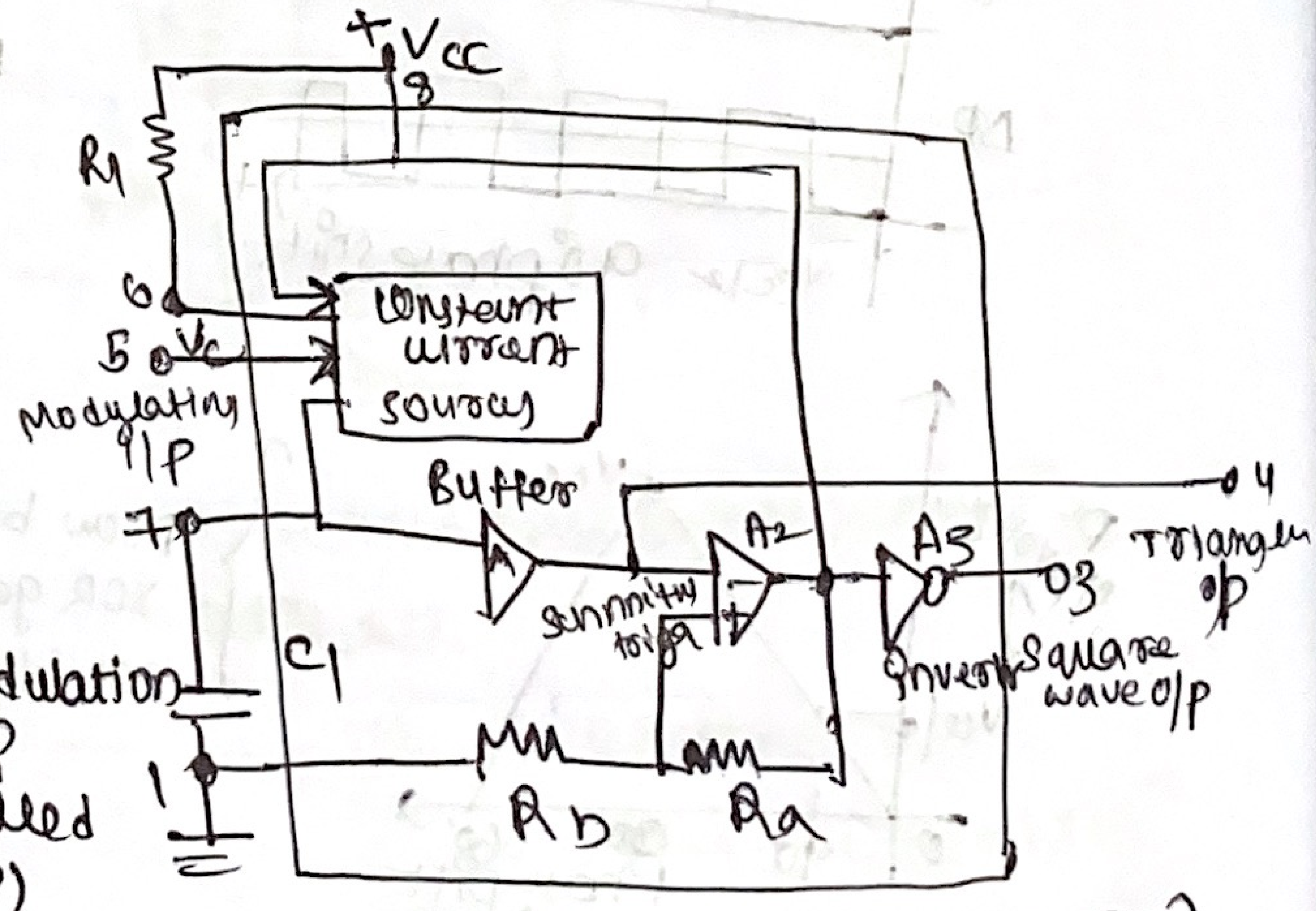
$f_{in} = f_{out}$ = lock stage.

$V_e = \frac{K V_S V_0}{2} [\cos(-\phi) - \cos(2\pi \times 2 f_{in} t + \phi)]$.

VCO



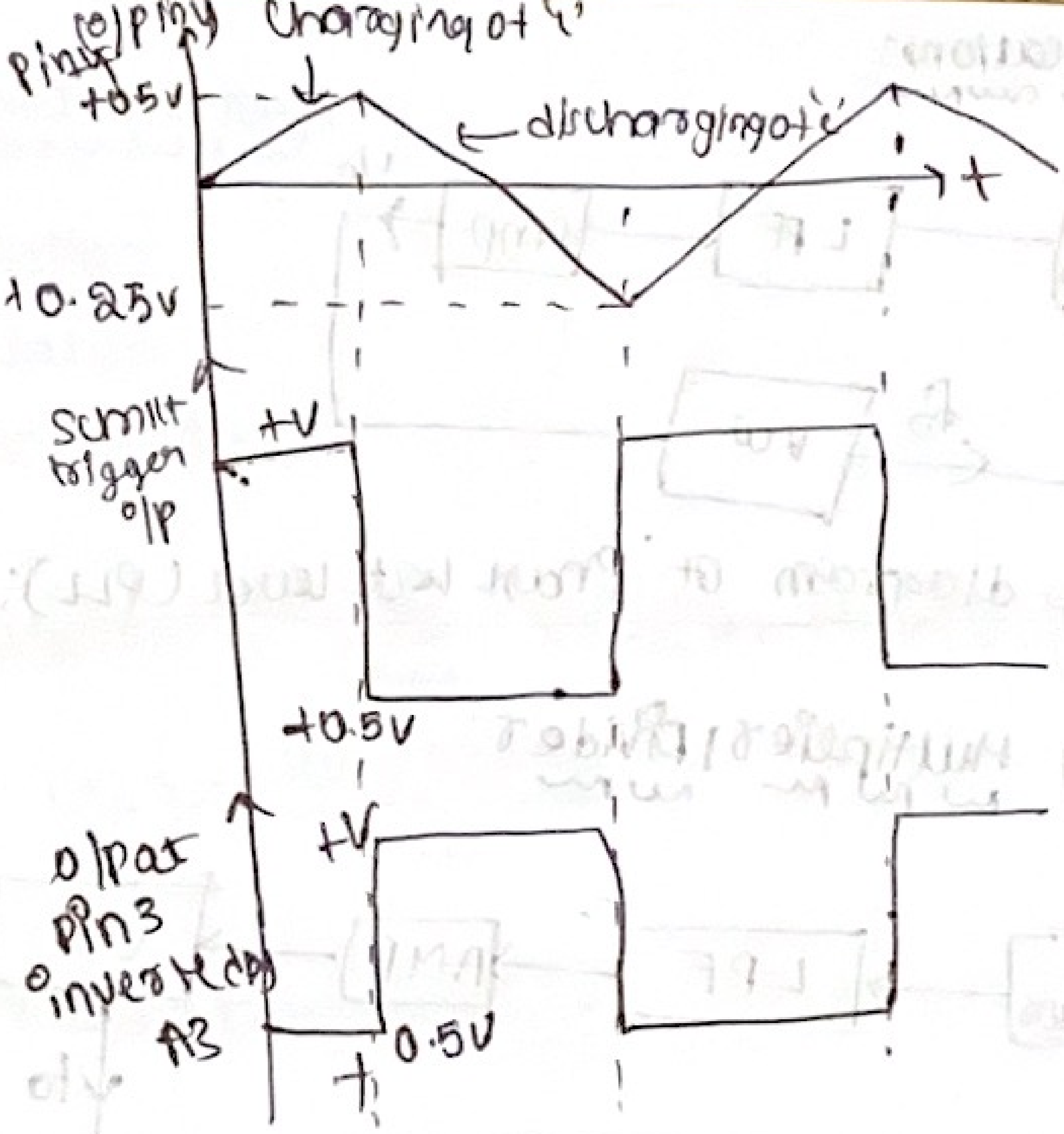
Pin diagram



Block diagram (566 VCO)

→ 566 VCO is most commonly used VCO.

o/p wave form:



Output frequency of VCO (f_o):

$$\Delta V_c = 0.25V_{cc}$$

$$\frac{\Delta V_c}{\Delta t} = \frac{i}{C_1} \text{ (capacitor voltage with const. current source).}$$

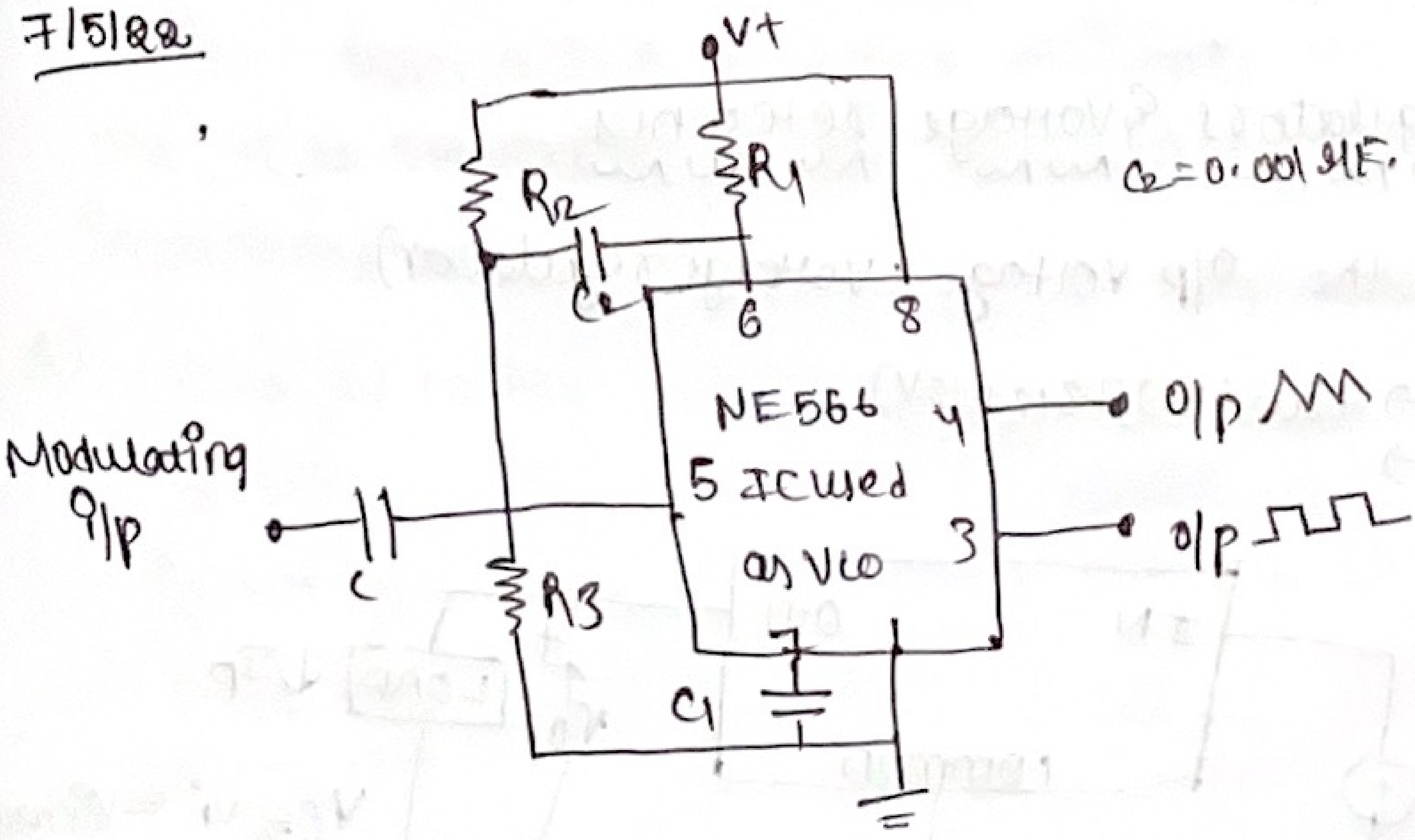
$$\frac{0.25V_{cc}}{\Delta t} = \frac{i}{C_1} \Rightarrow \Delta t = \frac{0.25V_{cc}C_1}{i}$$

$$T = 2\Delta t \Rightarrow f_o = \frac{1}{T} = \frac{1}{2\Delta t}.$$

$$f_o = \frac{i}{0.5V_{cc}C_1} \Rightarrow \boxed{f_o = \frac{2(V_{cc}-V_c)}{C_1R_1V_{cc}}}$$

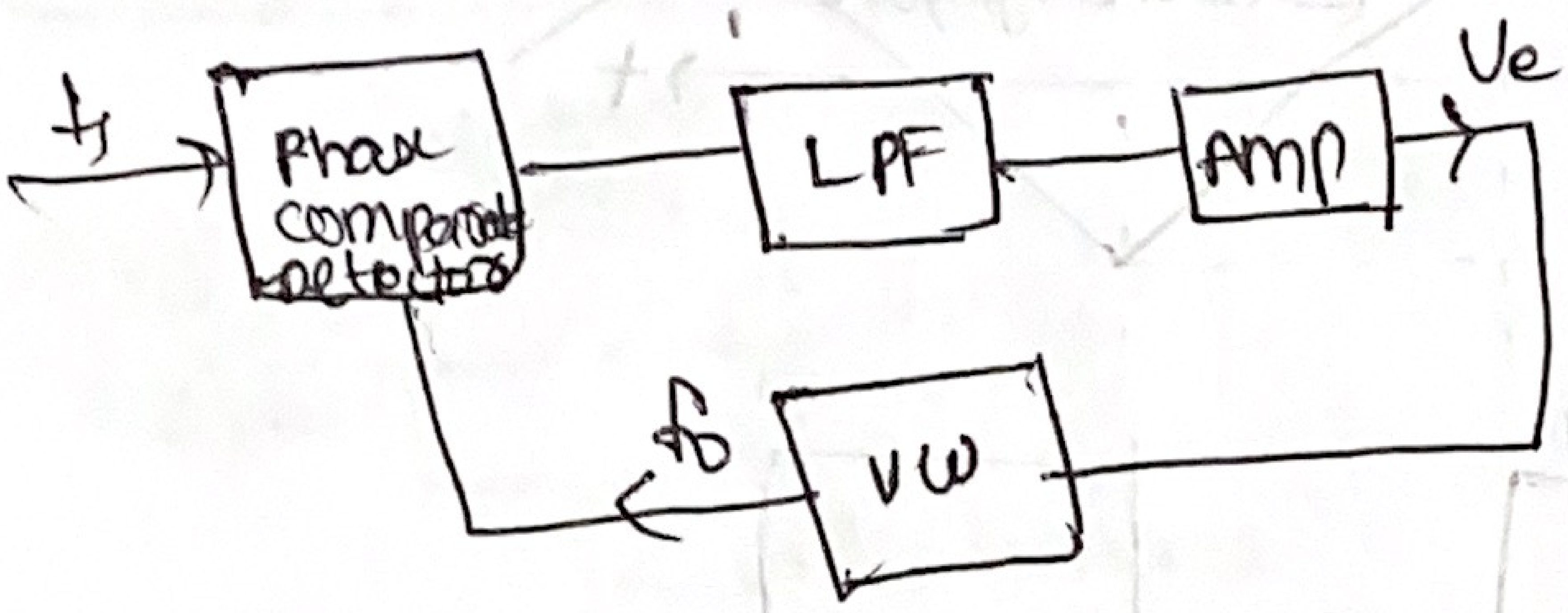
$$i = \frac{V_{cc}-V_c}{R_1}$$

7/5/22



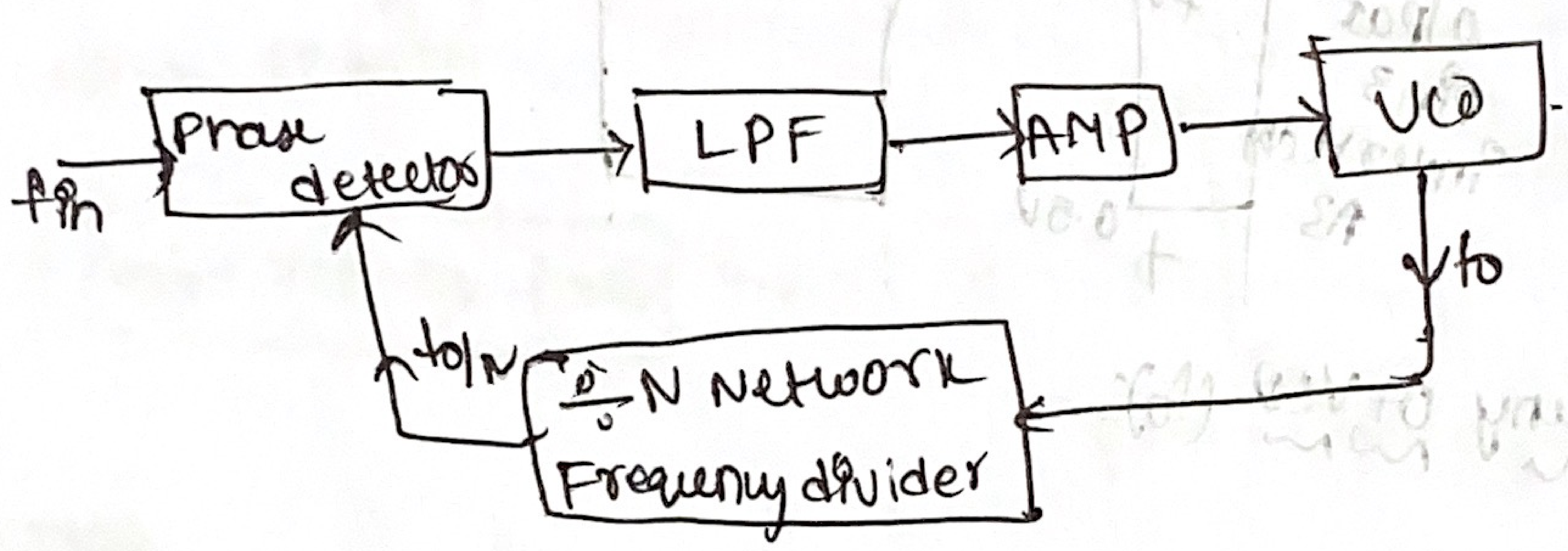
Typical connection diagram.

PLL Applications:

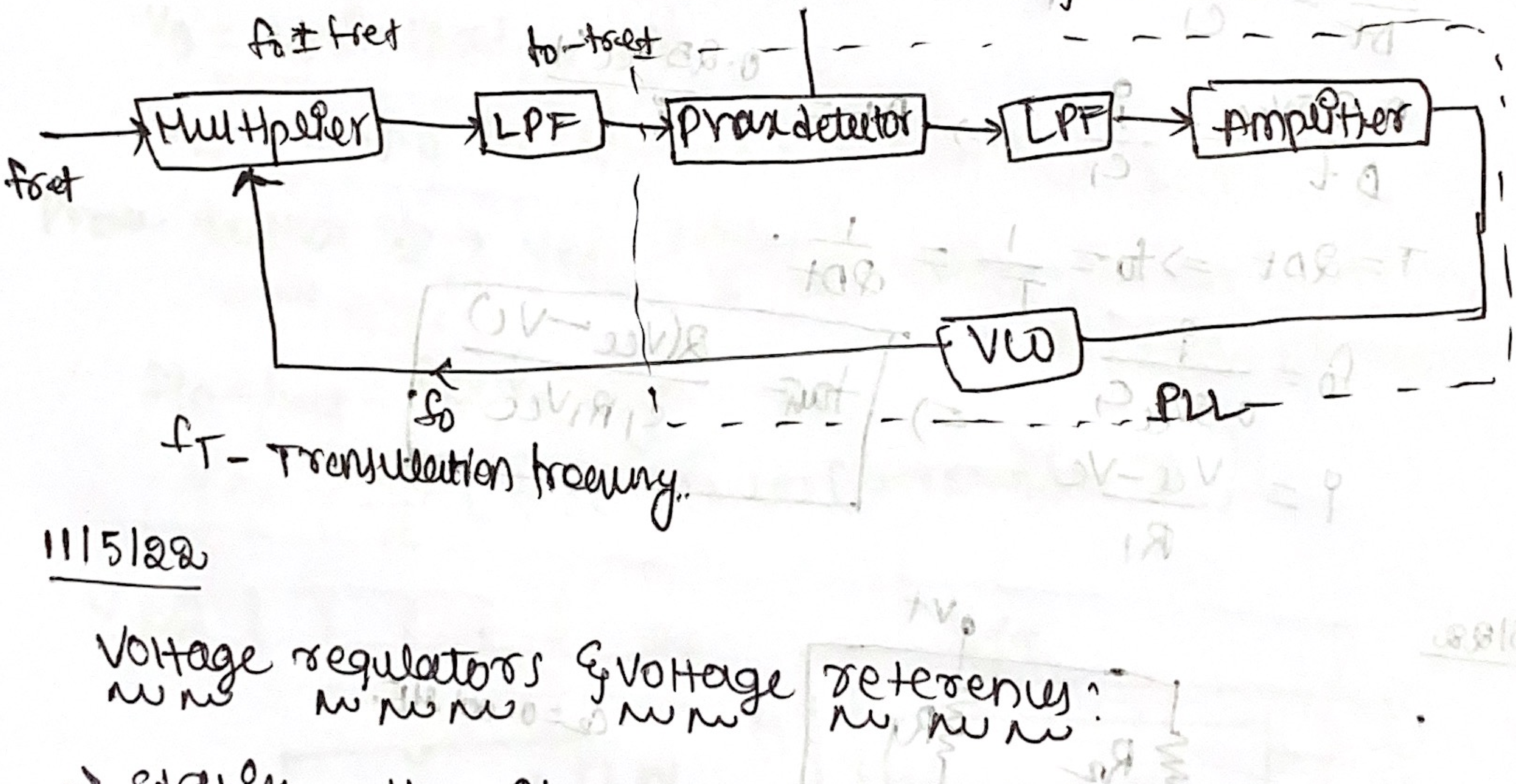


Block diagram of Phase lock level (PLL):

Frequency Multiplier / Divider:



Frequency Translation: f_T (frequency shifter).



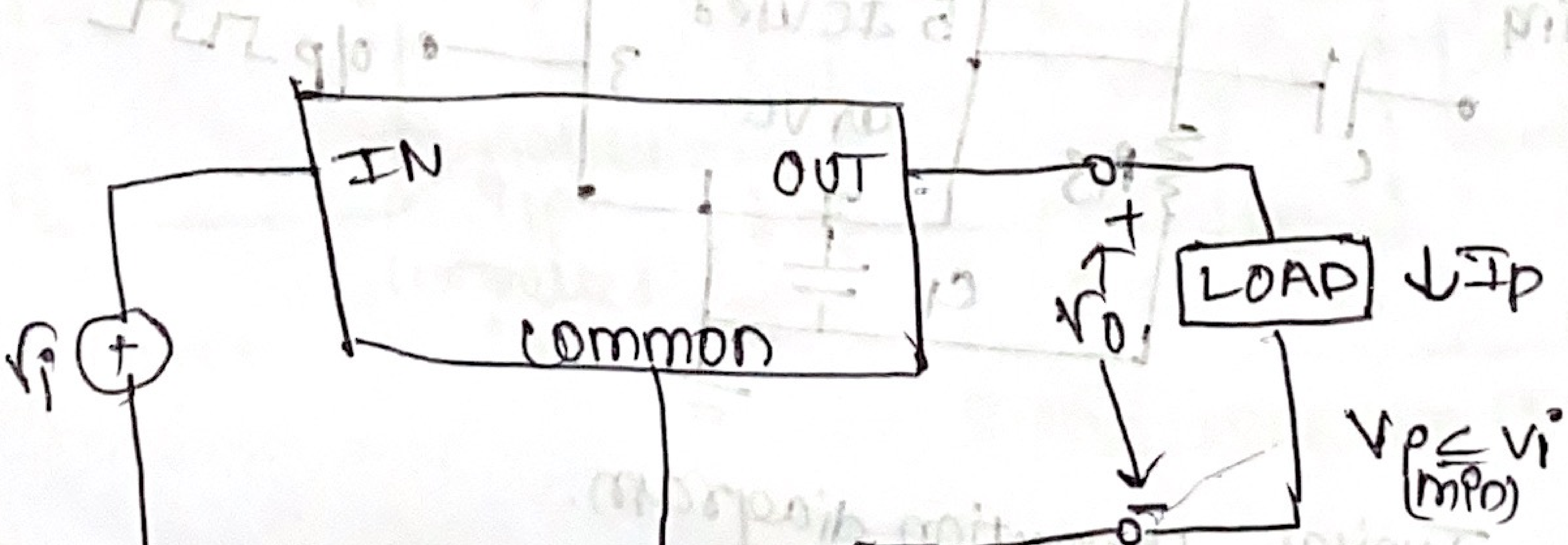
f_T - Translation frequency.

11/5/22

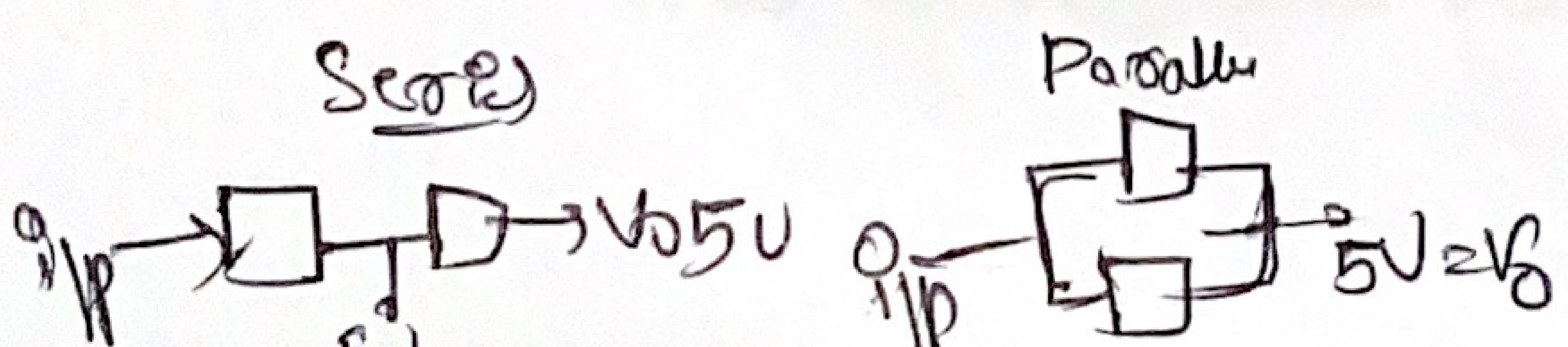
Voltage regulators & Voltage reference:

→ stabilize the o/p voltage (Voltage regulator).

LM78XX → 7805 (5V), 7812 (12V).
79XX →



$V_0 \le V_i \le V_{i(max)}$
(MPO)



Performance specifications:

① line regulation
② Load Regulation.
③ thermal coefficient.

① Line regulation $= \frac{\Delta V_0}{\Delta V_i}$ (mV or μV) / V. [mV/V (or) μV/V].

$$(\%) = \frac{100 \times \Delta V_0 / V_0}{\Delta V_i}$$

② Load regulation $= \frac{\Delta V_0}{\Delta I_0}$ μV/A (or) mV/A.

$$(\%) = \frac{100 \times \Delta V_0 / V_0}{\Delta I_0}$$

③ Thermal coefficient ~~(TC)~~ $T_C(V_0) = \frac{\Delta V_0}{\Delta T}$ mV/°c (or) μV/°c

$$(\%) = 100 \times \frac{\Delta V_0 / V_0}{\Delta T}$$

$$= 10^6 \frac{\Delta V_0 / V}{\Delta T} \text{ ppm/°c}$$ (For changing to parts per million)

Q1) From the data sheet of μA7805, 5V voltage regulator indicates that V_0 typically changes by 3 mV when V_i is varied from 7V to 25V and by 5 mV when i_0 is varied from 0.25 A to 0.75 A estimate the line and the load regulation of the device also find the o/p impedance of regulator.

Impedance $(R_0) = \frac{V_0}{\Delta I_0} = \frac{5}{0.5}$

(R0) Impedance $= 10\,\Omega$.

A) $V_i \rightarrow 7V$ to $25V$

$V_0 \rightarrow 5$

$i_0 \rightarrow 0.25$ A to 0.75

$\Delta V_0 = 3$ mV

$\Delta V_i = 18$ V

$\Delta V_0 \rightarrow 5$ mV (I_0).

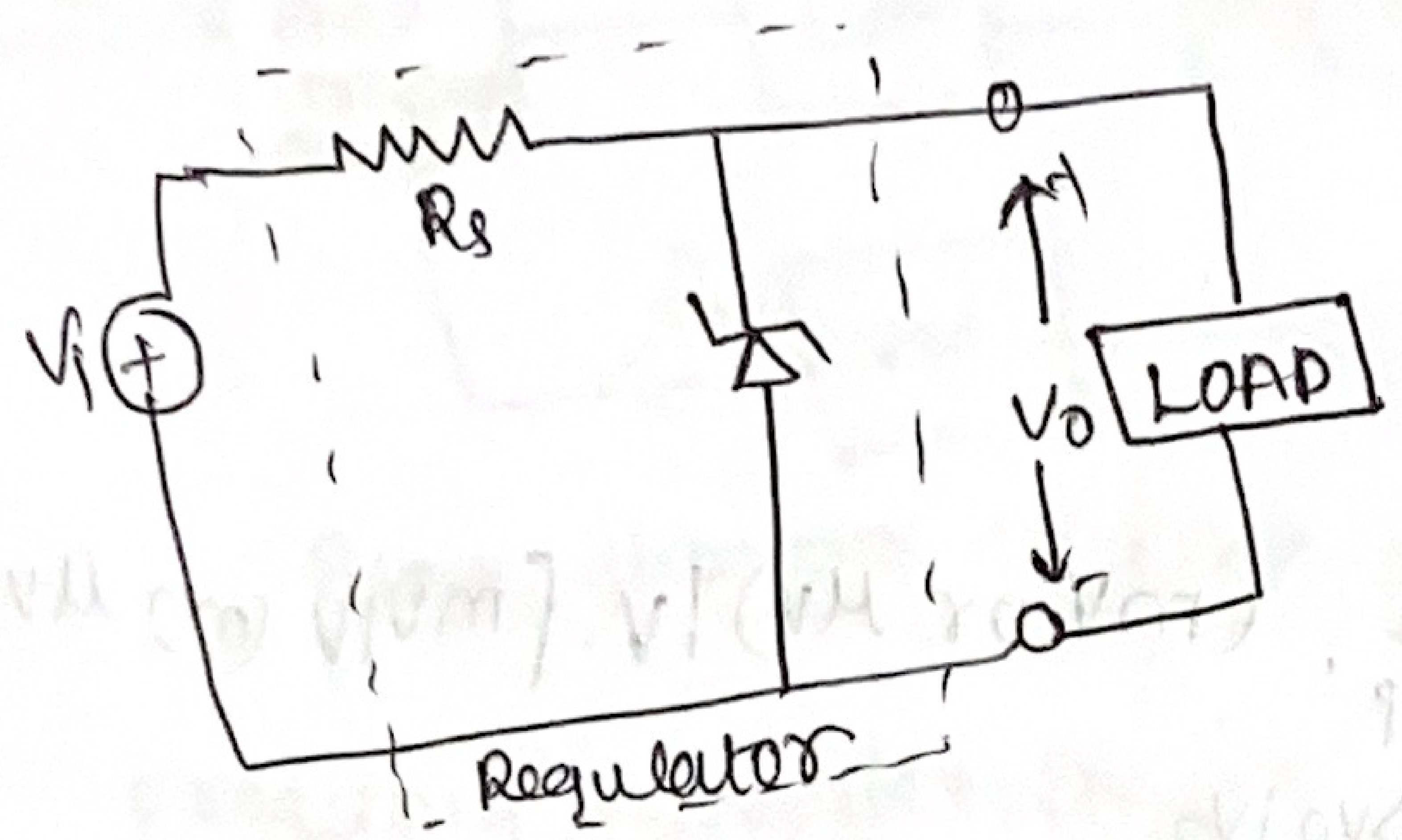
Line regulation $= \frac{3}{18} \times 10^{3}$

Line regulation $= 0.16 \frac{mV}{V}$

load $= \frac{\Delta V_0}{\Delta I_0} = \frac{5 mV}{0.50}$

load $= 10 \frac{mV}{A}$

Shunt regulator:



Q2) The Datasheet of REF101KM, 10V precision voltage reference gives a typical line regulation of 0.001%/V & typical load regulation of 0.001%/mA and a maximum thermal coefficient of 1ppm/°c. find the variation of V_o brough by ① ~~[illegible]~~ change of V_i from 13.5V to 35V,

① ± 1mV

② 1mA

③ 0.7mV

② ±10mA change in I_o.

③ Temparature change from 0°c to 70°c

Ans)

$V_o = 10V$

(i) $\Delta V_i = 21.5V$

$$0.001 = \frac{100 \times \frac{\Delta V_o}{10}}{21.5}$$

$$\Rightarrow \Delta V_o = 2.15mV$$

(ii) $$\frac{0.001}{10^{-3}} = \frac{100 \times \frac{\Delta V_o}{10}}{10}$$

$$\Delta V_o = 1mV$$

(iii) $\Delta T = 70°C$

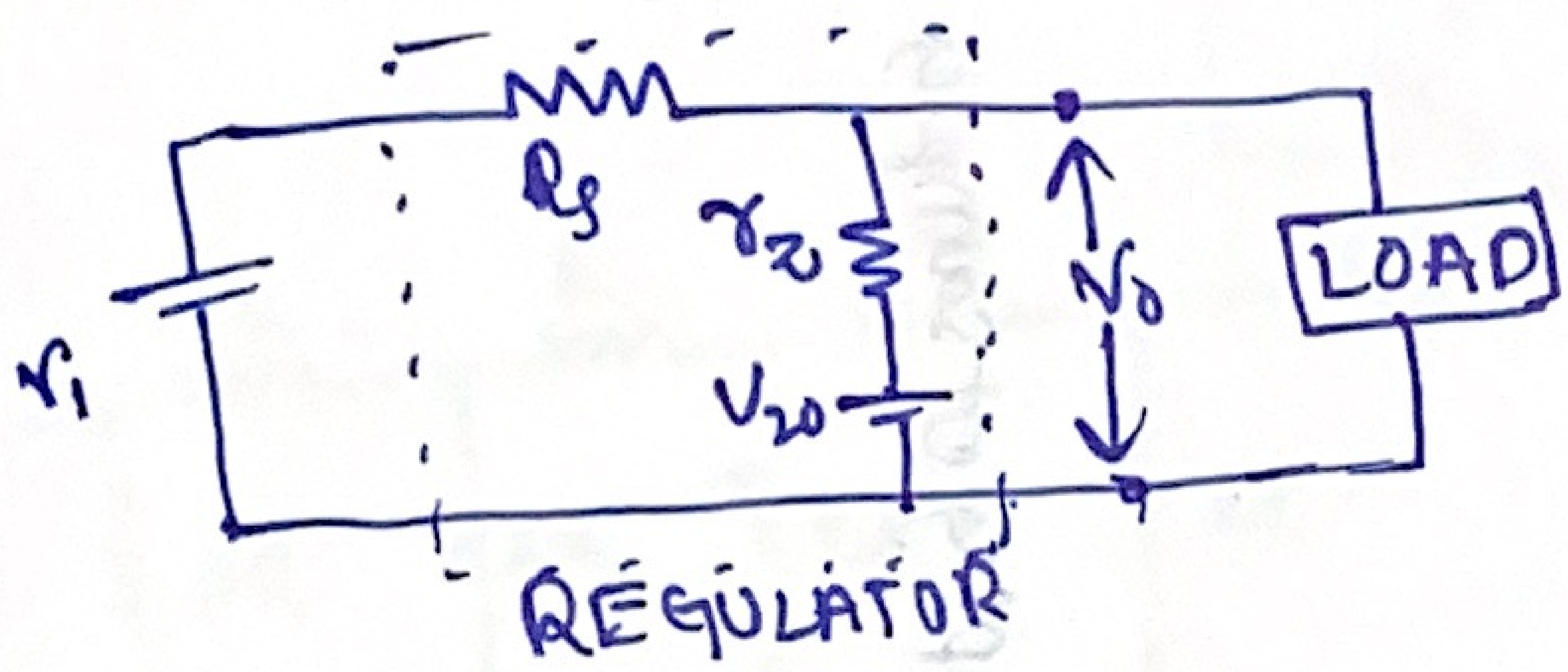
$$1 = 10^6 \times \frac{\Delta V_o / V_o}{\Delta T}$$

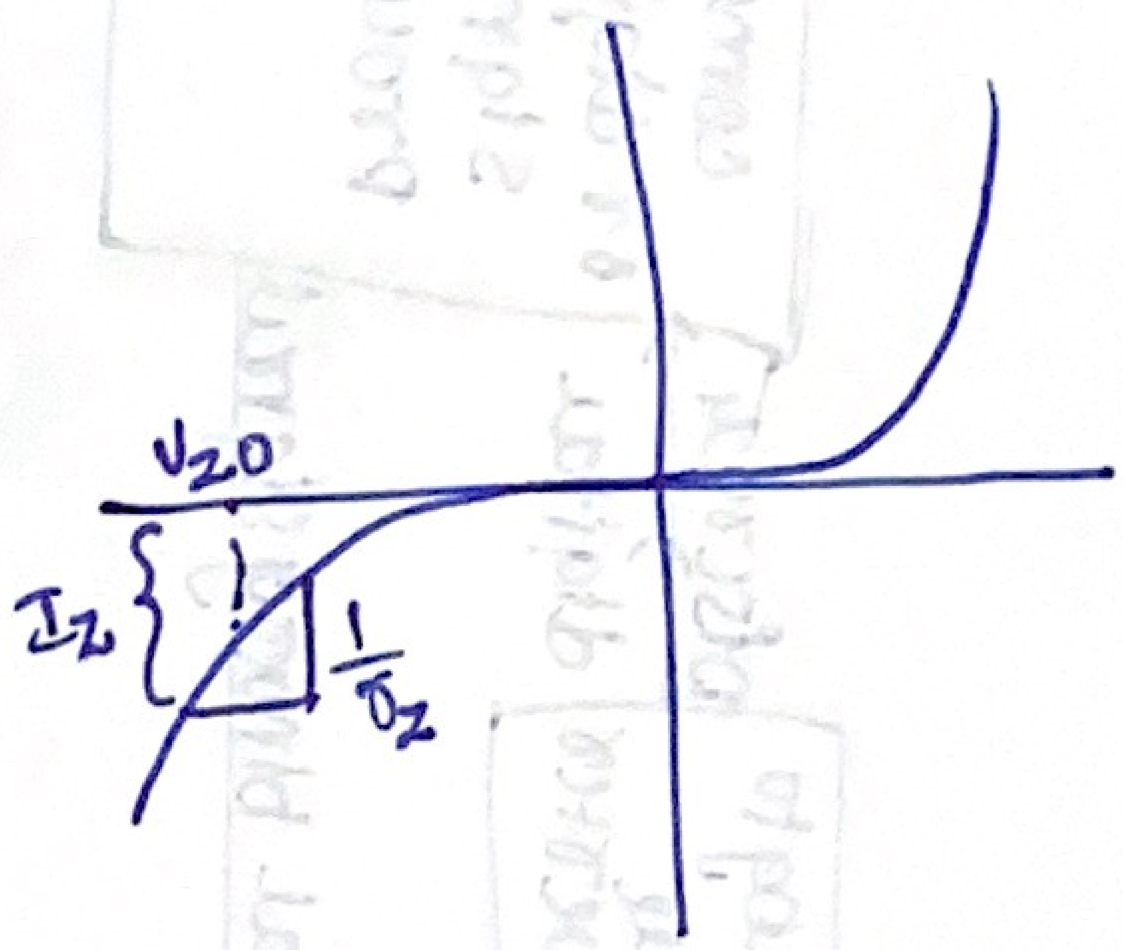
$$1 = 10^6 \times \frac{\frac{\Delta V_o}{10}}{70}$$

$$\frac{70}{10^5} = \Delta V_o \Rightarrow \Delta V_o = 0.7mV.$$

25-5-22

Shunt regulator:





V_z - zener voltage

$\boxed{V_z = V_{z0} + I(r_z) \cdot V_{r_z}}$

$V_o = V_{z0} + r_z I_z$

$V_{z0} = V_z - r_z I_z$.

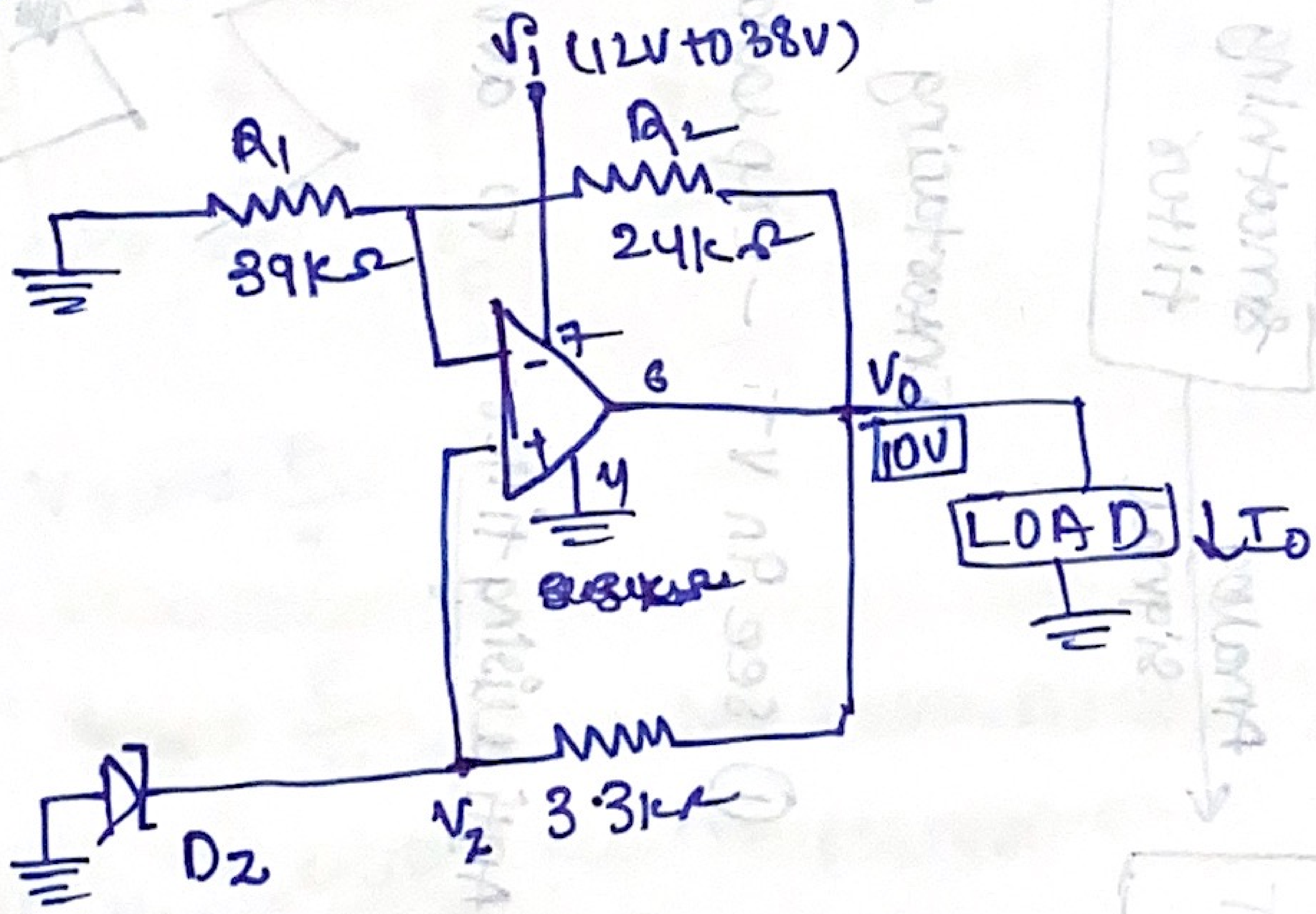
$V_{z0} = 5.43V$.

$$I_z = \left(\frac{P_z}{2}\right) \Big/ V_z$$

$$\text{Line regulation} = \frac{\Delta V_o}{\Delta V_i}.$$

$$\text{load regulation} = \frac{\Delta V_o}{\Delta I_o}.$$

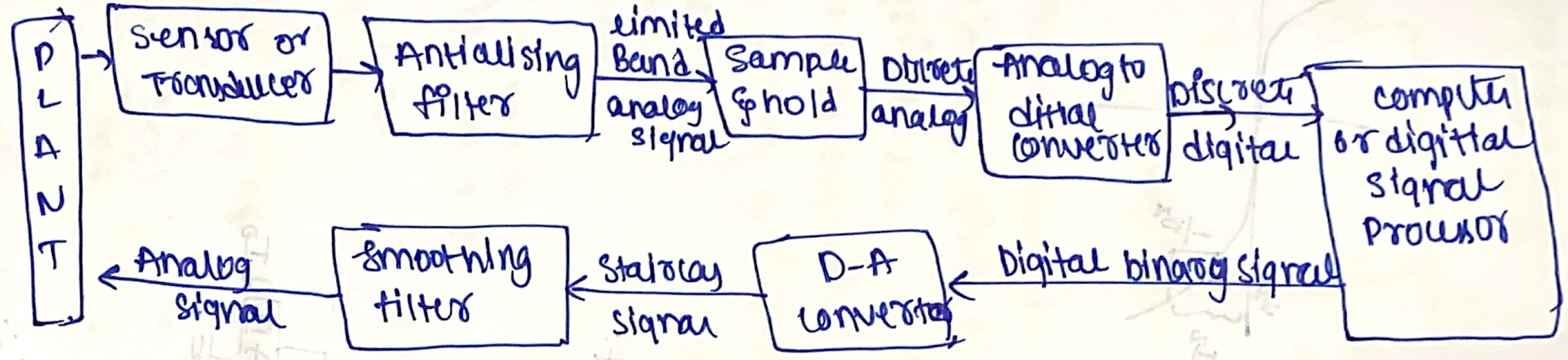
Self regulated 10V reference circuit:



$$V_o = \frac{r_z}{R_s + r_z} V_i + \frac{R_s}{R_s + R_z} V_{z0} - (R_s \| r_z) I_o$$

Load.

* 3m

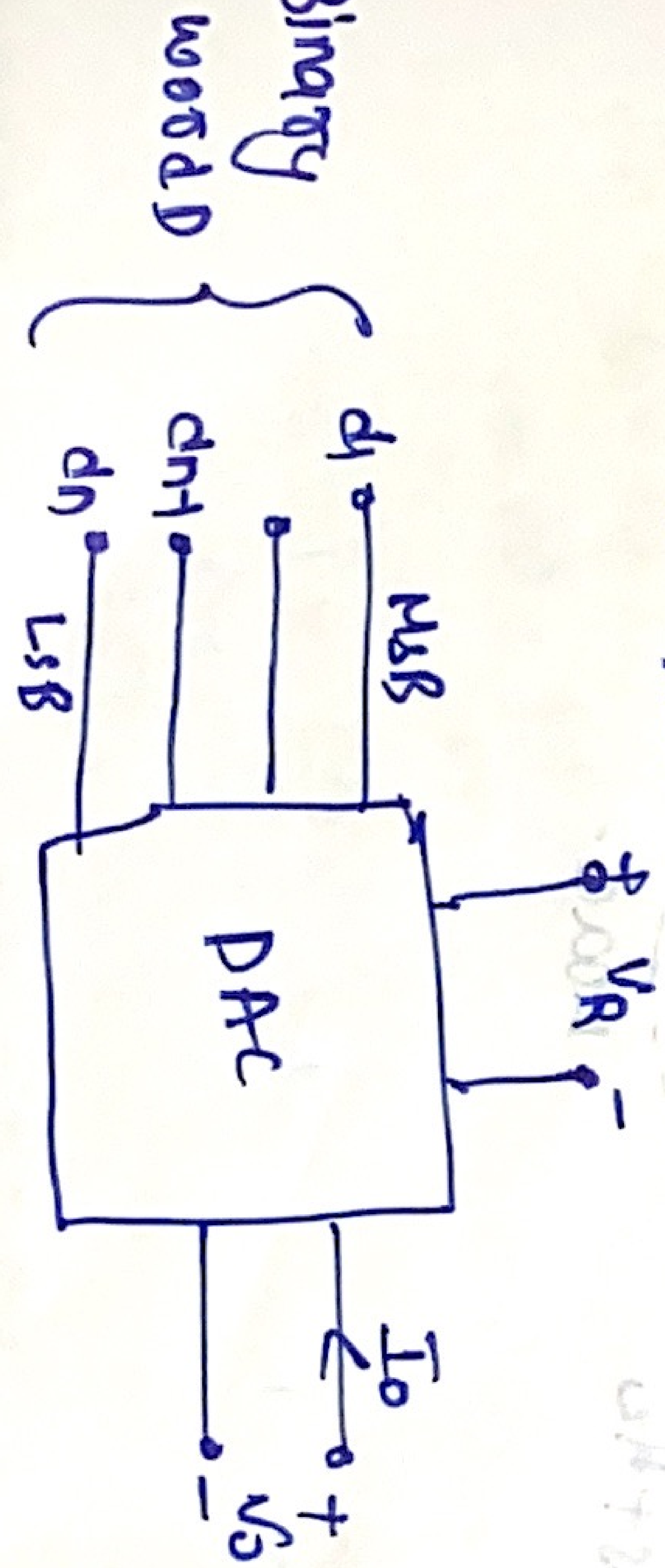


Interfacing a digital computer to the analog world.

① see 9n VT - explanation.

Antialising filter - to avoid loss of signals due to overlapping of samples

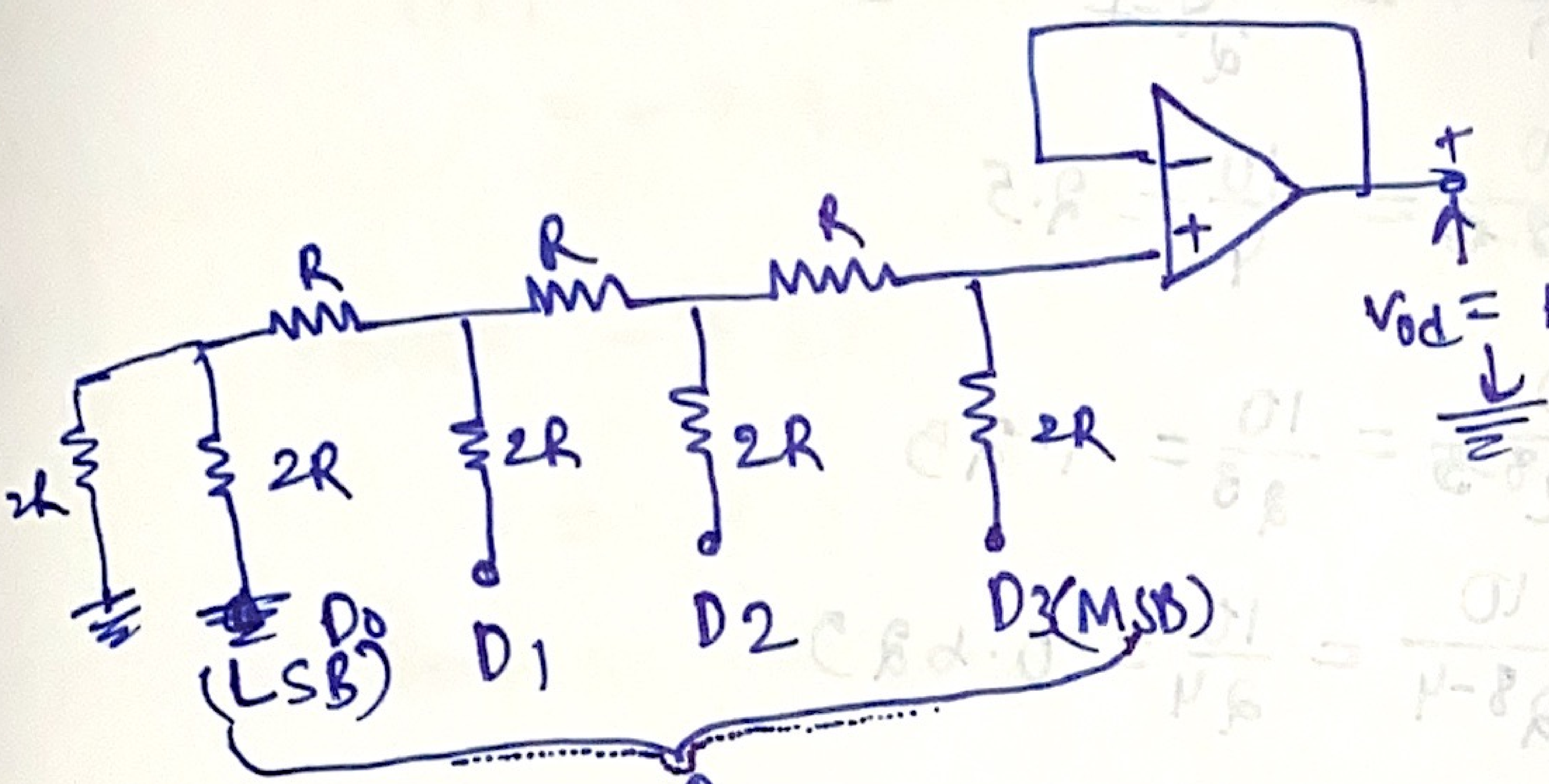
Schematic of DAC:



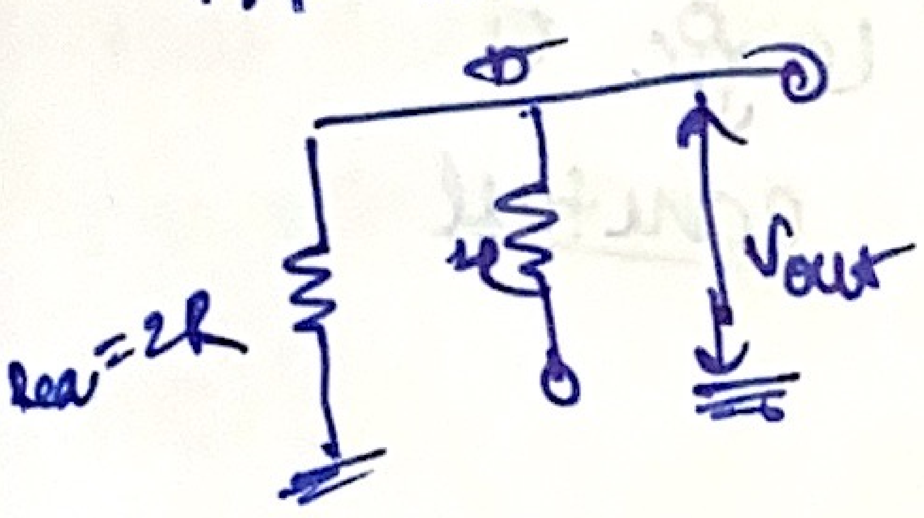
Voltage output $\propto$ input binary number.

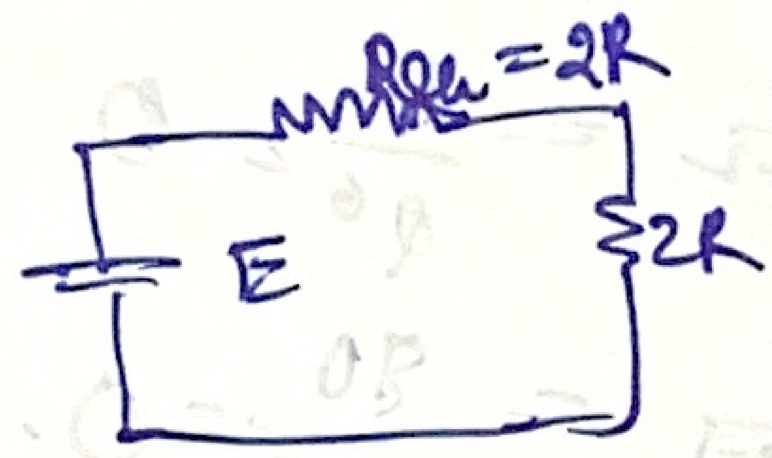
→ Analog output = K * digital output

R-2R Ladder type DAC:



i/p 1000



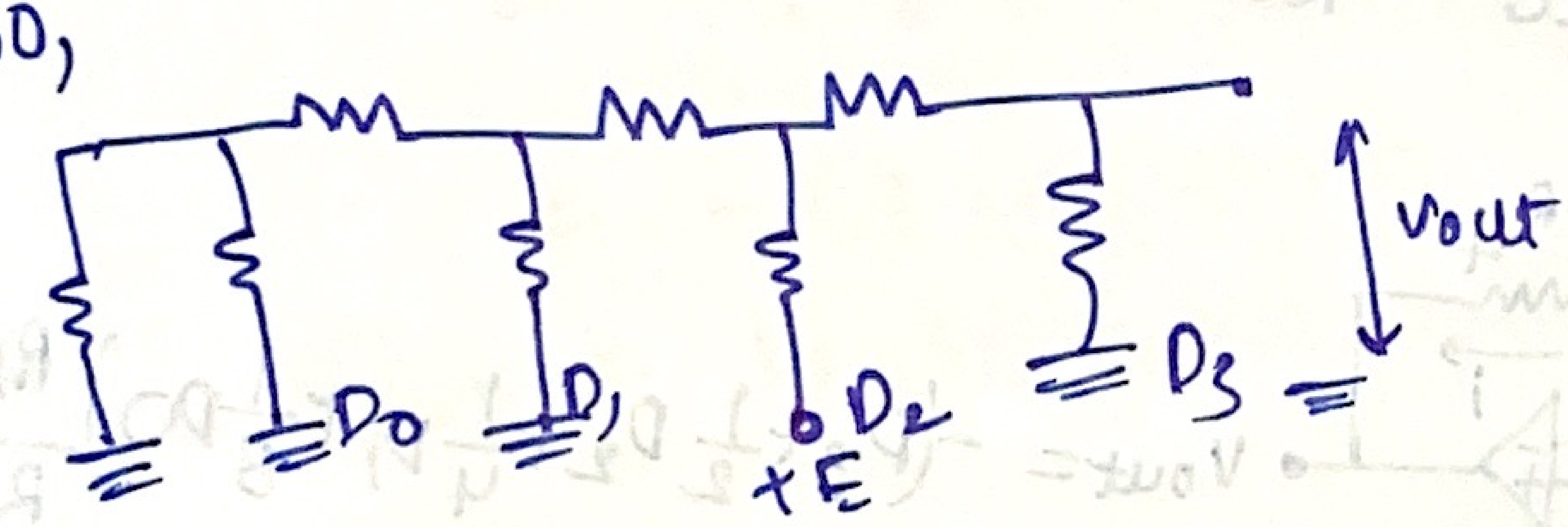


$V_{out} = E\left(\frac{2R}{2R+2R}\right) = \frac{E}{2}.$

H.W

① when i/p = 0100 ⎤
= 0010 ⎬ → V_{out} = ??
= 0001 ⎦

0100,



$V_{out} = \frac{E}{4}.$

0010, $V_{out} = \frac{E}{8}.$

0001, $V_{out} = \frac{E}{16}.$ N = total no. of binary bits

D_n bits, $V_{out} = \frac{E}{2^{N-n}}$ n = position of bit where i/p is high.

Eg: $D_3D_2D_1D_0$
0100

$V_{out} = \frac{5}{2^{4-2}} = \frac{5}{4}.$

Q1) what are the output voltages causes by logic 1 in each bit position in a R-2R ladder with input 1111 0001 if the input level for 0 is 0V and that for 1 is 10V?

Ans) $I/p = 11110001$.

$D_7 = V_{out} = \frac{E}{2^{N-n}} = \frac{10}{2^{8-7}} = 5$

$D_6 = V_{out} = \frac{10}{2^{8-6}} = \frac{10}{4} = 2.5$

$D_5 = V_{out} = \frac{10}{2^{8-5}} = \frac{10}{2^3} = 1.25$

$D_4 = V_{out} = \frac{10}{2^{8-4}} = \frac{10}{2^4} = 0.625$

$D_3 = V_{out} = \frac{\cancel{10}}{2^{8-3}} = \frac{\cancel{10}}{2^5} = 0$

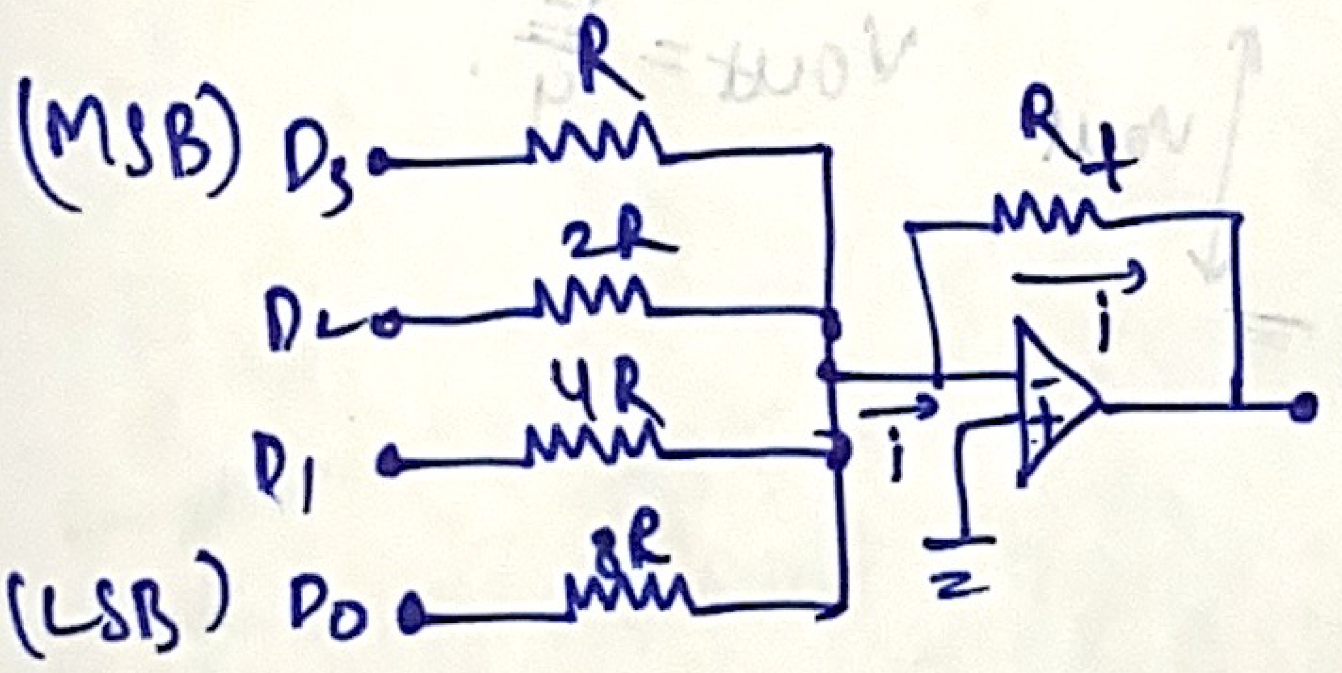
$D_2 = V_{out} = \frac{\cancel{10}}{2^{8-2}} = \frac{\cancel{10}}{2^6} = 0$

$D_1 = V_{out} = \frac{0}{2^{8-1}} = \frac{\cancel{10}}{2^7} = 0.$

Not asked for logic '0' careful

$D_0 = V_{out} = \frac{10}{2^8} = \frac{10}{256} = 0.0391$

Weighted resistor type DAC:



$V_{out} = -\left(D_3 + \frac{1}{2}D_2 + \frac{1}{4}D_1 + \frac{1}{8}D_0\right)\frac{R_f}{R}$

Q2) For the 4 bit weighted resistor DAC, determine (a) the weight of each input are 0V and 5V, (b) the full scale output, if $R_f = R = 1k\Omega$. Also, (c) find the scale output if R_f is changed to 500Ω.

A) (a) $\frac{R_f}{R} = 1$

D_3 = MSB → gain = 1 ⇒ weight = 5V

$V_{out} = \left(D_3 + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8}\right)\frac{R_f}{R}$

D_2 = gain = 1/2 ⇒ weight = 5/2 = 2.5V

D_1 = gain = 1/4 ⇒ weight = 5/4 = 1.25V

D_0 = gain = 1/8 ⇒ weight = (5/8) = 0.625V.

(b) Full scale o/p is when all i/p are high.

1111

$= -9.375V.$

(c) $V_{out} = -9.375 \times \frac{500\Omega}{1k\Omega}$

$= -9.375 \times 0.5$

$V_{out} = -4.6875V.$

Q5) Design a 4-bit weighted-resistor DAC whose full scale o/p voltage is -5V. The logic levels are 1 = +5V and 0 = 0V - What is o/p voltage when i/p is 1101?

A) $V_{out} = -\left(D_3 + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8}\right) \frac{R_f}{R}$

$= -(5 + 2.5 + 0 + 0.625) \times 0.53$

$= -(8.125) \times 0.53$

$V_{out} = -4.3V$

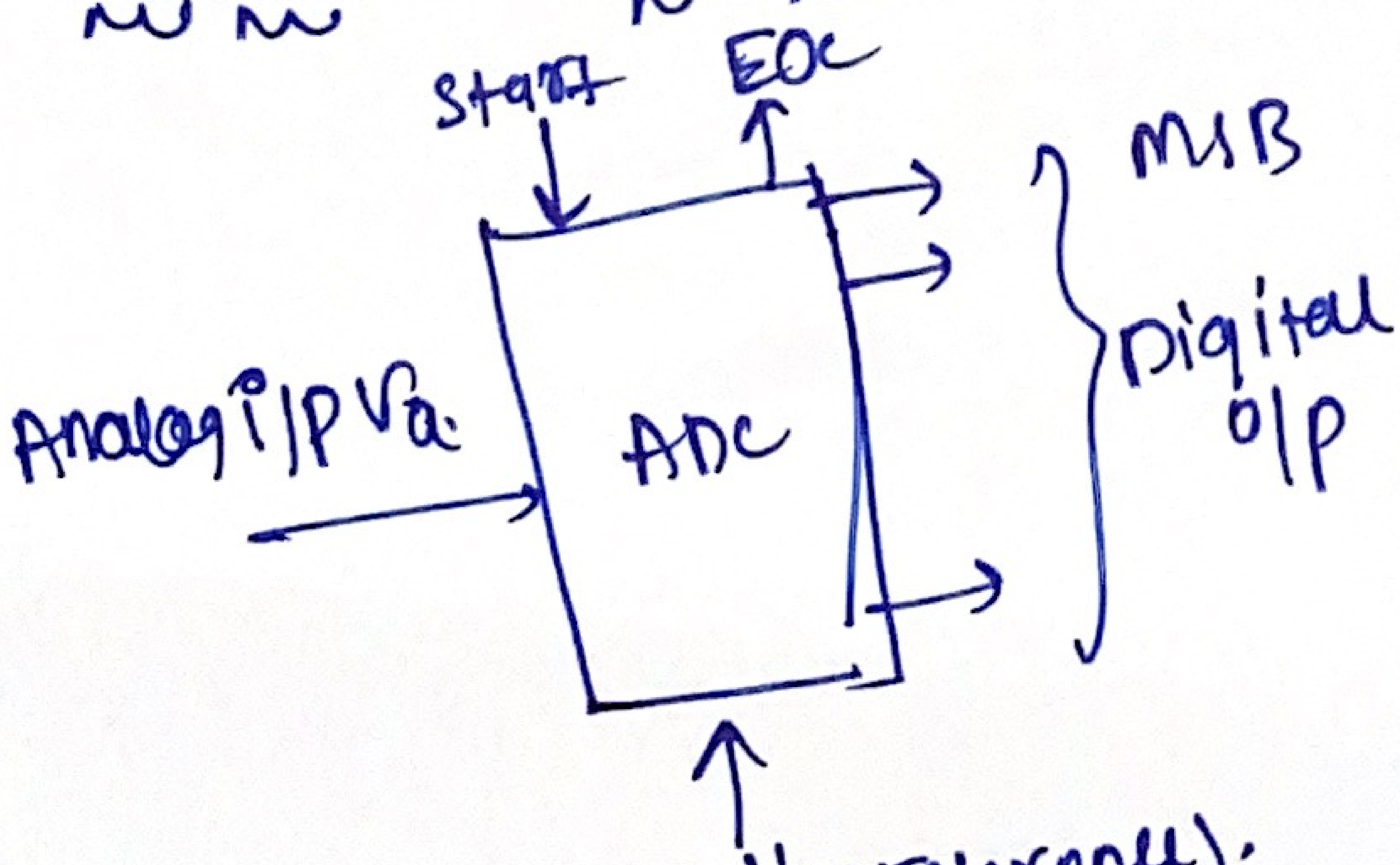
$-5 = -9.375 \times \frac{R_f}{R}$

$\frac{R_f}{R} = 0.53$

$R = 1k\Omega$

$R_f = 530\Omega$

Schematic of DAC:



Classification Based on their conversion Techniques

Direct type DAC:

- compare a given analog signal with the internally generated equivalent.
-

Integrating type ADC:

- Performs a conversion in a indirect manner by 1st changing the analog i/p signal to a linear function of time or freq & then to a digital code.

A) Counter type ADC: