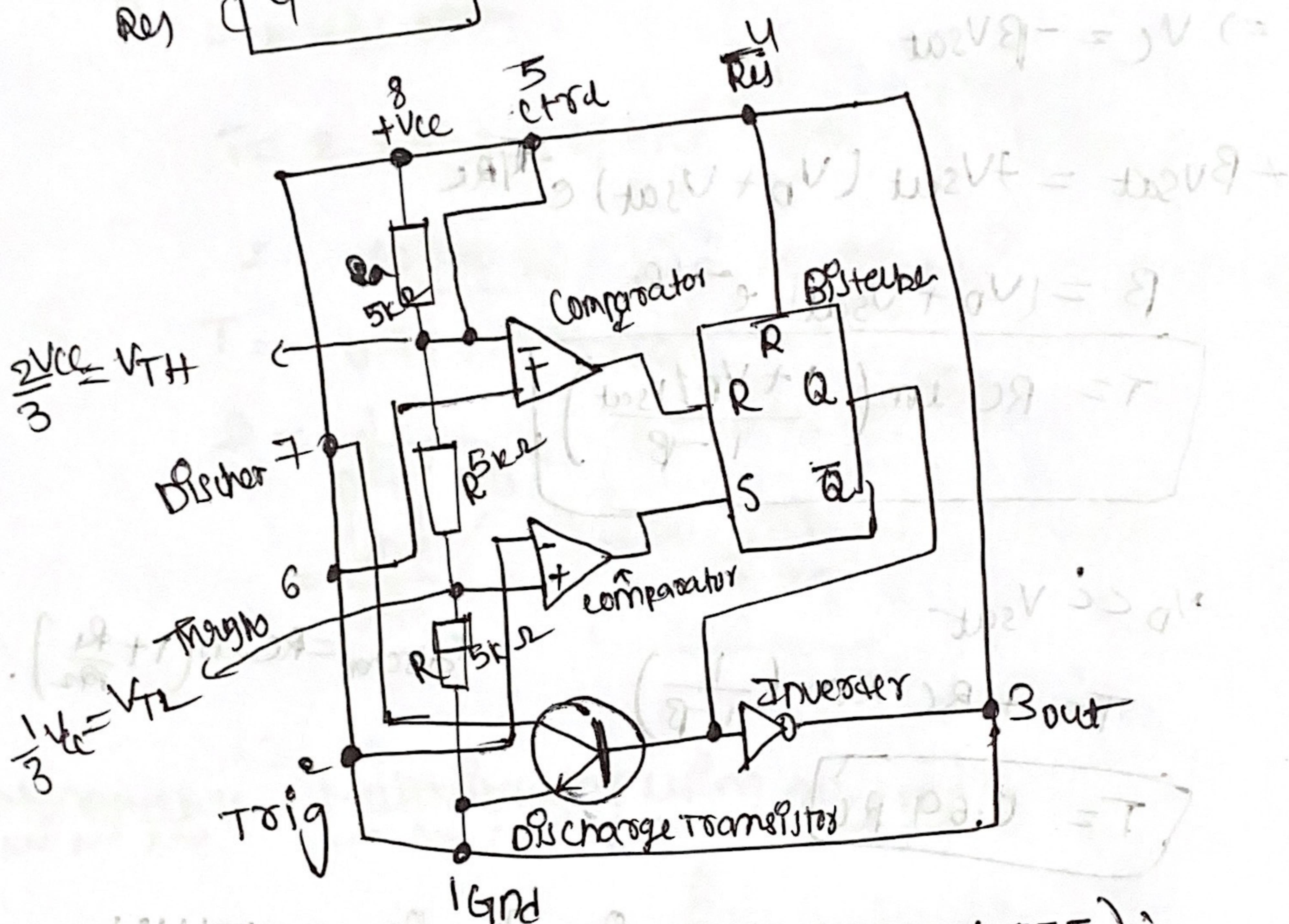
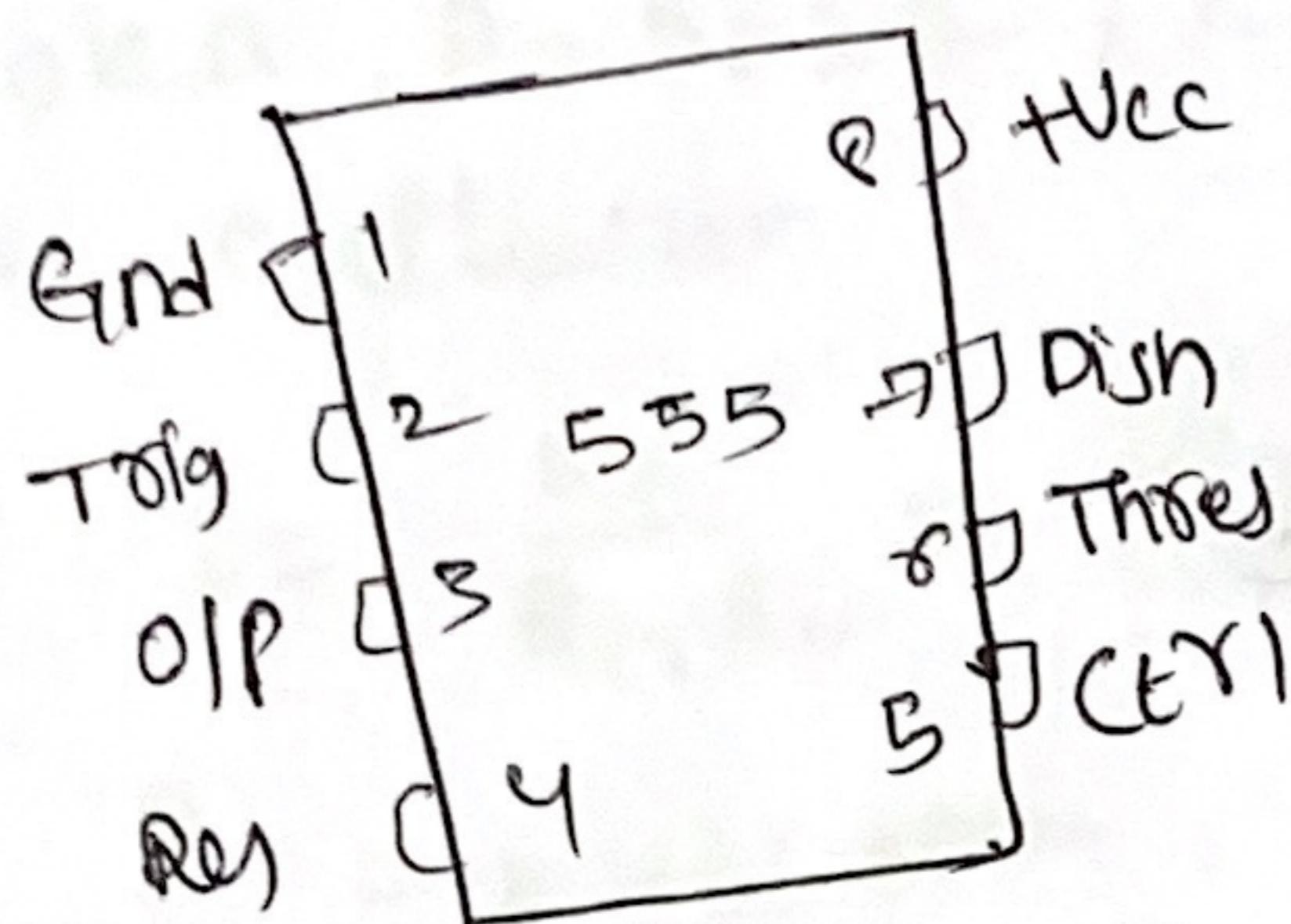


## 555 timer

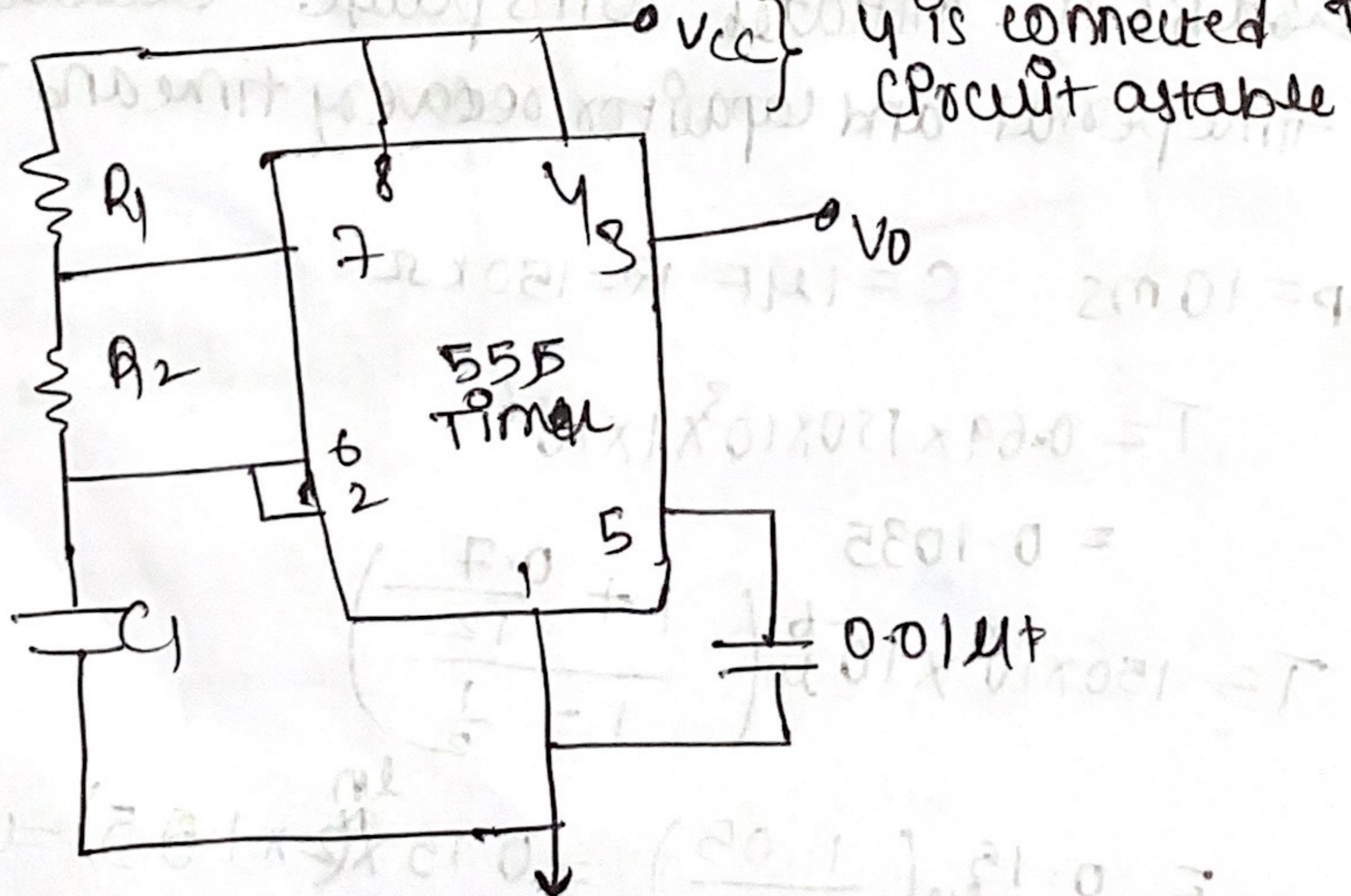
### Pin diagram



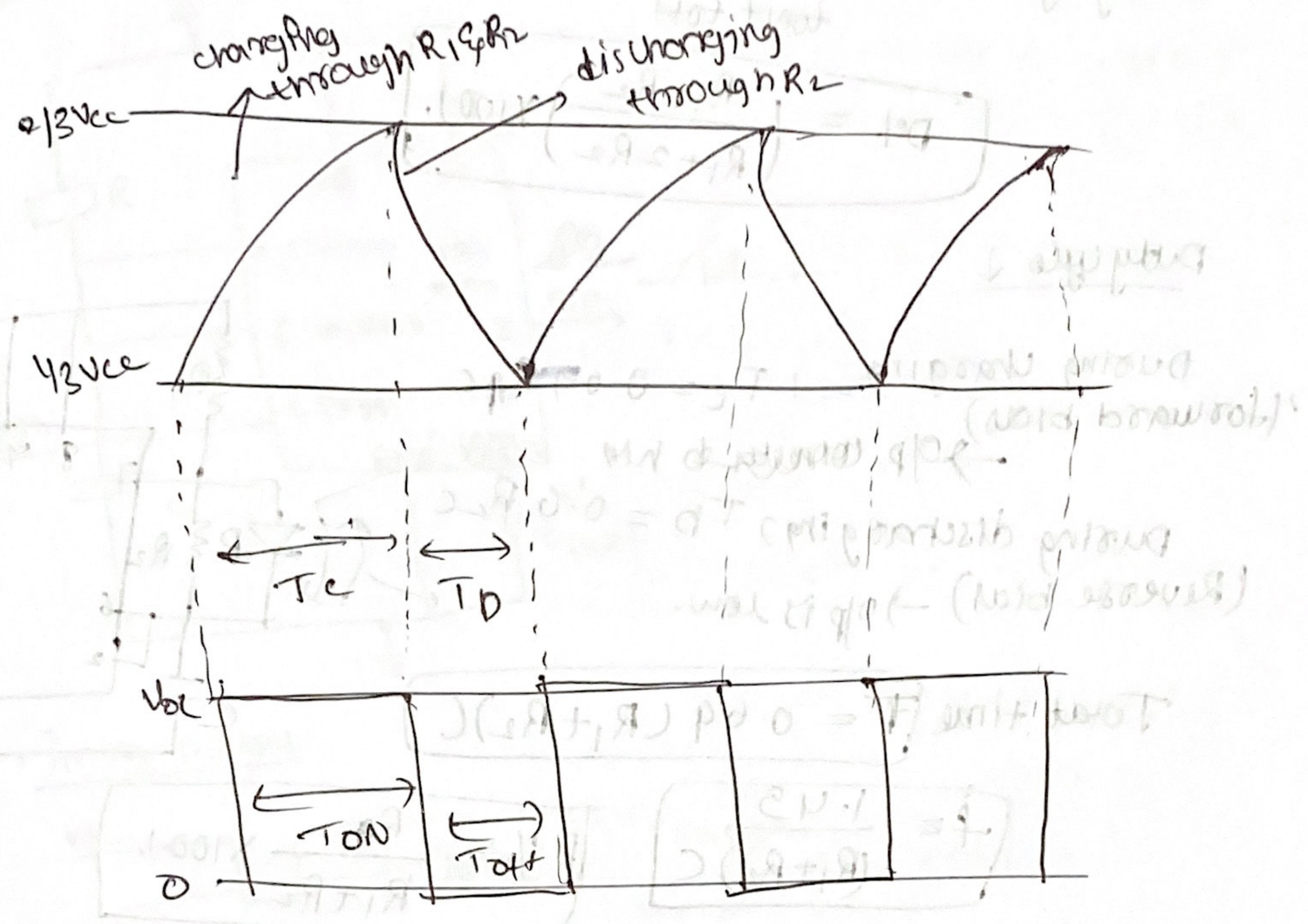
Block diagram of timer(555):

A Stable Multivibrator using 555 timer:

$V_{CC}$  is connected to make circuit astable Multivibrator.



23/4/22



Derivation for expression of duty cycle:

$$V_C = V_{CC} (1 - e^{-t_1/RC})$$

$\rightarrow t_1$  taken by the circuit to charge from  $0 \rightarrow \frac{2}{3} V_{CC}$  ( $0 \rightarrow V_{TH}$ )

$$V_C = \frac{2}{3} V_{CC} = V_{CC} (1 - e^{+t_1/RC})$$

$$1 - \frac{2}{3} = e^{+t_1/RC}$$

$$t_1 = RC \ln \frac{1}{\frac{1}{3}}$$

$$t_1 = 1.09 RC$$

$$t_{ON} = t_1 - t_L$$

$$t_{ON} = 0.69 RC$$

$$t_{ON} = 0.69(R_1 + R_2)C$$

$\rightarrow t_2$  to charge from  $0 \rightarrow 1/3 V_{CC}$

$$V_C = \frac{1}{3} V_{CC} = V_{CC} (1 - e^{-t_2/RC})$$

(Charging time).

$$\frac{1}{3} = \frac{RC}{t_2} \ln \frac{1}{\frac{1}{3}}$$

$$t_2 = 0.40 RC$$

$\rightarrow$  Discharging time,

$$\frac{1}{3} V_{CC} = \frac{2}{3} V_{CC} e^{-t_3/RC}$$

$$t_3 = 0.69 R_2 C$$

$$T = t_{ON} + t_{OFF}$$

$$T = 0.69(R_1 + 2R_2)C$$

$$f = \frac{1.45}{(R_1 + 2R_2)C}$$

frequency.

$$\text{Duty cycle (D)} \% = \frac{\text{ton}}{\text{ton} + \text{toff}} \times 100\%.$$

$$D\% = \left( \frac{R_1 + R_2}{R_1 + 2R_2} \right) \times 100\%,$$

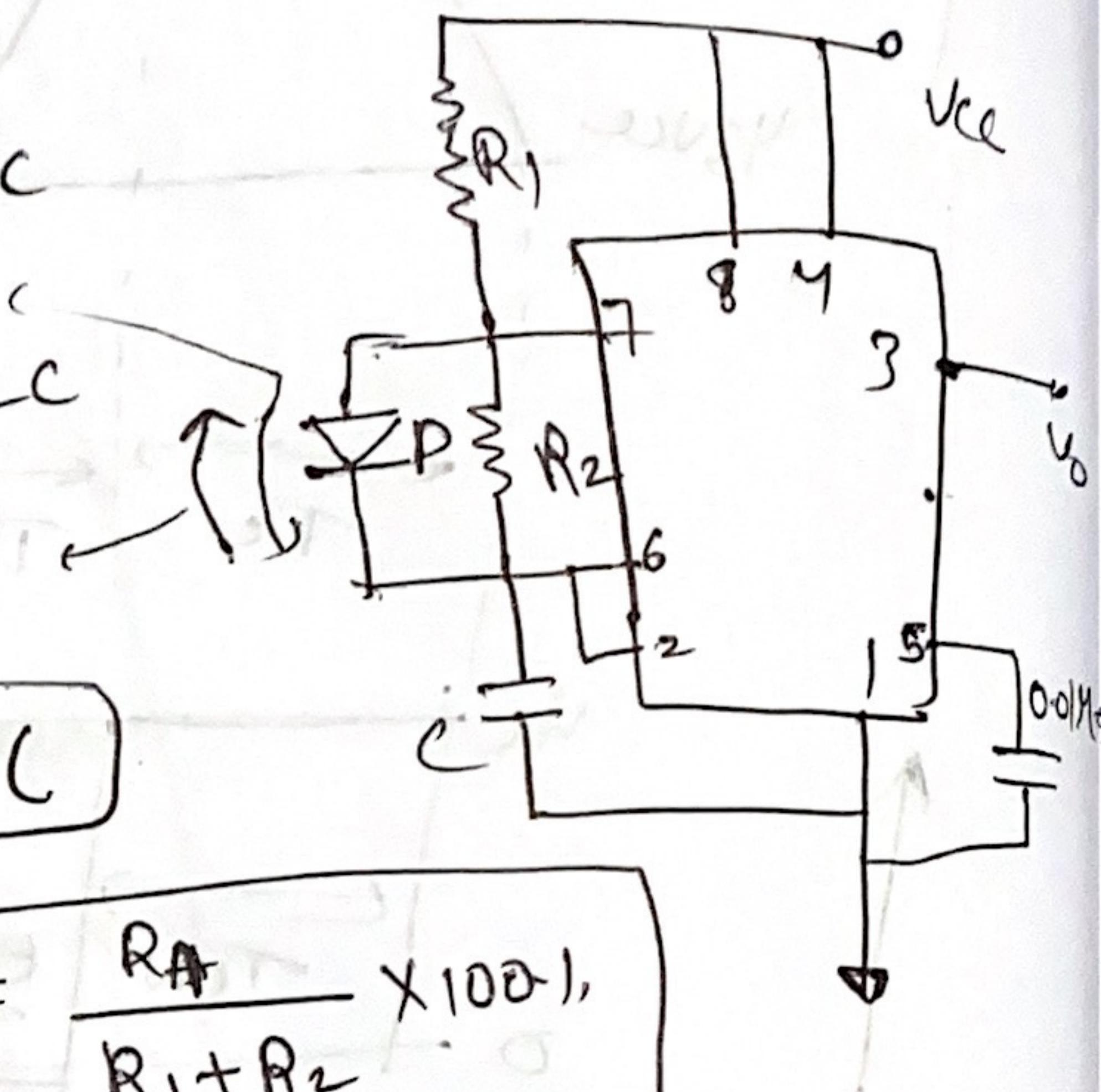
Duty cycle ↓

During charging,  $T_c = 0.69 R_{AC}$   
(Forward bias)  
→ op corrects to why

$$\rightarrow \text{up} \quad \text{down} \quad \text{left} \quad \text{right}$$
$$N = T_B = 0$$

Durchdurchströmung)  $T_b = 0.6 \text{ Rec}$

(Reverse bias)  $\rightarrow$  open now.



$$\text{Total Head } F = 0.6q (R_1 + R_2) C$$

$$f = \frac{1.45}{(R_1 + R_2)C}$$

$$P\% = \frac{R_A}{R_1 + R_2} \times 100\%,$$

(Q1) For stable multi vibrator using 555 timer,  $R_1 = 6.8 \text{ k}\Omega$

A)

$$(a) \quad t_{ON} = 0.6q(R_1 + R_2) C$$

$$= 0.64 (3.3 + 6.8) \times 10^3 \times 0.21 \times 10^6$$

$$= 6.969 \times 10^{-4} \quad \approx 0.7 \text{ ms}$$

$$(b) t_{off} = 0.09 R_2 C$$

$$= 2.277 \times 10^{-4}, \quad = 0.23 \text{ ms}$$

$$(c) T = (6.969 + 2.277) \times 10^{-4}$$

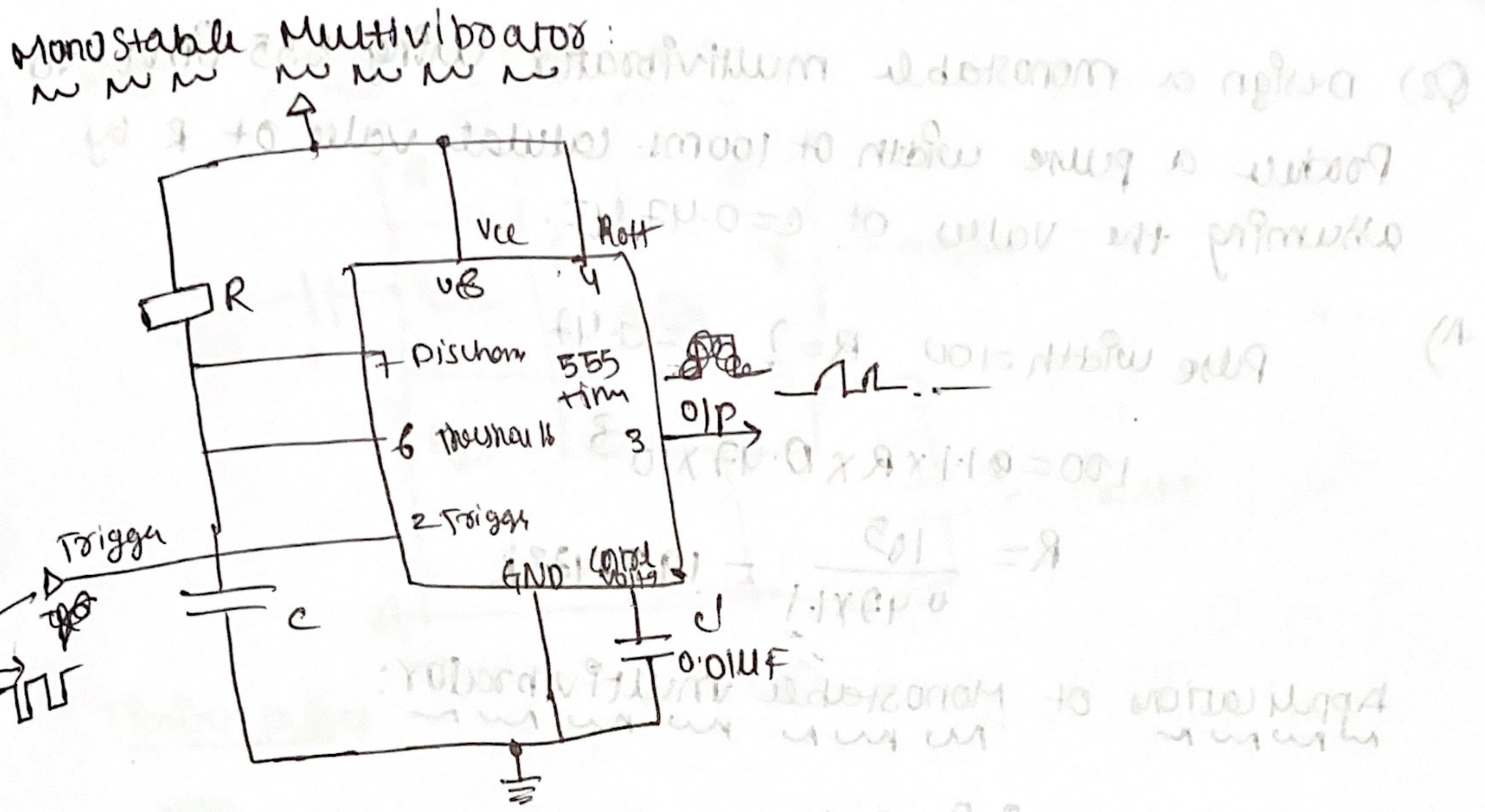
$$= (9.246) \times 10^{-4}$$

$$f = \frac{1}{9.246 \times 10^4} = 1081.5 \text{ Hz} = 1.07 \text{ kHz}$$

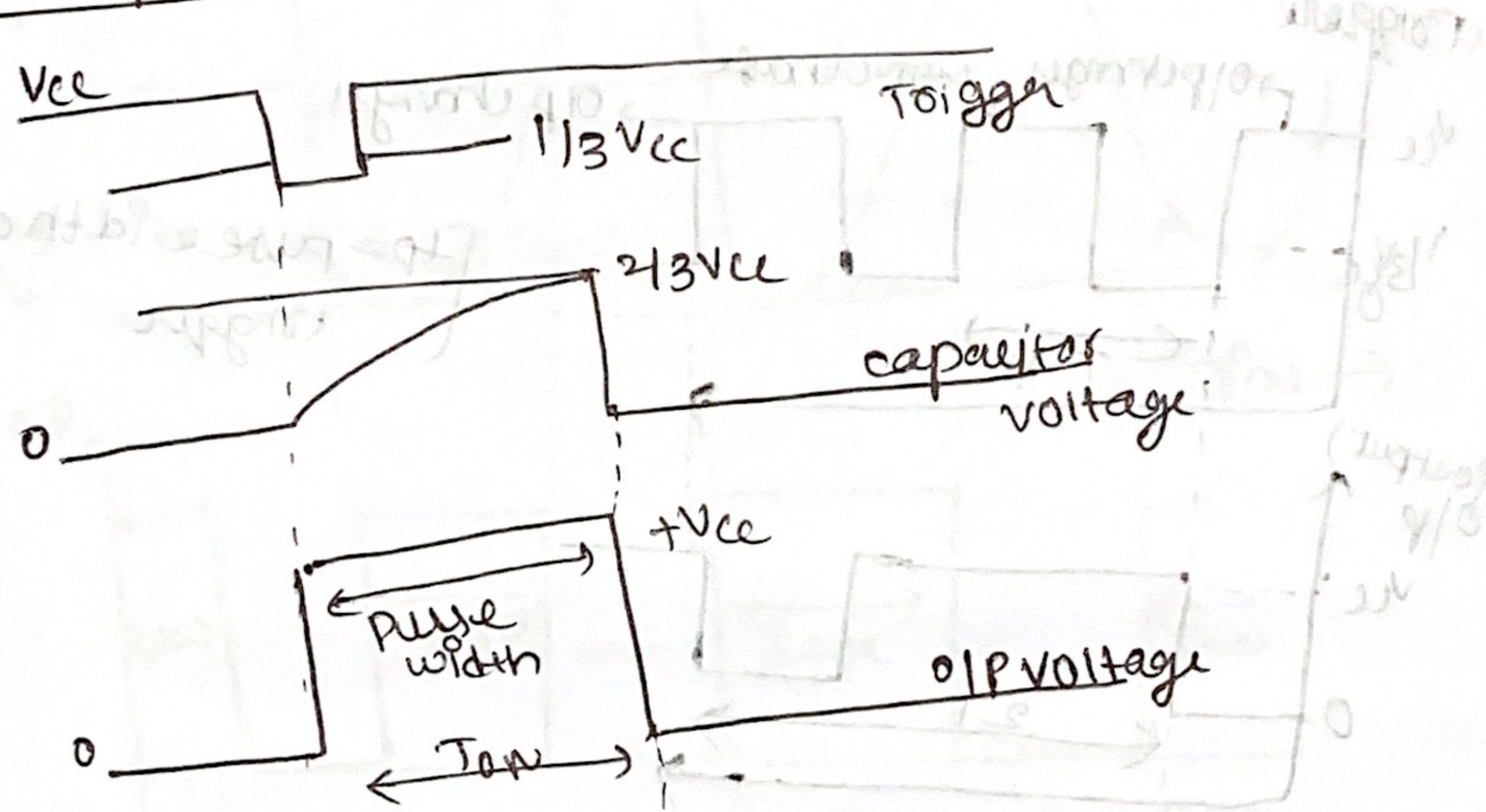
$$(d) \text{ DK} \quad \frac{\text{B.B } 6.969 \times 10^{-4}}{\text{A.I.S.A } 6.49} \times 100\%.$$

$$= 0.75 \times 100\%.$$

二七五



Timing pulse.



8514108

Total time period:

$$V_C = V_{CC} \left(1 - e^{-t/RC}\right)$$

$$\text{At } t=T, V_C = \frac{2}{3} V_{CC}$$

$$\frac{2}{3} V_{CC} = V_{CC} \left(1 - e^{-T/RC}\right)$$

$$\frac{2}{3} - 1 = -e^{-T/RC}$$

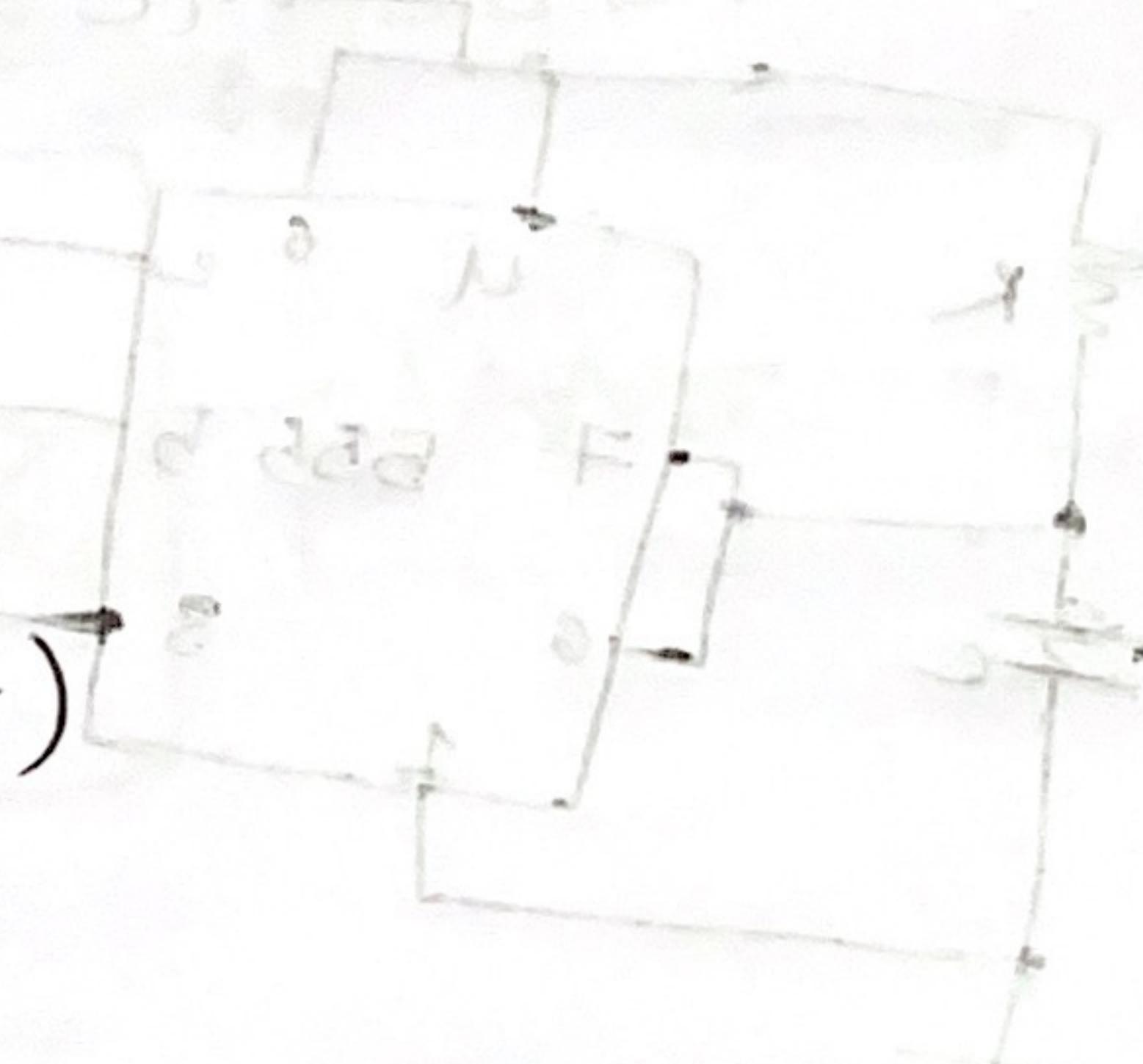
$$\frac{2}{3} - 1 = -e^{-T/RC}$$

$$T = RC \ln \frac{2}{3}$$

$$T = 1.1RC$$

(Pulse width)

$$T = 1.1RC$$



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Q2) Design a monostable multivibrator using 555 timer to produce a pulse width of 100ms. Calculate value of R by assuming the value of  $C = 0.47 \mu F$ .

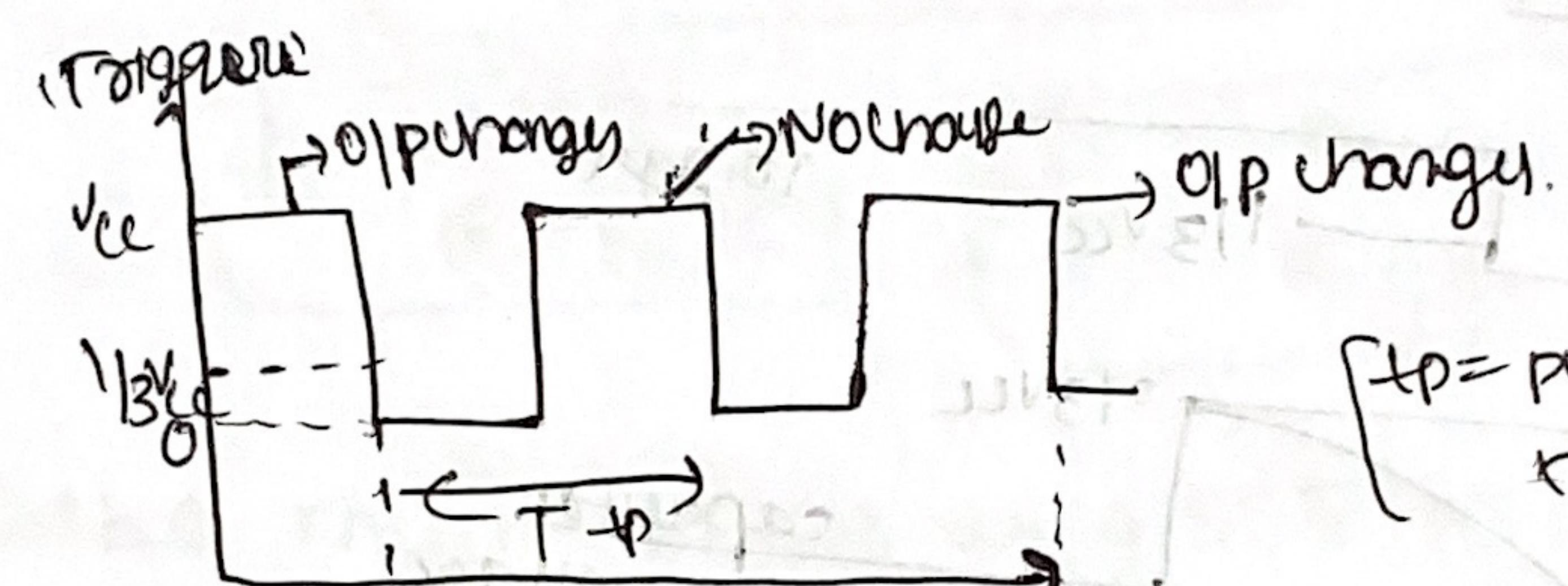
(i) Pulse width = 100 ms?  $C = 0.47 \mu F$

$$100 = 0.11 \times R \times 0.47 \times 10^{-6}$$

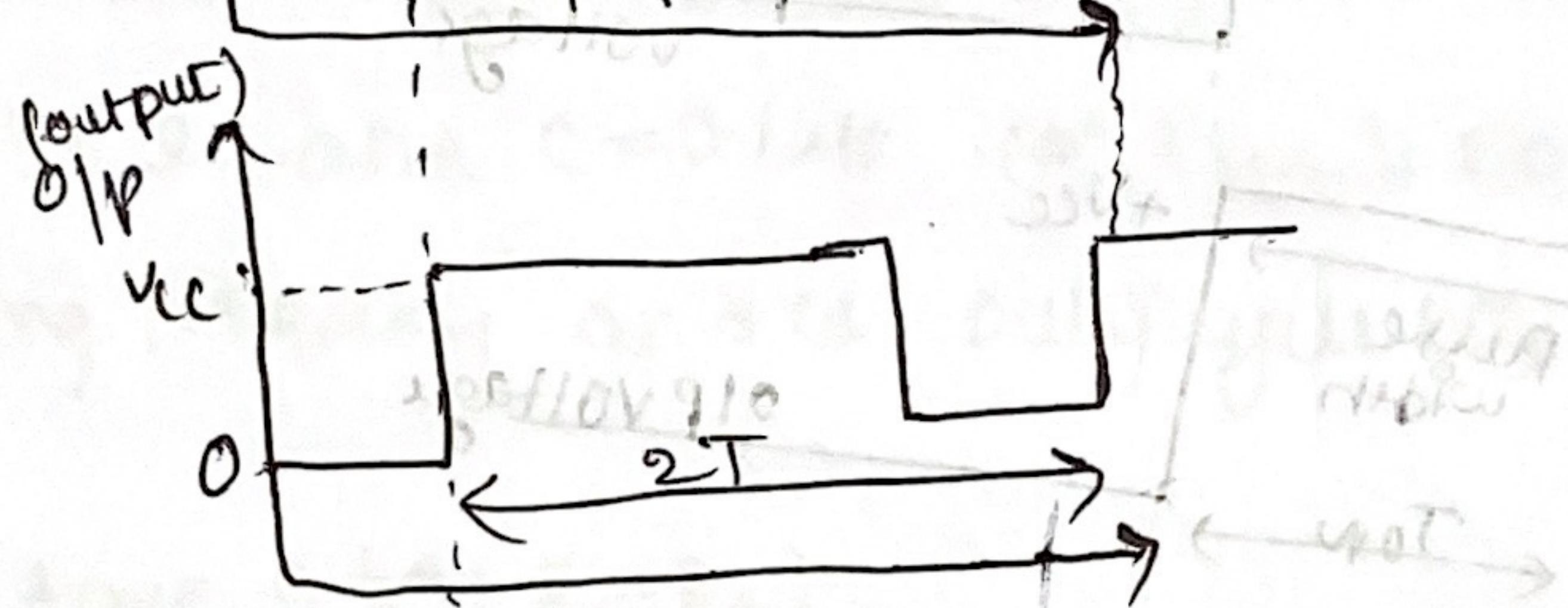
$$R = \frac{10^5}{0.47 \times 0.11} = 193.0423 k\Omega$$

Applications of Monostable Multivibrator:

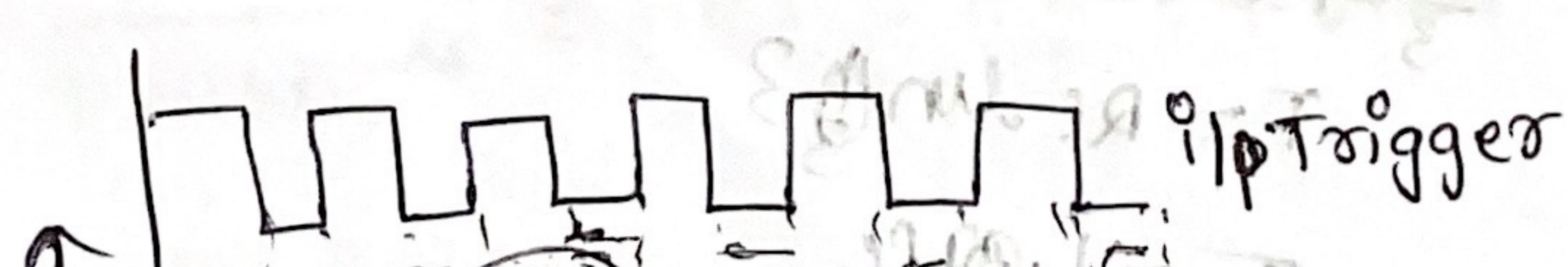
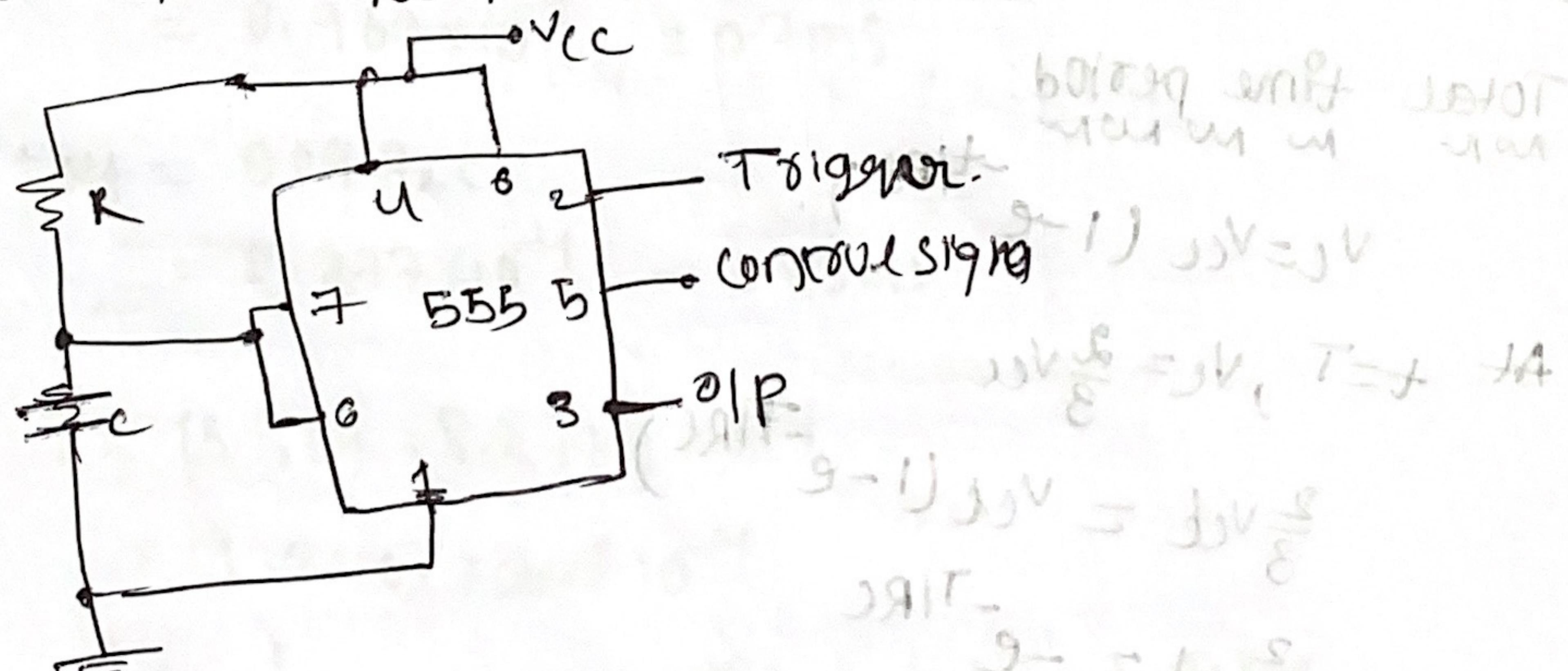
### Frequency Divider



$T_{dp}$  = pulse width at output  
trigger

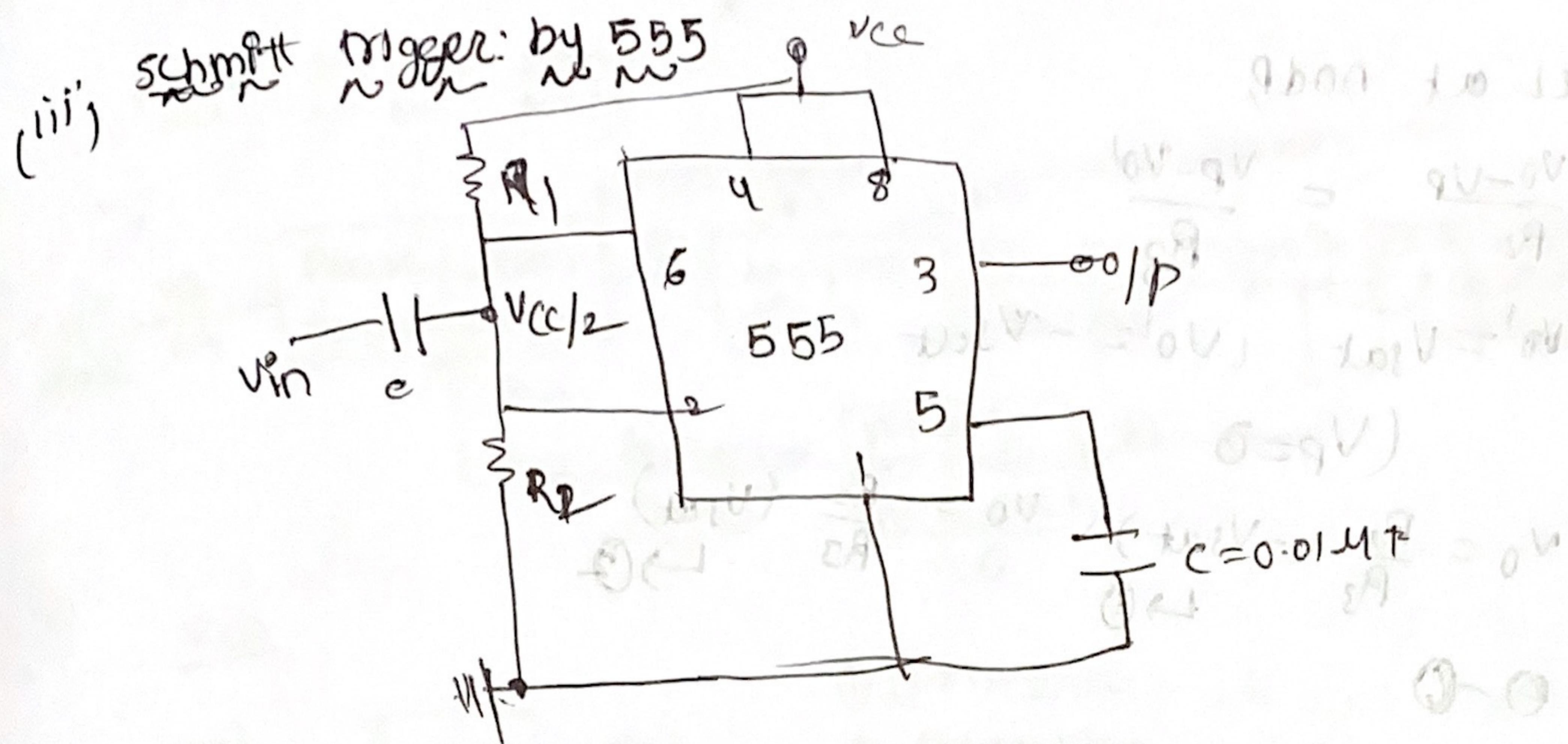


### Pulse width Modulation

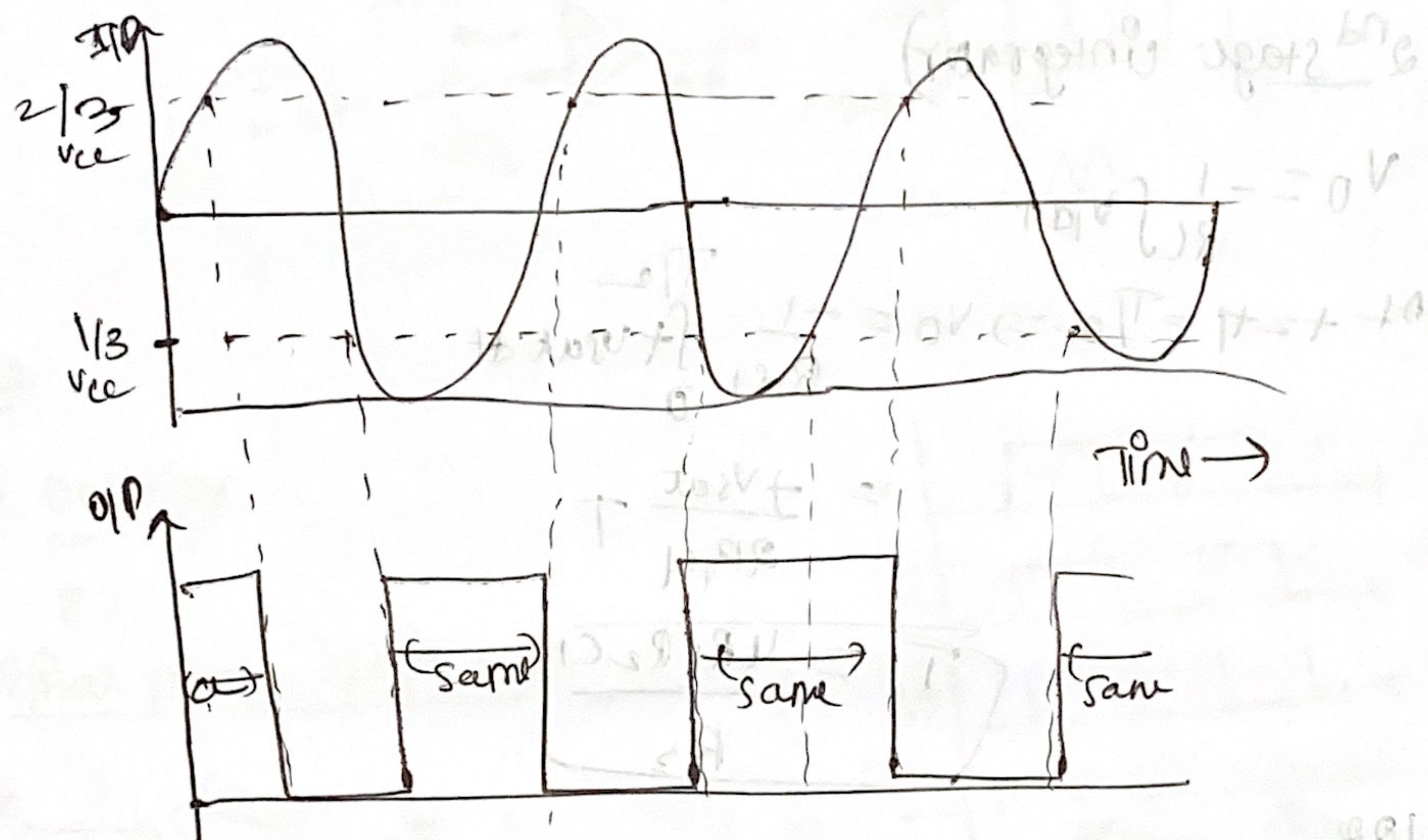


Pulse width  
Modulated O/P.

(or graphically wrong drawn).

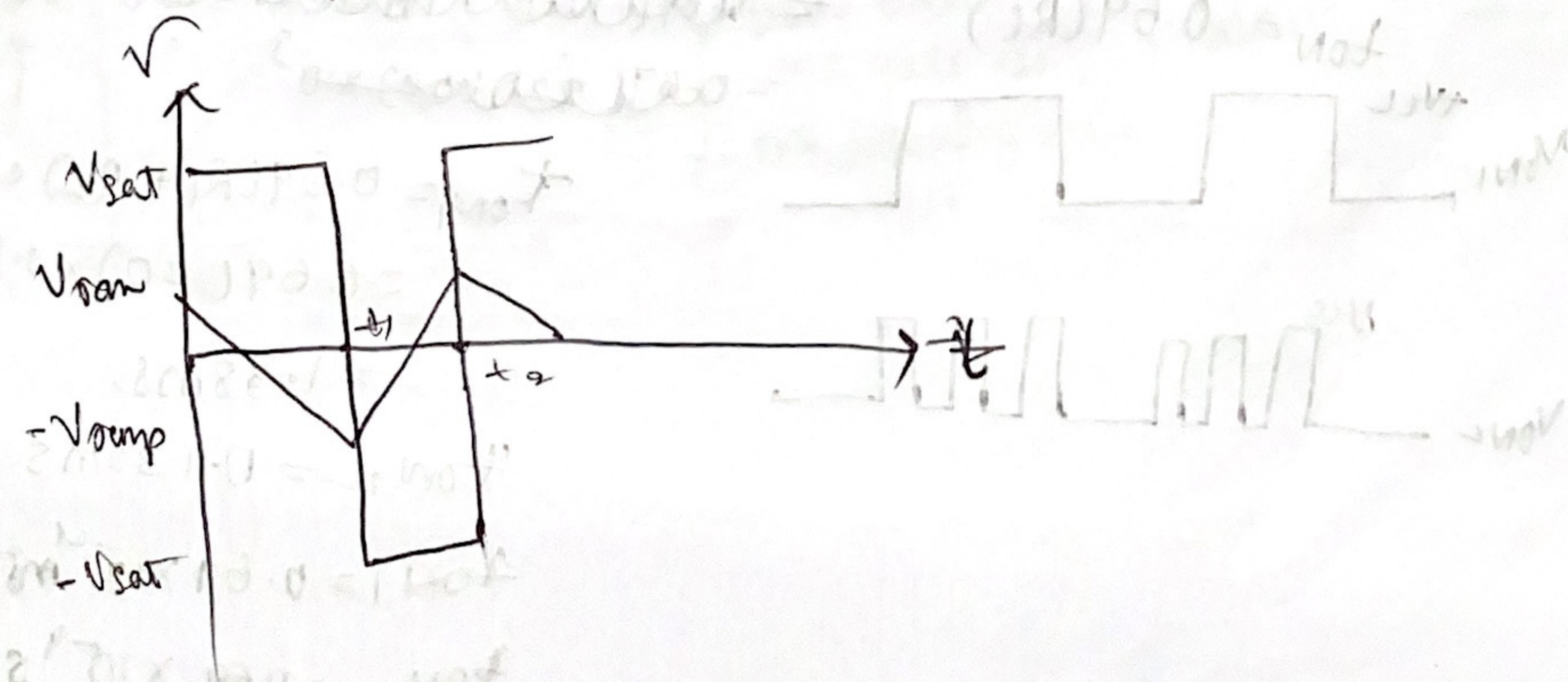
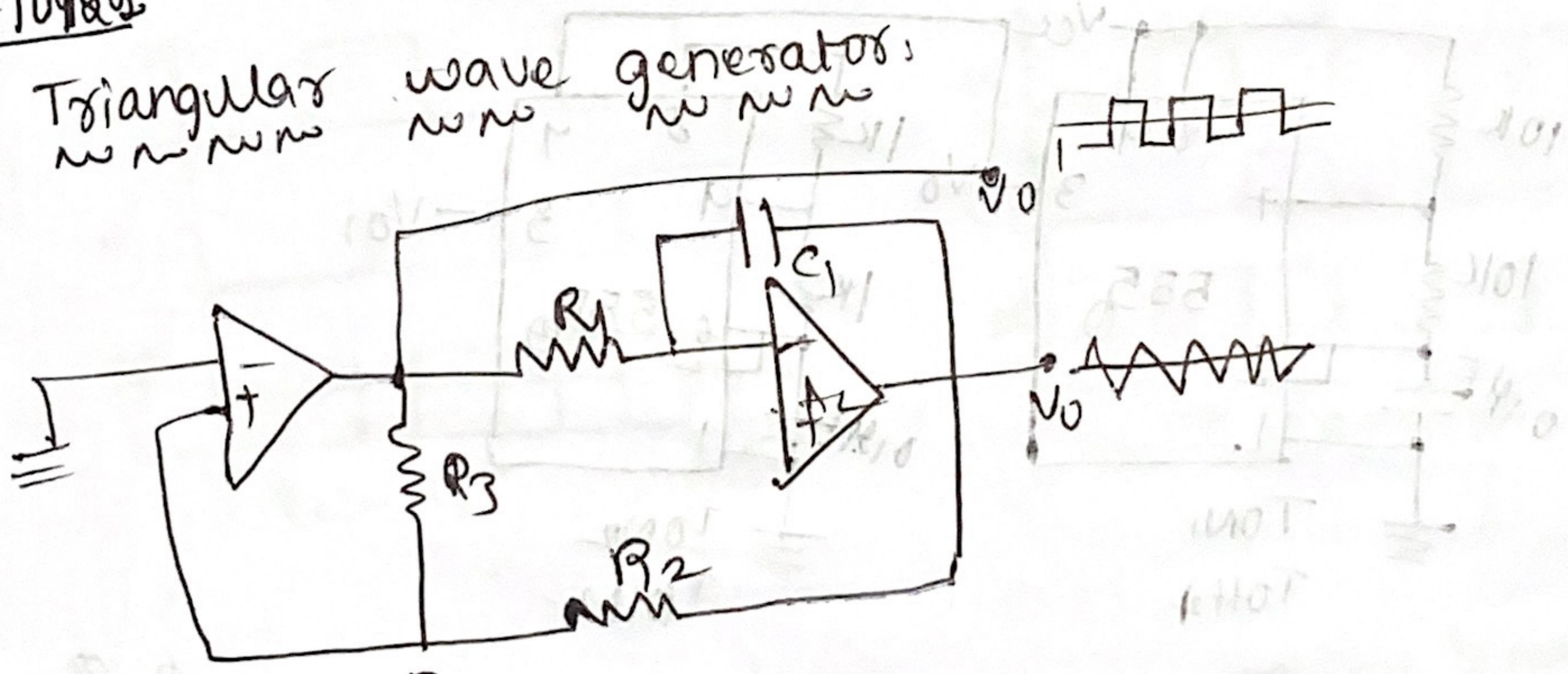


Timing pulses



27/04/2022

Triangular wave generator:



Look at node P,

$$\frac{V_0 - V_P}{R_2} = \frac{V_P - V_O}{R_3}$$

$$V_O^1 = V_{sat}, \quad V_O^1 = -V_{sat}$$

$$(V_P = 0)$$

$$V_O = \frac{R_2}{R_3} (-V_{sat}) \quad \text{①}$$

$$V_O = \frac{R_2}{R_3} (V_{sat}) \quad \text{②}$$

② - ①

$$V_O(PP) = \frac{2R_2}{R_3} (V_{sat}).$$

2nd Stage: Integrator

$$V_O = -\frac{1}{RC} \int V_I dt$$

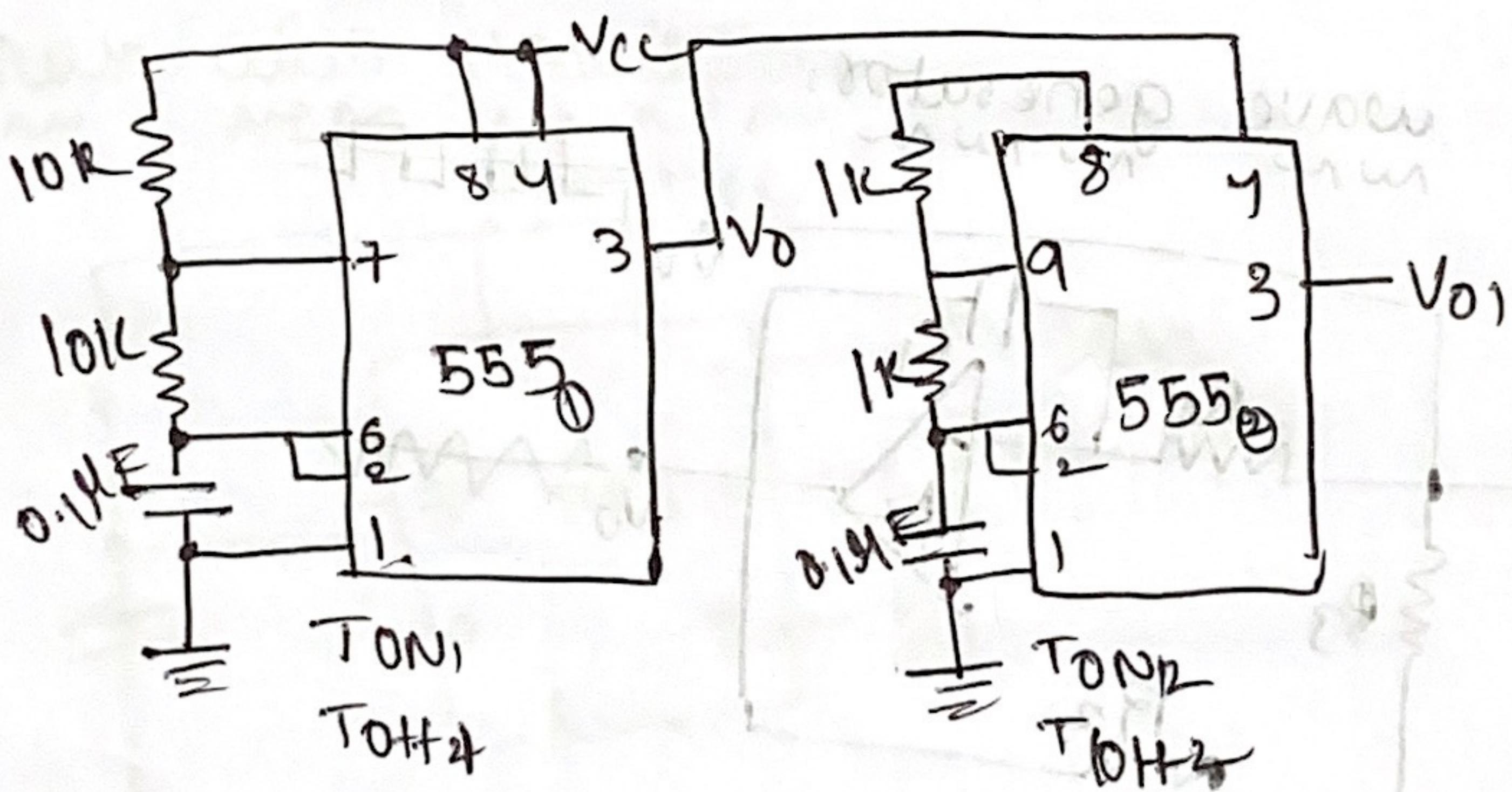
$$At t=0, V_I = V_{sat} \Rightarrow V_O = -\frac{1}{R_1 C_1} \int_0^{T/2} V_{sat} dt$$

$$= \frac{-V_{sat}}{2R_1 C_1} T$$

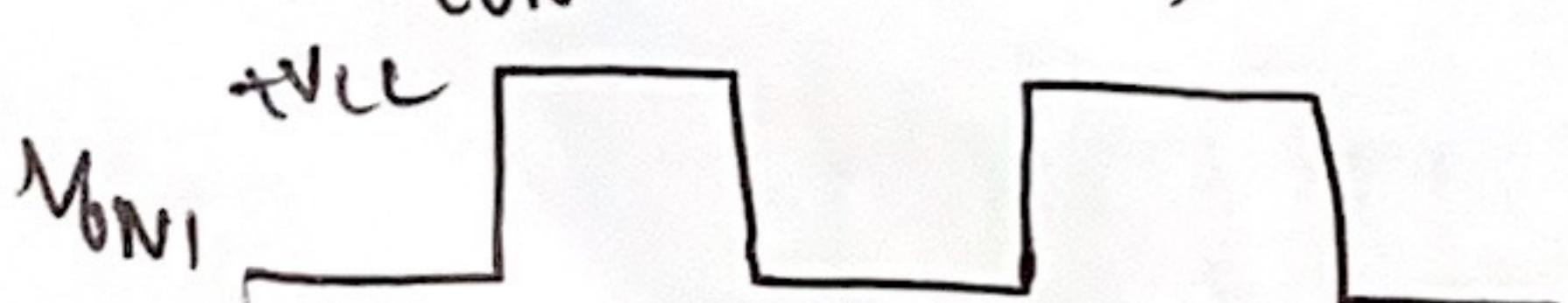
$$T = \frac{4 R_1 R_2 C_1}{R_3}$$

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(Q1)



$$t_{on} = 0.69(RC)$$



$$= 0.69(10k \times 10^{-6}) \times 10^{-3}$$

$$= 0.69(220 \times 10^{-3}) \times 10^{-3}$$

$$t_{on1} = 0.69(R_1 + R_2)C$$

$$= 0.69(20) \times 0.1 \times 10^{-3}$$

$$= 1.38 \text{ ms.}$$

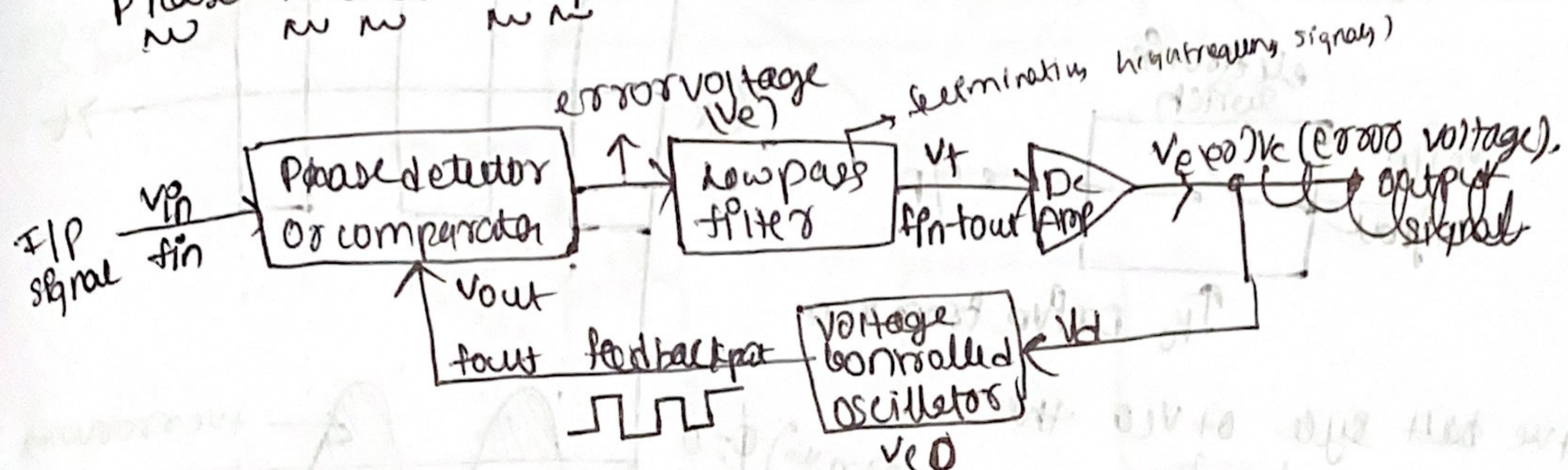
$$t_{off1} = 0.138 \text{ ms.}$$

$$t_{off1} = 0.69 \times 10^{-4} \text{ ms}$$

$$t_{off2} = 0.69 \times 10^{-4} \text{ s}$$



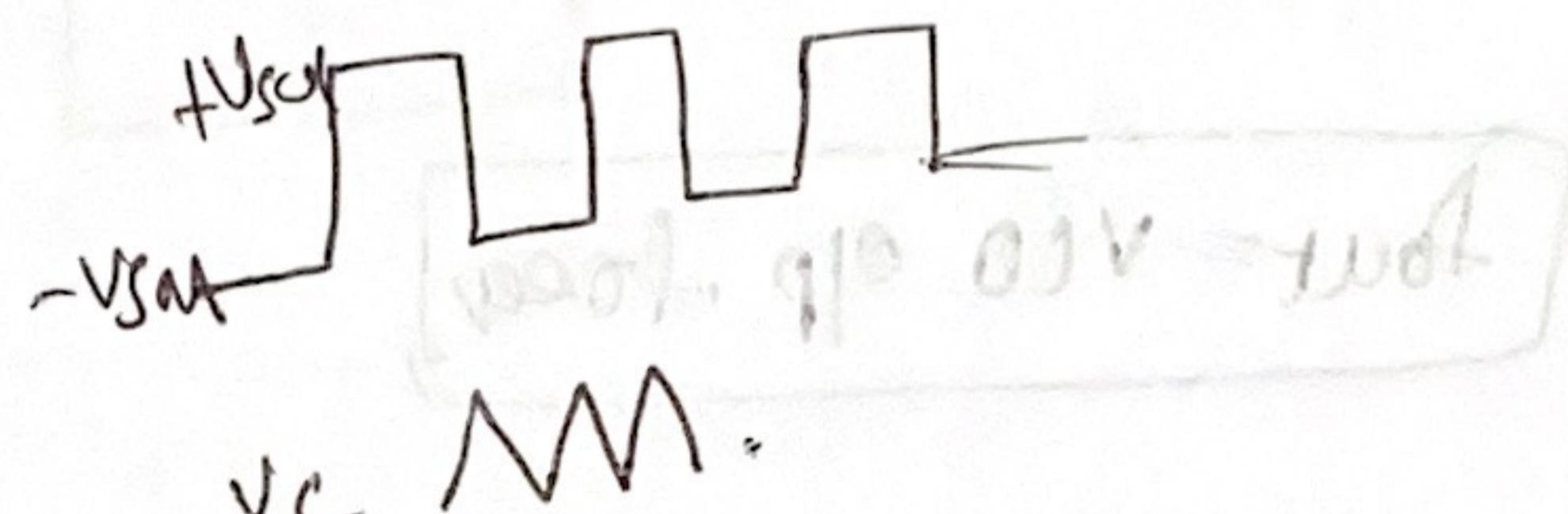
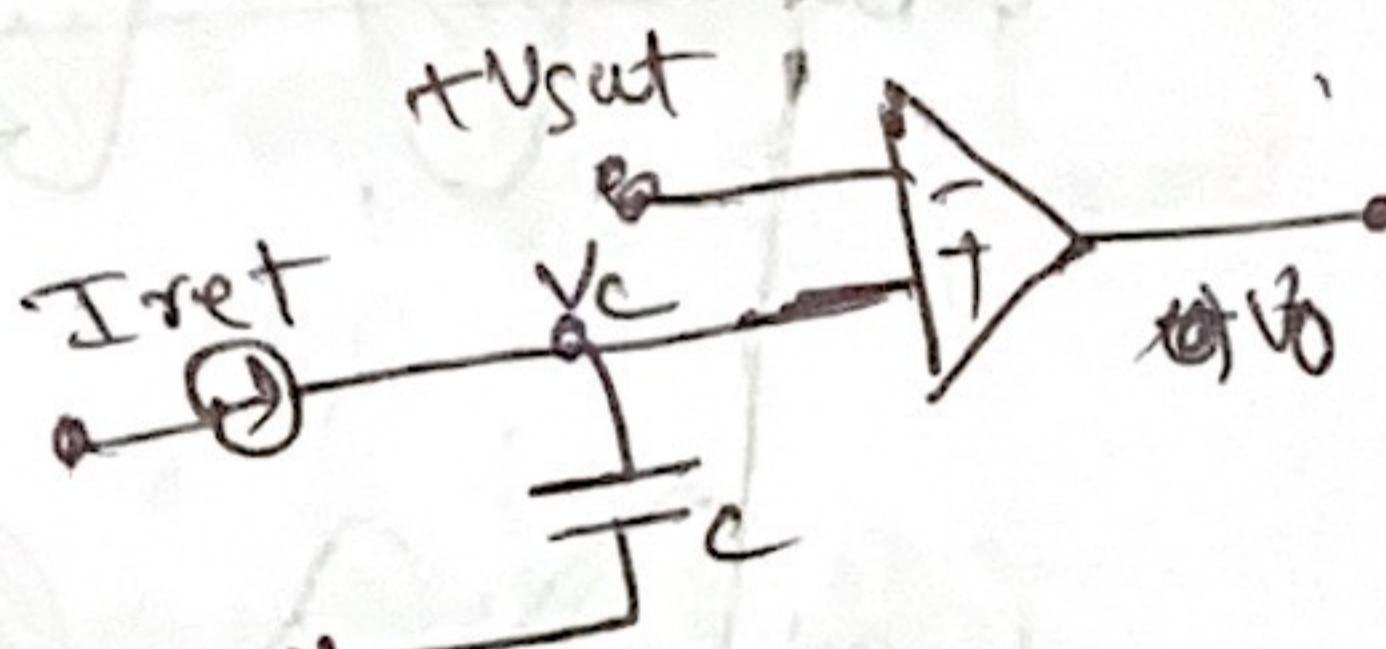
## Phase locked loop:



$v_{CO}$

control voltage  $\rightarrow v_{CO} \rightarrow \text{O/p}$

- ① Harmonic.
- ② Relaxation.

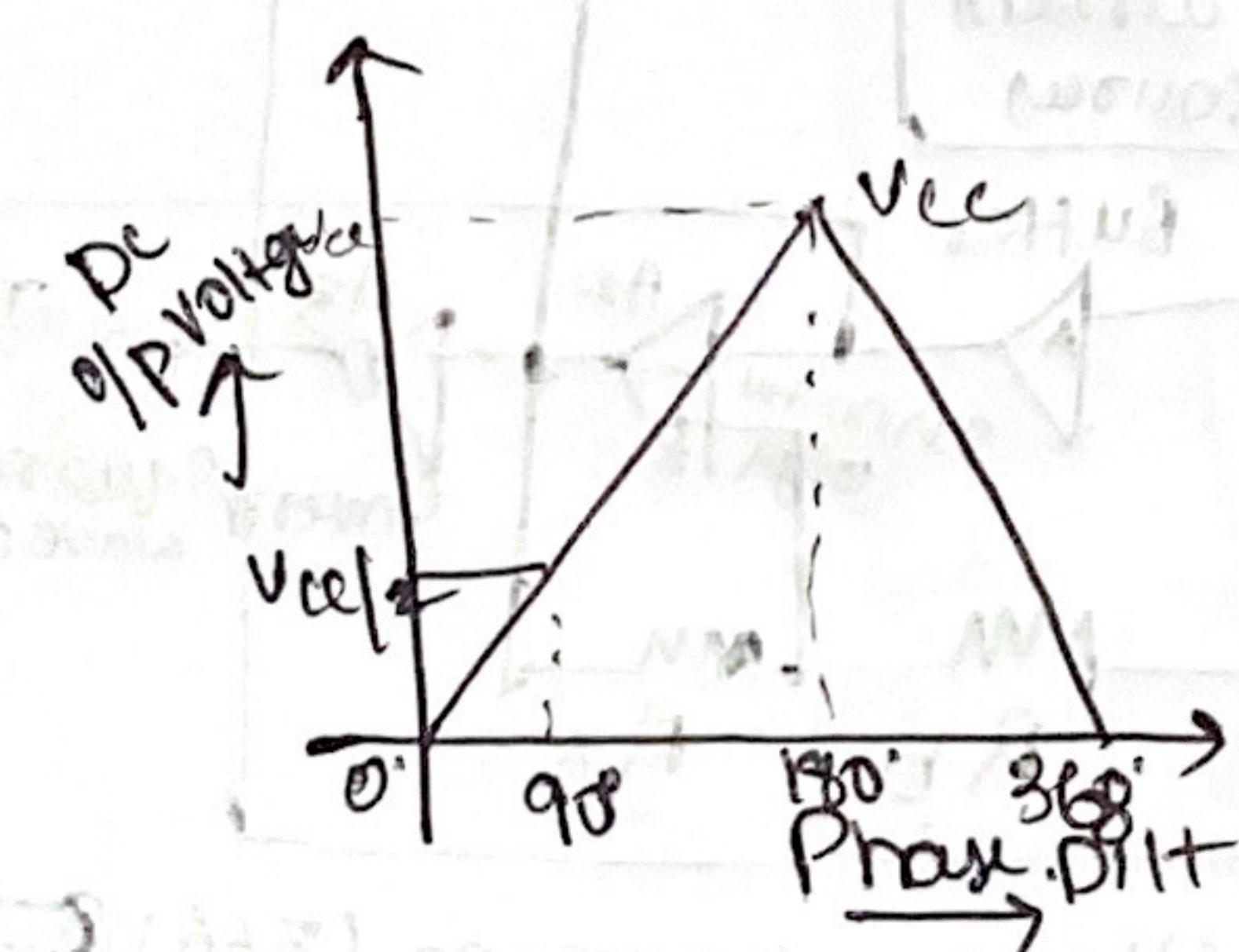
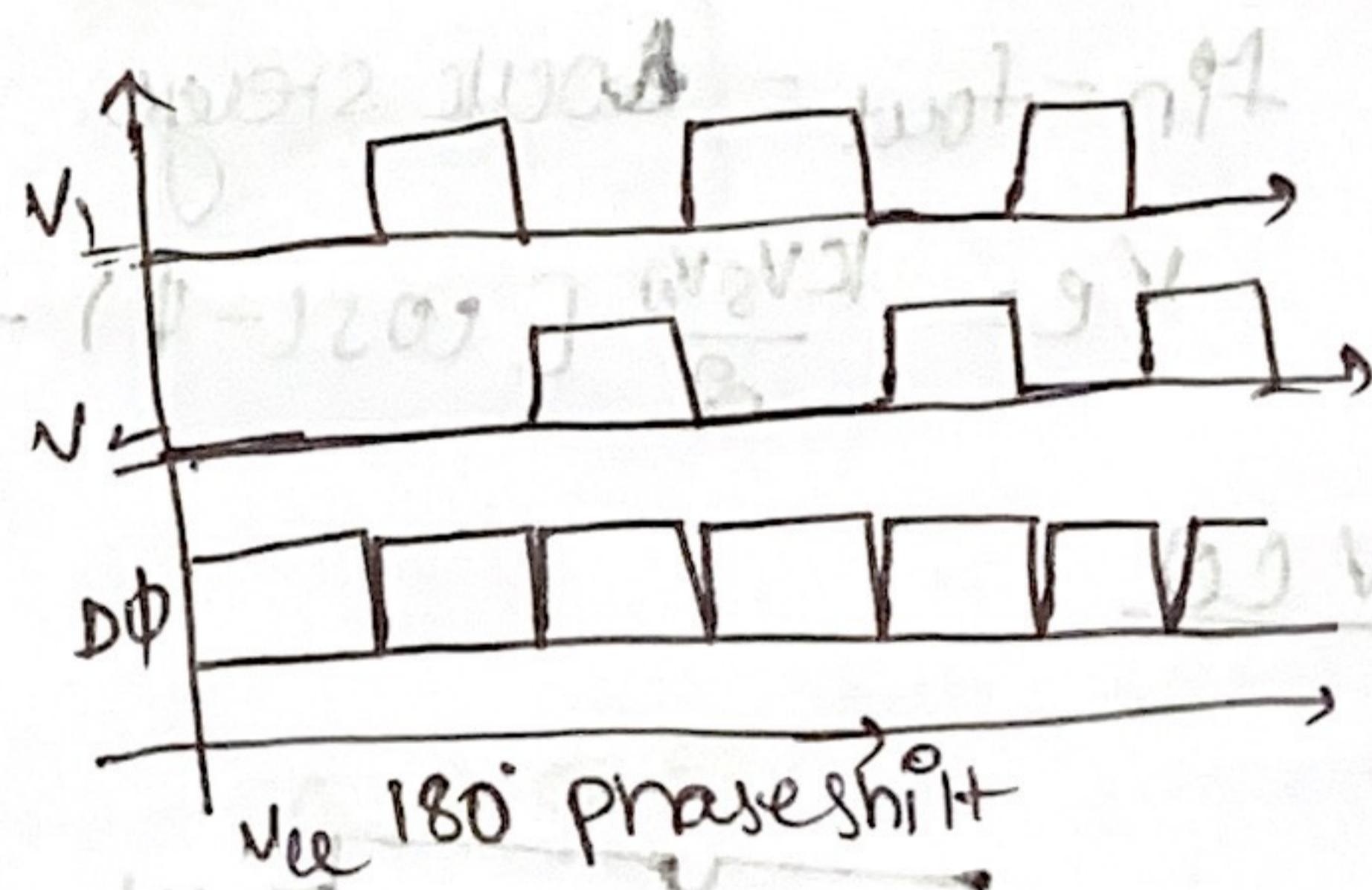
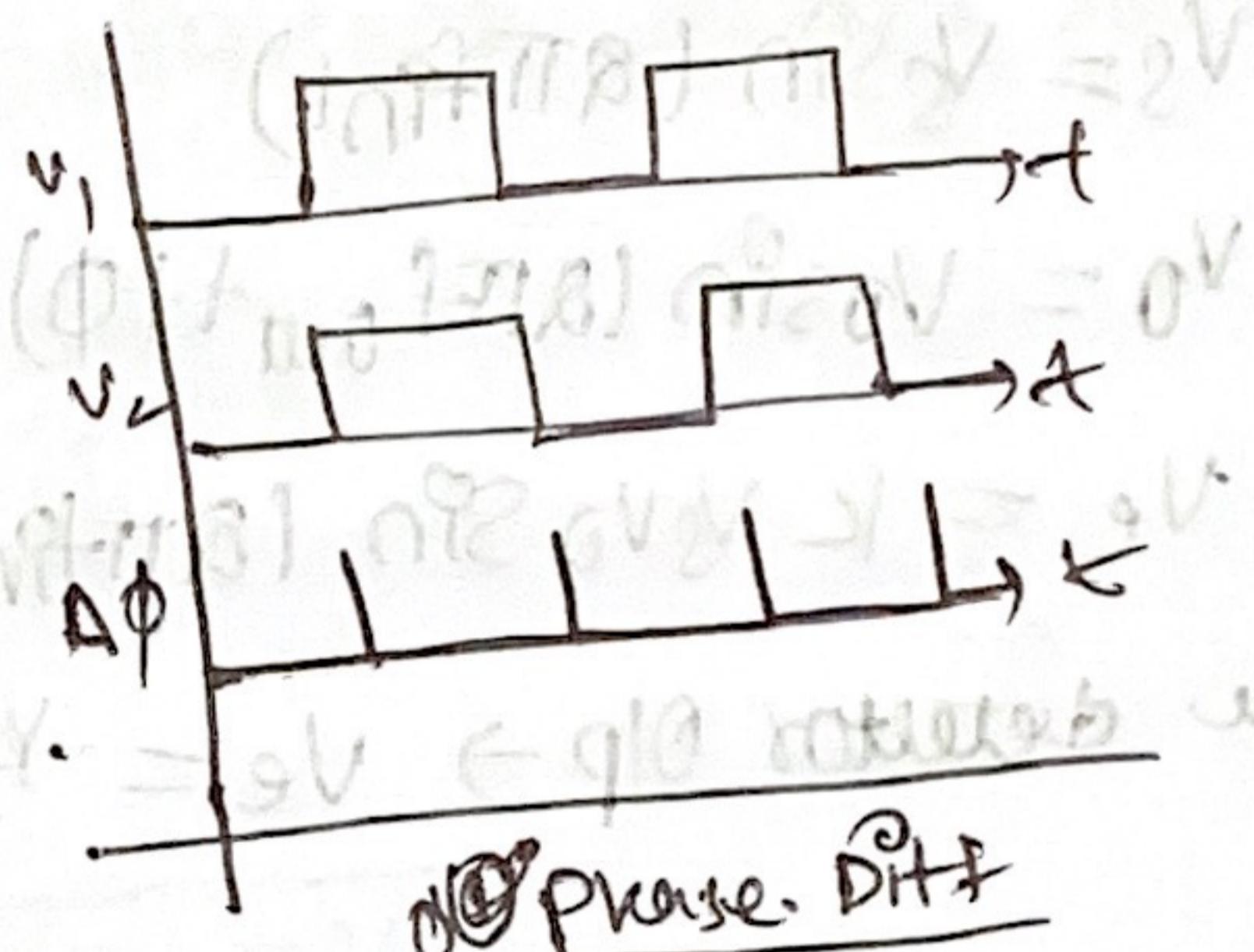
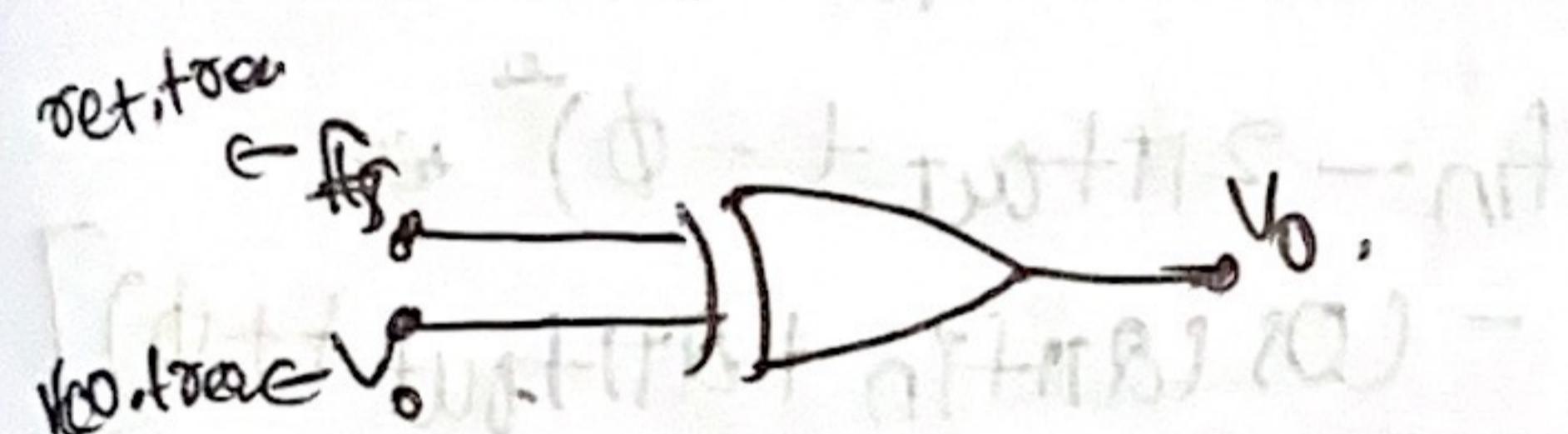


215 & 2

Phase detector:

$\alpha \rightarrow \beta \rightarrow$

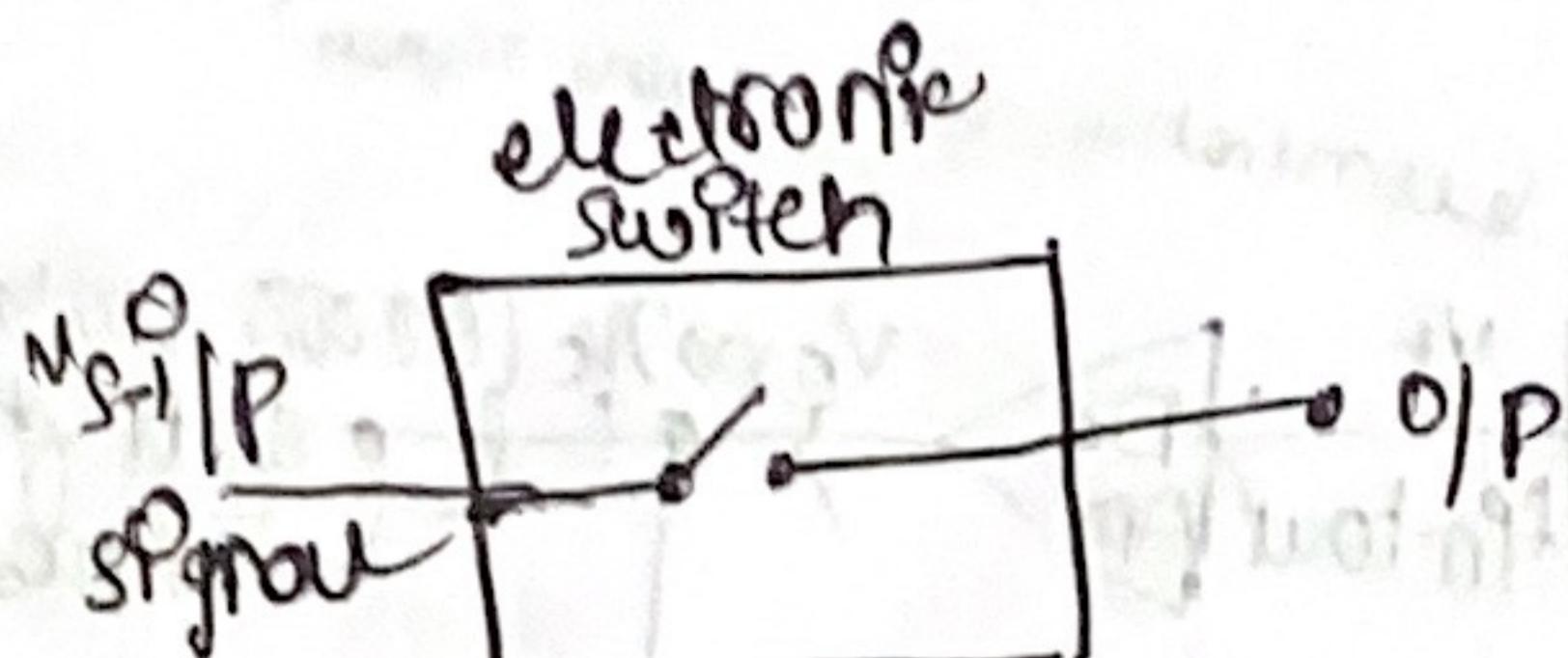
① Digital phase detector:



draw back of XOR gate as not following wave, so XOR is not used alone.

Q1 V  $\approx$  0.7 V, Q2 V  $\approx$  0.3 V, Q3 V  $\approx$  0.7 V, Q4 V  $\approx$  0.3 V

## ② Analog phase detector:

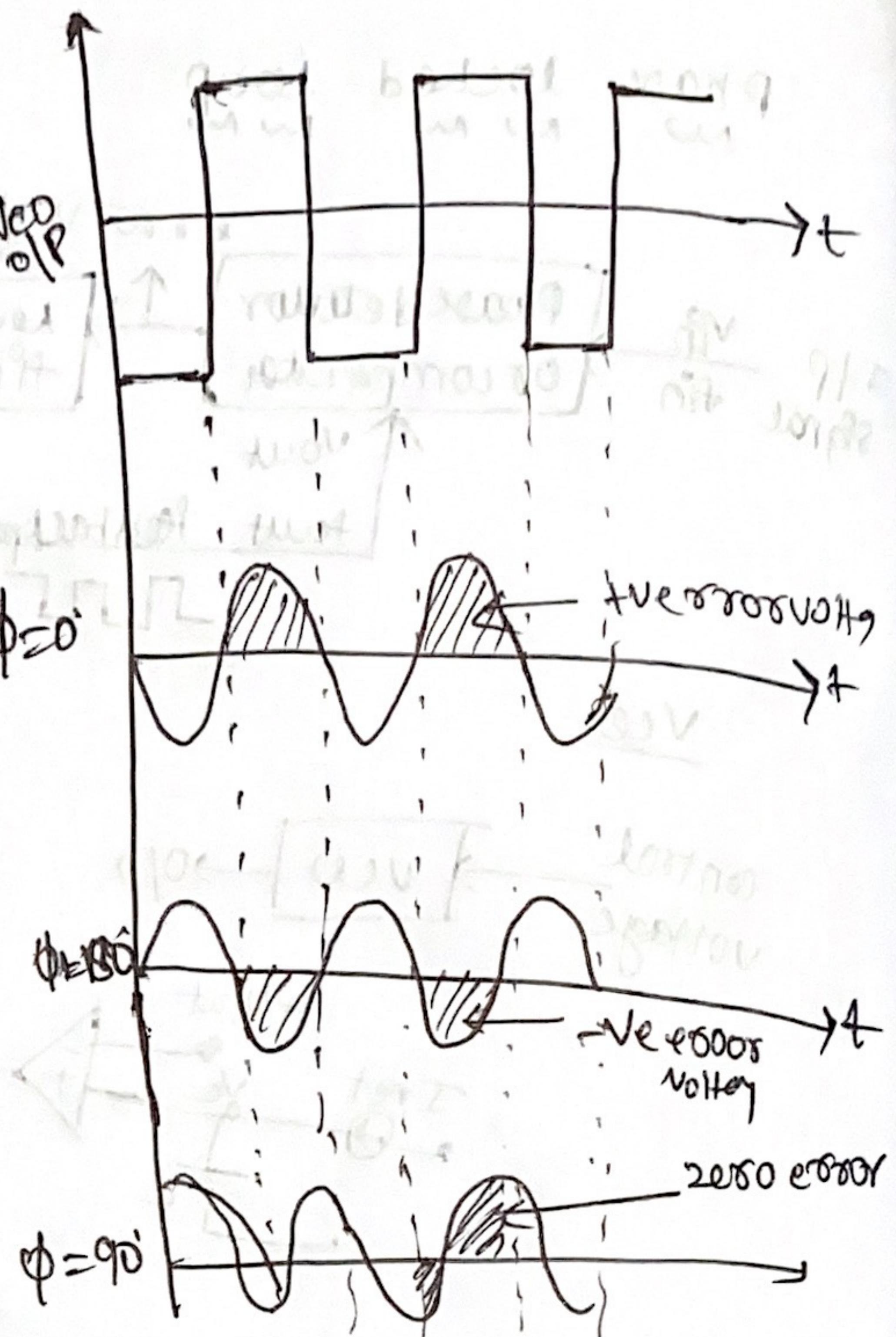


$T_{V_0}$  or frequency from VCO:

→ +ve half cycle of VCO the switch will be off!

→ -ve half cycle the VCO switch will be on.

$$fout = VCO \text{ opp. freq.}$$



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$$V_S = V_0 \sin(2\pi f_{in} t)$$

$$V_0 = V_{os} \sin(2\pi f_{out} t + \phi)$$

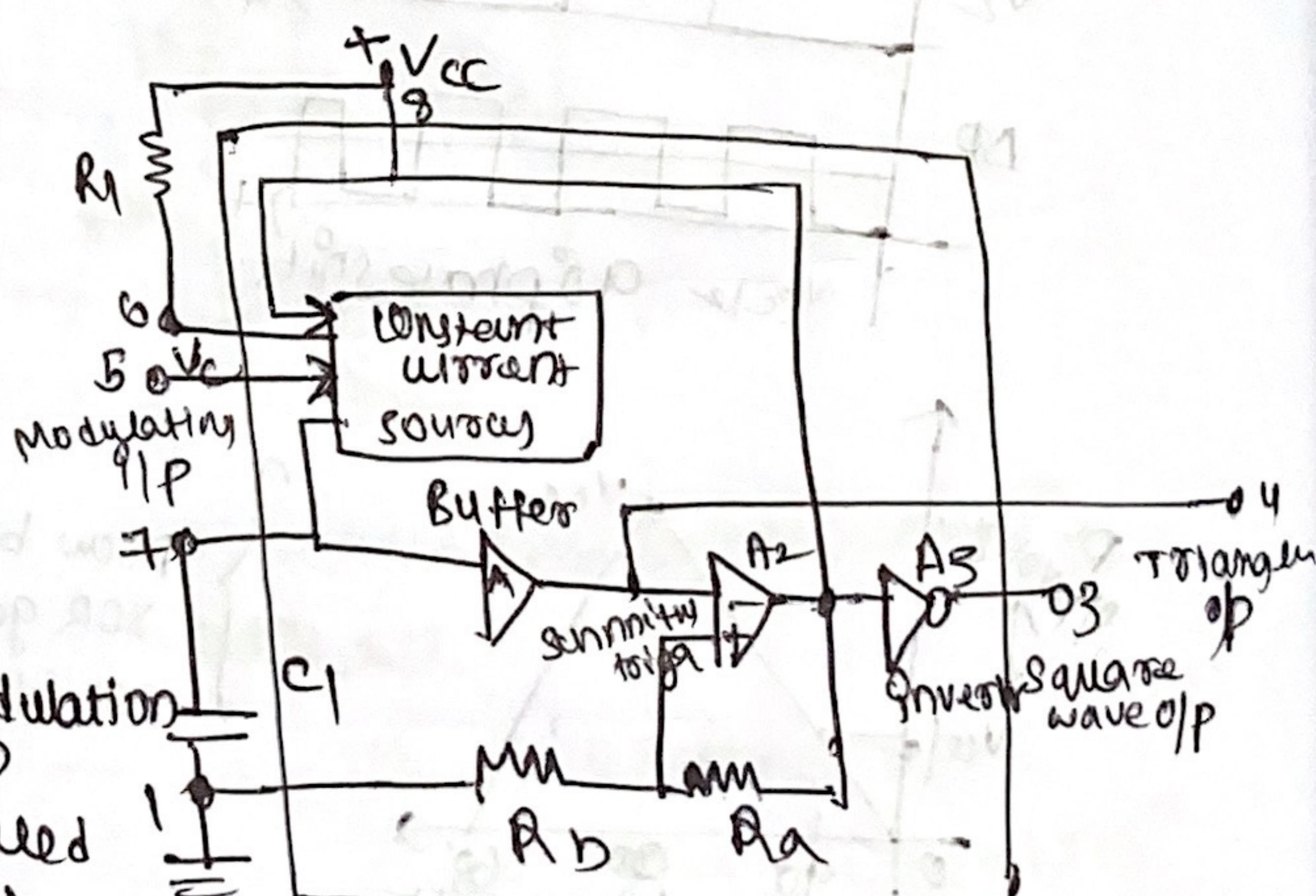
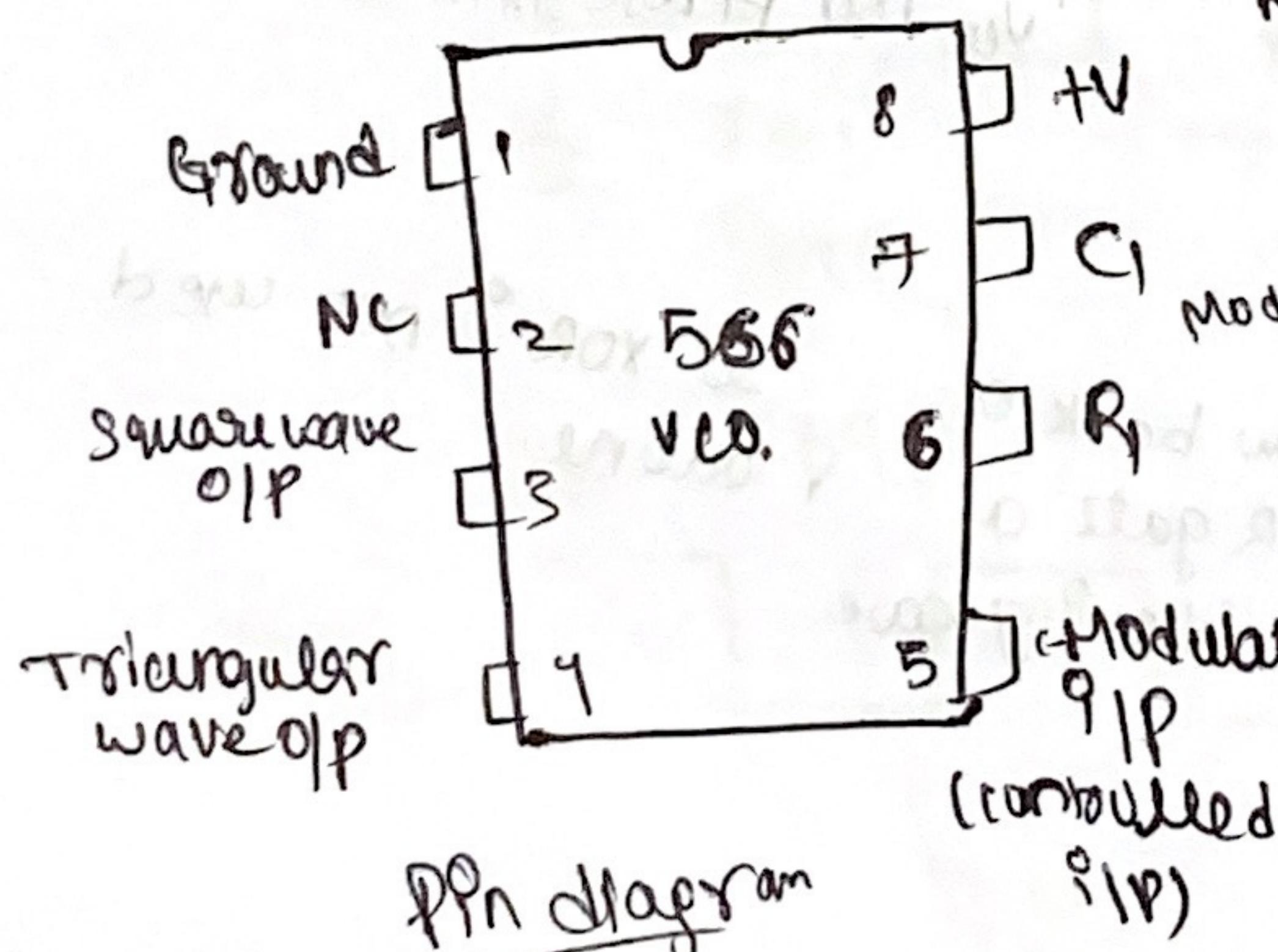
$$V_e = k V_S V_0 \sin(2\pi f_{in} t) \times \sin(2\pi f_{out} t + \phi)$$

$$\text{Phase detector O/p} \rightarrow V_e = \frac{k V_S V_0}{2} [\cos(2\pi f_{in} t - 2\pi f_{out} t - \phi) - \cos(2\pi f_{in} t + 2\pi f_{out} t + \phi)]$$

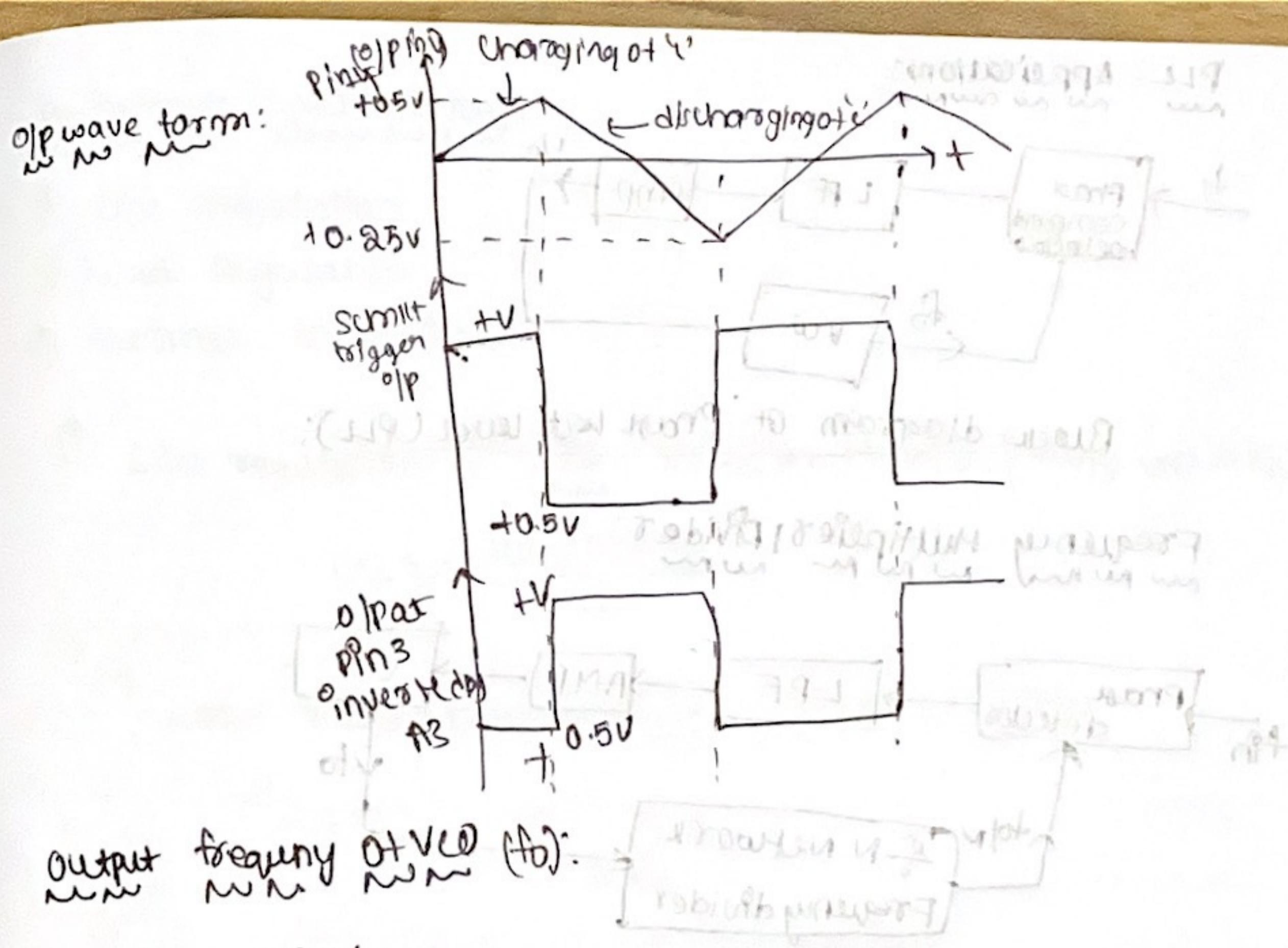
$f_{in} = f_{out} = \text{local stage.}$

$$V_e = \frac{k V_S V_0}{2} [\cos(-\phi) - \cos(2\pi \times 2 f_{in} t + \phi)].$$

VCO



→ 566 VCO is most commonly used VCO.



Output frequency of VCO ( $f_0$ ):

$$\Delta V_C = 0.25V_{CC}$$

$\frac{\Delta V_C}{\Delta t} = \frac{q}{C_1}$  (Capacitor voltage with const. current source).

$$\frac{0.25V_{CC}}{\Delta t} = \frac{q}{C_1} \Rightarrow \Delta t = \frac{0.25V_{CC}C_1}{q}$$

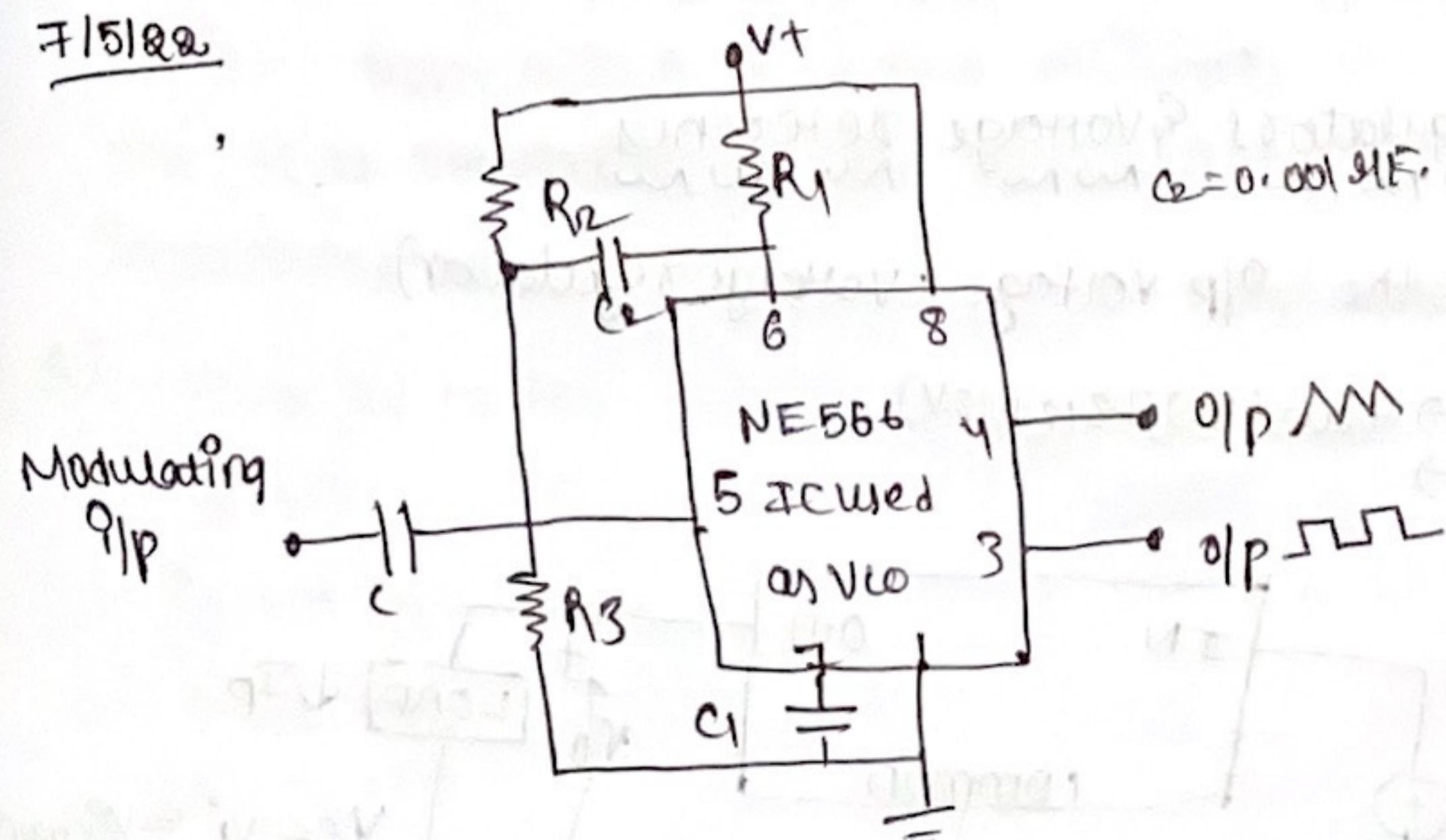
$$T = 2\Delta t \Rightarrow f_0 = \frac{1}{T} = \frac{1}{2\Delta t}$$

$$f_0 = \frac{q}{0.5V_{CC}C_1}$$

$$q = \frac{V_{CC} - V_C}{R_1}$$

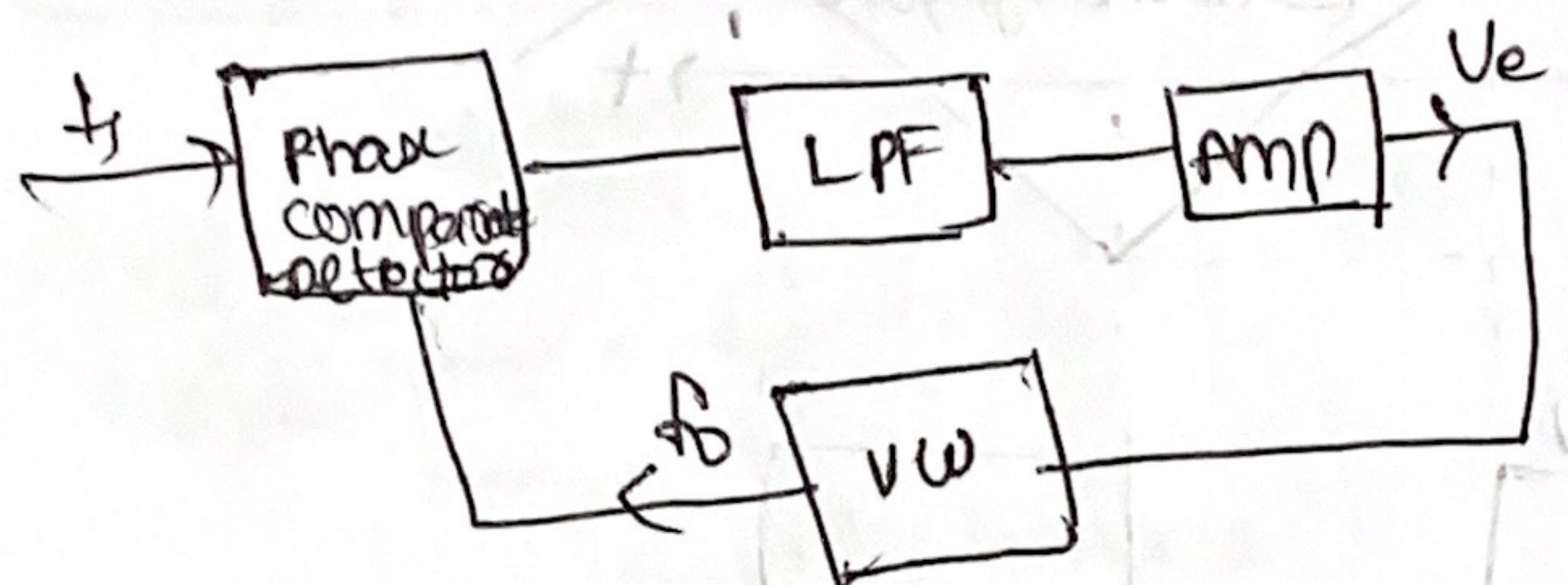
$$\Rightarrow T = \frac{2(V_{CC} - V_C)}{q R_1 V_{CC}}$$

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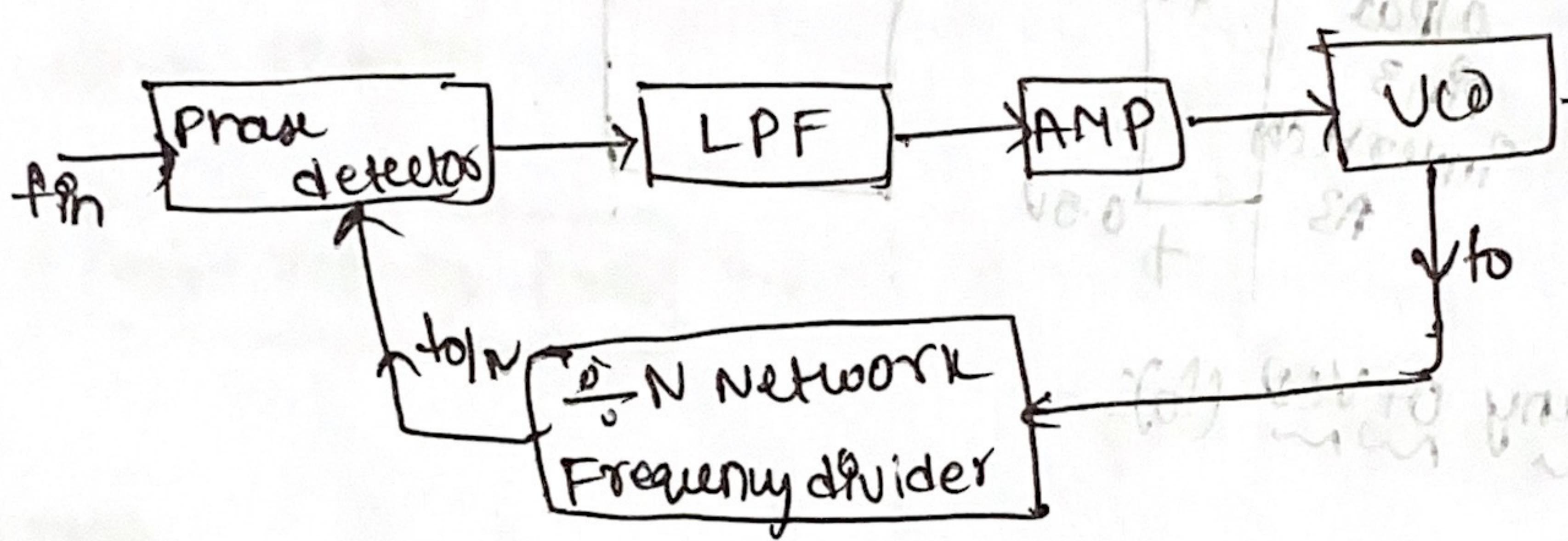


Typical connection diagram.

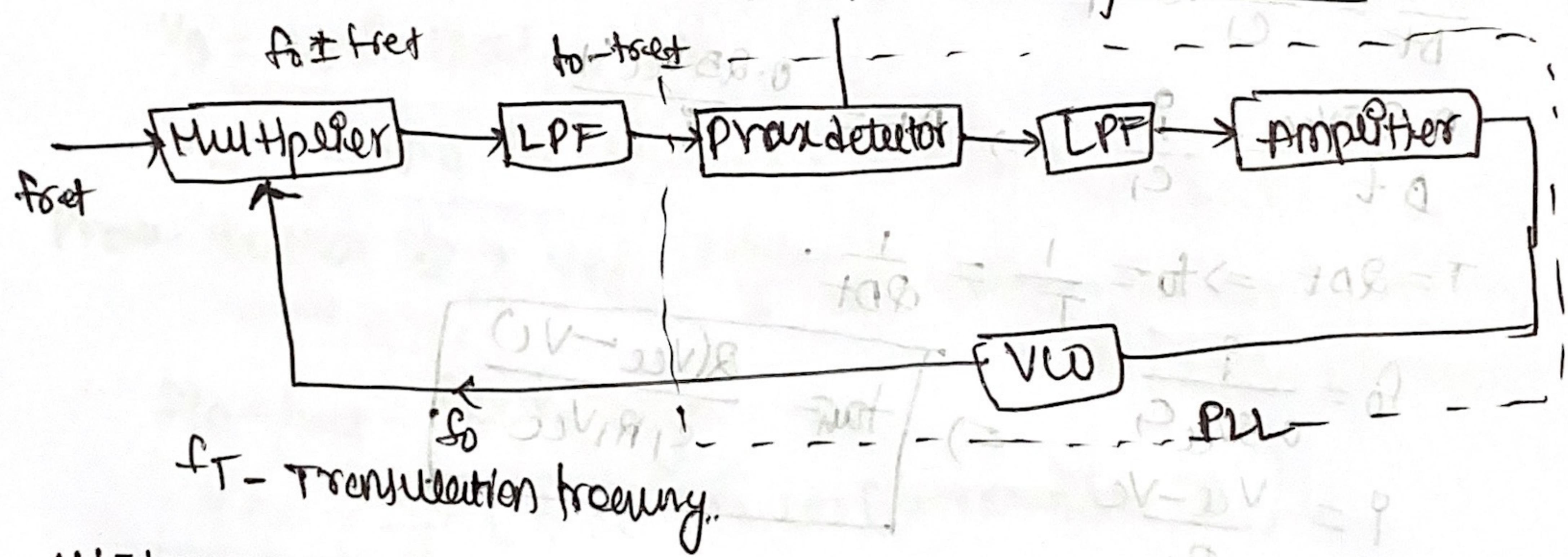
## PLL Applications



Frequency Multipliers, Dividers:



Frequency translation:  $f_{out}$  (frequency shifter).

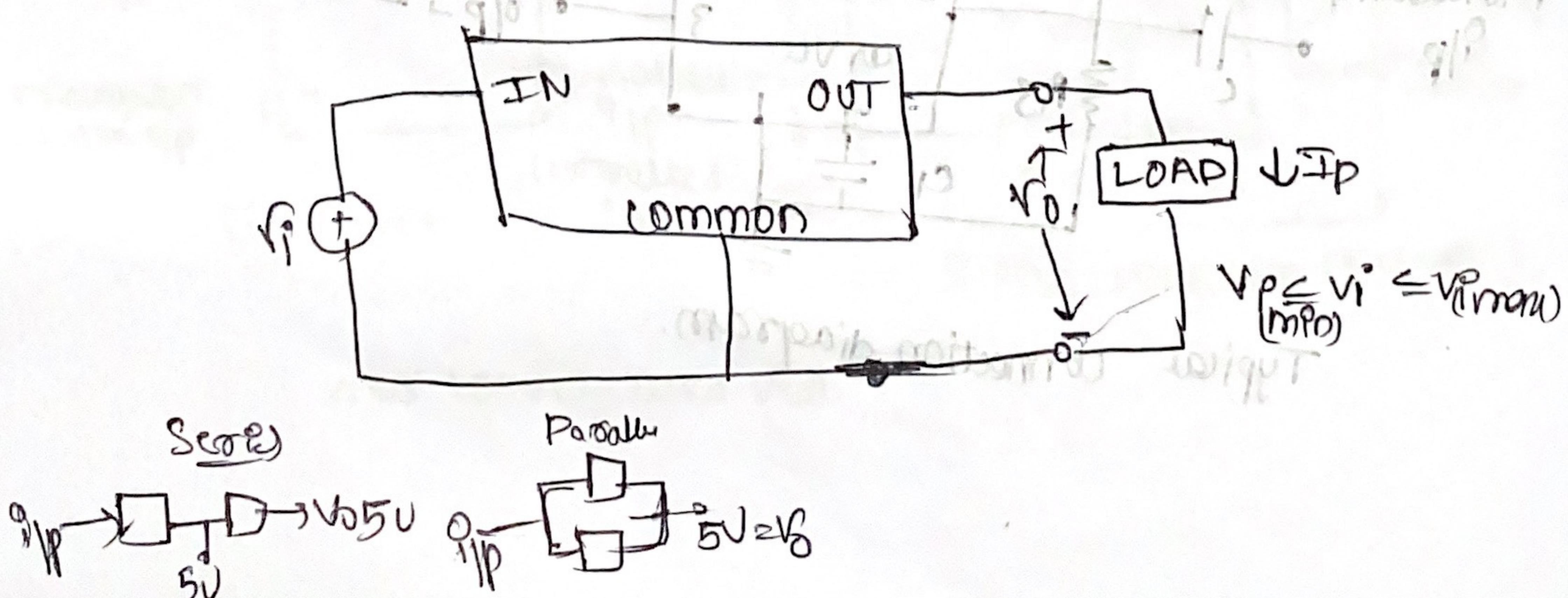


11/5/22

Voltage regulators & Voltage references:

→ Stabilize the O/P voltage (Voltage regulator).

LN78XX → 7805 (5V) 7812 (12V).  
79XX →



## Performance Specification:

- ① Line regulation
- ② Load Regulation.
- ③ Thermal coefficient.

① Line regulation =  $\frac{\Delta V_o}{\Delta V_i} \cdot (\text{mV or } \mu\text{V}) / \text{V} \cdot [\text{mV/V (or } \mu\text{V/V)}]$ .

$$(\%) = \frac{100 \times \Delta V_o / V_o}{\Delta V_i}$$

② Load regulation =  $\frac{\Delta V_o}{\Delta I_o} \cdot \mu\text{V/A (or } \text{mV/A)}$ .

$$(\%) = 100 \times \frac{\Delta V_o / V_o}{\Delta I_o}$$

③ Thermal coefficient ( $\text{TC}_{(V_o)}$ ) =  $\frac{\Delta V_o}{\Delta T} \cdot \text{mV/}^\circ\text{C (or } \mu\text{V/}^\circ\text{C)}$

$$(\%) = 100 \times \frac{\Delta V_o / V_o}{\Delta T}$$

$$= 10^6 \frac{\Delta V_o / V}{\Delta T} \text{ ppm/}^\circ\text{C} \quad (\text{For changing to parts per million})$$

(Q1) From the data sheet of MA7805, 5V voltage regulator indicates that  $V_o$  typically changes by 3mV when  $V_i$  is varied from 7V to 25V and by 5mV when  $I_o$  is varied from 0.25A to 0.75A estimate the line and the load regulation of the device also find the input impedance of regulator.

$$\text{Impedance } (R_o) = \frac{V_o}{\Delta I_o} = \frac{5}{0.5} = 10 \Omega$$

A)  $V_i \rightarrow 7V \text{ to } 25V$

$$V_o \rightarrow 5$$

$$I_o \rightarrow 0.25A \text{ to } 0.75$$

$$\Delta V_o = 3 \text{ mV}$$

$$\Delta V_i = 18 \text{ V}$$

$$\text{Line regulation} = \frac{3}{18} \times 10^3$$

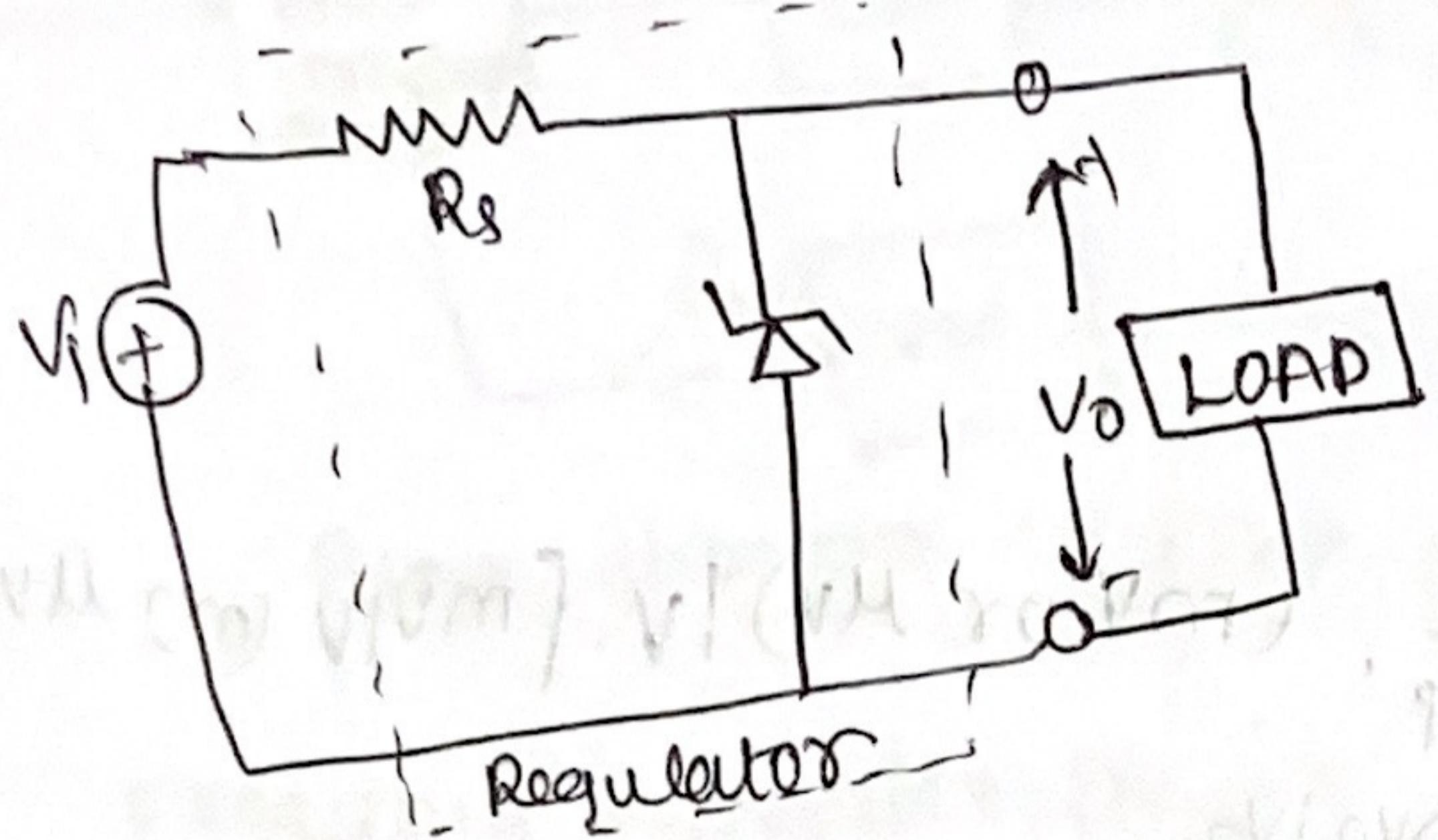
$$\text{Line regulation} = 0.16 \frac{\text{mV}}{\text{V}}$$

$$(R_o) \text{ Impedance} = 10 \Omega$$

$$\Delta V_o \rightarrow 5 \text{ mV } (I_o)$$

$$\text{Load} = \frac{\Delta V_o}{\Delta I_o} = \frac{5 \text{ mV}}{0.50} = 10 \frac{\text{mV}}{\text{A}}$$

Shunt regulators



(Q2) The Datasheet of REF101KM 10V precision voltage reference gives a typical line regulation of  $0.001\%/\text{V}$ , a typical load regulation of  $0.001\%/\text{mA}$  and a maximum thermal coefficient of  $1\text{ppm}/^\circ\text{C}$ . find the variation of  $V_o$  brought by (i) change of  $V_i$  from 13.5V to 35V,

$$\textcircled{1} \pm 1\text{mV}$$

$$\textcircled{2} \pm 10\text{mA} \text{ change in I}_o$$

$$\textcircled{3} 1\text{mA}$$

$$\textcircled{3} \text{ Temperature change from } 0^\circ\text{C to } 70^\circ\text{C}$$

Ans)

$$V_o = 10\text{V}$$

$$\text{(i)} \quad \Delta V = 9.5\text{V}$$

$$0.001 = \frac{100 \times \frac{\Delta V}{10}}{9.5}$$

$$\Rightarrow \Delta V = 9.15\text{mV}$$

$$\text{(ii)} \quad \frac{0.001}{10^{-3}} = \frac{100 \times \frac{\Delta V}{10}}{10}$$

$$\Delta V = 1\text{mV}$$

$$\text{(iii)} \quad \Delta T = 70^\circ\text{C}$$

$$1 = 10^6 \times \frac{\Delta V / V_o}{\Delta T}$$

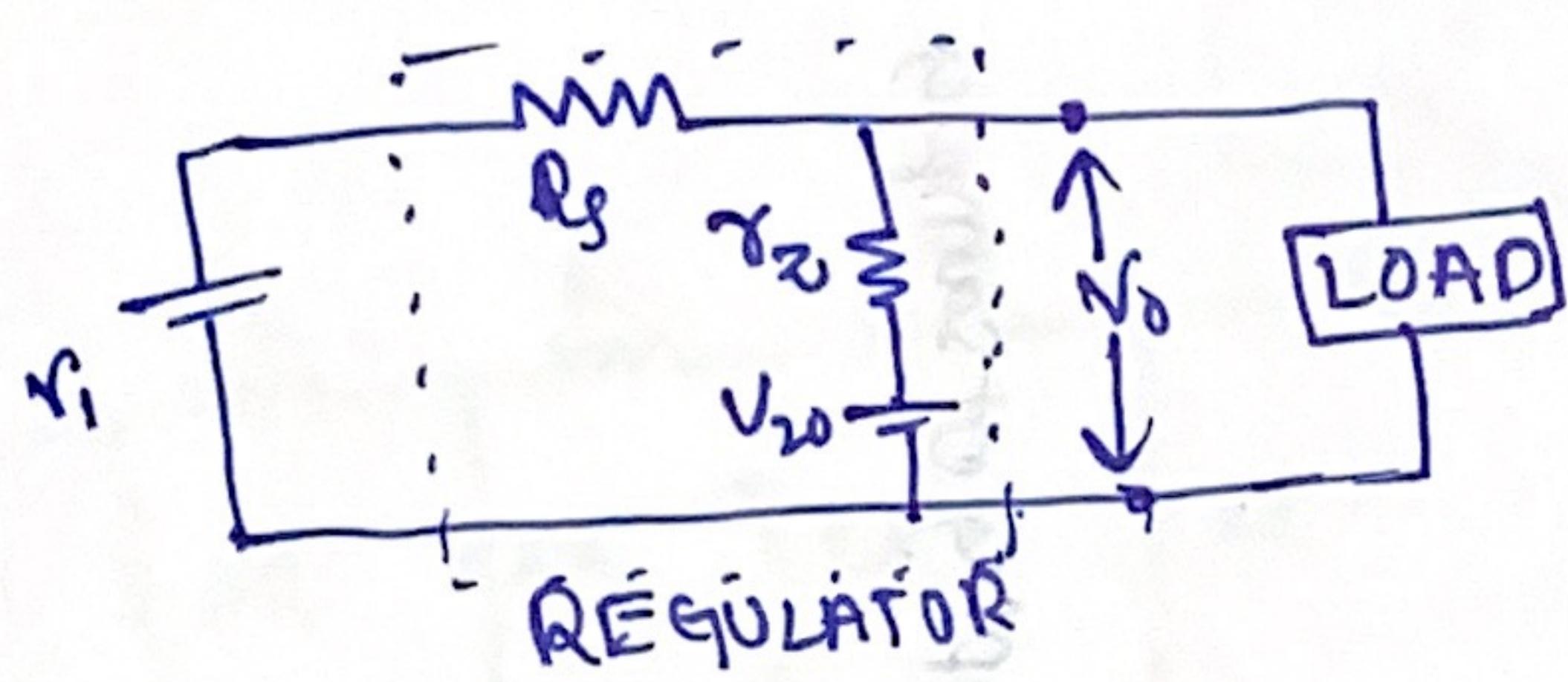
$$1 = 10^6 \times \frac{\Delta V}{10}$$

$$70$$

$$\frac{70}{10^5} = \Delta V \Rightarrow \Delta V = 0.7\text{mV}$$

25-5-22

shunt regulator:



$$V_o = V_{20} + \tau_z I_z$$

$$V_o = V_{20} + R_s I_o$$

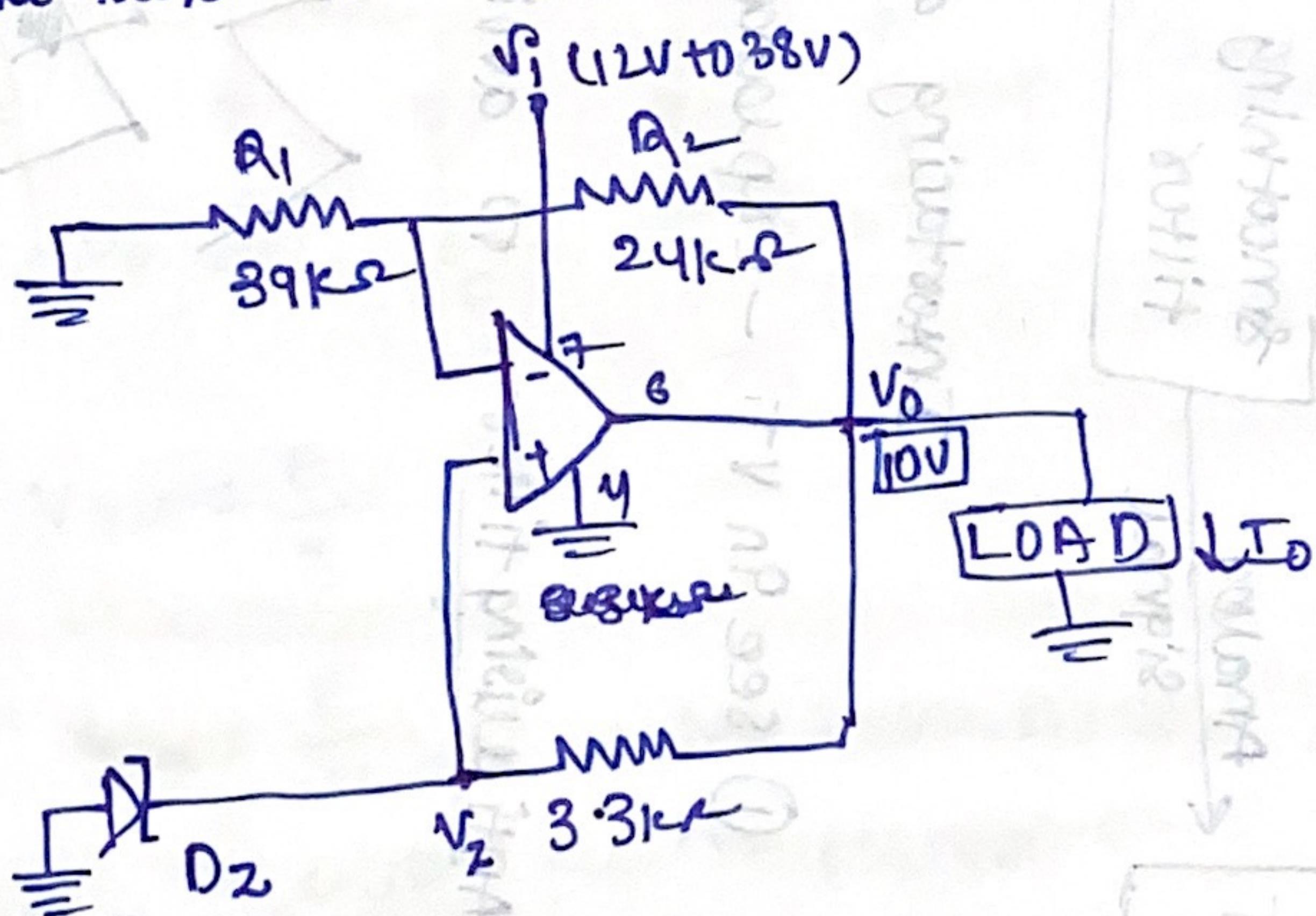
$$V_{20} = 5.43V.$$

$$I_z = \left( \frac{P_z}{2} \right) / V_z$$

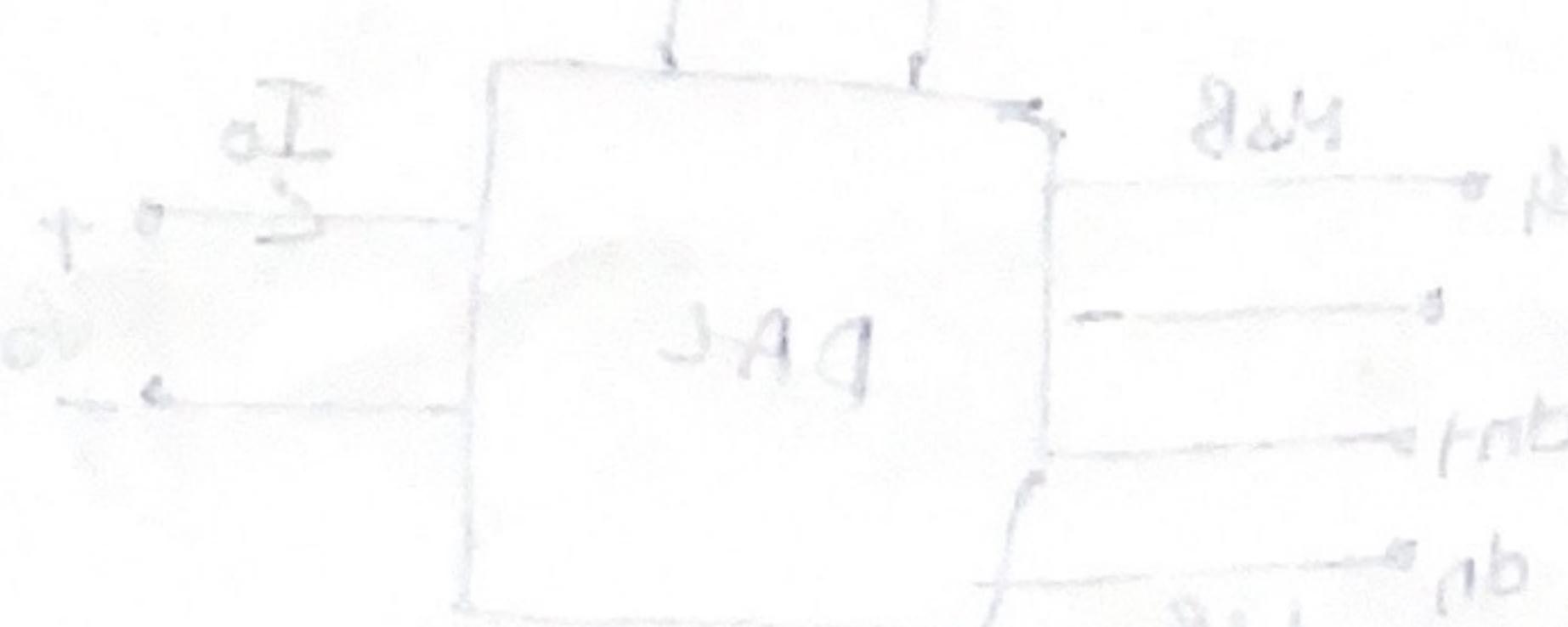
$$\text{line regulation} = \frac{\Delta V_o}{\Delta V_i}$$

$$\text{load regulation} = \frac{\Delta V_o}{\Delta I_o}$$

Selv regulated 10V reference circuit:

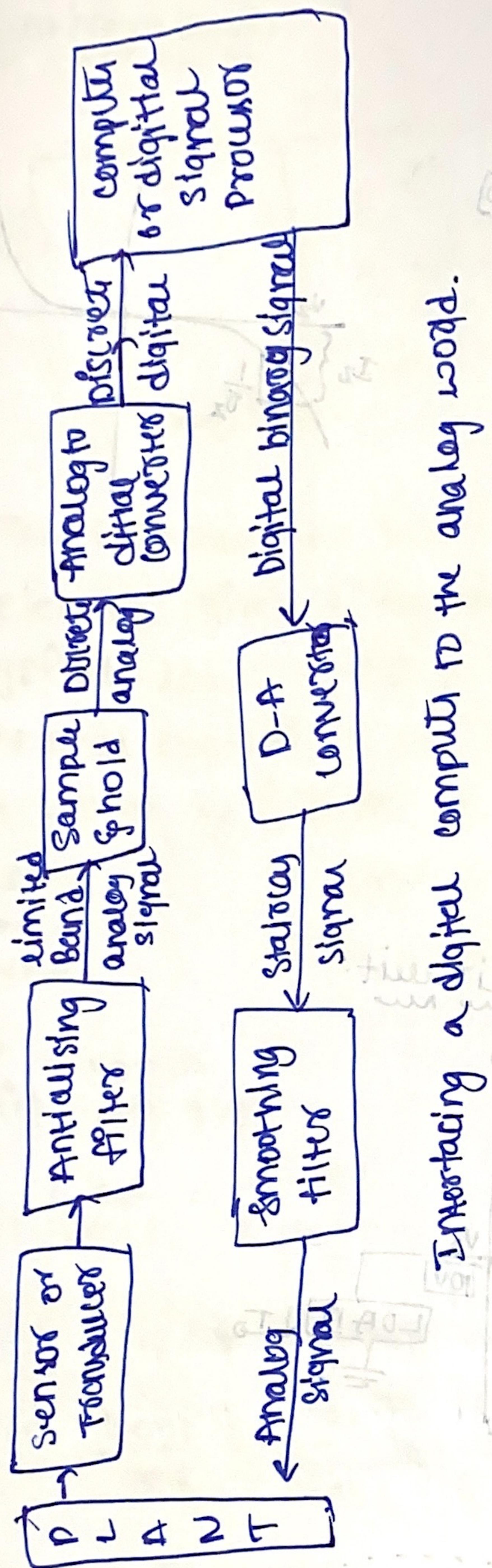


$$V_o = \frac{\tau_z}{R_s + \tau_z} V_i + \frac{R_s}{R_s + \tau_z} V_{20} + (R_s || \tau_z) I_o$$



using a rapid response higher gain  
higher initial & higher output e

\* 3m

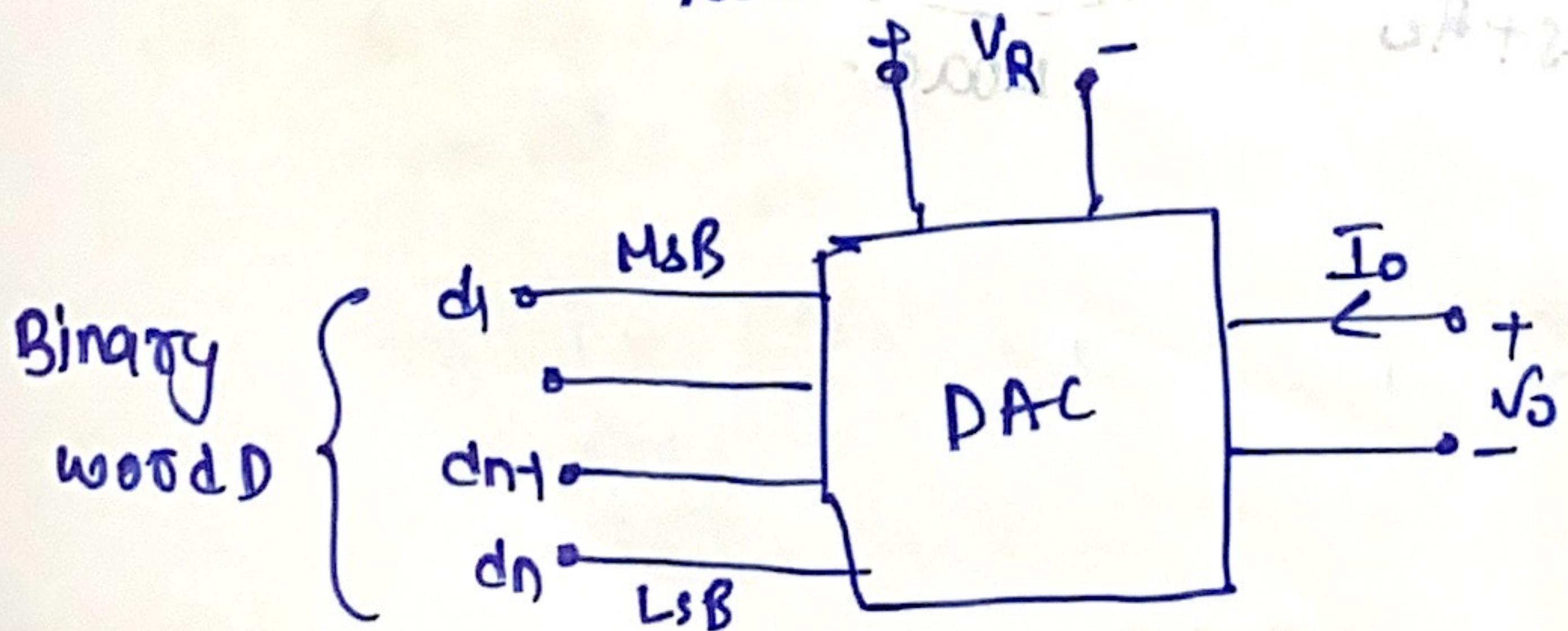


Interstating a digital computer to the analog word.

① See Qn VT - explanation.

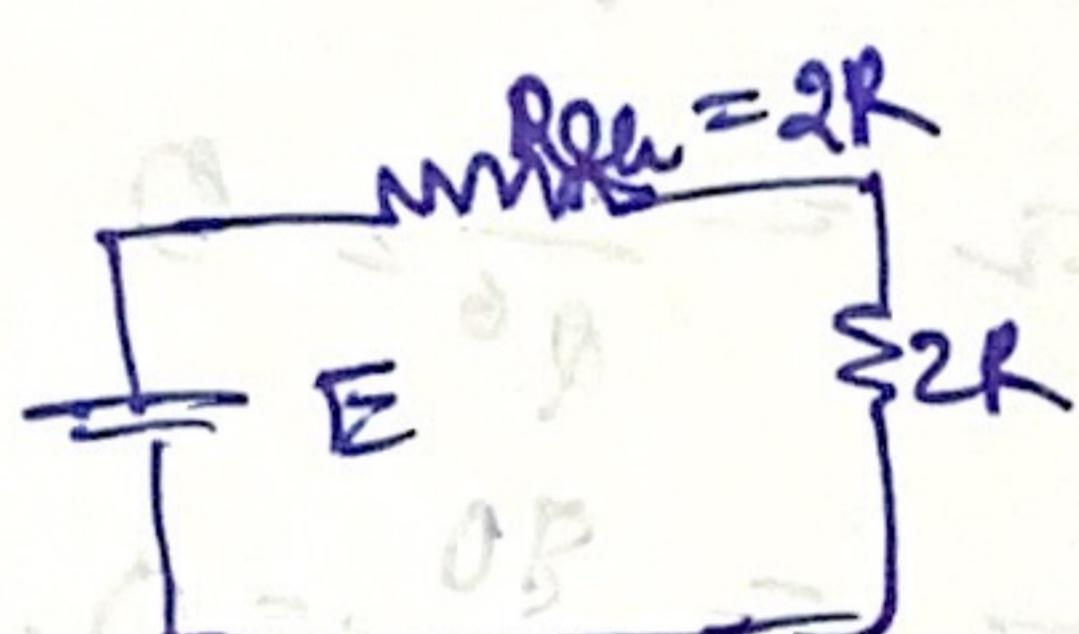
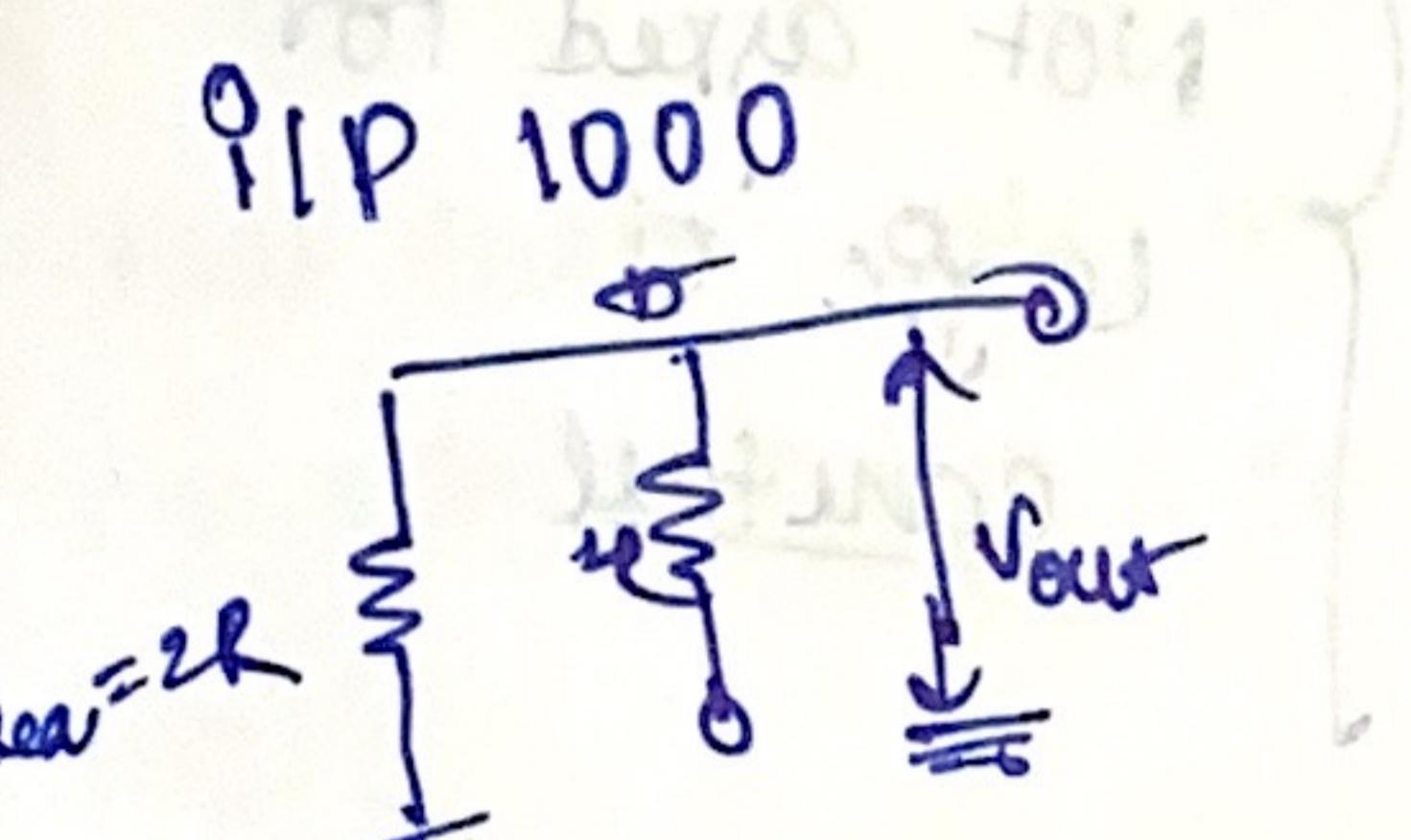
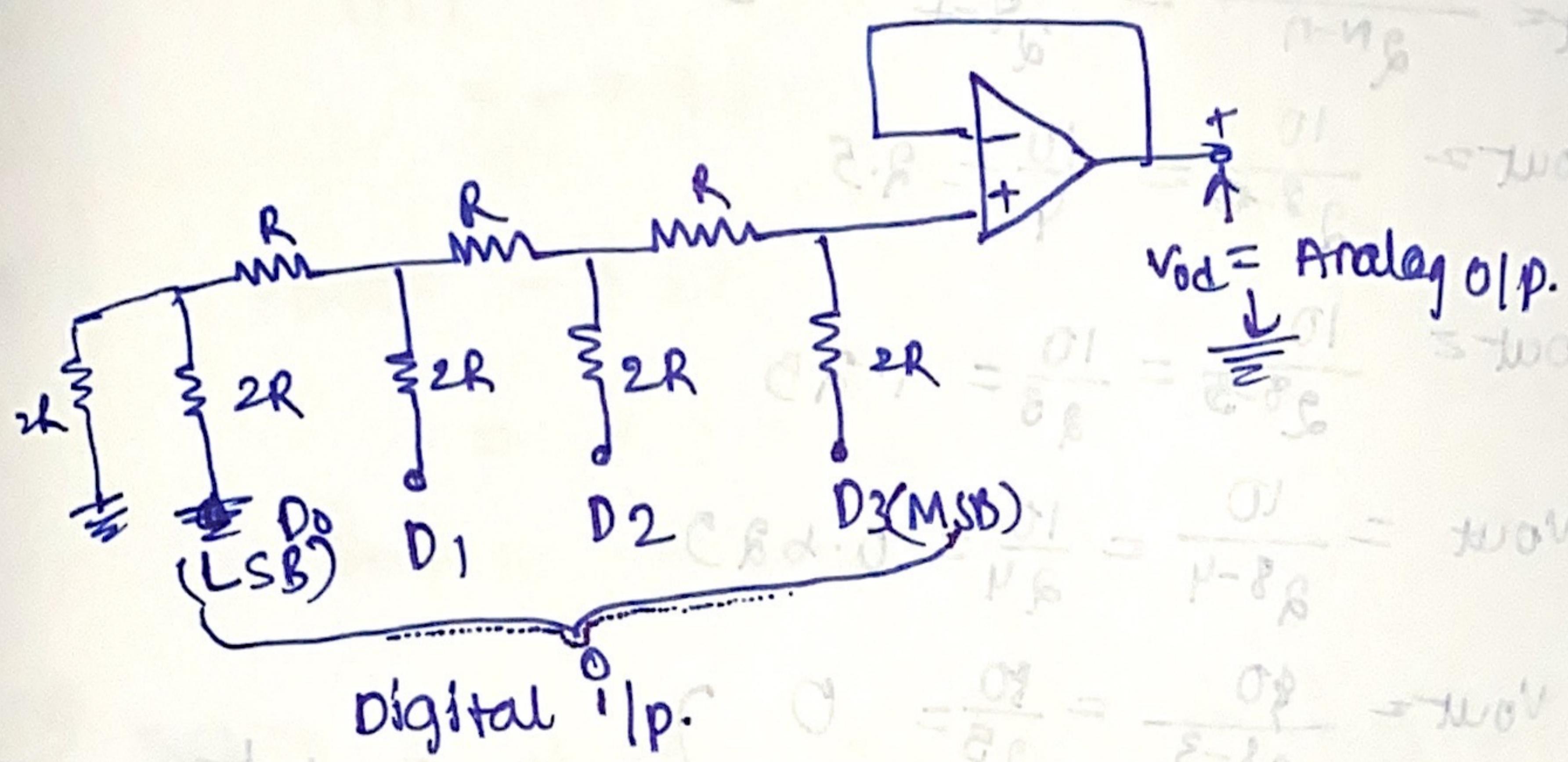
Anti aliasing filters → avoid loss of signals due to overlapping of samples

Schematic of DAC:



Voltage output  $\propto$  input binary number.  
→ Analog output =  $k \times$  digital output

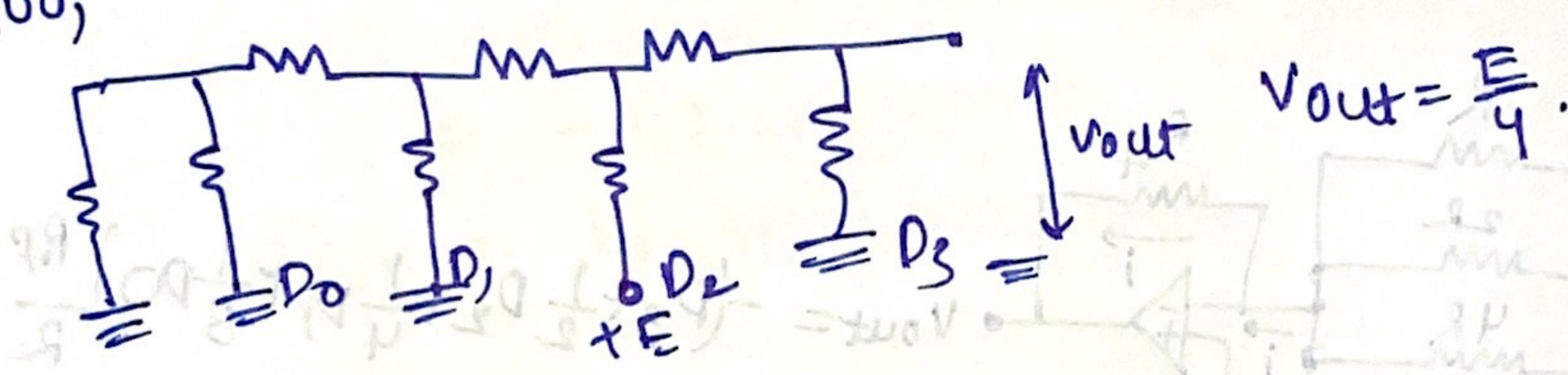
R-2R ladder type DAC:



$$V_{out} = E \left( \frac{2R}{2R + QR} \right) = \frac{E}{2}$$

(\*) When  $I/p = 0100 = 0010 = 0001 \rightarrow V_{out} = ??$

0100,



0010)

$$V_{out} = \frac{E}{8}$$

0001)

$$V_{out} = \frac{E}{16}$$

$N = \text{total no. of binary bits}$   
 $D_n \text{ bit}, V_{out} = \frac{E}{2^{N-n}}$  position of bit where QIP is high.

Eg:  $D_3 D_2 D_1 D_0$

$$V_{out} = \frac{5}{2^4 - 2} = \frac{5}{4}$$

(i) what are the output voltages caused by logic 1 at each bit position in a R-2R ladder with QIP 11110001 if the input level for 0 is 0V and that for 1 is 10V?

Q1)  $D_7 = 11110001$ .

$$D_7 = V_{out} = \frac{E}{2^{N-n}} = \frac{10}{2^{8-7}} = 5$$

$$D_8 = V_{out} = \frac{10}{2^{8-6}} = \frac{10}{4} = 2.5$$

$$D_5 = V_{out} = \frac{10}{2^{8-5}} = \frac{10}{2^3} = 1.25$$

$$D_4 \Sigma \quad V_{out} = \frac{10}{2^{8-4}} = \frac{10}{2^4} = 0.625$$

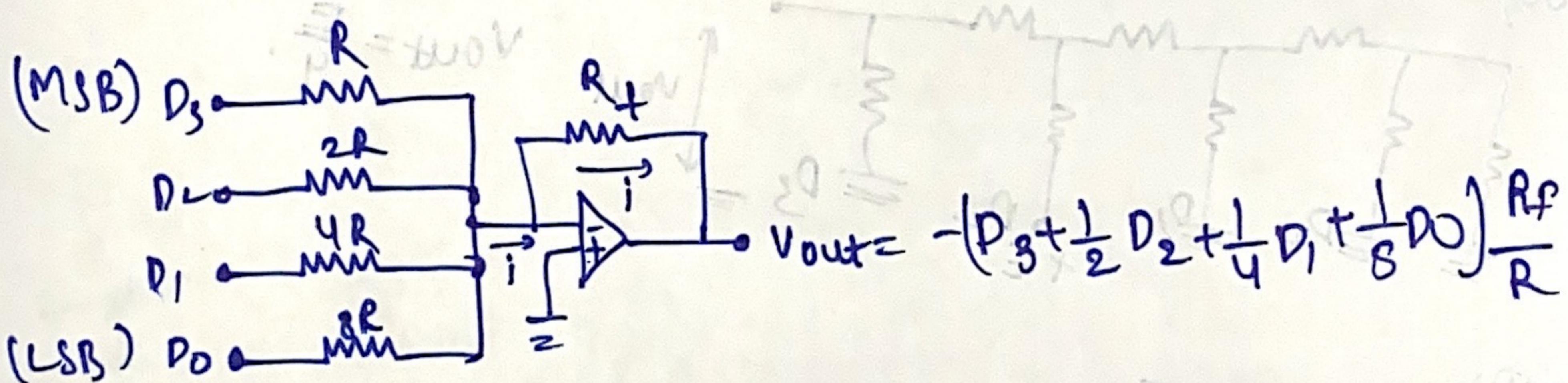
$$D_3 = V_{out} = \frac{10}{2^{8-3}} = \frac{10}{2^5} = 0$$

$$D_2 = V_{out} = \frac{10}{2^{8-2}} = \frac{10}{2^6} = 0$$

$$D_1 = V_{out} = \frac{0}{2^{8-1}} = \frac{0}{2^7} = 0$$

$$D_0 = V_{out} = \frac{10}{2^8} = \frac{10}{256} = 0.0391$$

Weighted resistor type DAC:



Q2)

- (a) For the 4 bit weighted resistor DAC, determine (a) the weight of each input are 0V and 5V, (b) the full scale output, if  $R_f = R = 1k\Omega$  Also, (c) find the scale output if  $R_f$  is changed to  $500\Omega$ .

(b) (a)  $\frac{R_f}{R} = 1$

$D_3 \Rightarrow$  MSB  $\rightarrow$  gain = 1  $\Rightarrow$  weight = 5V

$$V_{out} = \left( D_3 + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8} \right) \frac{R_f}{R}$$

$D_2 =$  gain =  $1/2 \Rightarrow$  weight =  $5/2 = 2.5V$

$D_1 =$  gain =  $1/4 \Rightarrow$  weight =  $5/4 = 1.25V$

$D_0 =$  gain =  $1/8 \Rightarrow$  weight =  $5/8 = 0.625V$

Not asked for  
logic '0'  
cancel

(b) full scale OIP is when all QIP are high.

111

$$= -9.375V.$$

e)  $V_{out} = -9.375 \times \frac{500\Omega}{1k\Omega}$   
 $= -9.375 \times 0.5$   
 $\sqrt{V_{out}} = -4.6875V$ .

Q2) Design a 4-bit weighted resistor DAC whose full scale OIP voltage is -5V. The logic levels are 1 = +5V and 0 = 0V - what is OIP voltage when QIP is 1101?

A)  $V_{out} = -\left(D_3 + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8}\right) \frac{R_f}{R}$

REARRANGE

$$= -\left(5 + 2.5 + 0 + 0.625\right) \times 500 \times 0.53$$

$$= -(8.125) \times 0.53$$

$$V_{out} = -4.3V$$

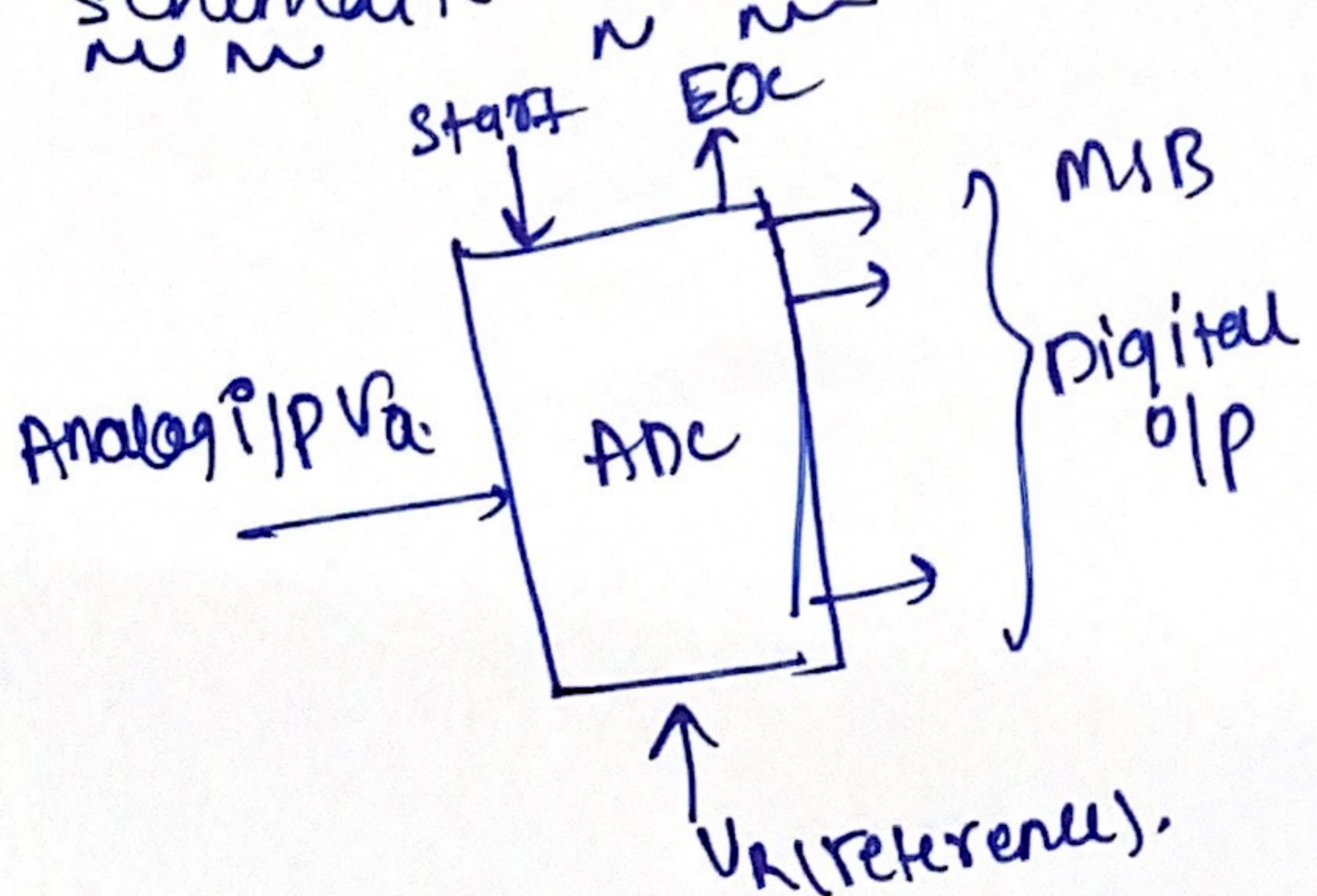
$$-5 = -9.375 \times \frac{R_f}{R}$$

$$\frac{R_f}{R} = 0.53$$

$$R = 1k\Omega$$

$$R_f = 530\Omega$$

schematic of DAC:



classification Based on their conversion Techniques

### Direct type DAC:

- Compare a given analog signal with the internally generated equivalent.

.

### Integrating type ADC:

- performs a conversion in a sequential manner by first changing the analog input signal to a linear function of time or frequency then to a digital code.

#### A1) Counter type ADC:

