MANIPAL INSTITUTE OF TECHNOLOGY
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DEPARTMENT OF INSTRUMENTATION AND CONTROL ENGINEERING

ANALOG CIRCUITS LABORATORY MANUAL – ICE 2261

IV SEMESTER B.TECH

Students Name: .....

Registration Number: .....

Signature: .....

March 2022

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
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Department of Instrumentation & Control Engineering
Manipal Institute of Technology, Manipal
A Constituent unit of MAHE, Manipal

MANIPAL-576104

CERTIFICATE

This is to certify that the Laboratory Manual for the lab titled Analog Circuits Laboratory submitted by Mr/Ms _____ (Reg. No.:_____) of IV Semester of Electronics and Instrumentation Engineering for the academic year 2021-2022 has been submitted as per laboratory course requirements, which has been evaluated and duly certified.

Place:

Date: Lab In-Charge

ICE-2261 ANALOG CIRCUITS LAB [0-1-3-2]

Total number of Lab Sessions: 10

CONTENTS

Evaluation plan

- Internal Assessment Marks : 60%
  - ✓ Continuous evaluation component (for each experiment):10 marks
  - ✓ The assessment will depend on punctuality, circuit implementation, maintaining the observation note and answering the questions in viva voce
  - ✓ Total marks of the 10 experiments reduced to marks out of 60

- End semester assessment of 2 hour duration: 40 %

EXPT. 1: WAVE SHAPING CIRCUITS USING DIODES

Aim: To study clipping and clamping circuits using diodes.

Equipment and Components Required: DC power supply**,** Digital Storage Oscilloscope **(**DSO), Audio Frequency Oscillator (AFO), Digital Multi Meter (DMM), Diode 1N4007/ BY127 & discrete components.

A. CLIPPING CIRCUITS:

Rig up the following circuits. For sinusoidal input signal observe the output waveform and the transfer characteristics on the DSO.

Circuit diagrams: Choose R= 3.3kΩ.

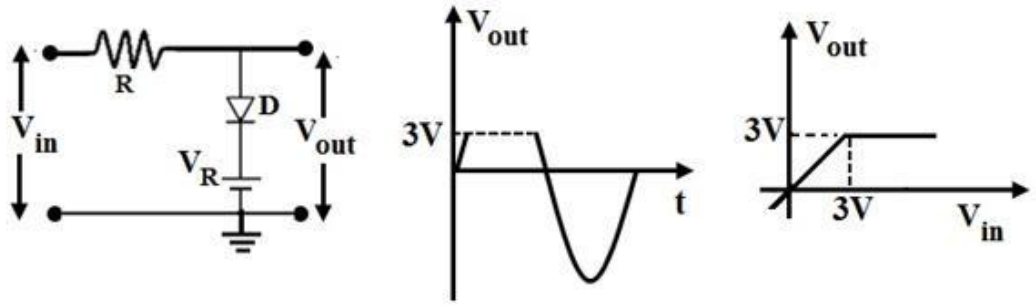


Fig. 1.1 (a) Shunt Clipping Circuit (b) Output Waveform (c) Transfer Characteristic

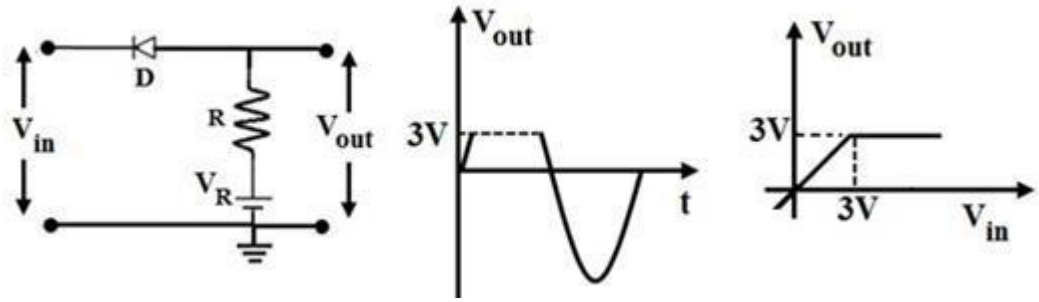


Fig. 1.2 (a) Series Clipping Circuit (b) Output Waveform (c) Transfer Characteristic

Note: 1. Waveforms shown are for ideal diode. Sketch the practical waveforms.

2. $V_{out(max)} = V_\gamma + V_R$ (where V_γ = 0.6V for (BY127)

Example: If output V_{out} to be clipped to 3V, V_R = 3.0 - 0.6V = 2.4V.

B. CLAMPING CIRCUITS:

Rig up the following circuits. For sinusoidal input signal observe the output waveform.

Selection of R and C:

If R_f – Diode forward resistance = 100Ω, Rr – Diode Reverse resistance = 1MΩ.

$R = \sqrt{R_f R_r}$ = 10kΩ, RC >> T = 1ms [f =1 kHz]

Let RC = 10T = 10ms, Hence C = 1μF.

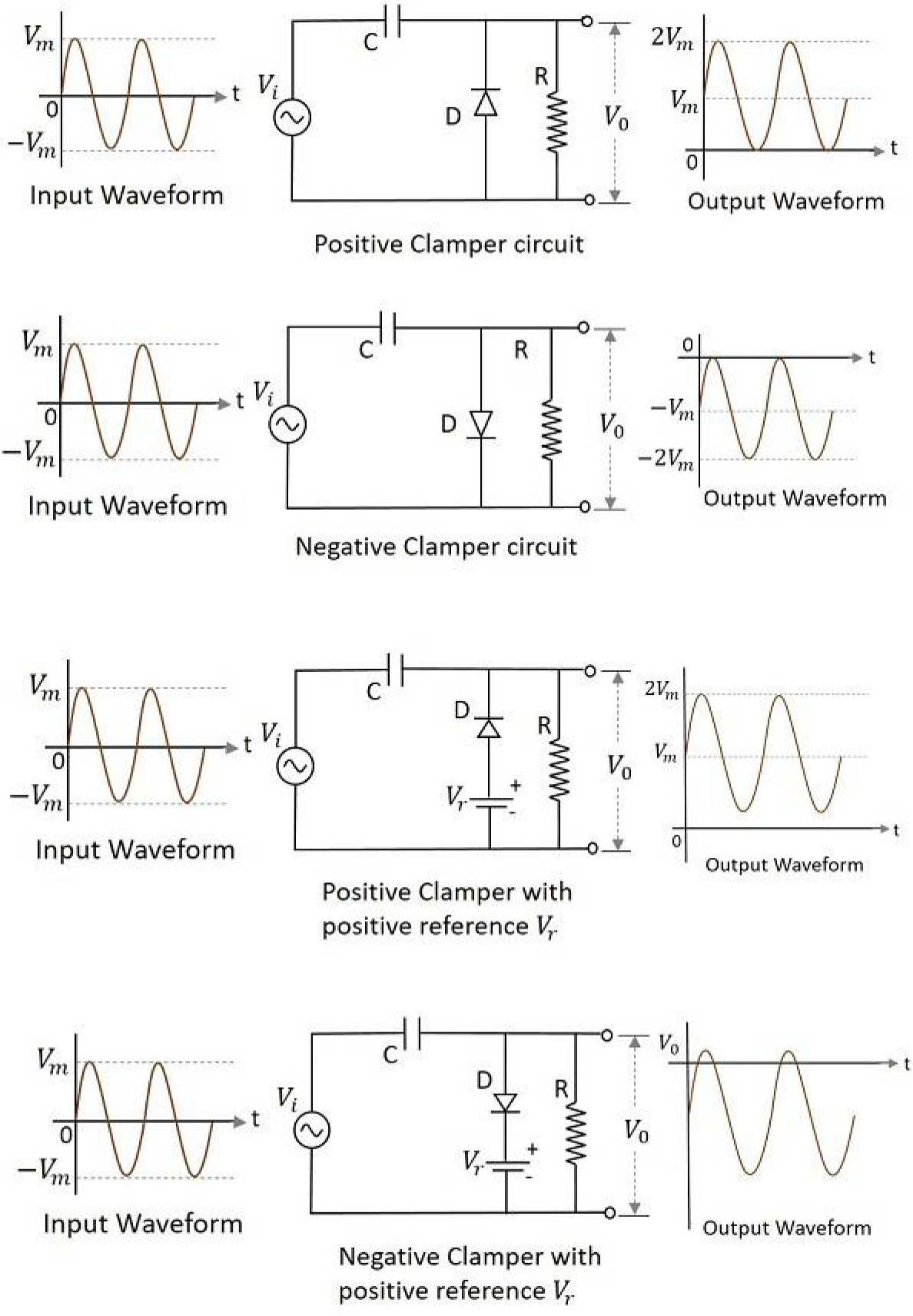
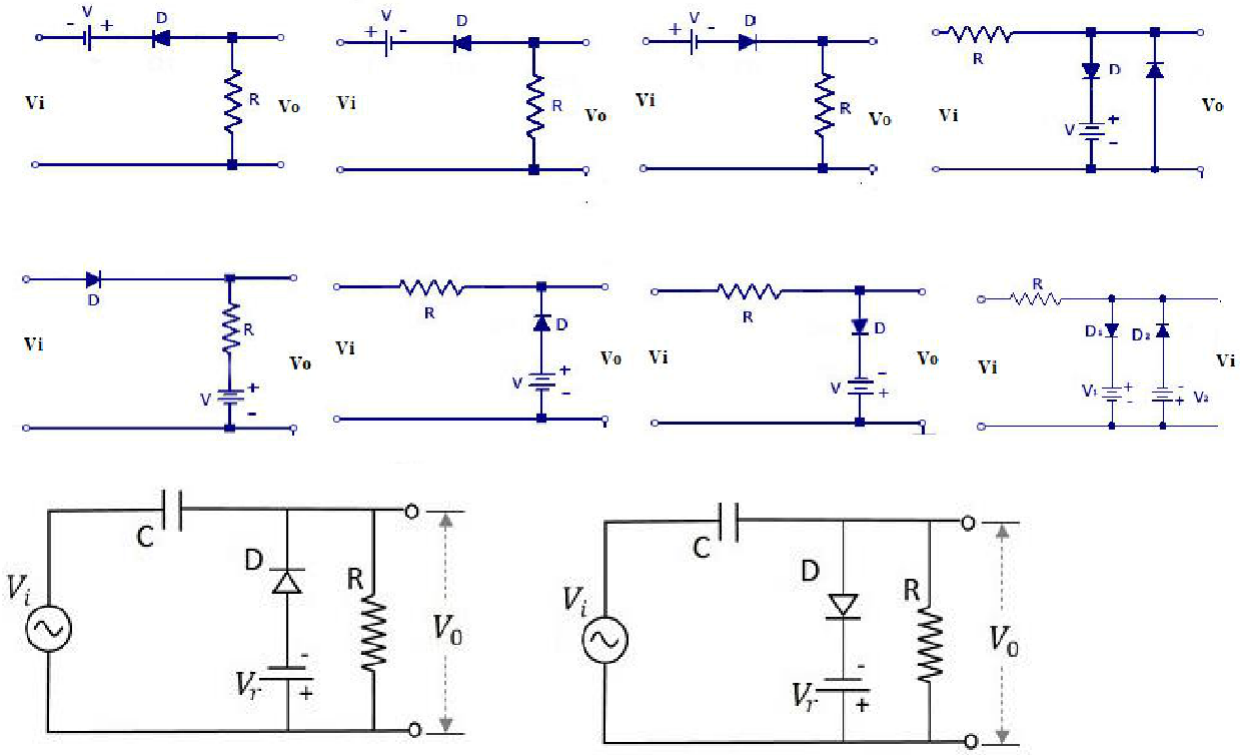


Fig. 1.3: Different Clamper Circuits with its sample output.

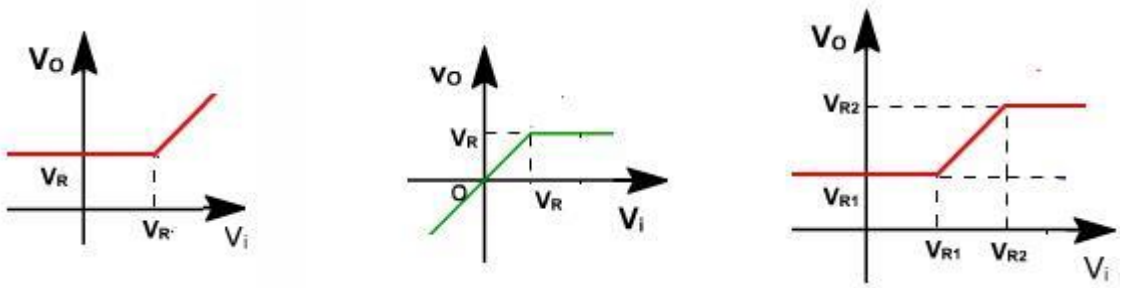
Conclusion/ inference:

Experiments for Further Practice

1. For each of the following circuit draw output wave form for sinusoidal input.



2. Design circuits having following transfer characteristics.



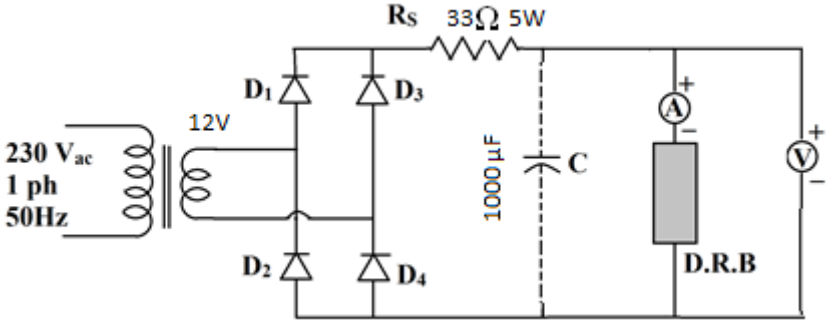
3. Clamp the positive peak of a square wave of 20V pp to 3V.

EXPT. 2: BRIDGE RECTIFIER AND ZENER VOLTAGE REGULATOR

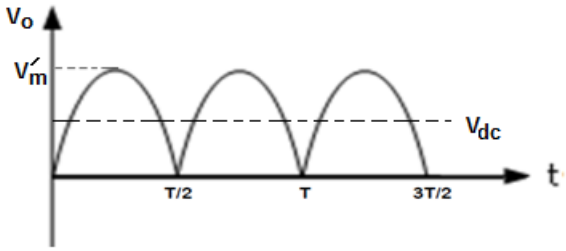
Aim: To study a bridge rectifier circuit and Zener voltage regulator.

Equipment and Components required: DC power supply, Step down transformer, DMM, Diode 1N4007/ BY127, Zener diode, Decade Resistance Box (DRB) & discrete components.

2.1: Full-wave bridge rectifier:



Output waveform without C Filter:



Output waveform with C Filter:

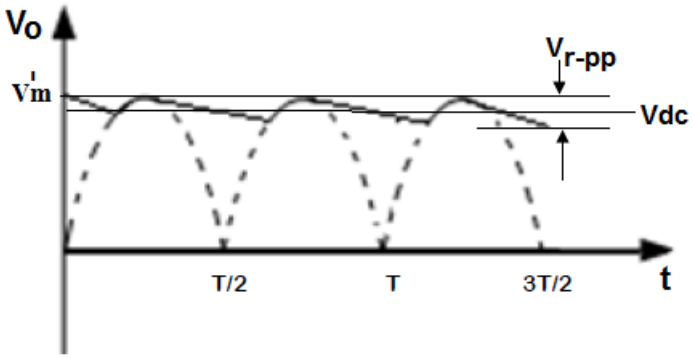


Fig. 2.1: Full wave bridge rectifier with its sample outputs.

Precaution: Do not try to observe both the input and output at the same time in dual mode of the oscilloscope. This may lead to short-circuit in the circuit (it may burn some of the components).

Procedure:

a. FWR without filter:

1. Connect the circuit as per circuit diagram shown without connecting capacitor.
2. Connect DMM and DSO across the load, set DRB value to 200Ω.
3. Note down the values of V_{DC}, V_{AC}, I_L for R_L between 200 to 800Ω in steps of 100Ω.
4. Calculate theoretical and practical values of ripple factor.

5. Observe the waveform on DSO.

b. FWR with filter:

1. Connect the circuit as per circuit diagram shown in figure with capacitor.
2. Connect DMM and DSO across the load, set DRB value to 200Ω.
3. Note down the values of V_{DC}, V_{AC}, I_L for R_L between 200 to 800Ω in steps of 100Ω.
4. Calculate theoretical and practical values of ripple factor.

Ripple factor with Capacitor filter = $1/\left(4\sqrt{3}f_r C R_L\right)$

Tabular Column:

1. Without Filter

R_L	V_{dc} (Volts)	V_{ac} (Volts)	I_L (mA)	Ripple factor	
				Theoretical	Practical V_{ac}/V_{dc}

2. With capacitor Filter

R_L	V_{dc} (Volts)	V_{ac} (Volts)	I_L (mA)	Ripple factor	
				Theoretical	Practical V_{ac}/V_{dc}

2.2: Zener voltage regulator:

Design a voltage regulator using zener diode to provide output voltage of 5V at 150 mA.

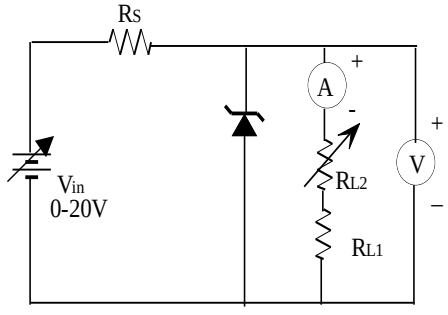


Fig. 2.2: Zener Voltage Regulator

Design hints:

R_{L1}= 5.0/150mA ≈ 33 ohm (1W); R_{L2}=5.0/40mA-R_{L1} ≈ 100 ohm;

$Rs = (V_{smin} - V_0) / (I_z + I_L max) = (10-5) / (25mA+151.5mA) = 33$ ohm (5W)

Procedure:

1. Rig the circuit as shown in fig. 2.2.
2. For line regulation, increase the input voltage from 10 – 20V in steps using the power supply and note down the input and output voltages for a prefixed value of load current (say 60mA).
3. For load regulation, keep the input voltage constant say at 10V and vary the load resistance and note down the corresponding output voltage.
4. Reduce the input voltage to Zero and switch off the power supply.

Load Regulation**:** V_{in} =

Load Current I_L (mA)	Output Voltage V_0 (V)

Line regulation: I_L =

Input Voltage V_1 (V)	Output Voltage V_0 (V)

Sample Viva Questions

1. What is depletion region or space charge region?
2. What is junction potential or potential barrier in PN junction diode?
3. How do you identify the resistance of a resistor?
4. Name different types of capacitors.
5. Explain difference between clipper and clamper circuit.
6. What are clipping circuits? Classify them.
7. What are clamping circuits? Classify them. Mention the application of clipping circuits
8. What is the other name of clamping circuits?
9. Mention the applications of clamping circuits.
10. Define a rectifier? What are the merits of FWR over HWR?
11. What are the disadvantages of centre-tapped FWR?
12. What is PIV? What is its importance? What is the PIV of HWR, centre-tapped FWR and bridge rectifier?
13. What is the PIV of HWR, centre-tapped FWR and bridge rectifier?
14. What are the merits of bridge rectifier?
15. What is the function of shunt capacitor filter?
16. Define the following: (i) ripple factor (ii) rectification efficiency (iii) voltage regulation (iv) PIV of a diode (v) knee voltage or cut-in voltage
17. What is the output frequency of a FWR?
18. What is the need for the transformer in the rectifier circuit?
19. What are the applications of a rectifier?
20. Why capacitor filter is preferred for light load applications?

EXPT. 3: COMMON EMITTER AMPLIFIER

Aim: To obtain the frequency response, input resistance and output resistance of common emitter amplifier using BJT.

Equipment and components required:

DC Power supply, AFO, DSO, DMM, DRB, Transistor BC107, Discrete Components.

Circuit diagram:

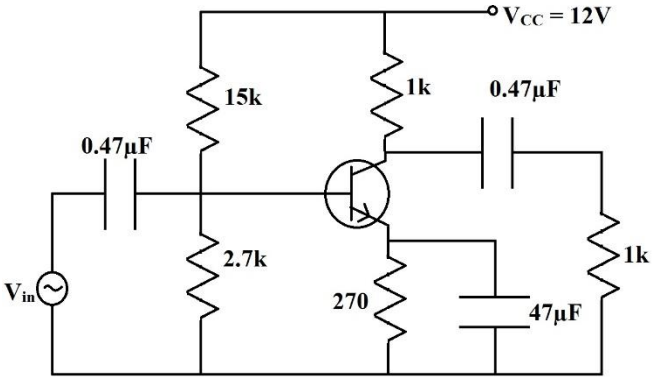


Fig. 3.1: Circuit diagram of common emitter amplifier

Fig. 3.2: Pin diagram of SL 100

Design Hints:

V_{CC} = 12V, I_C = 4.5mA, V_E = 1.2V, V_{CE} = 6V, hfe = 100.

$R_E = {V_E}/{I_E} \approx {V_E}/{I_C} = 270\Omega,\ R_C = \frac{(V_{CC} - V_{CE} - V_E)}{I_C}$

$V_{CC} = I_C R_C + V_{CE} + V_E \rightarrow R_C = 1k\Omega$

$hfe \times R_E = 10R_2 \rightarrow R_2 = 2.7k\Omega$

$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} \rightarrow R_1 \simeq 15k\Omega$

Use $C_{C_1} = 0.47\mu F, C_{C_2} = 0.47\mu F, C_E = 47\mu F$

Procedure:

1. Rig up the circuit as shown in Fig. 3.1.
2. Apply DC supply voltage to the circuit. Measure and record all the dc parameters listed in Table 3.1 in the absence of ac input signal to find Q point.
3. Apply ac sinusoidal input of 50 mV peak-to-peak and 1 kHz frequency.
4. Observe the input and output waveforms simultaneously on the DSO.
5. Determine the maximum signal handling capacity by increasing the input voltage just before the output signal gets distorted.
6. By keeping amplitude of V_{in} constant, vary the frequency from 10 Hz to 1MHz, note down the output voltages as shown in Table 4.2.
7. Plot the frequency response (gain in dB Vs input frequency) on a semi-log graph sheet and determine the bandwidth.

Table 3.1: Observation of DC values

Parameter	Computed value	Observed value
$V_B = V_{cc}R_2 / (R_1+R_2)$		
$V_E = V_B - V_{BE}$		
$I_C \approx I_E = V_E/R_E$		
$V_{CE} = V_{CC} – I_C (R_C+R_E)$		

Operating point (V_{CEQ}, I_{CQ}) = _____

Table 3.2: Frequency Response

V_{in} = _____ (mV)

Frequency (Hz)	Output Voltage (V_O)	Gain(V_O/V_{in})	Gain in dB $20 \log(V_O/V_{in})$

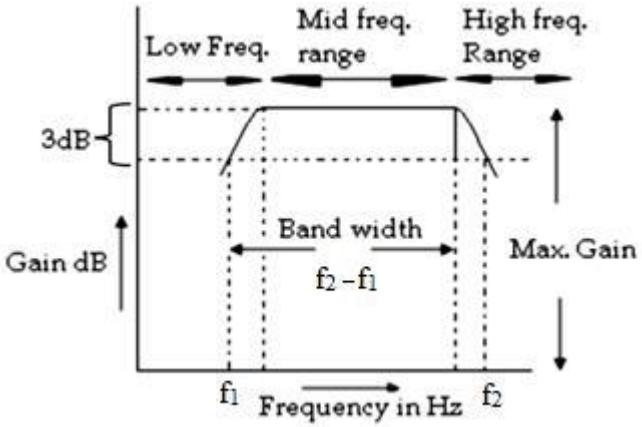


Fig. 3.3. Frequency response plot

To calculate the input impedance:

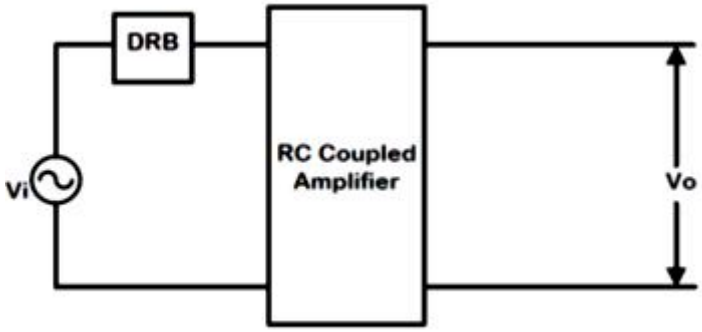


Fig. 3.4. Measurement of input resistance

Procedure:

1) Keep the DRB at minimum position and connect it in series with the input as shown in Fig. 3.4.
2) Set the circuit to work in the mid band region and note down the output voltage.
3) Increase the value of resistance until output voltage is reduced to half.
4) The value of DRB is the input resistance of the circuit.

To calculate the output impedance:

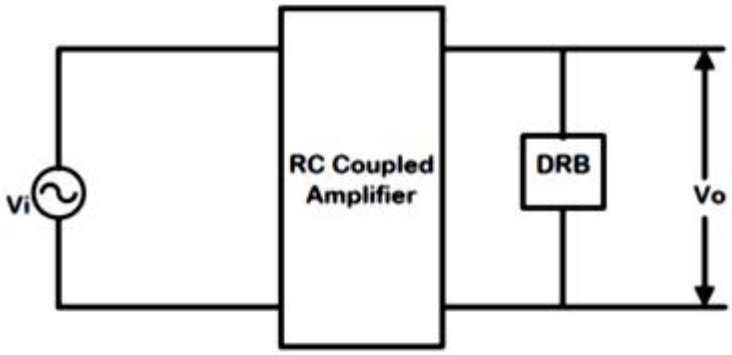


Fig. 3.5. Measurement of output resistance

1. Keep the DRB at maximum position and connect it in parallel with the output as shown in Fig. 3.5.
2. Set the circuit to work in the mid band region and note down the output voltage.
3. Decrease the value of resistance until output voltage is reduced to half.
4. The value of DRB is the output resistance of the circuit.

Part B:

Remove the bypass capacitor C_E and observe the gain of the amplifier.

Viva Questions

1. What is the figure of merit of the amplifier?
2. What is the need for coupling capacitors?

3. Define α, β of a transistor.
4. Why CE configuration is preferred for voltage amplification?
5. What is the phase relation between input and output in CE and CC configurations?
6. Which region of transistor operation is preferred for amplifier applications?
7. What is the effect of bypass capacitor?
8. What is the need for transistor biasing? Why is it necessary?
9. How do you classify amplifiers?
10. What is faithful amplification? How do you achieve this?
11. What is the need for coupling in amplifiers? Name different types of coupling used in multistage amplifiers.
12. What is operating point or quiescent point?
13. What is the significance of the frequency response of an amplifier?
14. What are the advantages of RC coupled amplifier?
15. What are half-power frequencies? What is the significance of 3dB frequency?
16. What is D.C load line?
17. Why do we choose the Q point at the centre of the load line?
18. What is a bipolar and unipolar device? Give examples
19. Why transistor is called current controlled device?
20. What do you mean by thermal runway?
21. What is semi-log graph sheet? Why it is used to plot frequency response? Explain the use of the decibel unit.
22. Why common collector amplifier is known as emitter follower circuit?
23. What is the need for coupling capacitor and bypass capacitor? How do you select their values?
24. Mention the application of emitter follower circuit. What is Darlington emitter follower circuit?
25. Draw a dc equivalent circuit and ac equivalent circuit for a RC coupled amplifier.

EXPT. 4: CLASS B AMPLIFIER

Aim: To study complementary symmetry Class B Push Pull Power Amplifier.

Equipment and Components Required: Dual source DC power supply, AFO, DSO and discrete components, probes and wires.

Circuit diagram:

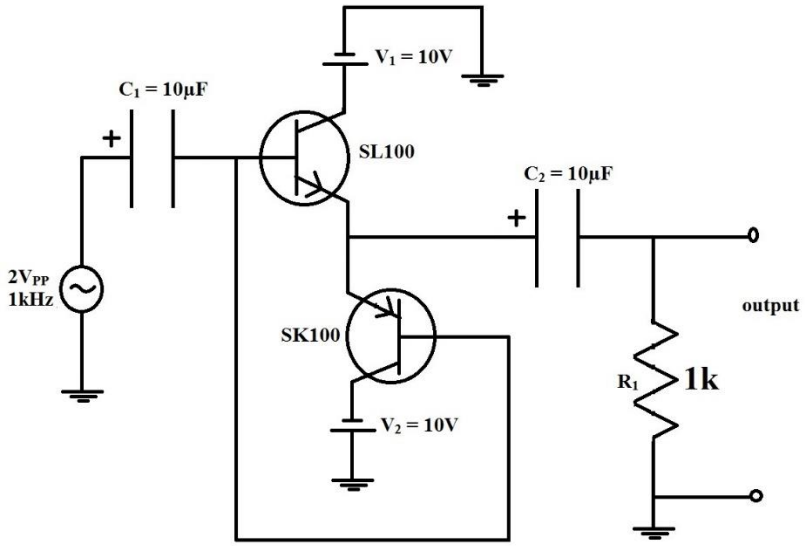


Fig 4.1: Complementary symmetry push pull amplifier

Design Hints:

$$P_O = \frac{V_{L(P)}^2}{2R_L}$$

$$P_i = V_{CC}\left(\frac{2}{\pi} I_{(P)}\right)$$

$$I_{(P)} = \frac{V_{L(P)}}{R_L}$$

Let R_L = 1kΩ and V_{CC} = 10V

$$\eta = \frac{P_O}{P_i} \times 100\%$$

Procedure:

1. Rig up the circuit as shown in Fig 4.1.
2. Apply ac sinusoidal input of 2V peak-to-peak and 1 kHz frequency.
3. Observe the input and output waveforms simultaneously on the DSO.
4. Vary the input voltage, note down the output voltage and calculate the efficiency using given formulae.
5. In order to remove crossover distortion, rig up the circuit as shown in Fig. 4.2 and observe the output waveform.

Tabular Column:

$V_{i\,PP}$ (V)	P_O (in W)	P_i (in W)	η (in %)
2			
4			
6			
8			
10			

To remove cross over distortion:

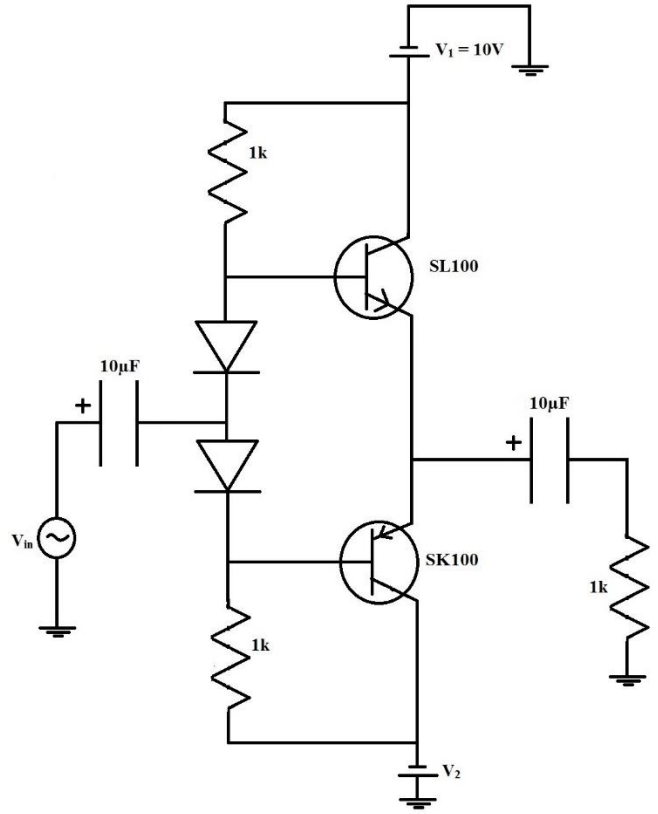


Fig 4.2: Cross over distortion elimination of Class B amplifier.

EXPT. 5: LINEAR APPLICATIONS OF OPERATIONAL AMPLIFIER

Aim: To design an inverting amplifier, Summing amplifier and Integrator using Operational amplifier.

Equipment and Components Required: Dual source DC power supply, AFO, DSO and DMM, Op-amp µA741, resistors, capacitors, probes and wires.

INVERTING AMPLIFIER:

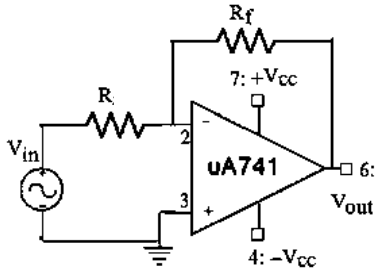


Fig. 5.1: Inverting amplifier

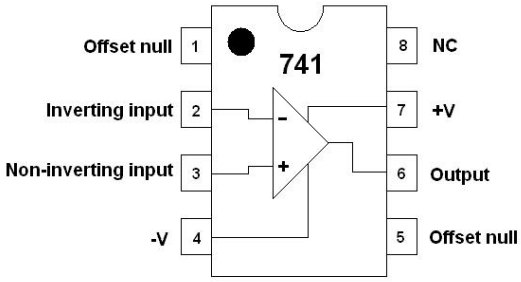


Fig. 5.2: µA741 Pin diagram

Design Hints:

Design the circuit for voltage gain = 2.

Voltage gain, $A_V = \frac{-R_f}{R}$

Choose R =10kΩ, then R_f = 22kΩ. (Use R_f = 22kΩ)

Procedure:

1. Rig up the circuit as shown in the Fig. 5.1.
2. With DC input signal tabulate the readings as shown below.

Tabular column:

Vin	V_{out})

SUMMING AMPLIFIER:

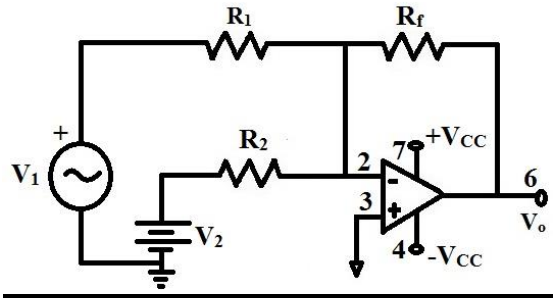


Fig. 5.3: Inverting Summing amplifier

Design Hints:

Design the circuit to obtain $V_{OUT} = -(V_1 + V_2)$

For Summing amplifier, $V_{OUT} = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)$

Let $R_f = 10k\Omega$; $R_1 = R_f = 10k\Omega$; $R_2 = R_f = 10k\Omega$

Procedure:

1. Rig up the circuit as shown in Fig. 5.3.
2. Give V_1 and V_2 from two different input sources and measure the output.
3. Repeat for three to four sets of -/+ values and measure the output.

Tabular column:

Input voltage (V_i)		Output voltage (V_o)
V_1	V_2	

INTEGRATOR:

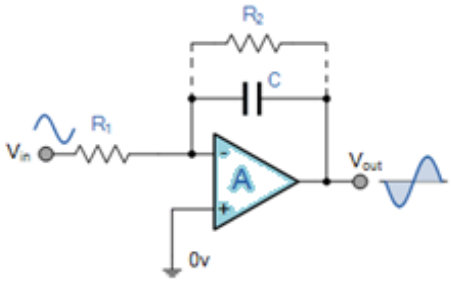


Fig. 5.4: Inverting Integrator

DESIGN:

Corner Frequency, $f_c = \frac{1}{2\pi R_2 C}$ and unity gain frequency, $f_u = \frac{1}{2\pi R_1 C}$

$V_{out} = -\frac{1}{R_1 C}\int V_{in}\, dt$ and input signal will be integrated properly if time period $T \geq R_1C$.

For input signal time period of 0.1msec, take $R_1 = 10\ k\Omega$ and $C = 0.01\mu F$. Select $R_2 = 10R_1$.

Note: The circuit acts as an integrator in the frequency range f_c to f_{unity}. Select R_1, R_2 and C such that $f_c < f < f_u$

PROCEDURE:

1. Apply 1V p-p Square wave of 1 kHz to Op-amp based integrator circuit given in Fig. 5.4 without R_2. Observe the input and output waveforms for (i) $T \geq R_1C$ (ii) $T = R_1C$ (iii) $T \leq R_1C$.
2. Vary the amplitude and frequency of the square wave and observe the changes in the output waveform with respect to the input waveform.
3. Repeat steps 1 and 2 with R_2 connected in parallel to the capacitor in the feedback path.

Expected waveform for perfect integrator:

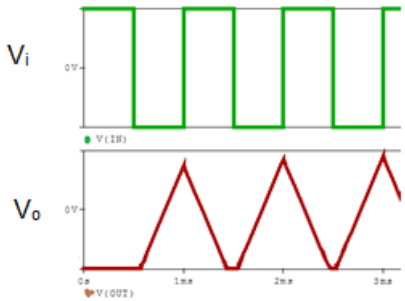


Fig. 5.5: Input and output waveforms of Op-amp Integrator

Exercise:

1. Design a non-inverting amplifier for gain of 10. Obtain the frequency response and transfer characteristics.
   Design: $A_f = \frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R}$
2. Design a differentiator circuit using OPAMP and observe the output for sinusoidal, square and triangular signals of 1 kHz. (Input signal will be differentiated properly if time period $T \geq R_F C$)
3. Design a summing amplifier using single IC µA 741 op-amp to realize
   (i) $V_{out} = 2\,V_{in1} - 4\,V_{in2} - 2\,V_{in3}$
   (ii) $V_{out} = 8\,V_{in1} - 3\,V_{in2} - 0.5\,V_{in3}$

VIVA VOCE

1. Does the closed-loop gain-bandwidth product remain constant for a given op-amp?
2. What is slew rate? Give the value of slew rate for op-amp IC µA741.
3. List all the ideal and practical parameter values of op-amp IC µA741.
4. State true or false and justify: "The lower the value of slew rate better is the op-amp"
5. State true or false and justify: "The higher the value of CMRR better is the op-amp"
6. What is meant by virtual ground in the op amp?
7. Give the pin configuration of IC µA 741.
8. List the OPAMP ideal characteristics.
9. What is the typical value of following in µA 741 IC? (i) Unity gain bandwidth (ii) output resistance (iii) slew rate (iv) 3 dB bandwidth (v) Common mode rejection ratio (CMMR)

EXPT. 6: OPAMP BASED COMPARATOR APPLICATIONS

Aim: [i] To design and implement a zero and a level crossing detector.
[ii] To design and implement Schmitt Trigger circuits using µA 741 for symmetrical and unsymmetrical threshold levels.

Equipment's and Components required: Dual-mode DC power supply, AFO, DSO, µA741, 1N4001, Resistors.

6.1 Zero crossing detector and level crossing detector:

Circuit Diagram:

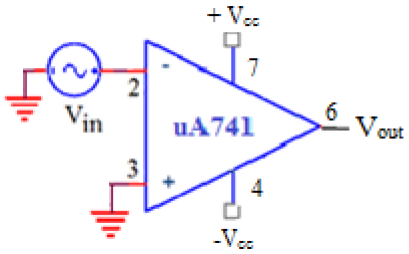


Fig. 6.1: Zero crossing detector (ZCD)

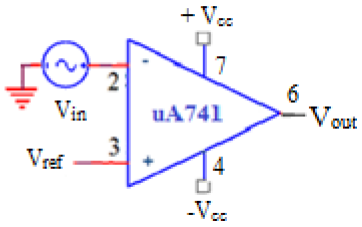


Fig. 6.2: Level crossing detector

Procedure:

[i] Rig up the circuit as shown in Fig. 6.1.
[ii] Using AFO apply sinusoidal signal.
[iii] Note down the input and output voltage waveforms.
[iv] Now connect dc reference voltage as shown in Fig. 6.2 and note down input and output waveforms for various negative and positive reference voltages.

6.2 Schmitt Trigger:

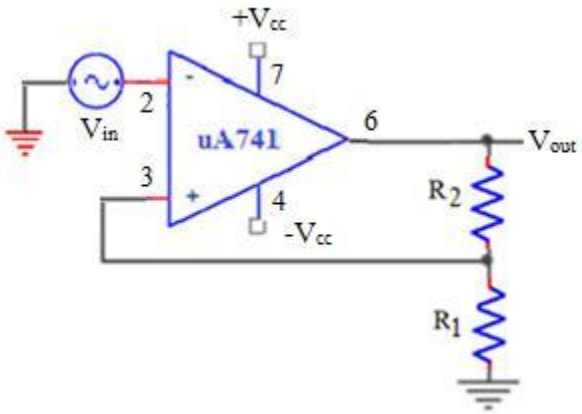


Fig. 6.3: Inverting type Schmitt Trigger circuit with equal UTP and LTP.

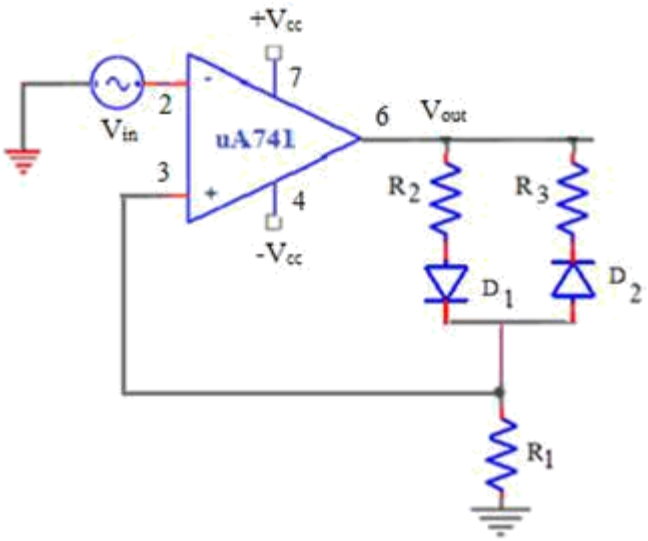


Fig. 6.4: Inverting type Schmitt Trigger circuit with unequal UTP and LTP.

Design: $V_{out} = \pm V_{sat}$

[1] To design for $V_{UTP} = 3V, V_{LTP} = -3$ V; (Refer circuit of Fig. 6.3)

a. $V_{UTP} = \frac{R_1}{R_1+R_2} V_{sat}$; $V_{LTP} = -\frac{R_1}{R_1+R_2} V_{sat}$;

For $V_{sat} = \pm 10V$, if $R_1 = 10k\Omega$, then $R_2 = 23.33k\Omega$ (Use $22k\Omega$)

[2] To design $V_{UTP} = 3V$, $V_{LTP} = -2V$; (Refer circuit of Fig. 6.4)

$V_{UTP} = \frac{R_1}{R_1+R_2} V_{sat}$; $V_{LTP} = -= \frac{R_1}{R_1+R_3} V_{sat}$; For $V_{sat} = \pm 10V$,

if $R_1 = 10k\Omega$, then $R_2 = 23.33k\Omega$ (Use $22k\Omega$) and $R_3 = 40k\Omega$ (Use $39k\Omega$)

Procedure:

[i] Rig up the circuit as shown in Fig. 6.3.

[ii] Using AFO apply sinusoidal signal.

[iii] Note down the input and output voltage waveforms. Also note down transfer characteristics.

[iv] Rig up the circuit as shown in Fig. 6.4 and repeat the above given steps.

Experiments for Further Practice

1. **Window Detector using OPAMP:**

Circuit diagram:

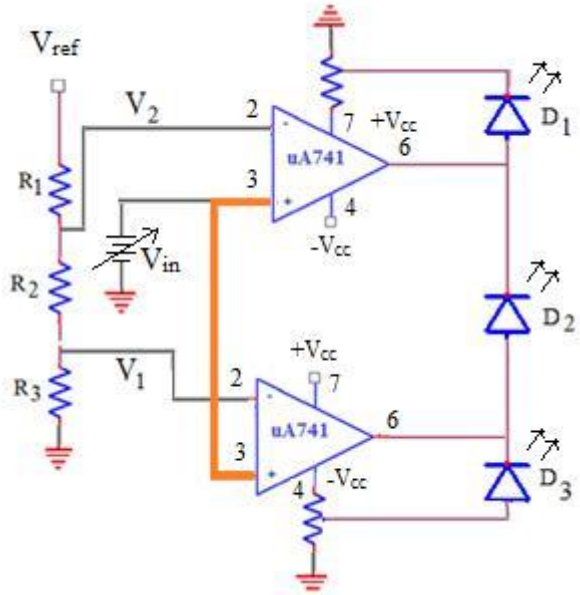


Fig. 6.5: Opamp based Window comparator

Design: To design three voltage windows: (0 to V_1, V_1 to V_2, V_2 to V_{ref})

$V_1 = \frac{R_3}{R_1+R_2+R_3} V_{ref}$ and $V_2 = \frac{R_2+R_3}{R_1+R_2+R_3} V_{ref}$

Observations:

Input voltage (V_{in}) volts	Status of LEDs		
	D_1	D_2	D_3
0 V < V_{in} < Lower window level			
Lower window level < V_{in} < Upper window level			
V_{ref} > V_{in} > upper window level			

2. Design and implement an inverting Schmitt trigger for the following specifications
(i) V_{UTP} = 5V, V_{LTP} = −5V
(ii) V_{UTP} = 7.5V, V_{LTP} = −5V
(iii) V_{UTP} = 3V, V_{LTP} = 1V (Hint: connect reference voltage in series with R1 in Fig. 6.6)

3. Design and implement a non-inverting Schmitt trigger for the following specifications
(i) V_{UTP} = 5V, V_{LTP} = −5V
(ii) V_{UTP} = 7.5V, V_{LTP} = −5V
(iii) V_{UTP} = 3V, V_{LTP} = 1V (Hint: connect reference voltage in series with R1)

Circuit diagram

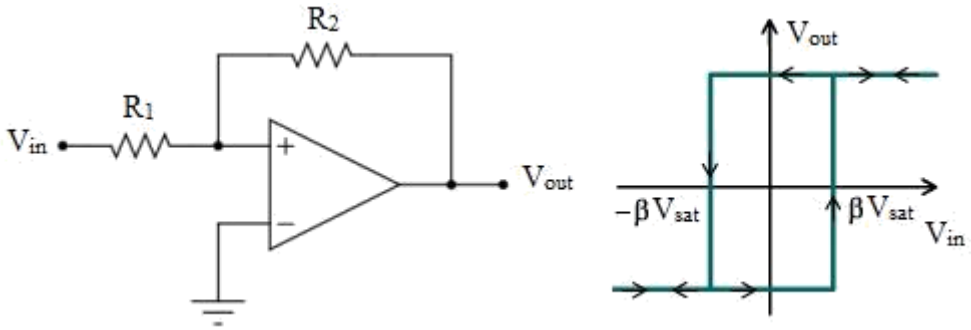


Fig. 6.6: Non-inverting type Schmitt trigger circuit and its Hysteresis curve

Circuit diagram

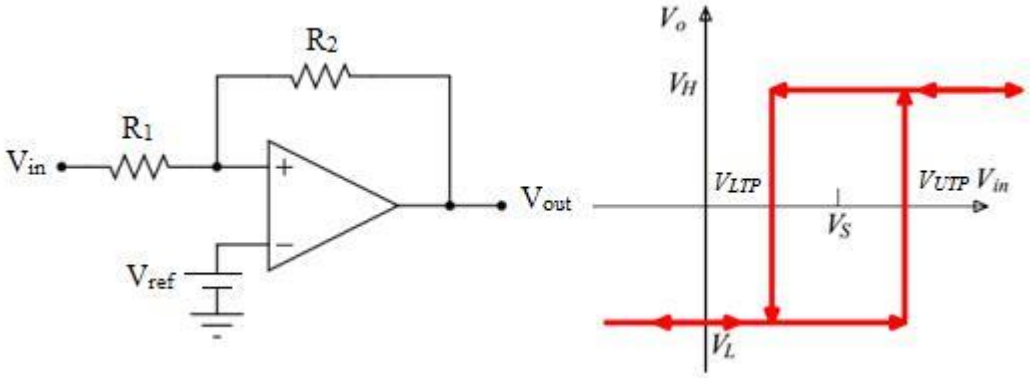


Fig. 6.7: Non-inverting type Schmitt trigger with reference voltage and its Hysteresis curve

4. Implement a three level window detector using OPAMP to detect whether the signal voltage is below 2 V, between 2 V and 4 V or greater than 4 V.

Sample Viva-Voce Questions

1. What happens if Zener diode of 6.2V is connected back to back across the output terminal in Fig. 7.1?

2. What happens if the input is given to the non-inverting terminal and inverting terminal is grounded in Fig. 7.1? Draw the waveforms.

3. What is the significance of connecting two diodes in opposite direction in parallel between the inverting and non-inverting terminals in Fig. 7.1, Fig. 7.2?

4. Draw the circuit of a two level window detector.
5. What is advantage of Schmitt trigger circuit over the basic comparators?
6. What is hysteresis?

7. Which type of feedback is used in inverting type and non-inverting type Schmitt trigger?

EXPT. 7: SINUSOIDAL OSCILLATORS USING OPAMP

Aim: To design and test a RC phase shift and a Wein Bridge Oscillator for generating the sine wave.

Equipment's and Components required: DSO, OPAMP μA741 & discrete components.

RC Phase shift oscillator: Design an oscillator to oscillate at 1kHz.

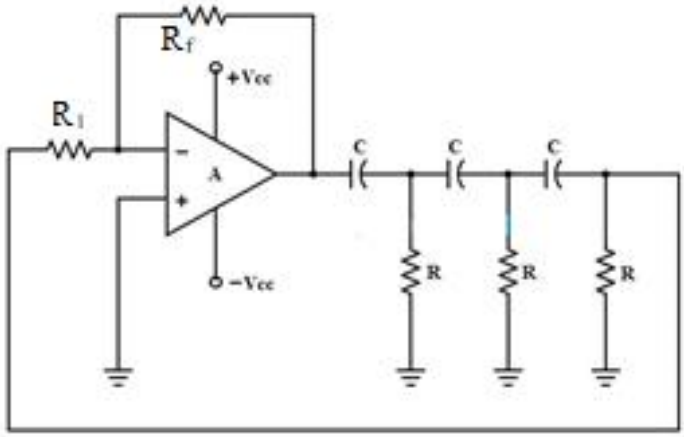


Fig. 7.1: RC Phase shift Oscillator

Design: Design the RC Phase Shift Oscillator for a frequency of 300Hz.

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

Assume C= 0.1 μF. Therefore, R= 2.17kΩ. (Use 2.2kΩ)

$R_1 > 10R$; Choose $R_1 = 22k\Omega$; $R_f = 29R_1 = 638k\Omega$ (Use 680kΩ and Potentiometer)

Procedure:

1. Rig up the circuit as shown in the Fig. 7.1.
2. Measure the frequency of oscillation from the DSO and compare it with the theoretical value.

Wein Bridge Oscillator: Design Wein Bridge oscillator to oscillate at 1kHz.

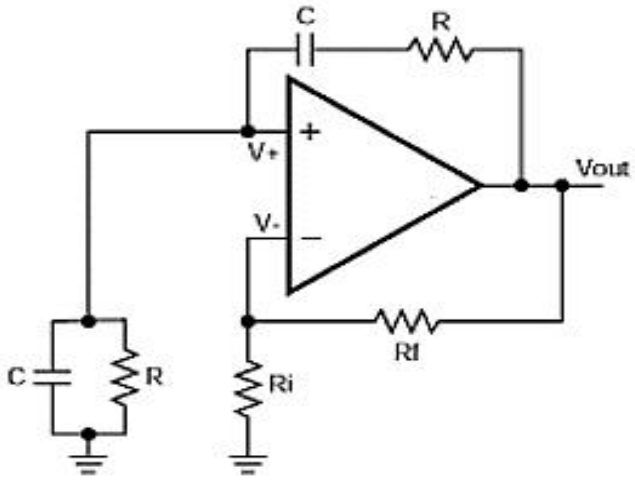


Fig. 7.2: Wein Bridge Oscillator

Design: $f_o = \frac{1}{2\pi RC}$ Choose C = 0.1μF then R = 1.6kΩ
$R_f = 2R_i$. If R_i = 10kΩ, then take R_f = 20kΩ. (Use 10kΩ and 22kΩ Potentiometer)

Procedure:

1. Rig up the circuit as shown in the Fig. 7.2.
2. Measure the frequency of oscillation from the DSO and compare it with the theoretical value.

Sample Viva questions

1. What are the conditions necessary for generating Oscillations?
2. Classify oscillators.
3. How oscillations are produced in oscillators?
4. What are disadvantages of RC Phase Shift Oscillator?
5. Compare RC and LC oscillators.
6. Why Wein Bridge Oscillator uses both positive and negative feedback?
7. What is frequency stability?

EXPT. 8: ACTIVE FILTER AND PRECISION RECTIFIERS USING OPAMP

Aim: (i) To design a half-wave precision rectifier using OPAMP and observe input and output waveforms.
(ii) To design second order and fourth order Low pass Butterworth filter.

Equipment's and Components Required: Dual source DC power supply, AFO, DSO and Op-amp μA741, diode 1N4001, Bread board, resistors, probes and wires.

I. Half-wave Precision Rectifier:

Circuit Diagram:

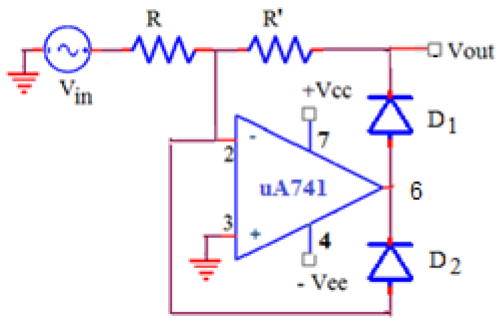


Fig. 8.1: Half-wave precision rectifier

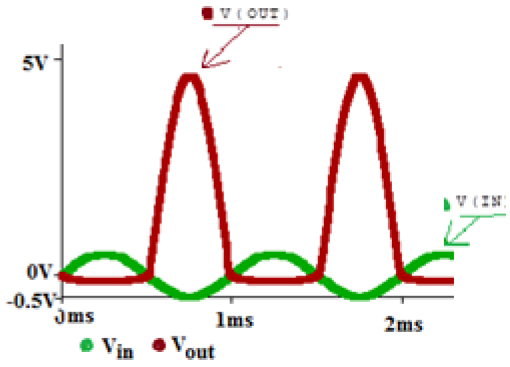


Fig. 8.2: Expected Input and output waveforms

Design: It is intended to obtain an output of 5V peak amplitude for given sinusoidal input of 0.5V peak. $V_{out}/V_{in} = R'/R$, i.e., for gain of 10, Let R = 4.7kΩ then R'= 47kΩ.

Procedure:

1. Rig up the circuit as shown in the Fig. 8.1.
2. Using AFO, apply 1 kHz sinusoidal input with a peak-to-peak amplitude of 1V (positive peak = 0.5V). Observe the input and output using DSO.
3. Note down the input and output voltage waveforms.

II. Low Pass Filter (LPF):

Circuit Diagram:

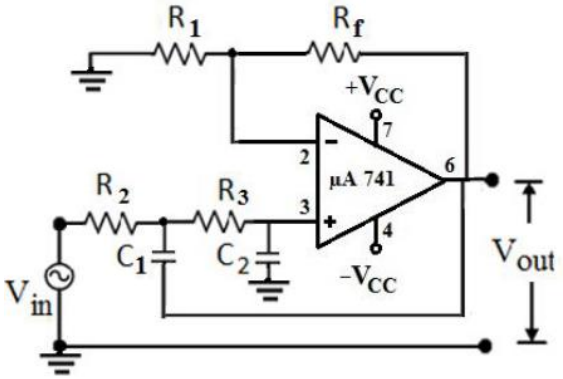


Fig. 8.3: Second order LPF

Design:

f_c = 1 kHz, with pass band gain = 2. Assume $C_1 = C_2 = 0.1\mu F$.

Let R_1 = 10kΩ. Therefore, $A_v = 1 + \frac{R_f}{R_1} = 2$, then R_f = 10kΩ.

$f_c = \frac{1}{2\pi\sqrt{R_2R_3C_1C_2}}$, if $R_2 = R_3 = R$ & $C_1 = C_2 = C$, then $R = \frac{1}{2\pi f_c C}$ = 1.59kΩ

Procedure:

1. Rig up the circuit as shown in the Fig. 8.3.
2. Apply sinusoidal signal using AFO.
3. Keeping input voltage constant, vary the input frequency and tabulate the readings.
4. Plot the frequency response graph.
5. Repeat the same procedure for the fourth order Low Pass Butterworth filter.

Table 8.1

Input signal amplitude =

Trial No.	Frequency(Hz)	Output voltage (V_O)	Voltage gain $A_v = V_O/V_i$	Gain in dB = 20 log (A_v)

Experiments for Further Practice

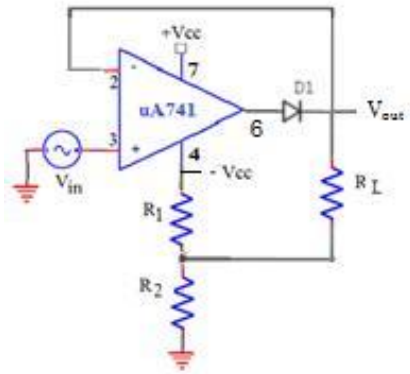


Fig. 8.4

1. Implement the circuit in Fig. 8.4. Apply the sinusoidal input signal of 0.5 V p-p and 10 kHz frequency and observe the input and output voltage waveforms. Draw the ideal and practical output waveforms.
2. Observe the input and output voltage waveforms after interchanging the diode connection.
3. Observe the effect of increasing amplitude of the input signal for the given circuit.

Sample Viva Questions

1. What do you mean by *precision rectifier*?
2. Why OPAMP is used in precision rectifier circuits? Justify
3. What happens if the diodes D_1 and D_2 are interchanged in half-wave precision rectifier circuit of Fig. 8.1?
4. What happens if the non-inverting terminal of OP-AMP is connected to 1V instead of ground in half-wave precision rectifier circuit of Fig. 8.1?

EXPT. 9: NON-SINUSOIDAL WAVEFORM GENERATION USING OPERATIONAL AMPLIFIERS

Aim: To design a square wave and pulse generator using operational amplifier IC µA741.
Equipment's and Components required: Dual mode DC Power Supply, AFO, DSO, IC µA741, resistors and capacitors.

9.1 Square wave generation:

Circuit Diagram:

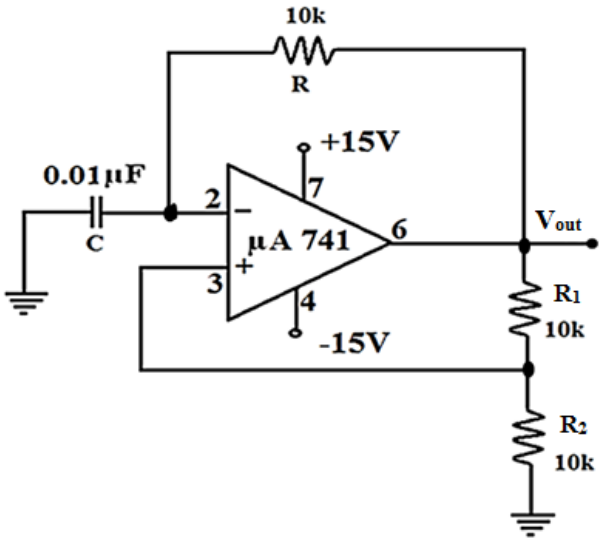


Fig. 9.1: Op-amp based Astable multivibrator

Design: To design for square wave output of frequency f = 4.5 kHz

$T = 2\,RC \ln \left\{\frac{(1+\beta)}{(1-\beta)}\right\}$ ------ (1)

where, $\beta = \left[\frac{R_2}{R_1+R_2}\right]$ ------ (2)

Let $R_1 = R_2 = 10$ kΩ so that $\beta = 0.5$

Thus equation (1) will get reduced to,

T= 2 RC ln (3) = 2.197 RC ------ (3)

Now, $T = \frac{1}{f} = \frac{1}{4.5\text{ kHz}} = 0.22$ msec

Select the value of C = 0.01 µF

$R = \frac{0.22\text{ msec}}{2.197 \text{ x } 0.01\mu F} = 10.1$ kΩ (Select 10 kΩ)

Procedure:

i. Connect the circuit as shown in the Fig. 9.1.
ii. Observe the output waveform at pin 6 of the OPAMP on the DSO.
iii. Also note down the voltage across the Capacitor at pin 2 (inverting input) of the OPAMP.

Observations: Sketch Capacitor voltage (at pin 2) and output voltage (at pin 6) waveforms indicating amplitude and time.

9.2: Negative Edge Triggered Monostable Multivibrator:

Circuit Diagram:

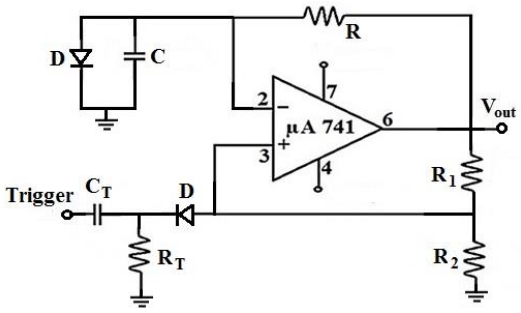


Fig. 9.2: Negative edge triggered monostable multivibrator circuit

Design:

$$T = RC\ \frac{ln\left(1+\frac{V_D}{V_{sat}}\right)}{1-\beta}$$ where, $\beta = \left[\frac{R_2}{R_1+R_2}\right]$

If $R_1 = R_2 = 10k\Omega$, $\beta = 0.5$ and $T = 0.69RC$
If T = 0.1ms and C = 0.01µF, then R = 10kΩ.
(Choose $C_T = 0.01\mu F$; $R_T = 1k\Omega$)

Procedure:

i. Connect the circuit as shown in Fig. 9.2.
ii. Apply trigger pulse from AFO.
iii. Observe and plot the output waveform at pin 6 with respect to trigger pulse input and capacitor voltage.
iv. Compare the theoretical and practical values of Pulse width.

Experiments for Further Practice

1. **Triangular wave generation**

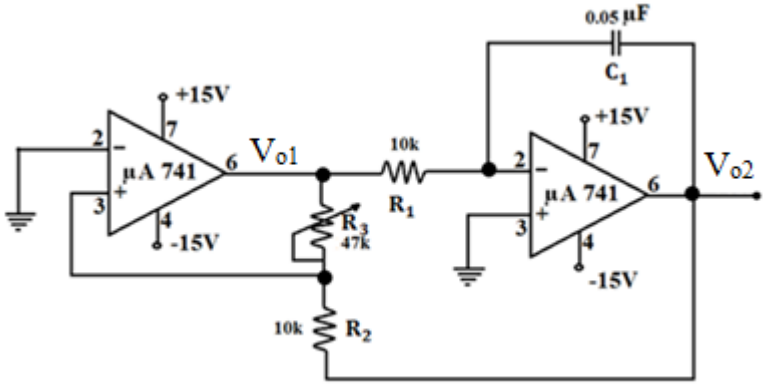


Fig. 9.3: Op-amp based triangular wave generator

Design: To generate triangular wave output of 2 kHz frequency and $V_{o(pp)} = 7\ V$ using a 15V dual mode DC power supply.

$$V_{o(pp)} = 2\,V_{Ramp} = 2\frac{R_2}{R_3}\,(V_{sat})$$

Now, select $R_2 = 10$ kΩ, then $R_3 = 40$ kΩ (select 47 kΩ pot.)

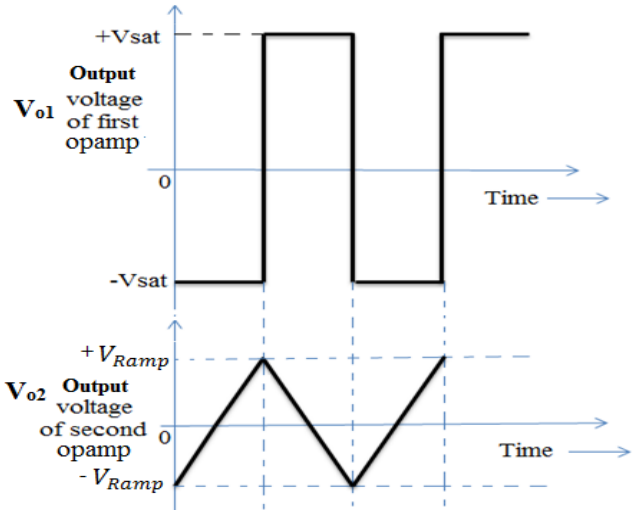
$$\text{Output frequency} = \frac{R_3}{4\,R_1\,C_1\,R_2}$$

Select $C_1 = 0.05$ µF, then $R_1 = 10$ kΩ

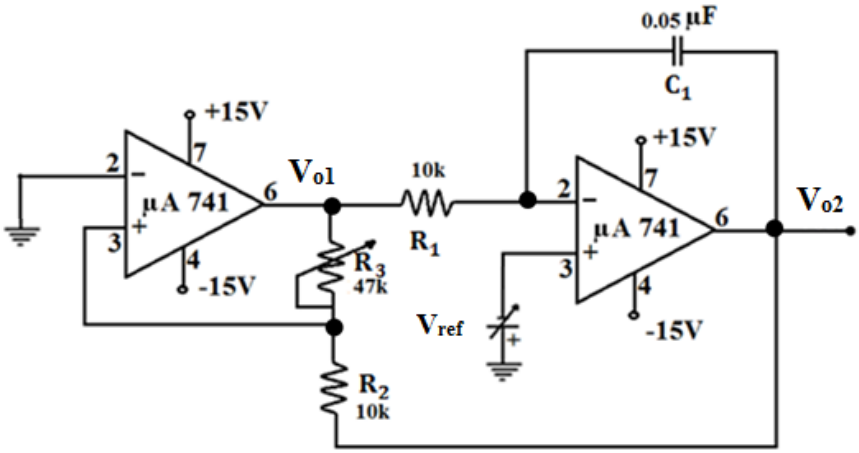
Procedure:

[i] Connect the circuit as shown in Fig. 9.3.
[ii] Adjust R_3 (DRB/ 47 kΩ potentiometer) to 40kΩ.
[iii] Observe the waveforms at output of both op-amps and note down the signal parameters.
[iv] Vary R_3 and repeat the above procedure to observe the change in amplitude and frequency of triangular wave.

Expected waveform:



2. To generate a sawtooth waveform with $T_{RISE} >> T_{FALL}$.

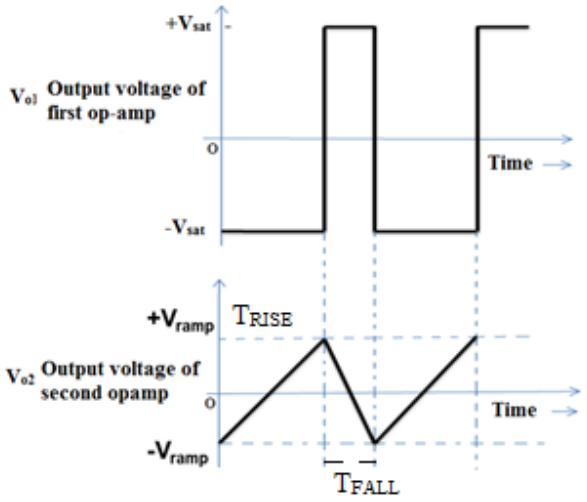


Design: Same as triangular wave generator circuit

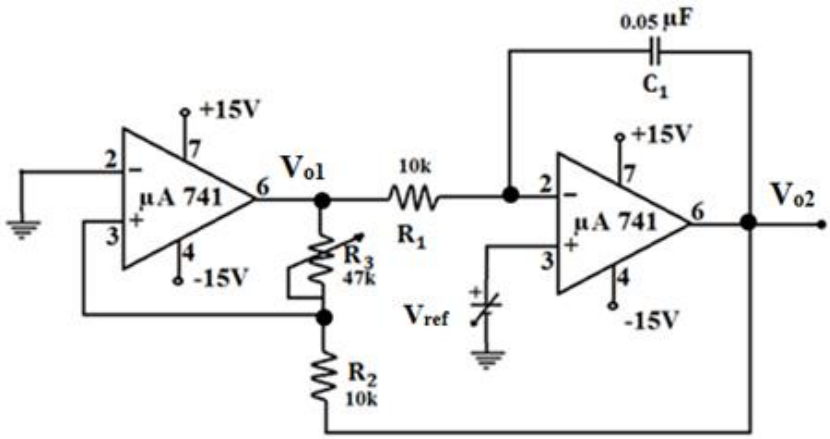
Procedure:

[i] Follow the same procedural steps as that of the triangular wave generator.
[ii] Fix the value of R_3 to 40 kΩ and vary the value of V_{ref} from -3V to -10V and observe the waveforms at output of both op-amps and note down the signal parameters.

Expected waveform:



3. To generate a sawtooth waveform with $T_{FALL} >> T_{RISE}$.



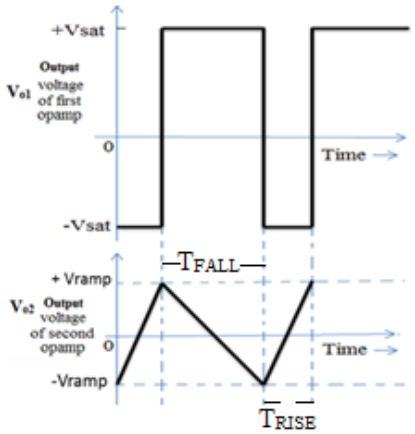
Design:

Same as triangular waveform

Procedure:

1) Follow the same procedural steps as that of the triangular wave generator.
2) Fix the value of R_3 to 40 kΩ and vary the value of V_{ref} from 3V to 10V and observe the waveforms at output of both op-amps and note down the signal parameters

Expected waveform:



EXPT. 10: 555 TIMER IC APPLICATIONS

Aim: To design Astable and Monostable multivibrators using IC 555.

Equipments and Components required: DC Power Supply, DSO, IC 555, resistors and capacitors.

10.1: Astable multivibrator with Square wave output (duty cycle ≠ 50%)

Aim: To design a square wave of frequency 1 kHz using IC 555 with 75% duty cycle.

Circuit Diagram:

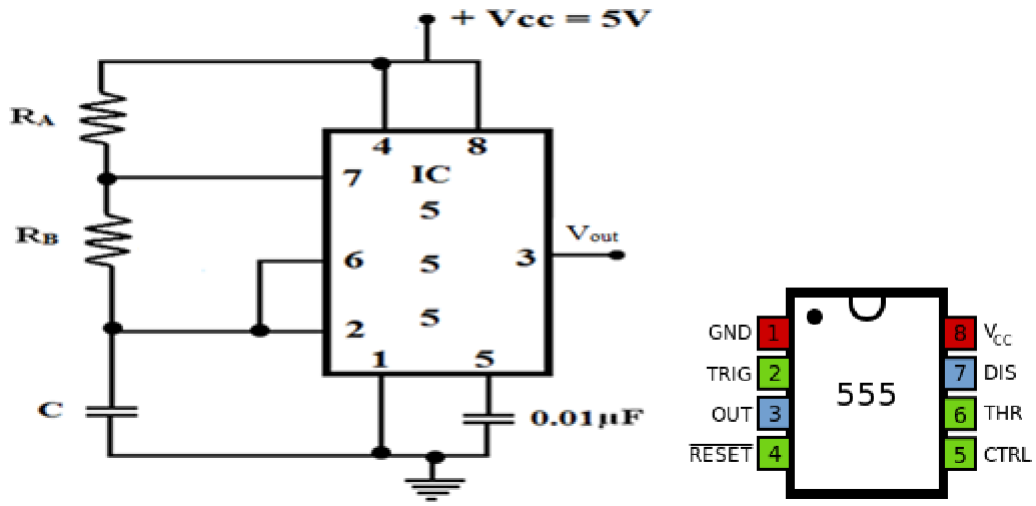


Fig. 10.1: Astable multivibrator with Square wave output (duty cycle ≠ 50%)

Design:

Duty cycle = $\frac{T_{ON}}{T_{OFF}}$; $T_{ON} = 0.69(R_A + R_B)\,C$; $T_{OFF} = 0.69R_BC$.

T=1/f=1msec; Duty cycle = $\frac{T_{ON}}{T_{OFF}}$; 0.75 = $\frac{T_{ON}}{0.001}$;

T_{ON} = 0.75msec; T_{OFF} = 0.25msec.

Choose C= 0.1μF, R_A = 7.25kΩ and R_B = 3.6kΩ

Procedure:

1. Connect the circuit as shown in the Fig. 10.1.
2. Observe the voltage across the Capacitor at pin 2 and output at pin 3 of IC 555 on the DSO.

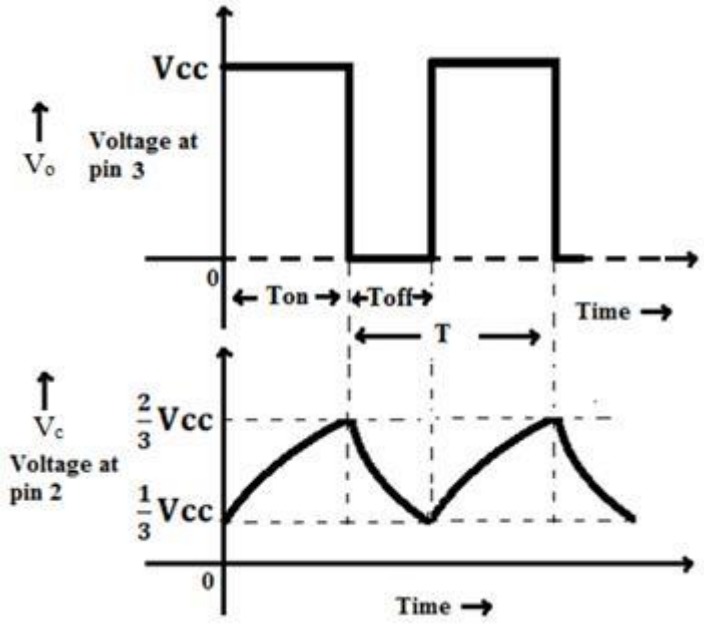
Observations: Sketch capacitor and output voltage waveforms. Note down T_{ON}, T_{OFF}, duty cycle and frequency.

T_{ON}: _____ T_{OFF}: _____

Duty Cycle = T_{ON}/T = _____

Output Frequency: Theoretical: ----- kHz Practical: ……..

Expected waveform:



10.2 Astable multivibrator with Square wave output (50% duty cycle)

Aim: To design a square wave of frequency 1 kHz using IC 555 with 50% duty cycle.

Circuit Diagram:

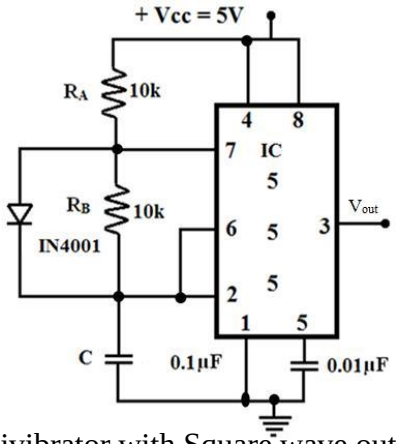


Fig. 10.2: Astable multivibrator with Square wave output (duty cycle = 50%)

Design:

$T = 1/f = 1msec$; $T_{ON} = 0.5msec$; $T_{OFF} = 0.5msec$.

$T_{OFF} = 0.69R_BC$; $T_{ON} = 0.69R_AC$, Choose $C = 0.1\mu F$, then $R_A = R_B = 7.2k\Omega$.

Sketch capacitor and output voltage waveforms. Note down T_{ON}, T_{OFF}, duty cycle and frequency

10.3 Monostable multivibrator

Circuit Diagram:

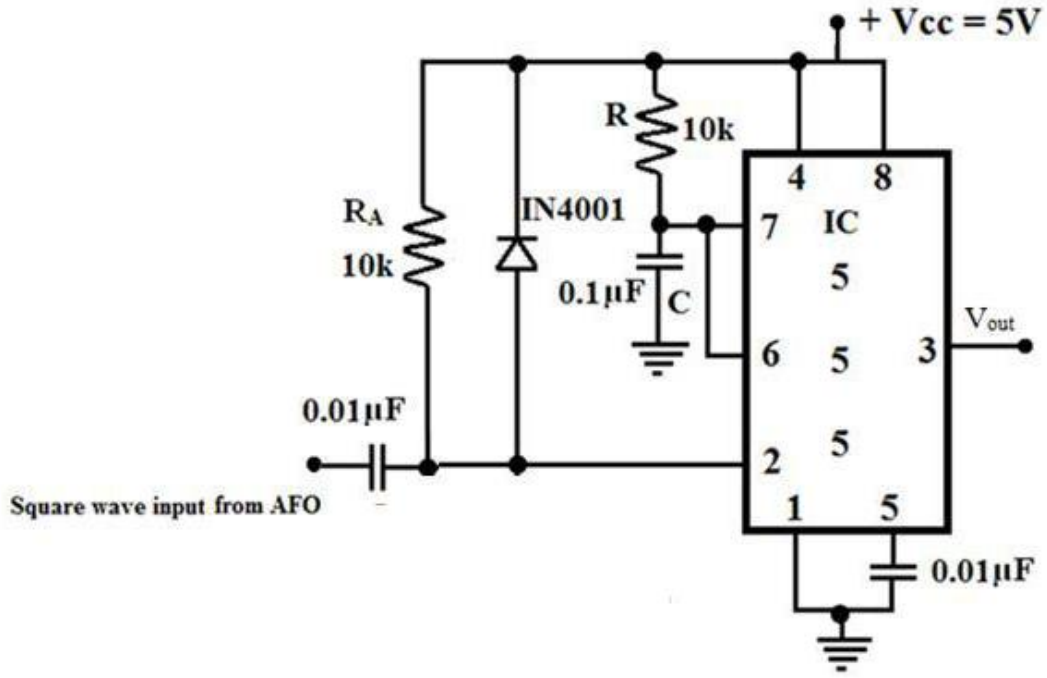


Fig. 10.3 Monostable multivibrator

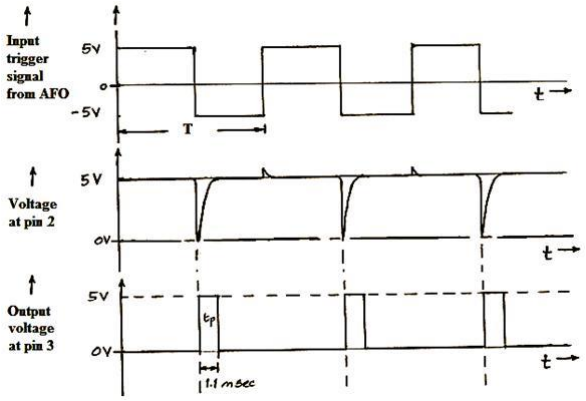
Design: To generate a pulse output having width of 1msec.

T =1.1 RC, Select R = 10kΩ then C = 0.1 µF

Procedure:

1. Rig up the circuit as shown in Fig. 10.3.
2. Apply square wave trigger input from the signal generator and observe the negative going trigger at pin 2.
3. Observe the output waveform and measure the amplitude and pulse width of the signals and compare it with theoretical values.

Expected (specimen) waveform:



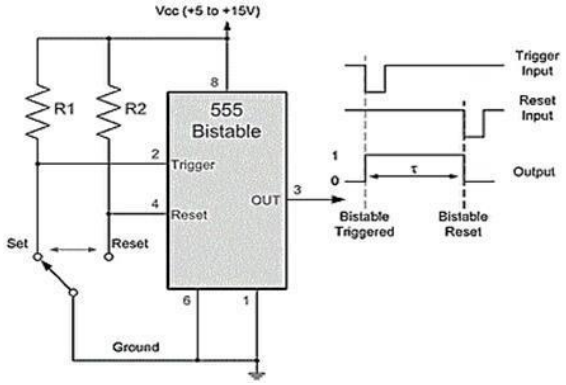
Observations:

Pulse Width: - Theoretical: _____msec. Practical: _____.

Experiments for Further Practice

1. Bistable multivibrator

Circuit Diagram with waveform:



$R_1 = R_2 = 1\ k\Omega$

Procedure:

1. Keep the switch at set position and see the output goes high.
2. Keep the switch at reset position and see the output goes low.

Sample Viva-Voce Questions

1) Explain the function of each pin of timer IC?
2) Explain the functional block diagram of a 555 timer.
3) List the basic blocks of IC 555 timer?
4) What is a multivibrator?
5) What is a bistable multivibrator?
6) Why astable multivibrator is called as *free running* multivibrator?
7) What do you mean by *relaxation oscillator*?
8) List the applications of 555 timers in monostable mode of operation
9) Explain the function of reset.
10) What are the modes of operation of timer?
11) What is the expression of time delay of an astable multivibrator?
12) Discuss some applications of timer in astable mode?
13) What is the expression of time delay of a monostable multivibrator?