MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

COURSE PLAN

Department	:	Instrumentation & Control Engineering
Course Name & code	:	Digital System Design & ICE-2251
Semester & branch	:	IV & E&I
Name of the faculty	:	Ganesh Nayak & Aneesha Acharya K
No of contact hours/week:	:	L: 2, T: 1, P: 0, C: 3

Course Outcomes (COs)

	At the end of this course, the student should be able to:	No. of Contact Hours	Marks
CO1:	Understand digital system design flow with programmable logic devices.	4	8
CO2:	Comprehend concepts of Verilog programming.	6	20
CO3:	Model and design combinational and sequential systems using Verilog programming	16	46
CO4:	Analyze the design of systems with ASICs and FPGAs.	6	18
CO5:	Evaluate the performance of combinational and sequential systems by testing and verification.	4	8
	Total	36	100

Assessment Plan

Components	Assignments	Sessional Tests	End Semester/ Make-up Examination
Duration	20 to 30 minutes	60 minutes	180 minutes
Weightage	20 % (4 X 5 marks)	30 % (2 X 15 Marks)	50 % (1 X 50 Marks)
Typology of Questions	Understanding; Applying; Analyzing; Evaluating; Creating	Remembering; Understanding; Applying	Understanding; Applying; Analyzing; Evaluating; Creating
Pattern	Answer one randomly selected question from the problem sheet (Students can refer their class notes)	MCQ (10 marks): 10 questions of 0.5 marks each Short Answers (10 marks): questions of 2 or 3 marks	Answer all 5 full questions of 10 marks each. Each question may have 2 to 3 parts of 3/4/5/6/7 marks
Schedule	As notified by Associate Director (Academics) at the start of each semester	Calendared activity	Calendared activity
Topics Covered	Assignment 1 (L 1-7 & T 1-3) **(CO1 and CO2)**	Test 1 (L 1-12 & T 1-6) **(CO1, CO2, CO3)**	Comprehensive examination covering full syllabus. Students are expected to answer all questions **(CO1-5)**
	Assignment 2 (L **8-12** & T 4-6) **(CO3)**		
	Assignment 3 (L 13-18 & T 7-9) **(CO3)**	Test 2 (L 13-18 & T 7-9) **(CO3)**	
	Assignment 4 (L 19-22 & T 10) **(CO4)**		

Lesson Plan

L. No./ T. No.	Topics	Course Outcome Addressed
L0	Introduction to the Course.	CO
L1	Implementation of digital systems using SPLDs.	CO1
L2	Implementation of digital systems using ASICs and FPGAs.	CO1
T1	Architecture of FPGA, Levels and domains of abstraction.	CO1
L3	HDL-based design flow, Introduction to CAD tools.	CO1
L4	Introduction to Verilog: Lexical conventions, Data Types.	CO2
T2	Modules and ports.	CO2
L5	Module modeling styles.	CO2
L6	Simulation.	CO2
T3	Structural modeling: Gate types	CO2
L7	Gate Delays	CO2

L8	Dataflow Modeling: Continuous Assignments, Delays	CO3
T4	Design Examples.	CO3
L9	Expressions, Operators and Operands	CO3
L10	Expressions, Operators and Operands	CO3
T5	Design Examples.	CO3
L11	Design Examples.	CO3
L12	Behavioral Modeling: Structured Procedures.	CO3
T6	Design Examples.	CO3
L13	Procedural Assignments.	CO3
L14	Timing controls.	CO3
T7	Conditional and branching statements.	CO3
L15	Loops.	CO3
L16	Sequential and Parallel Blocks.	CO3
T8	Design Examples.	CO3
L17	Generate Blocks.	CO3
L18	Tasks and Functions, Useful modeling techniques.	CO3
T9	Programmable ASICs: Architecture of CPLDs and FPGAs.	CO3
L19	Programming technologies.	CO4
L20	Design examples.	CO4
T10	Programmable logic blocks, interconnects and programmable I/O blocks.	CO4
L21	Design flow.	CO4
L22	Design examples.	CO4
T11	Testing and Verification: Testing of combinational circuits.	CO5
L23	Testing sequential circuits	CO5
L24	Functional and timing simulation.	CO5
T12	Boundary scan, BIST, Verification.	CO5

References:

1.	Samir Palnitkar, Verilog HDL: A guide to digital design and synthesis, Pearson (2e), 2003.
2.	Design through Verilog HDL by T R Padmanabhan and B Bala Tripura Sundari
3.	J. Bhasker, A Verilog HDL Primer (1e), 2001.
4.	Stephen Brown, Fundamentals of Digital Logic with Verilog Design, TMH, (3e), 2013.
5.	Digital System Design with FPGA by Cem Unsalan and Bora Tar
6.	Michael John, Sebastian Smith, Application Specific Integrated Circuits, Addison Wesley
7.	Click or tap here to enter text.

Submitted by: Ganesh Nayak & Aneesha Acharya K

(Signature of the faculty)

Date: 07-02-2022

Approved by: Dr. Shreesha C

(Signature of HOD)

Date: 07-02-2022

FACULTY MEMBERS TEACHING THE COURSE (IF MULTIPLE SECTIONS EXIST):

FACULTY	SECTION	FACULTY	SECTION
Ganesh Nayak	A	Aneesha Acharya K	B

****