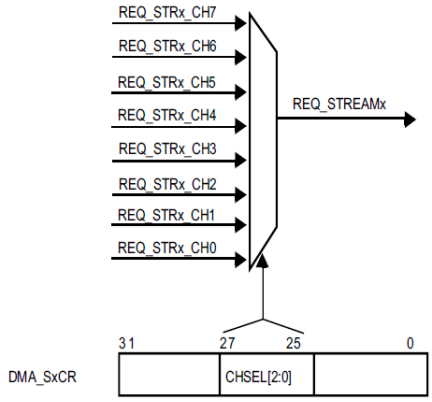
DMA -Direct Memory Access TUTORIAL

Introduction:

1. 8 streams for each DMA controller, up to 8 channels (requests) per stream.
2. A regular channel that supports peripheral-to-memory, memory-to-peripheral and memory-to-memory transfers.
3. Supports incremental burst transfers of 4, 8 or 16 beats.
4. DMA channel selection is done using DMA_SxCR register as shown in figure below.



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5. The direction is configured using the DIR[1:0] bits in the DMA_SxCR register and offers three possibilities mentioned in step2 above.

Bits DIR[1:0] of the DMA_SxCR register	Direction	Source address	Destination address
00	Peripheral-to-memory	DMA_SxPAR	DMA_SxM0AR
01	Memory-to-peripheral	DMA_SxM0AR	DMA_SxPAR
10	Memory-to-memory	DMA_SxPAR	DMA_SxM0AR
11	Reserved	-	-

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STEPS TO PROGRAM A DMA

1. Enable DMA2 using AHB1ENR register.
2. Configure DMA_SxCr register as follows

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	CHSEL[2:0]			MBURST [1:0]		PBURST[1:0]		Res.	CT	DBM	PL[1:0]	
				rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PINCOS	MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR[1:0]		PFCTRL	TCIE	HTIE	TEIE	DMEIE	EN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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i. Bit 0 EN: stream enable / flag stream ready when read low

This bit is set and cleared by software.

0: stream disabled

1: stream enabled

ii. Bit 6:7: Data transfer direction (M2M).

00: peripheral-to-memory

01: memory-to-peripheral

10: memory-to-memory

11: reserved

iii. Bit 9 PINC: peripheral increment mode

This bit is set and cleared by software.

0: peripheral address pointer fixed

1: peripheral address pointer incremented after each data transfer (increment done according to PSIZE)

This bit is protected and can be written only if EN = 0.

iv. Bit 10 MINC: memory increment mode

This bit is set and cleared by software.

0: memory address pointer is fixed

1: memory address pointer is incremented after each data transfer (increment is done according to MSIZE)

This bit is protected and can be written only if EN = 0.

v. Bits 12:11 PSIZE[1:0]: peripheral data size

These bits are set and cleared by software.

00: byte (8-bit)

01: half-word (16-bit)

10: word (32-bit)

11: reserved

These bits are protected and can be written only if EN = 0.

vi. Bits 14:13 MSIZE[1:0]: memory data size

These bits are set and cleared by software.

00: byte (8-bit)

01: half-word (16-bit)

10: word (32-bit)

11: reserved

These bits are protected and can be written only if EN = 0.

vii. Bits 17:16 PL[1:0]: priority level

These bits are set and cleared by software.

00: low

01: medium

10: high

11: very high

viii. Bits 27:25 CHSEL[2:0]: channel selection

These bits are set and cleared by software.

000: channel 0 selected => Load 0 value to select this channel

001: channel 1 selected

010: channel 2 selected

011: channel 3 selected

100: channel 4 selected

101: channel 5 selected

110: channel 6 selected

111: channel 7 selected

3. DMA stream x number of data register (DMA_SxNDTR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDT[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bits 15:0 NDT[15:0]: number of data items to transfer (0 up to 65535)

4. DMA stream x memory 0 address register (DMA_SxM0AR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M0A[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M0A[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bits 31:0 M0A[31:0]: memory 0 address. This is used as destination address.

5. DMA stream x peripheral address register (DMA_SxPAR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PAR[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAR[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bits 31:0 PAR[31:0]: peripheral address. This is used as source address.

7. Call DMA initialization and start functions from main to transfer the data.