



SRI KRISHNA COLLEGE OF TECHNOLOGY
 An Autonomous Institution, (Approved by AICTE and affiliated to Anna University)
Coimbatore, Tamil Nadu
Academic Year 2023-2024 (ODD SEM)



CONTINUOUS INTERNAL ASSESSMENT - I - QUESTION BANK

Class	Course Code	Course Title	Date
I	23EC102	Digital Logic design and Computer Architecture	

Course Outcomes:		
CO1	Implement logic circuits and simplify Boolean functions	[AP]
CO2	Analyse combinational and sequential logic circuits	[AN]
CO3	Interpret the design of control unit	[U]
CO4	Illustrate cache memory and virtual memory	[AP]
CO5	Examine parallelism in multicore and hazards in pipelining	[AP]
CO6	Distinguish the different ways of communication with I/O devices	[U]

Part – A (09 x 02 = 18 Marks) Answer All Questions			RBT	CO	Marks
1	Convert the decimal number 42 to binary.		U	C01	2
42 in binary  $ \begin{array}{r} 42 \\ \hline 2 21 \\ 2 10 \\ 2 5 \\ 2 2 \\ \hline & 1 \end{array} $ $\therefore 42_{10} = 101010_2$ <p style="text-align: center;">42 in binary is 101010.</p>					
2	Determine the decimal value of 1101.		U	C01	2

Part – A (09 x 02 = 18 Marks) Answer All Questions		RBT	CO	Marks
<ul style="list-style-type: none"> Step by step solution: <ul style="list-style-type: none"> Step 1: Write down the binary number: 1101 Step 2: Multiply each digit of the binary number by the corresponding power of two: $1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$ Step 3: Solve the powers: $1 \times 8 + 1 \times 4 + 0 \times 2 + 1 \times 1 = 8 + 4 + 0 + 1$ Step 4: Add up the numbers written above: $8 + 4 + 0 + 1 = 13$ So, $(1101)_2 = (13)_{10}$ 				

3	Convert the decimal number 75 to hexadecimal.	U	C01	2
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Step by step solution

Step 1: Divide $(75)_{10}$ successively by 16 until the quotient is 0:

$75/16 = 4$, remainder is 11

$4/16 = 0$, remainder is 4

Step 2: Read from the bottom (MSB) to top (LSB) as 4B. So, **4B** is the hexadecimal equivalent of decimal number 75 (Answer).

4	Find the binary equivalent of hexadecimal number 1A3.	U	C01	2
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Step by step solution

Step 1: Look up each octal digit to obtain the equivalent group of four binary digits. You can use the table below to make these conversions.

$$(1)_{16} = (0001)_2$$

$$(A)_{16} = (1010)_2$$

$$(3)_{16} = (0011)_2$$

Step 2: Group each value of step 1

0001 1010 0011

Step 3: Join these values and remove zeros at left (if necessary) to get the binary result.

110100011

So, 110100011 is the binary equivalent

5	Convert the octal number 64 to decimal.	U	C01	2
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Part – A (09 x 02 = 18 Marks)
Answer All Questions

RBT

CO

Marks

$$(64)_8 = (52)_{10}$$

Step by step solution

Step 1: Write down the octal number:

64

Step 2: Multiply each digit of the octal number by the corresponding power of eight:

$$6 \times 8^1 + 4 \times 8^0$$

Step 3: Solve the powers:

$$6 \times 8 + 4 \times 1$$

Step 4: Add up the numbers written above:

$$48 + 4 = 52$$

So, 52 is the decimal equivalent of the octal number 64.

6	Convert the binary number 101101 to octal.	U	C01	2
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Step 1: Write down the binary number

$$(101101)_2$$

Group all the digits in sets of three starting from the LSB (far right). Add zeros to the left of the last digit if there aren't enough digits to make a set of three.

101 101

Step 2: Use the table below to convert each set of three into an octal digit. In this case, 101=5, 101=5.

So, the number 55 is the octal equivalent to 101101 in binary.

To convert from binary to octal use the following table:

Bin:	000	001	010	011	100	101	110	111
Octal:	0	1	2	3	4	5	6	7

7	Identify the binary value of 135 and convert it into hexadecimal.	U	C01	2
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135 in binary

2	135	1
2	67	1
2	33	1
2	16	0
2	8	0
2	4	0
2	2	0
	1		

$$\therefore 135_{10} = 10000111_2$$

Step 1: Write down the binary number:

10000111

Step 2: Group all the digits in sets of four starting from the LSB (far right). Add zeros to the left of the last digit if there aren't enough digits to make a set of four:

1000 0111

Step 3: Use the table below to convert each set of three into an hexadecimal digit:

1000 = 8, 0111 = 7

So, 87 is the hexadecimal equivalent to the decimal number 10000111.

To convert from binary to hexadecimal use the following table:

Bin: 0000 0001 0010 0011 0100 0101 0110 0111

Hexa: 0 1 2 3 4 5 6 7

Bin: 1000 1001 1010 1011 1100 1101 1110 1111

Hexa: 8 9 A B C D E F

8

Convert the hexadecimal number 3F to decimal and then to binary.

U

c01

2

Part – A (09 x 02 = 18 Marks)
Answer All Questions

RBT

CO

Marks

$$(3F)_{16} = (63)_{10}$$

Step by step solution

Step 1: Write down the hexadecimal number:

$$(3F)_{16}$$

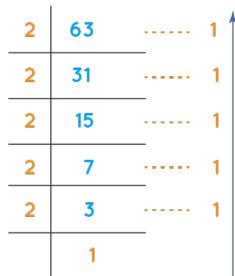
Step 2: Show each digit place as an increasing power of 16:

$$3 \times 16^1 + F \times 16^0$$

Step 3: Convert each hexadecimal digits values to decimal values then perform the math:

$$3 \times 16 + 15 \times 1 = (63)_{10}$$

63 in binary



$$\therefore 63_{10} = 111111_2$$

9

Convert the octal number 127 to binary and then to decimal.

U

C01

2

Part – A (09 x 02 = 18 Marks)
Answer All Questions

RBT

CO

Marks

$$(127)_8 = (1010111)_2$$

Step by step solution

Step 1: Look up each octal digit to obtain the equivalent group of three binary digits. You can use the table below to make these conversions.

Hexadecimal to Binary Conversion Table

Oct:	0	1	2	3	4	5	6	7
Bin:	000	001	010	011	100	101	110	111

$$(1)_8 = (001)_2$$

$$(2)_8 = (010)_2$$

$$(7)_8 = (111)_2$$

Step 2: Group each value of step 1 to make a binary number:

001 010 111

So, $(1010111)_2$ is the binary equivalent to $(127)_8$

$$(1010111)_2 = (87)_{10}$$

Step by step solution

Step 1: Write down the binary number:

1010111

Step 2: Multiply each digit of the binary number by the corresponding power of two:

$$1 \times 2^6 + 0 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$$

Step 3: Solve the powers:

$$1 \times 64 + 0 \times 32 + 1 \times 16 + 0 \times 8 + 1 \times 4 + 1 \times 2 + 1 \times 1 = 64 + 0 + 16 + 0 + 4 + 2 + 1$$

Step 4: Add up the numbers written above:

$$64 + 0 + 16 + 0 + 4 + 2 + 1 = 87$$

10

Convert the binary number 11011011 to hexadecimal and then to octal.

AP

CO1

2

$$(11011011)_2 = (\text{DB})_{16}$$

Step by step solution

Step 1: Write down the binary number:

11011011

Step 2: Group all the digits in sets of four starting from the LSB (far right). Add zeros to the left of the last digit if there aren't enough digits to make a set of four:

1101 1011

Step 3: Use the table below to convert each set of three into an hexadecimal digit:

1101 = D, 1011 = B

So, DB is the hexadecimal equivalent

$$(11011011)_2 = (333)_8$$

Step by step solution

Step 1: Write down the binary number

(011011011)₂

Group all the digits in sets of three starting from the LSB (far right). Add zeros to the left of the last digit if there aren't enough digits to make a set of three.

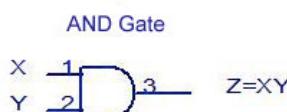
011 011 011

Step 2: Use the table below to convert each set of three into an octal digit. In this case, 011=3, 011=3, 011=3.

So, the number 333 is the octal equivalent to 11011011 in binary.

11	List the basic Boolean operations.	U	C01	2
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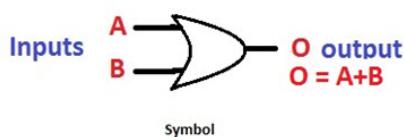
12	Sketch the circuit diagram of AND Gate with its truth Table.	U	C01	2
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TRUTH TABLE

INPUTS		OUTPUT
X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

13	Sketch the circuit diagram of OR Gate with its truth Table.	U	C01	2
----	---	---	-----	---



Inputs		Output
A	B	O
0	0	0
0	1	1
1	0	1
1	1	1

Truth table

14	Sketch the circuit diagram of NOT Gate with its truth Table.	U	C01	2
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Part – A (09 x 02 = 18 Marks)
Answer All Questions

RBT

CO

Marks

A	X = \bar{A}
0	1
1	0



15 Simplify the Boolean expression $A \cdot (B + C)$ using Boolean algebra.

AP

C01

2

AB + AC [Distribution Law]

16 Give the significance of truth table in Boolean Algebra

U

C01

2

Every Boolean expression can be viewed as a truth table. The truth table identifies all possible input combinations and the output for each. It is common to create the table so that the input combinations produce an unsigned binary up-count.

17 Deduce the logic diagram of half adder with its Boolean expression

U

C02

2

Step-01:

Identify the input and output variables-

- Input variables = A, B (either 0 or 1)
- Output variables = S, C where S = Sum and C = Carry

Step-02:

Draw the truth table-

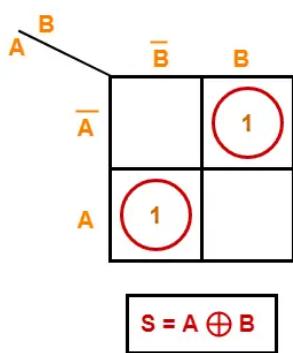
Inputs		Outputs	
A	B	C (Carry)	S (Sum)
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Truth Table

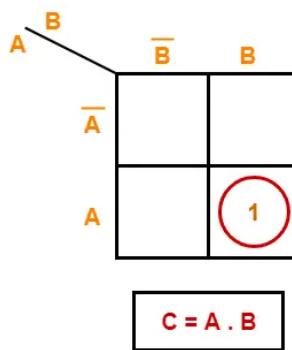
Step-03:

Draw K-maps using the above truth table and determine the simplified Boolean expressions-

For S:



For C:



K Maps

Part – A (09 x 02 = 18 Marks) Answer All Questions					RBT	CO	Marks
18	Obtain the alternative formulae of SUM and CARRY of full adder using minimization of Boolean function.				U	C02	2

A full adder is a combinational circuit that forms the arithmetic sum of three bits. It consists of three inputs and two outputs. Two of the input variables, denoted by x and y represent the two significant bits to be added. The third input, z , represents the carry from the previous lower significant position.

Draw the truth table-

Inputs			Outputs	
x	y	z	C (Carry)	S (Sum)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Truth Table

Step-03:

$$S = x'y'z + x'yz' + xy'z' + xyz$$

$$S = z \oplus x \oplus y$$

$$C = xy + xz + yz$$

19	Differentiate Combinational logic and Sequential logic circuits.	U	C02	2
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Part – A (09 x 02 = 18 Marks) Answer All Questions		RBT	CO	Marks
Combinational circuits	Sequential circuits			
<p>Combinational circuits are defined as the time independent circuits which do not depends upon previous inputs to generate any output are termed as combinational circuits. Sequential circuits are those which are dependent on clock cycles and depends on present as well as past inputs to generate any output. Combinational Circuit –</p> <ol style="list-style-type: none"> 1. In this output depends only upon present input. 2. Speed is fast. 3. It is designed easy. 4. There is no feedback between input and output. 5. This is time independent. 6. Elementary building blocks: Logic gates 7. Used for arithmetic as well as boolean operations. 8. Combinational circuits don't have capability to store any state. 9. As combinational circuits don't have clock, they don't require triggering. 10. These circuits do not have any memory element. 11. It is easy to use and handle. <p>Examples – Encoder, Decoder, Multiplexer, Demultiplexer Block Diagram</p>	<p>Sequential Circuit –</p> <ol style="list-style-type: none"> 1. In this output depends upon present as well as past input. 2. Speed is slow. 3. It is designed tough as compared to combinational circuits. 4. There exists a feedback path between input and output. 5. This is time dependent. 6. Elementary building blocks: Flip-flops 7. Mainly used for storing data. 8. Sequential circuits have capability to store any state or to retain earlier state. 9. As sequential circuits are clock dependent they need triggering. 10. These circuits have memory element. 11. It is not easy to use and handle. 			

Part – A (09 x 02 = 18 Marks)
Answer All Questions

RBT

CO

Marks

20

Give the truth table of half subtractor with logic circuit.

U

CO2

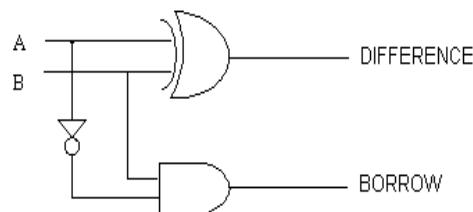
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TRUTH TABLE:

A	B	BORROW	DIFFERENCE
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

$$\text{DIFFERENCE} = A'B + AB'$$

$$\text{BORROW} = A'B$$



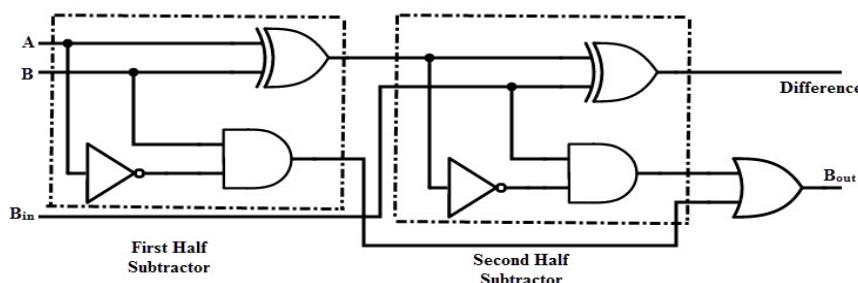
21

Design a full subtractor with logic diagram using half subtractor.

AP

CO2

2



22

Integrate a 2-4 Line decoder logic circuit using the truth table.

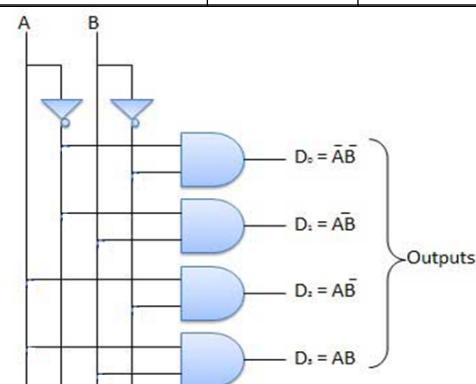
AP

CO2

2

Inputs		Output				
A	B	D ₀	D ₁	D ₂	D ₃	
0	0	1	0	0	0	
0	1	0	1	0	0	
0	1	0	0	1	0	
1	1	0	0	0	1	

Truth Table



Logic Circuit

23

Realize F (X,Y,Z) = $\Sigma (1, 4, 7)$ with a decoder and draw its diagram

AP

CO2

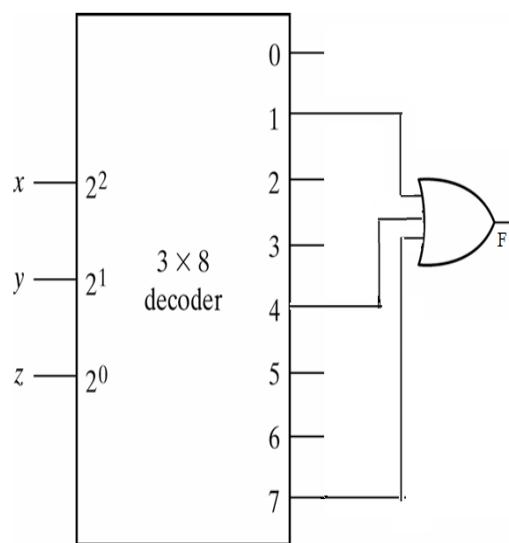
2

Part – A (09 x 02 = 18 Marks)
Answer All Questions

RBT

CO

Marks



24	List the applications of decoder	U	CO2	2
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- Decoders are used for code conversions.
- Decoders are extensively used in memory systems of computers.
- Decoders are also used for de-multiplexing or data distribution.
- Decoders are also used in data routing applications where very short propagation delay is required.

25	Distinguish encoder and decoder in terms of its input and output	U	CO2	2
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Part – A (09 x 02 = 18 Marks) Answer All Questions		RBT	CO	Marks
ENCODER	DECODER			
Encoder circuit basically converts the applied information signal into a coded digital bit stream.	Decoder performs reverse operation and recovers the original information signal from the coded bits.			
In case of encoder, the applied signal is the active signal input.	Decoder accepts coded binary data as its input.			
The number of inputs accepted by an encoder is $2n$.	The number of input accepted by decoder is only n inputs.			
The output lines for an <u>encoder</u> is n .	The output lines of an decoder is $2n$.			
The encoder generates coded data bits as its output.	The decoder generates an active output signal in response to the coded data bits.			
The operation performed is simple.	The operation performed is complex.			
The encoder circuit is installed at the transmitting end.	The decoder circuit is installed at the receiving side.			
OR gate is the basic logic element used in it.	AND gate along with NOT gate is the basic logic element used in it.			
It is used in E-mail, video encoders etc.	It is used in Microprocessors, memory chips etc.			
26	Write the Steps involved in designing a multiplexer.	AP	CO2	2
a. Prepare the function table of the 2:1 Mux b. Formulate the expression for output Y by considering only those FPs for which the output is 1. c. Draw the logic diagram for the expression d. The circuit can also be designed by having an active low enable input as shown in logic table				
27	Estimate the no of MUX needed to create a 4-1 Mux with its diagram	AP	CO2	2
28	Distinguish Latch and Flip flop	U	CO2	2

Part – A (09 x 02 = 18 Marks) Answer All Questions			RBT	CO	Marks
SNO	Flip-flop	Latch			
1	Flip-flop is a bistable device i.e., it has two stable states that are represented as 0 and 1.	Latch is also a bistable device whose states are also represented as 0 and 1.			
2	It checks the inputs but changes the output only at times defined by the clock signal or any other control signal.	It checks the inputs continuously and responds to the changes in inputs immediately.			
3	It is a edge triggered device.	It is a level triggered device.			
4	Gates like NOR, NOT, AND, NAND are building blocks of flip flops.	These are also made up of gates.			
5	They are classified into asynchronous or synchronous flipflops.	There is no such classification in latches.			
6	It forms the building blocks of many sequential circuits like counters.	These can be used for the designing of sequential circuits but are not generally preferred.			
7	a, Flip-flop always have a clock signal	Latches doesn't have a clock signal			
8	Flip-flop can be build from Latches	Latches can be build from gates			
9	ex:D Flip-flop, JK Flip-flop	ex:SR Latch, D Latch			
29	Discuss the connection between memory and processor	U	C03	2	
30	Classify the functional units of Computer organization.	U	C03	2	
31	Infer the advantages of One, two and three address instruction format.	U	C03	2	
32	Give the features of instruction set.	U	C03	2	
33	Mention the types of instruction set.	U	C03	2	
34	Interpret addressing modes and its types in 8086 processor.	U	C03	2	
35	Compare hardwired and micro-programmed control unit design.	U	C03	2	
36	Differentiate half adder and full adder with a neat sketch.	U	C03	2	
37	Annotate three address instruction set with suitable block diagram	U	C03	2	
38	Classify the important terms in addressing modes	U	C03	2	

Part – A (09 x 02 = 18 Marks) Answer All Questions		RBT	CO	Marks
39	Infer Immediate addressing mode using suitable block diagram	U	C03	2
40	Compare two types of indirect addressing modes.	U	C03	2

Part – B (02 x 16 = 32 Marks) Answer All Questions		RBT	CO	Mar ks
1a	Simplify the given Boolean function using three-variable K-map $F(x, y, z) = \sum(0, 1, 2, 3, 5)$ a. Write the minterms in truth table format	AP	C01	8

$x \backslash y$	00	01	10	11
0	1	1	1	1
1	1	1	1	0
	4	5	6	7

$$F = x' + y'z$$

Truth Table

x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

circuit diagram

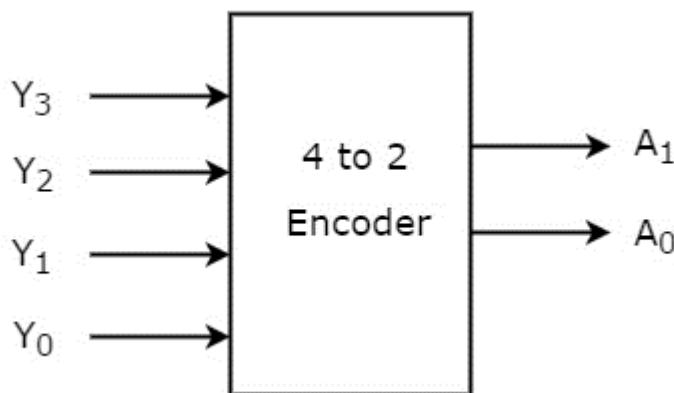
x AND y AND z; P NAND T NOT P

Part – B (02 x 16 = 32 Marks) Answer All Questions						RBT	CO	Mar ks																																		
1b	For the above mentioned minterm in 1.a Plot K-map and Simplify the expression and draw the circuit diagram for the expression					AP	C01	8																																		
2a	Convert the following other base values to decimal a. $(0.234)_6$ b. $(0.653)_7$					AP	C01	8																																		
2b	Convert the following other base values to decimal a. $(211)_7$ b. $(F5)_{16}$					AP	C01	8																																		
3	The truth table of a 4 to 2 Encoder is given: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="4">INPUTS</th> <th colspan="2">OUTPUTS</th> </tr> <tr> <th>Y_3</th> <th>Y_2</th> <th>Y_1</th> <th>Y_0</th> <th>A_1</th> <th>A_0</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	INPUTS				OUTPUTS		Y_3	Y_2	Y_1	Y_0	A_1	A_0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0	1	1	1			AP	C01	16
INPUTS				OUTPUTS																																						
Y_3	Y_2	Y_1	Y_0	A_1	A_0																																					
1	0	0	0	0	0																																					
0	1	0	0	0	1																																					
0	0	1	0	1	0																																					
0	0	0	1	1	1																																					
	i) Draw the logical diagram of 4 to 2 Encoder. ii) Using the truth table of 4 to 2 Encoder obtain the conversion of an Octal to Binary Encoder (i.e. 8 to 3 Encoder). iii) Identify the expressions for the outputs. iv) Draw the circuit diagram depicting the expressions obtained.																																									

An **Encoder** is a combinational circuit that performs the reverse operation of Decoder. It has maximum of 2^n input lines and 'n' output lines. It will produce a binary code equivalent to the input, which is active High. Therefore, the encoder encodes 2^n input lines with 'n' bits. It is optional to represent the enable signal in encoders.

4 to 2 Encoder

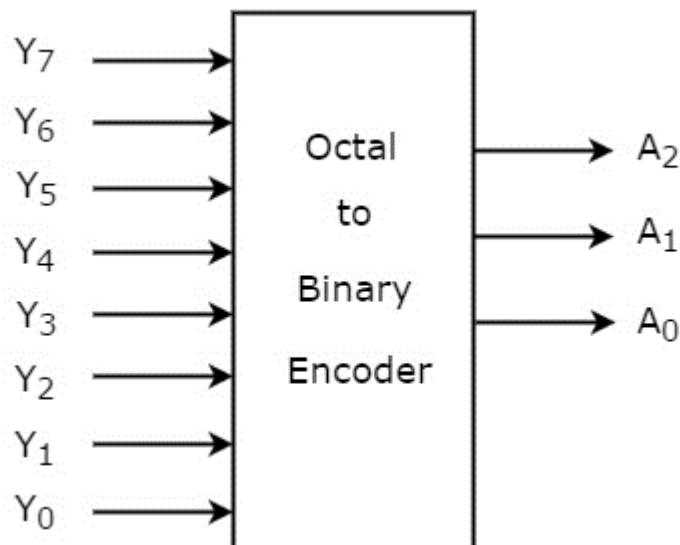
Let 4 to 2 Encoder has four inputs Y_3, Y_2, Y_1 & Y_0 and two outputs A_1 & A_0 . The **block diagram** of 4 to 2 Encoder is shown in the following figure.



ii)

Octal to Binary Encoder

Octal to binary Encoder has eight inputs, Y_7 to Y_0 and three outputs A_2, A_1 & A_0 . Octal to binary encoder is nothing but 8 to 3 encoder. The **block diagram** of octal to binary Encoder is shown in the following figure.



At any time, only one of these eight inputs can be '1' in order to get the respective binary code. The **Truth table** of octal to binary encoder is shown below.

Inputs

Outputs

Part – B (02 x 16 = 32 Marks) Answer All Questions			RBT	CO	Marks
4a	Write the following laws of Boolean algebra: a. Commutative law b. Associative law		U	C01	8

COMMUTATIVE LAW

LAW 1 : $A + B = B + A$

LAW 2 : $A \cdot B = B \cdot A$

ASSOCIATIVE LAW

LAW 1 : $A + (B + C) = (A + B) + C$

LAW 2 : $A \cdot (B \cdot C) = (A \cdot B) \cdot C$

4b	Explain the following Boolean algebra: a. Distributive law b. Demorgans law	U	C01	8
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Distributive Laws

LAW 1 : $A \cdot (B + C) = A \cdot B + A \cdot C$

LAW 2 : $A + (B \cdot C) = (A + B) \cdot (A + C)$

Demorgan's Laws

LAW1 : $(A \cdot B)' = A' + B'$

LAW2 : $(A + B)' = A' \cdot B'$

5	Describe in detail consensus Theorem with example	U	C01	16
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Part – B (02 x 16 = 32 Marks)
Answer All Questions

RBT

CO

**Mar
ks**

Consensus Theorem

Given a pair of terms for which a variable appear in one term and its complement appear in another, the consensus term can be obtained by multiplying the two original terms together leaving out a selected variable and its complement

$$AB + A'C + BC$$

$$= AB + A'C + (A + A')BC$$

$$= AB + A'C + ABC + A'BC$$

$$= AB + ABC + A'C + A'BC$$

$$= AB(1 + C) + A'C(1 + B)$$

$$= AB \cdot 1 + A'C \cdot 1$$

$$= AB + A'C$$

6a	Simplify the following Boolean expressions: a. $ABC + A'B + ABC'$	AP	C01	8
	$\begin{aligned} & AB(C+C') + A'B \\ & = AB + A'B \\ & = B(A+A') \\ & = B \end{aligned}$			
6b	Simplify the following Boolean expressions: a. $(BC' + A'D).(AB' + CD')$	AP	C01	8
$AB'BC' + AB'A'D + CD'BC' + CD'A'D = 0$				
7a	Simplify the following Boolean expressions. a. $(X+Y).(X+Y')$	AP	C01	8
7b	Simplify the following Boolean Function and draw its K map. $F=X+X'Y$	AP	C01	8
8	Explain in detail logic gates (AND, OR, NAND, NOR) with its logical diagram, Truth table, Boolean expression.	U	C01	16
9a	Minimize the given function $((CD' + A')' + A + CD + AB$ to three literal format.	AP	C01	8
9b	Minimize the given function $(ABC + BD + BC)(ACD)$ into three literal format	AP	C01	8
10a	Explain Toggle flip-flop with its Logical diagram, function table and characteristic equation.	U	C01	8

Part – B (02 x 16 = 32 Marks) Answer All Questions			RBT	CO	Marks
10b	Explain JK Flip-flop with logic symbol and truth table		U	C01	8
11	Design a 1 to 4 De-multiplexer using 1 to 2 De-multiplexer.		AP	C01	8
12a	Design a 4-bit Binary adder using twos complement Circuit diagram.		AP	C02	8
12b	Design a 4-bit Binary subtractor using twos complement Circuit diagram.		AP	C02	8
13a	Explain the quadruple 2-1 multiplexers with neat sketch		U	C02	8
13b	Explain cascading multiplexer with neat sketch		U	C02	8
14a	Design a real-time circuit for adding two binary numbers using a half adder.		AP	C02	8
14b	Differentiate full adder and half adder in terms of carry and obtain the expression for carry in both Half and Full adders.		AP	C02	8
15a	Implement a Full adder with a decoder		AP	C02	8

Part – B (02 x 16 = 32 Marks)
Answer All Questions

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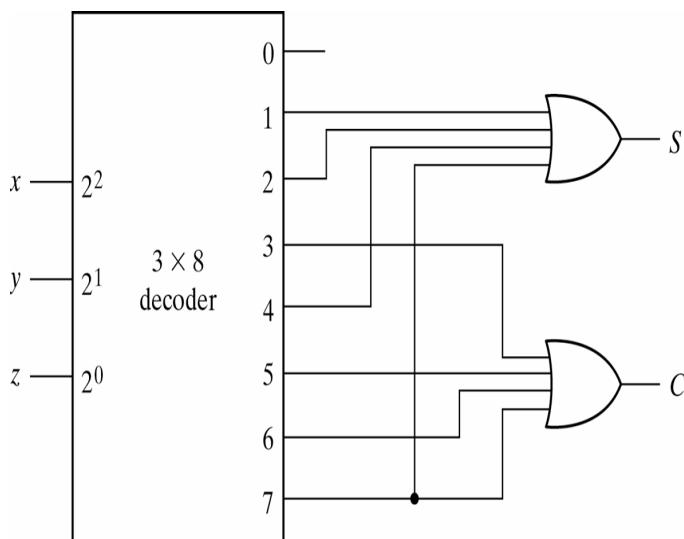
x	y	z	c	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Truth table

- The functions can be expressed in sum of min-terms.

$$S(x,y,z) = \Sigma m(1,2,4,7)$$

$$C(x,y,z) = \Sigma m(3,5,6,7)$$



15b	Design the circuit with decoder and external logic gates: $F_1=x'y'z'+xz$; $F_2=xy'z'+x'y$; $F_3=x'y'z+xy$	AP	CO2	8
16	Design 16x1 multiplexer with two 8x1 MUX and one 2-to-1 multiplexer and draw its truth table	AP	CO2	16

Part – B (02 x 16 = 32 Marks)
Answer All Questions

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Multiplexer is one of the basic building units of a computer system which in principle allows sharing of a common line by more than one input lines. It connects multiple input lines to a single output line. At a specific time one of the input lines is selected and the selected input is passed on to the output line.

Relation between multiple Input lines and Selection lines

Input lines $16 = 2^4$ i.e. 4 Selection lines

Input lines will be $I_0 - I_{15}$

Selection lines will be $S_0 - S_3$

Truth Table

Selection Inputs				Output
S_3	S_2	S_1	S_0	Y
0	0	0	0	I_0
0	0	0	1	I_1
0	0	1	0	I_2
0	0	1	1	I_3
0	1	0	0	I_4
0	1	0	1	I_5
0	1	1	0	I_6
0	1	1	1	I_7
1	0	0	0	I_8
1	0	0	1	I_9
1	0	1	0	I_{10}
1	0	1	1	I_{11}
1	1	0	0	I_{12}
1	1	0	1	I_{13}
1	1	1	0	I_{14}
1	1	1	1	I_{15}



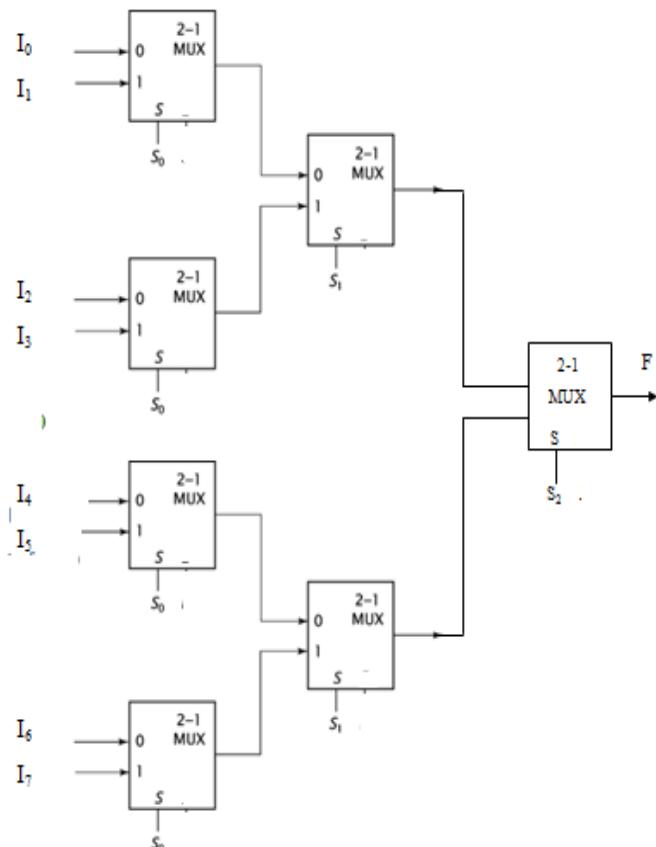
Part – B (02 x 16 = 32 Marks)
Answer All Questions

RBT CO Marks

17 Construct a 8-1 Line multiplexer using 2-1 multiplexers with its truth table

AP CO2 16

S ₂	S ₁	S ₀	F
0	0	0	I ₀
0	0	1	I ₁
0	1	0	I ₂
0	1	1	I ₃
1	0	0	I ₄
1	0	1	I ₅
1	1	0	I ₆
1	1	1	I ₇



18a Implement the min-term of Boolean Function using 4X1 MUX
 $F(A,B,C)=\sum m(1,3,5,6)$

AP CO2 8

Part – B (02 x 16 = 32 Marks)
Answer All Questions

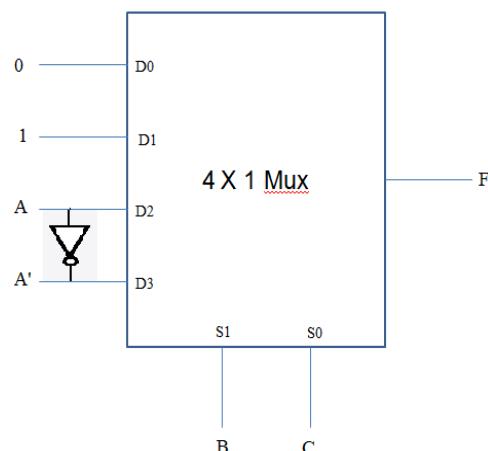
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	I ₀	I ₁	I ₂	I ₃
A'	0	1	2	3
A	4	5	6	7
	0	1	A	A'

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



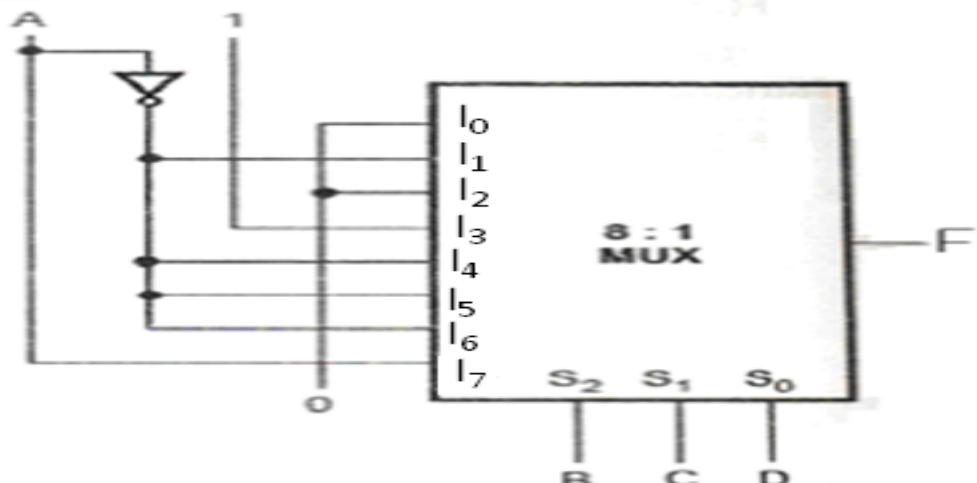
18b	Explain the applications of multiplexer in detail.	U	CO2	8
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19a	i) Implement the min-term of Boolean Function using 8X1 MUX $F(A,B,C,D)=\sum m(0,1,3,4,5,6,11,15)$	AP	CO2	8
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Implementation Table

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	0	A'	0	1	A'	A'	A'	A

Logic Circuit



19b	Explain the applications of De-multiplexer in detail	U	CO2	8
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20a	Convert the following decimal value 34 into excess three code	AP	CO2	8
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The excess-3 code plays an important role in representing the decimal numbers. The Excess-3 code can also be represented as the XS-3 code. In Excess-3 code, each digit of the decimal number is represented by adding 3 in each decimal digit. There are the following steps to convert the binary number into Excess-3 code:

1. Convert the binary number into decimal.
2. Add 3 in each digit of the decimal number.
3. Find the binary code of each digit of the newly generated decimal number.

We can also add 0011 in each 4-bit BCD code of the decimal number for getting excess-3 code.

$$(34)_{10} = (\underline{\quad ? \quad})_{\text{Excess 3}}$$

Solution:

$$(34)_{10} = (\underline{\quad \quad \quad})_{\text{XS3}}$$

$$\begin{array}{r}
 3 \qquad 4 \\
 +3 \qquad +3 \\
 \hline
 =6 \qquad =7 \\
 \hline
 0110 \quad 0111
 \end{array}$$

$$\therefore (34)_{10} = (01100111)_{\text{XS3}}$$

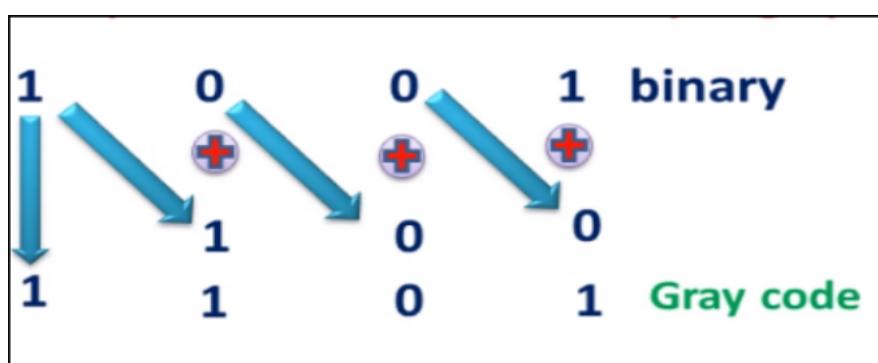
20b	Explain in detail gray code with suitable example	U	C02	8
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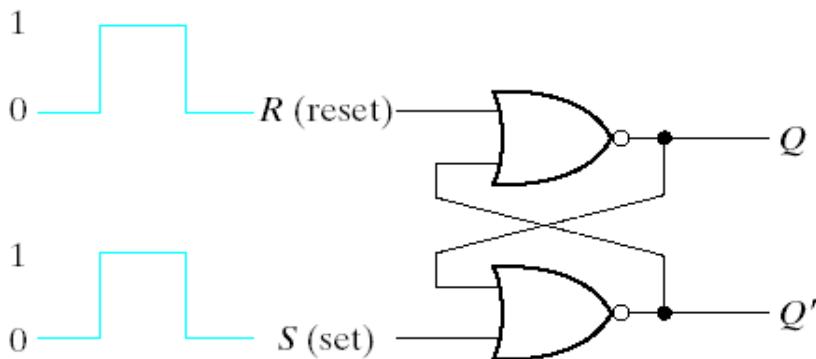
- **Unit Distance Code:** Two Consecutive numbers differ in one bit position only ie, each gray code differs from the preceding code by one bit.
- **Reflected Code:** Obtained by changing only one bit starting from any bit combination.
 - Gray Code is of both reflective and unit distance code. .
 - Gray code is not a BCD Code and it is non-weighted code.

Ensure that no two numbers have the same gray code.

Decimal	binary	Gray code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101

- Given Binary Number: 1001





(a) Logic diagram

S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

(after $S = 1, R = 0$)
 (after $S = 0, R = 1$)

(b) Function table

Fig. 5-3 SR Latch with NOR Gates

The latch has two useful states. When output $Q = 1$ and $Q' = 0$, the latch is said to be in the *set state*. When $Q = 0$ and $Q' = 1$, it is in the *reset state*. Outputs Q and Q' are normally the complement of each other. However, when both inputs are equal to 1 at the same time, a condition in which both outputs are equal to 0 (rather than be mutually complementary) occurs. If both inputs are then switched to 0 simultaneously, the device will enter an unpredictable or undefined state or a metastable state. Consequently, in practical applications, setting both inputs to 1 is forbidden. Under normal conditions, both inputs of the latch remain at 0 unless the state has to be changed. The application of a momentary 1 to the S input causes the latch to go to the set state. The S input must go back to 0 before any other changes take place, in order to avoid the occurrence of an undefined next state that results from the forbidden input condition.

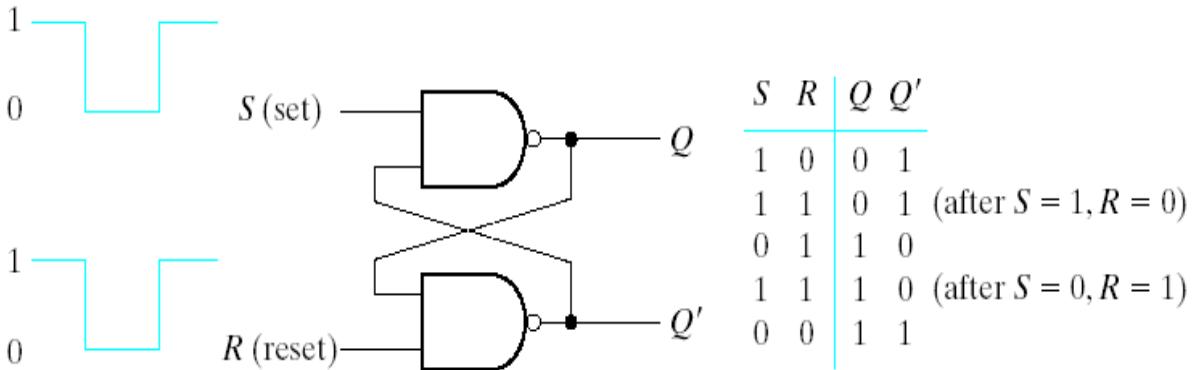
21b Explain the function table of SR Latch with NAND gates

U

CO2

8

Part – B (02 x 16 = 32 Marks) Answer All Questions	RBT	CO	Mar ks
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(a) Logic diagram

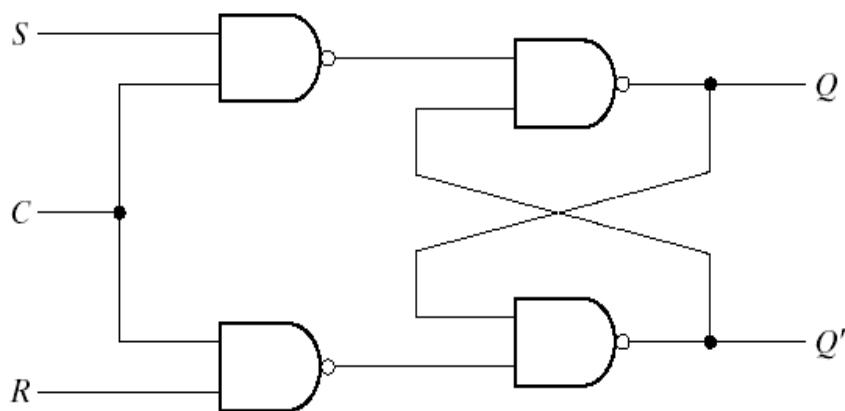
(b) Function table

Fig. 5-4 SR Latch with NAND Gates

The *SR* latch with two cross-coupled NAND gates is shown figure. It operates with both inputs normally at 1, unless the state of the latch has to be changed. The application of 0 to the *S* input causes output *Q* to go to 1, putting the latch in the set state. When the *S* input goes back to 1, the circuit remains in the set state. After both inputs go back to 1, we are allowed to change the state of the latch by placing a 0 in the *R* input. This action causes the circuit to go to the reset state and stay there even after both inputs return to 1. The condition that is forbidden for the NAND latch is both inputs being equal to 0 at the same time, an input combination that should be avoided. In comparing the NAND with the NOR latch, note that the input signals for the NAND require the complement of those values used for the NOR latch. Because the NAND latch requires a 0 signal to change its state, it is sometimes referred to as an *S'R'* latch. The primes (or, sometimes, bars over the letters) designate the fact that the inputs must be in their complement form to activate the circuit.

22	Describe different types of Flip-flops with truth table and logic symbol	U	C02	16
23a	Convert SR latch into clocked RS Flip-flop and draw its Logic diagram	AP	C02	8

The operation of the basic SR latch can be modified by providing an additional control input that determines when the state of the latch can be changed.



(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

Fig. 5-5 SR Latch with Control Input

The operation of the basic SR latch can be modified by providing an additional input signal that determines (controls) when the state of the latch can be changed by determining whether S and R (or S' and R') can affect the circuit. An SR latch with a control input is shown. It consists of the basic SR latch and two additional NAND gates. The control input En acts as an enable signal for the other two inputs. **The outputs of the NAND gates stay at the logic-1 level as long as the enable signal remains at 0.** This is the quiescent condition for the SR latch. When the enable input goes to 1, information from the S or R input is allowed to affect the latch. The set state is reached with S = 1, R = 0, and En = 1.

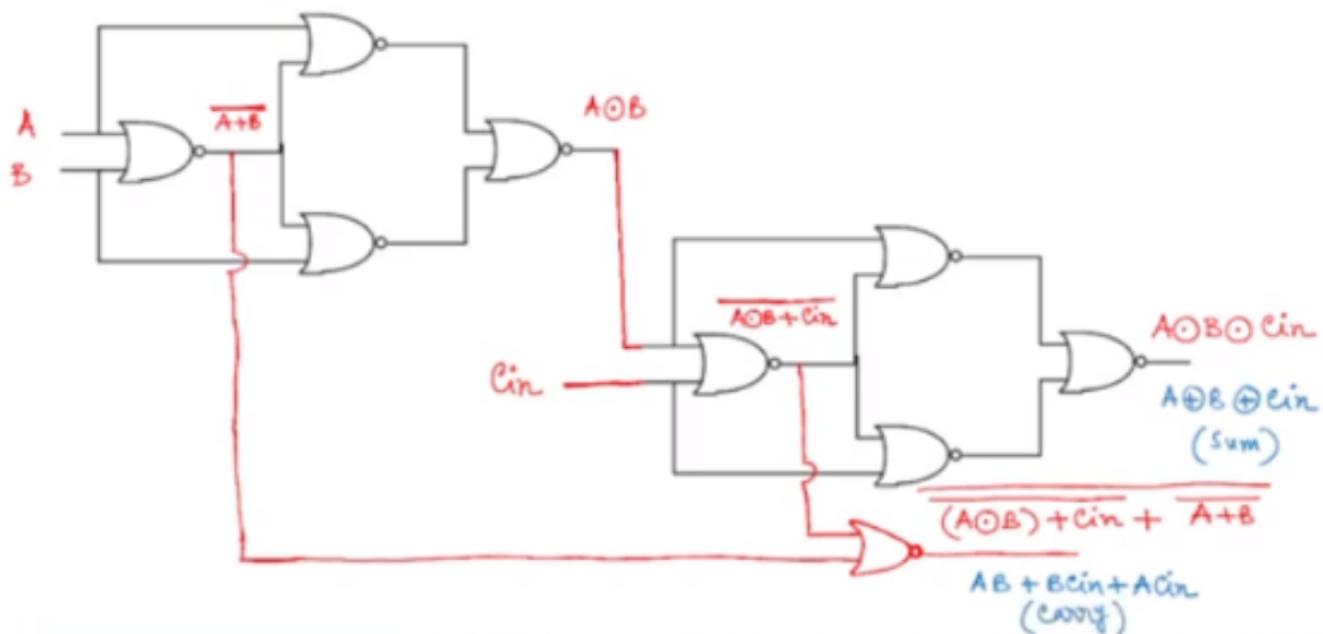
23b	Derive the characteristic equation of clocked RS Flip-flop	AP	CO2	8
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Characteristic table - Clocked RS Flip Flop

		Q(t)	S	R	Q(t+1)
SR		0	0	0	0/Q(t)/PS
Q(t)		0	0	1	0
0		0	1	0	1
1		0	1	1	Not allowed
1		1	0	0	1/Q(t)/PS
Q (t+1) = S+QR'		1	0	1	0
		1	1	0	1
		1	1	1	Not allowed

24a	Design a full adder circuit using only NOR gates.	AP	CO2	8
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~: Full Adder using Min no of NOR Gate:~



<https://youtu.be/izxslnX1RFg>

<https://de-iitr.vlabs.ac.in/exp/half-full-adder/theory.html>

24b	Design a half adder using at most three NOR gates.	AP	C02	8
25a	Explain registers and shift registers with a neat sketch.	U	C03	8

Part – B (02 x 16 = 32 Marks)
Answer All Questions

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- Register is simply a group of Flip-flops that can be used to store a binary number.
- There must be one Flip-flop for each bit in a binary number.

e.g.: A register used to store 8 bit binary number must have 8 Flip-Flops.

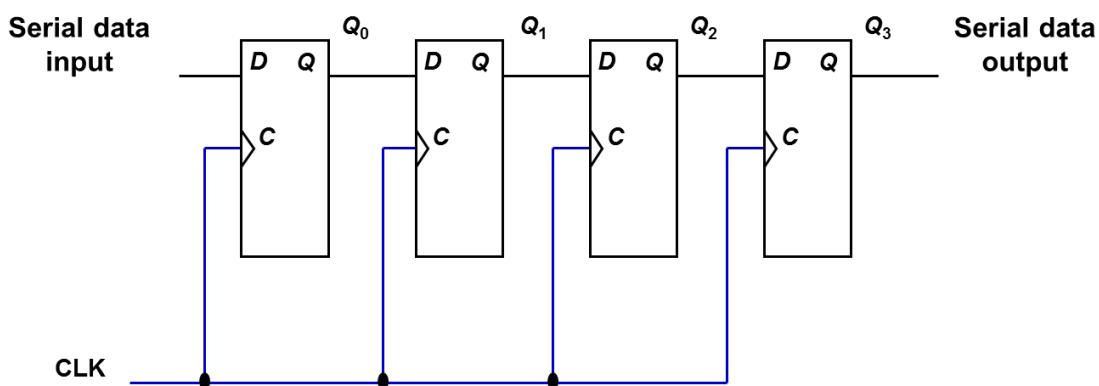
- Flip-flop can be constructed such that the binary number can be shifted into the register and possibly shifted out.
- Both of these functions can be performed by connecting a groups of Flip flops that is called Shift Register.
- A register capable of shifting its binary information in one or both direction is called a **shift register**.
- All flip-flops receive common clock pulses, which activate the shift from one stage to the next.
- Bits in a binary number can be moved from one place to another in either of the two ways:
- Shifting the data one bit at a time in a serial manner beginning with either MSB or LSB. This shifting is referred to as serial shifting.
- Shifting all the data bits simultaneously and it is referred to as parallel shifting. There are two ways to shift the data into the register and two ways to shift the data out of the register.

Types of Shift Register

- Serial-in/serial-out
- Serial-in/parallel-out
- Parallel-in/parallel-out
- Parallel-in/serial-out

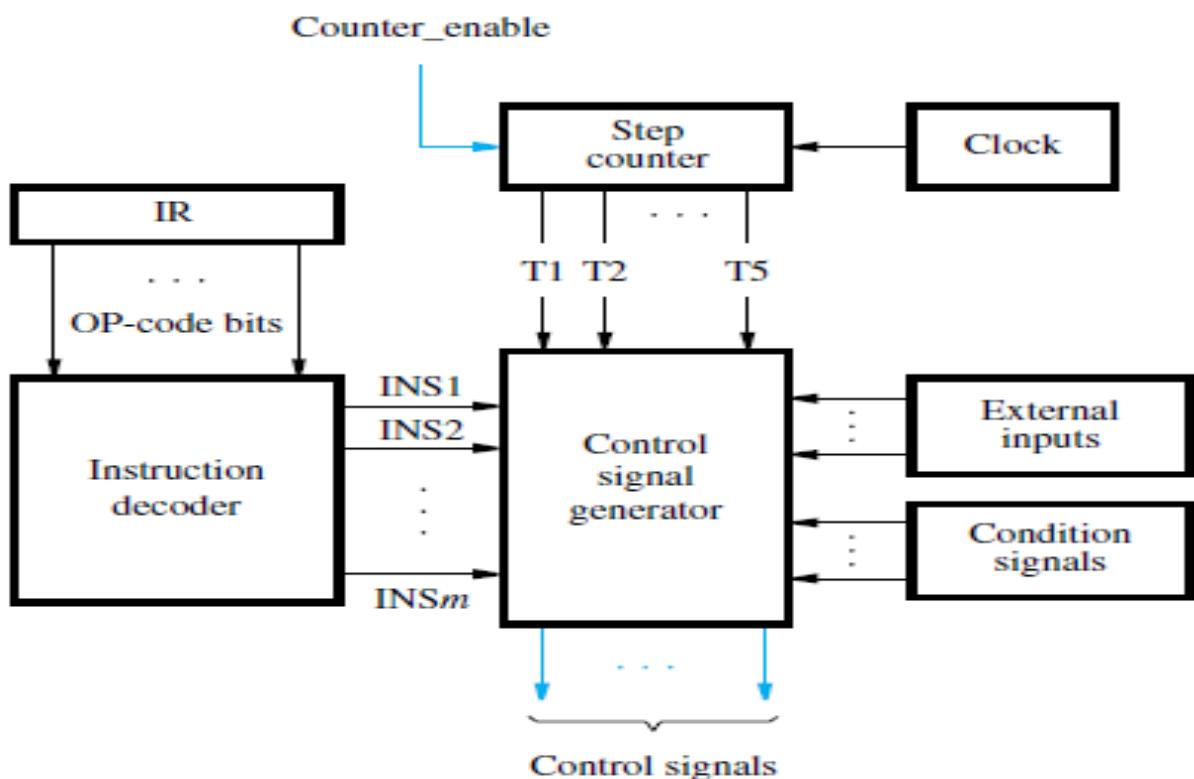
Serial In/Serial Out Shift Registers

- It accepts data serially, one bit at a time on a single line, and produces the sorted information on its output also in a serial form



Serial In/Parallel Out shift registers

Part – B (02 x 16 = 32 Marks) Answer All Questions		RBT	CO	Mar ks
25b	Compare and contrast the four types of Shift Registers and give their logical diagrams.	U	C03	8
26	Compare and contrast various types of CPU Design.	U	C03	8
27a	Summarize the importance of instruction sets	U	C03	8
27b	Describe the implementation of instruction sets computer architecture	U	C03	8
28	Explain in detail various functional units of computer organization with neat sketch.	U	C03	16
29a	Describe the various types of instruction formats with its pros and cons	U	C03	8
29B	Explain in detail different addressing modes with example	U	C03	8
30a	Explain in detail Hardwired design of CPU with neat diagram.	U	C03	8



Hardwired control Unit

- Hardwired system can operate at high speed.
- The setting of the control signals depends on:
 - Contents of the step counter
 - Contents of the instruction register
 - The result of a computation or a comparison operation (for branch instruction)
 - External input signals, such as interrupt requests
- The instruction decoder sets INS_i signal based on decoded instruction.
- During each clock cycle, one of the outputs T_i is set to 1 to indicate which of the five steps involved executing instructions.
- Modulo-5 counter is used.
- Hardwired control Unit
- Example,
- step 1 in the instruction execution process - new instruction is fetched from the memory.
- It is identified by signal T_1
- PC as the source of the memory address,

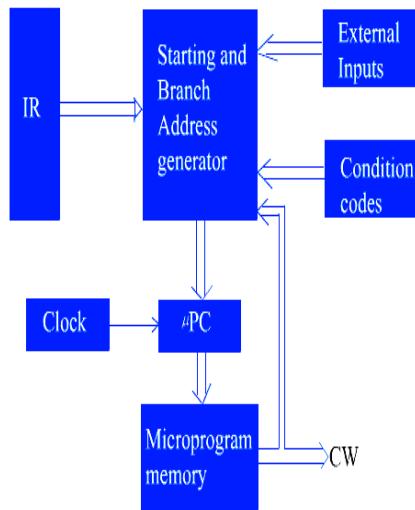
Part – B (02 x 16 = 32 Marks) Answer All Questions		RBT	CO	Mar ks
30b	Explain in detail Micro programmed design of CPU with neat diagram	U	CO3	8

Part – B (02 x 16 = 32 Marks)
Answer All Questions

RBT

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- Another type of control signal generation
- Controlled signals are generated using programmes
- Slower than hardwired approach
- Control word - A word whose individual bits

represent various control signals

- Microinstructions - The individual control words in the micro routine
- Micro routine or Micro program - A sequence of CW's corresponding to the instruction
- Control store – Special memory used to store the micro routines for all instructions

The control unit can generate the control signals by sequentially reading the CW's from the control store

