iCE40 UltraPlus Display Frame Buffer

User Guide

FPGA-UG-02009 Version 1.1

March 2017

Contents

1. Introduction 3
1.1. Clock Generator Module 3
1.2. Main Control Module 3
1.3. SPRAM Module 4
1.4. Decompress Module 4
1.5. 8BIT2RGB Module 4
1.6. MIPI DSI TX Module 4
2. Demo Setup 5
2.1. Requirements 5
2.2. Jumper Settings 6
3. Programming the Bitmaps to the MDP Board 7
4. Running the Demo 10
5. Resource Utilization 10
Technical Support Assistance 11
Revision History 12

Figures

Figure 1.1. Display Frame Buffer Demo Block Diagram 3
Figure 1.2. SPRAM Primitive 4
Figure 2.1. iCE40 UltraPlus MDP Board Details 5
Figure 3.2. Diamond Programmer Main Interface 7
Figure 3.3. Device Properties Dialog Box 8
Figure 3.5. Program Information 9

Tables

Table 5.1. Resource Utilization 10

© 2016-2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

1. Introduction

The iCE40 UltraPlus™ Display Frame Buffer demo consists of the following modules:

- Clock Generator
- SPRAM (Single Port RAM Memory)
- Main Control
- Decompress
- 8BIT2RGB
- MIPI DSI TX

Figure 1.1 shows the demo structure diagram.

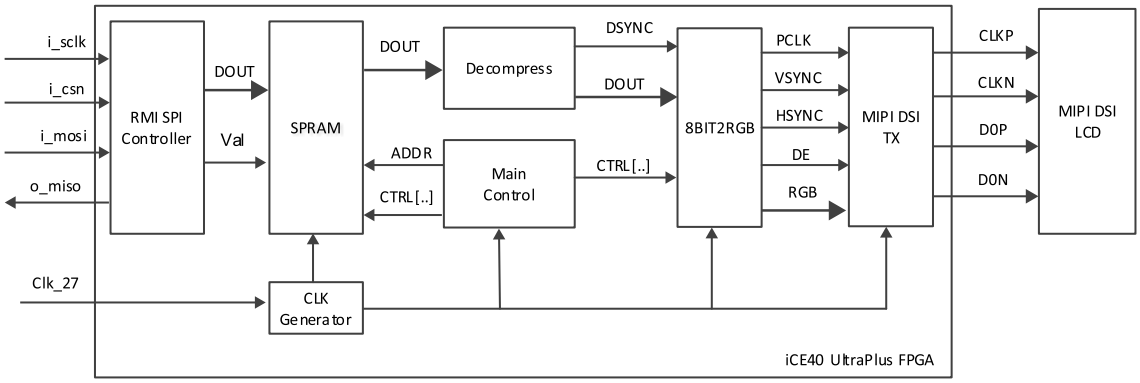

Figure 1.1. Display Frame Buffer Demo Block Diagram

1.1. Clock Generator Module

The iCE40 UltraPlus device has one sysClock PLL. The internal PLL generates two 54 MHz DDR clocks for other modules. One 54 MHz clock has a 90-degree phase shift relative to the other one.

1.2. Main Control Module

The basic functions of the main control module include:

- Reading image data from the internal SPRAM
- Sending the read data synchronously to the decompress module

In this demo, three images are stored in the internal SPRAM. The main control module continuously reads each image between an interval of three seconds.

© 2016-2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

1.3. SPRAM Module

iCE40 UltraPlus has a 1-Mbit sysMEM SPRAM. The SPRAM block is implemented to be accessed only as a single port. Each block of SPRAM is designed to be 16 Kb x 16 Kb (256 Kb) in size. In this demo, the System Solution Platform (SSP) tool is used to write three compressed image data to the SPRAM.

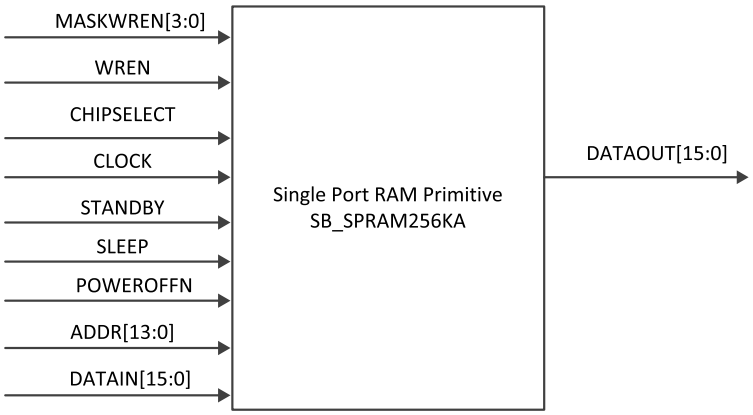

Figure 1.2. SPRAM Primitive

1.4. Decompress Module

The Decompress module decompresses the image data from the SPRAM and sends it to the 8BIT2RTB module.

1.5. 8BIT2RGB Module

The 8BIT2RGB module receives data from the Decompress module, generates synchronous signals and sends pixel data to the MIPI DSI TX module.

1.6. MIPI DSI TX Module

The MIPI DSI TX module packages standard parallel data into DSI byte packets. The input interface of the design consists of the following:

- data bus (PIXDATA))
- vertical and horizontal sync flags (VSYNC and HSYNC))
- data enable and clock (DE and PIXCLK)).

This parallel bus is converted to the appropriate DSI output format. The DSI output serializes HS (High Speed) data and controls LP (Low Power) data and transfers them using the Lattice MIPI D-PHY Reference IP.

© 2016-2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2. Demo Setup

2.1. Requirements

The iCE40 UltraPlus display frame buffer demo setup consists of the following hardware platforms and software operation tools.

- **Hardware**
  - iCE40 UltraPlus Mobile Development Platform (MDP) (Revision C)
  - USB to mini-USB cable
- **Software**
  - Diamond Programmer (Version 3.8)
  - System Solution Platform (SSP)

Note: SSP installer and installation guide are included with this solution under the SSP folder. Follow the instructions in the guide to install this application properly.

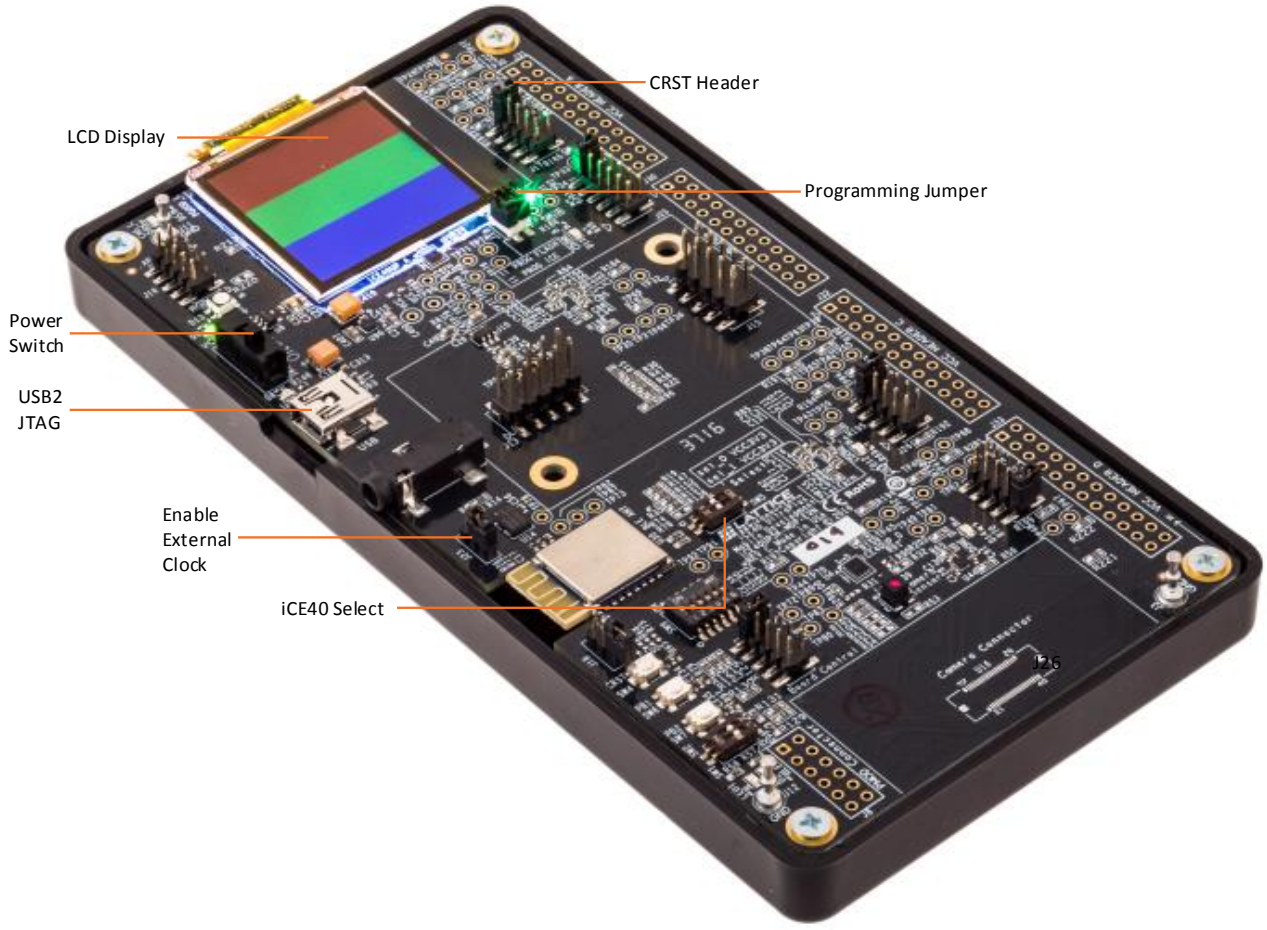

Figure 2.1. iCE40 UltraPlus MDP Board Details

© 2016-2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.2. Jumper Settings

To set the jumpers:

1. Connect jumper J19 for Flash program.
2. Switch SW5 to position “OFF/OFF” to program iCE40UP_A.
3. Connect jumper J23 Pin 2 and Pin 3 to enable osc_clk.
4. Connect jumper J17 Pin 1 and Pin 2.
5. Connect jumper J25, J26, J27 Pin 1 and Pin 2 respectively.
6. Connect LCD display to J2.

© 2016-2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

3. Programming the Bitmaps to the MDP Board

To program the bitmaps to the MDP board:

1. Install the Lattice SSP tool for this demo. For more details on the Lattice SSP tool, refer to SSP Installation and Deployment Usage Guide.pdf and SSP Operation Tool Kits Usage Guide.pdf.
   Note: The SSP user guides are included with this solution under the SSP folder.
2. Connect the iCE40 UltraPlus MDP to the PC using a USB mini port (J5).
3. Switch SW2 to ON to power up the iCE40 UltraPlus MDP.
4. Start the Diamond Programmer tool.
5. In the Getting Started dialog box, select **Create a new blank project** as shown in Figure 3.1.

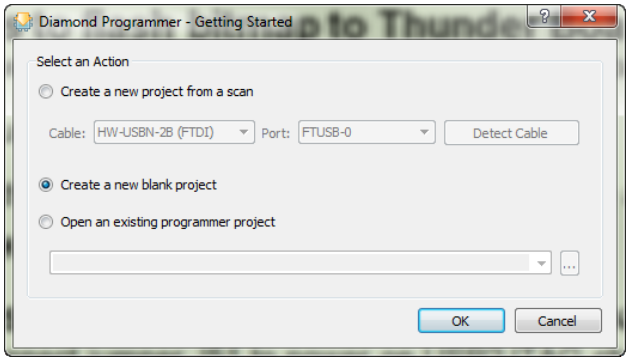

Figure 3.1. Getting Started Dialog Box

6. Click **OK**. This opens the Diamond Programmer main interface as shown in Figure 3.2.
7. Select **iCE40 UltraPlus** under **Device Family**.
8. Select **iCE40UP5K** under **Device**.
9. Set **Cable** to **HW-USBN-2B (FTDI)**.
10. Set Port to **FTUSB-0**.

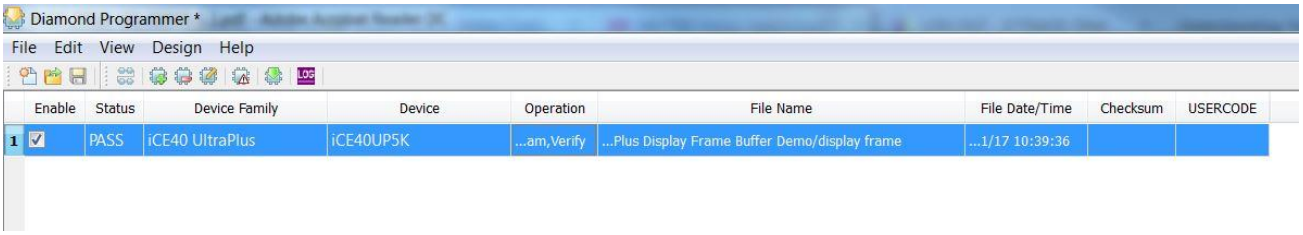

Figure 3.2. Diamond Programmer Main Interface

11. Double-click under **Operation** to open the Device Properties dialog box as shown in Figure 3.3.
12. Select **SPI Flash Programming** under **Access mode**.
13. Select **Numonyx** under **Vendor**.
14. Select **SPI-M25P80** under **Device**.
15. Select the program file `/Bitmap/Display_Frame_Buffer_bitmap.hex`.
16. Click **OK**.

© 2016-2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

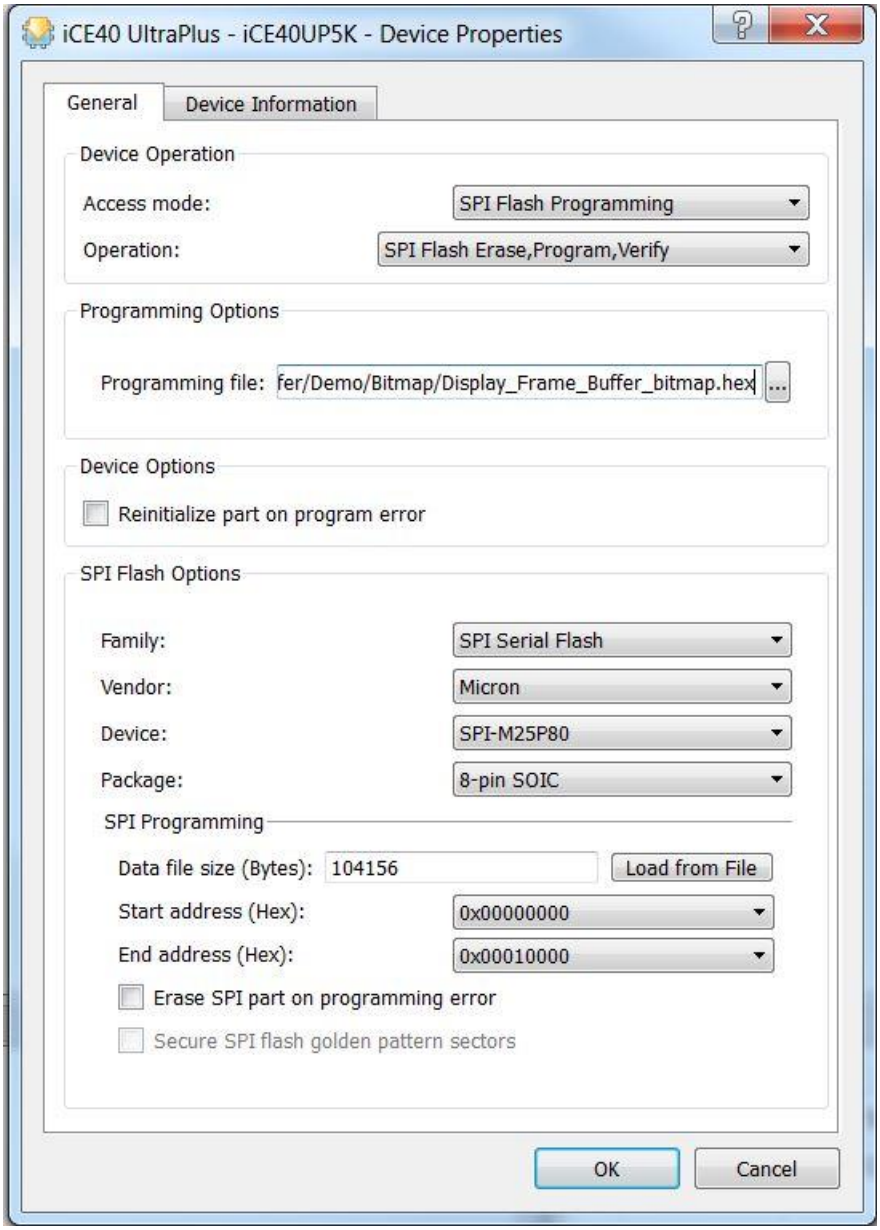

Figure 3.3. Device Properties Dialog Box

17. Click the **Program** button to program the FPGA.

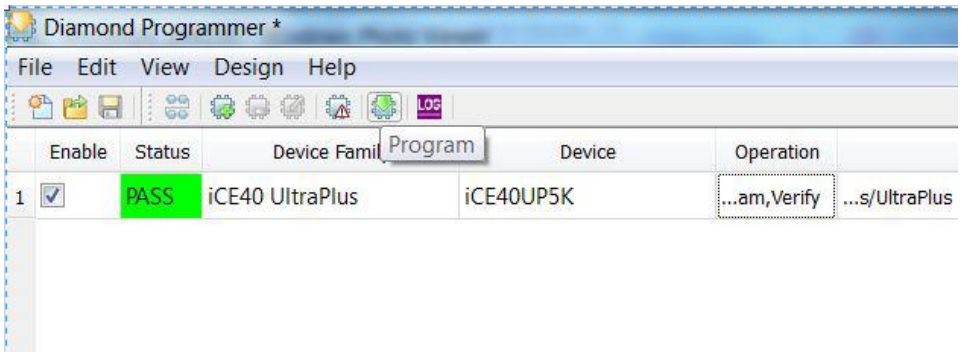

Figure 3.4. Program Button

© 2016-2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

18. Check the program information.

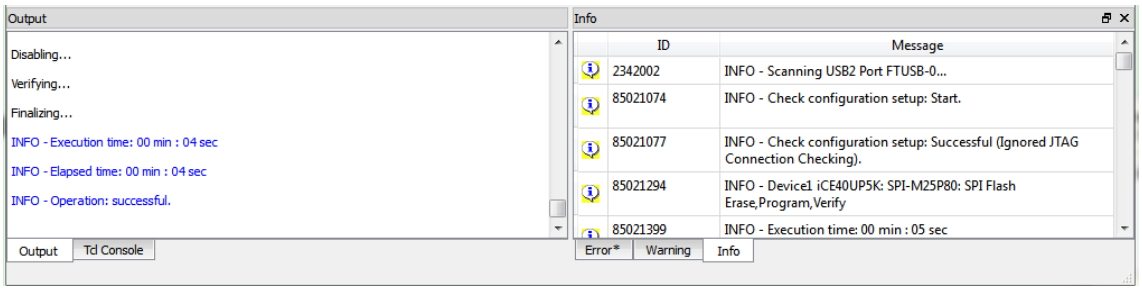

Figure 3.5. Program Information

© 2016-2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

4. Running the Demo

To run the demo:

1. Follow the steps in the Programming the Bitmaps to the MDP Board section so that the iCE40 UltraPlus MDP and SSP are ready with the necessary bitmap and picture data files.
2. Power ON the iCE40 UltraPlus MDP. DONE_A lights up and the LCD display shows a color bar.
3. Start CMD prompt, change directory to where the `Frame_buffer_demo.bat` file is located and run this file to write the picture data to the iCE40 UltraPlus SPRAM.
4. Picture images are displayed on the DSI LCD one after the other in an interval of three seconds.

5. Resource Utilization

Table 5.1. Resource Utilization

	Device and Demo	
Resource Type	**ICE40 UltraPlus (5K UWG30)**	**Current Demo**
LogicCells	5280	3122
PLBs	660	548
BRAMs	30	21
PLLs	1	1
I2Cs	2	0
SPIs	2	0
SBIOODs	3	0
DSPs	8	6
RGBADRVs	1	0
LEDDAIPs	1	0
LFOSCs	1	0
HFOSCs	1	0
SPRAMs	4	3

© 2016-2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Technical Support Assistance

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

© 2016-2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Revision History

Date	Version	Change Summary
March 2017	1.1	Changed document status from preliminary to final.
		Removed copyright page.
		Added minor editorial changes to the Introduction section.
		Created Demo Setup and placed Requirements, and Jumper Settings as subsections. • Updated Figure 2.1. iCE40 UltraPlus MDP Board Details. • Added minor editorial changes. • Revised note.
		Added note to step 1 in the Programming the Bitmaps to the MDP Board section.
		Revised step 3 in the Running the Demo section procedure.
December 2016	1.0	Initial release.

© 2016-2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7th Floor, 111 SW 5th Avenue
Portland, OR 97204, USA
T 503.268.8000
www.latticesemi.com