Timing Analysis

(selected problems from Harris&Harris)

1. Ben Bitdiddle has designed the circuit in Figure 2 to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps.

   a. If there is no clock skew, what is the maximum operating frequency of the circuit?

   b. How much clock skew can the circuit tolerate if it must operate at 2 GHz?

   c. How much clock skew can the circuit tolerate before it might experience a hold time Violation?

   d. Alyssa P. Hacker points out that she can redesign the combinational logic between the registers to be faster and tolerate more clock skew. Her improved circuit also uses three two-input XORs, but they are arranged differently. What is her circuit? What is its maximum frequency if there is no clock skew? How much clock skew can the circuit tolerate before it might experience a hold time violation?

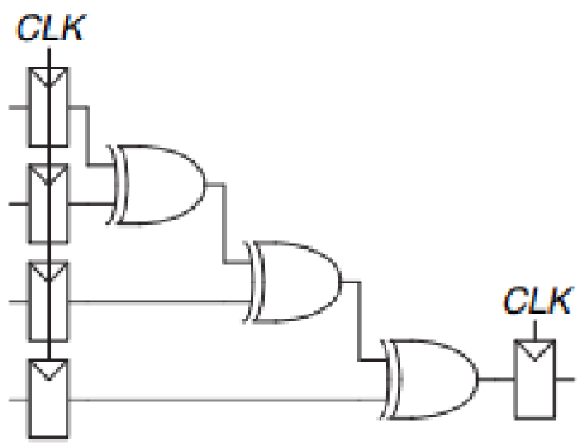

Figure 1: registered four-input XOR circuit

2. You would like to build a synchronizer that can receive asynchronous inputs with an MTBF of 50 years. Your system is running at 1 GHz, and you use sampling flip-flops with τ = 100 ps, T_0 = 110 ps, and t_{setup} = 70 ps. The synchronizer receives a new asynchronous input on average 0.5 times per second (i.e., once every 2 seconds). What is the required probability of failure to satisfy this MTBF? How many clock cycles would you have to wait before reading the sampled input signal to give that probability of error?

3. You are walking down the hallway when you run into your lab partner walking in the other direction. The two of you first step one way and are still in each other's way. Then you both step the other way and are still in each other's way. Then you both wait a bit, hoping the other person will step aside. You can model this situation as a metastable point and apply the same theory that has been applied to synchronizers and flip-flops. Suppose you create a mathematical model for yourself and your lab partner. You start the unfortunate encounter in the metastable state. The probability that you remain in this state after t seconds is $e^{-t/\tau}$: τ indicates your response rate; today, your brain has been blurred by lack of sleep and has $\tau = 20$ seconds.

> (a) How long will it be until you have 99% certainty that you will have resolved from metastability (i.e., figured out how to pass one another)?
>
> (b) You are not only sleepy, but also ravenously hungry. In fact, you will starve to death if you don't get going to the cafeteria within 3 minutes. What is the probability that your lab partner will have to drag you to the morgue?

4. Ben Bitdiddle invents a new and improved synchronizer in Figure 3 that he claims eliminates metastability in a single cycle. He explains that the circuit in box M is an analog "metastability detector" that produces a HIGH output if the input voltage is in the forbidden zone between VIL and VIH. The metastability detector checks to determine whether the first flip-flop has produced a metastable output on D2. If so, it asynchronously resets the flip-flop to produce a good 0 at D2. The second flip-flop then samples D2, always producing a valid logic level on Q. Alyssa P. Hacker tells Ben that there must be a bug in the circuit, because eliminating metastability is just as impossible as building a perpetual motion machine. Who is right? Explain, showing Ben's error or showing why Alyssa is wrong.

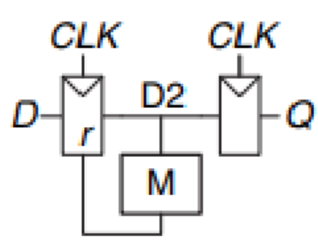

Figure 2: Ben Bitdiddle's synchronizer

Deliverables:

- Work and answers to each of the problems typed or neatly handwritten, included in a pdf submission.