

处理器设计实训-Lab2

学校：电子科技大学

姓名：代子祥

学号：2023090909008

测试截图

```
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ls
Makefile      config-generator.mak  config.log    log      obj      output      run.py
Makefile_run  config-software.mak  configure.sh  log_script  obj_dir  qemu_system_run.sh
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ./configure.sh --run func/func_lab9
Software func/func_lab9 unavailable!
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ./configure.sh --run func/func_lab9
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ./configure.sh --run func/func_lab9
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ make
CHIPLAB_HOME=/home/suhoisy/chiplab
ln -sf ../../chip/config-generator.mak .
echo func/func_lab9
func/func_lab9
echo func/func_lab9
func/func_lab9
make -j8 verilator
make[1]: Entering directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
=====
=====COMPILE verilog...
=====
=====
mkdir -p log
mkdir -p ./obj_dir
verilator -y /home/suhoisy/chiplab/IP/myCPU -y /home/suhoisy/chiplab/IP/CONFREG -y /home/suhoisy/chiplab/IP/AXI_DELAY_RAND -y /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE -y /home/suhoisy/chiplab/IP/AMBA -y /home/suhoisy/chiplab/IP/APB_DEV -y /home/suhoisy/chiplab/IP/APB_DEV/URT -y /home/suhoisy/chiplab/IP/APB_DEV/NAND -y ../testbench -y /home/suhoisy/chiplab/chip/soc_demo/sim --trace-fst --savable --threads 1 -O3 -Wno-fatal -DSIMU -DSIMULATION=1 -Wall --trace -cc -DDIFFTEST_EN simu_top.v difftest.v /home/suhoisy/chiplab/IP/myCPU/*.v /home/suhoisy/chiplab/IP/CONFREG/confreg_sim.v /home/suhoisy/chiplab/IP/AXI_DELAY_RAND/*.v /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE/*.v /home/suhoisy/chiplab/IP/AMBA/axi2apb.v /home/suhoisy/chiplab/IP/APB_DEV/apb_dev_top_no_nand.v /home/suhoisy/chiplab/IP/APB_DEV/apb_top_no_nand.v /home/suhoisy/chiplab/I
```

```
[NEMU] PC: 0x1c076040 [NEMU]: current mem addr = 0xd8cdb not 4 aligned
[NEMU] PC: 0x1c076090 [NEMU]: current mem addr = 0xda319 not 4 aligned
[NEMU] PC: 0x1c0760ec [NEMU]: current mem addr = 0xd1d2e not 4 aligned
[NEMU] PC: 0x1c07613c [NEMU]: current mem addr = 0xd7b61 not 4 aligned
[NEMU] PC: 0x1c076190 [NEMU]: current mem addr = 0xd1077 not 4 aligned
[NEMU] This is syscall 0x11, end
[src/cpu/cpu-exec.c,338,cpu_exec] nemu: HIT GOOD TRAP at pc = 0x1c000230
[src/cpu/cpu-exec.c,78,monitor_statistic] host time spent = 83285 us
[src/cpu/cpu-exec.c,80,monitor_statistic] total guest instructions = 120515
[src/cpu/cpu-exec.c,81,monitor_statistic] simulation frequency = 1447019 instr/s
END by Syscall
total clock is 1010174
=====
total clock      is 1010174
total instruction      is 120485
instruction per cycle      is 0.119272
simulation time      is 101.263445 s
difftest time      is 2.557205 s
nemu_step time      is 0.119204 s
verilator eval time      is 12.622305 s
=====

Terminated at 2020362 ns.
Test exit.
Reached test end PC.
total time is 101277457 us
make[2]: Leaving directory '/home/suhoisy/chiplab/sims/verilator/run_prog/tmp'
make[1]: Leaving directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$
```

```

suhoisy@Genshin-Impact:~/chiplab$ echo $DISPLAY
:0
suhoisy@Genshin-Impact:~/chiplab$ xeyes
Error: Can't open display: :0
suhoisy@Genshin-Impact:~/chiplab$ xeyes
Error: Can't open display: :0
suhoisy@Genshin-Impact:~/chiplab$ xeyes
Error: Can't open display: :0
suhoisy@Genshin-Impact:~/chiplab$ export DISPLAY=:0
suhoisy@Genshin-Impact:~/chiplab$ echo $DISPLAY
:0
suhoisy@Genshin-Impact:~/chiplab$ export DISPLAY=$(awk '/nameserver/ {print $2}' /etc/resolv.conf):0
suhoisy@Genshin-Impact:~/chiplab$ xeyes
suhoisy@Genshin-Impact:~/chiplab$ cd sims/verilator/run_prog/
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ cd log
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ls
compile.log  func
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ cd func/func_lab9_log/
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log/func/func_lab9_log$ ls
mem_trace.txt simu_trace.fst simu_trace.txt uart_output.txt uart_output.txt.real
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log/func/func_lab9_log$ gtkwave simu_trace.fst
error: XDG_RUNTIME_DIR is invalid or not set in the environment.

GTKWave Analyzer v3.3.116 (w)1999-2023 BSI

FSTLOAD | Processing 20499 facts.
FSTLOAD | Built 11815 signals and 8684 aliases.
FSTLOAD | Building facility hierarchy tree.
FSTLOAD | Sorting facility hierarchy tree.

```

