处理器设计实训-Lab4

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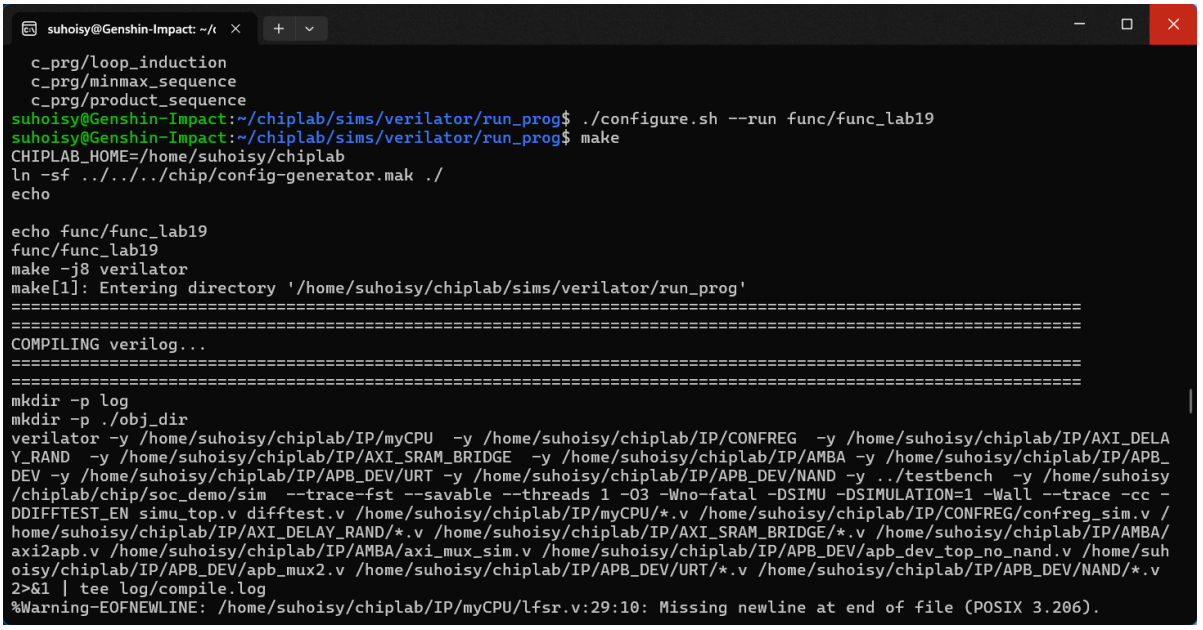
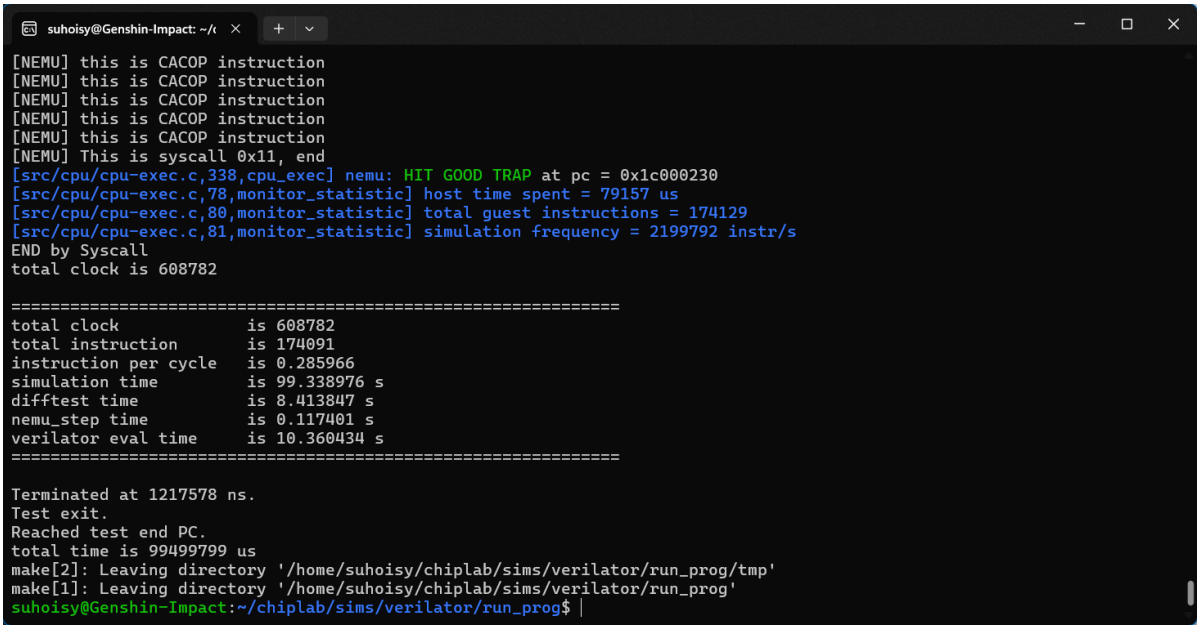
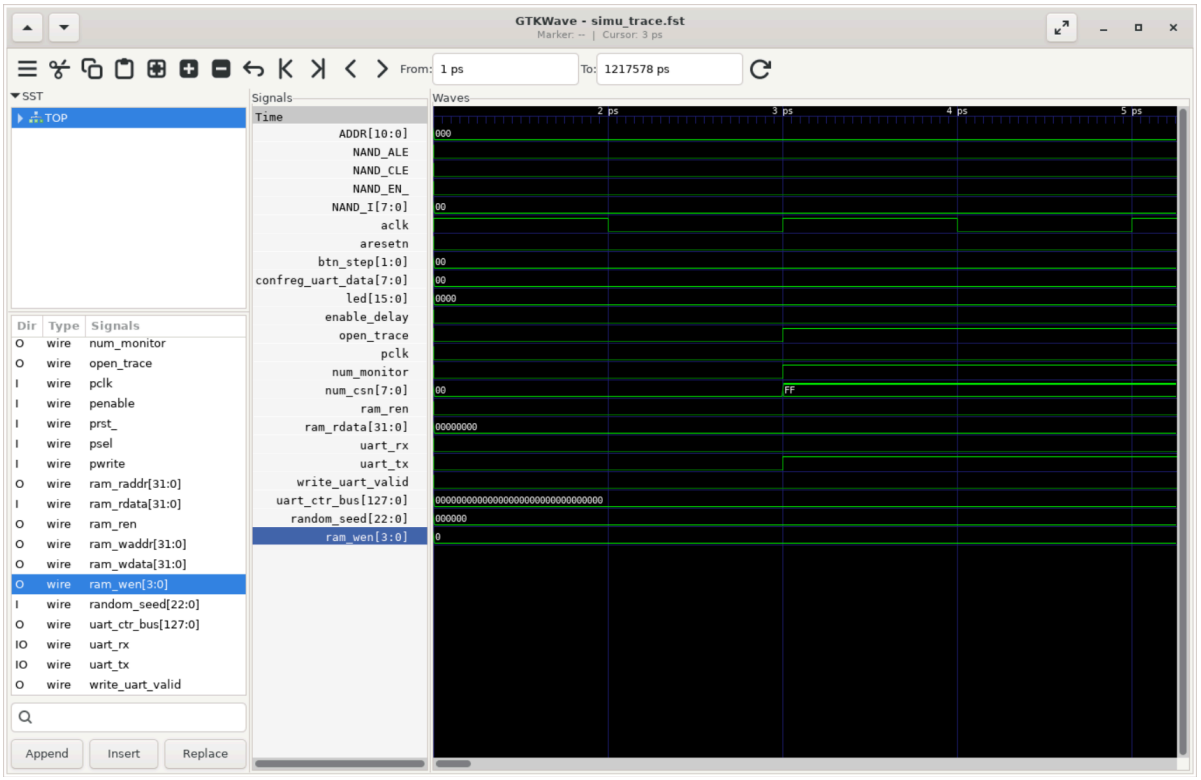
测试截图

func/func_lab19:

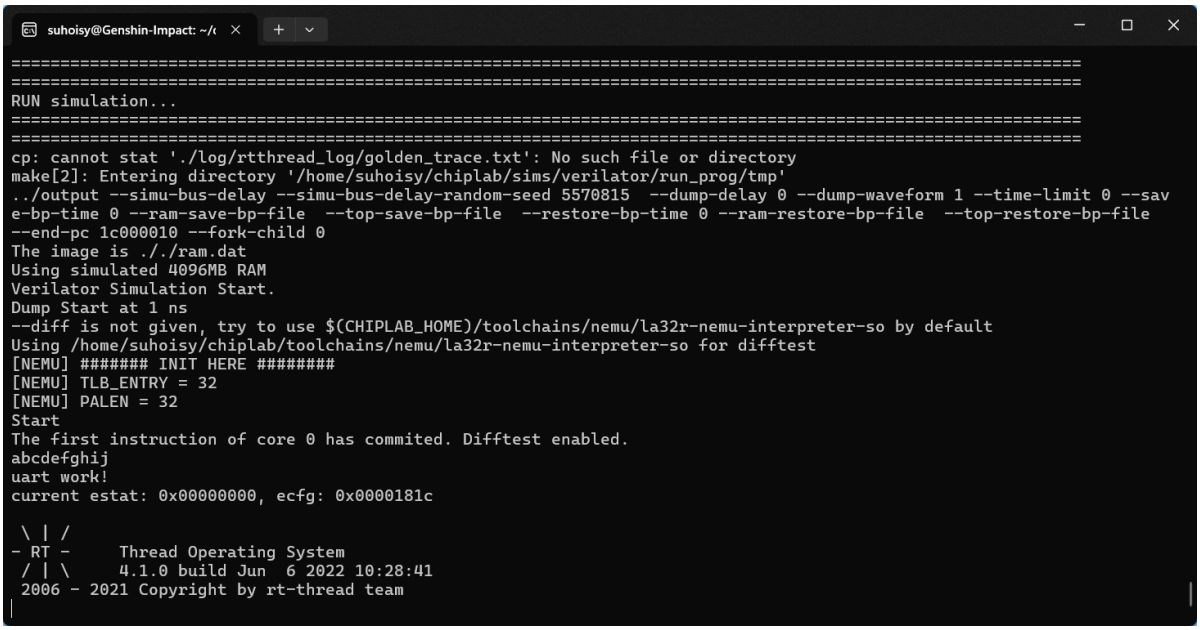




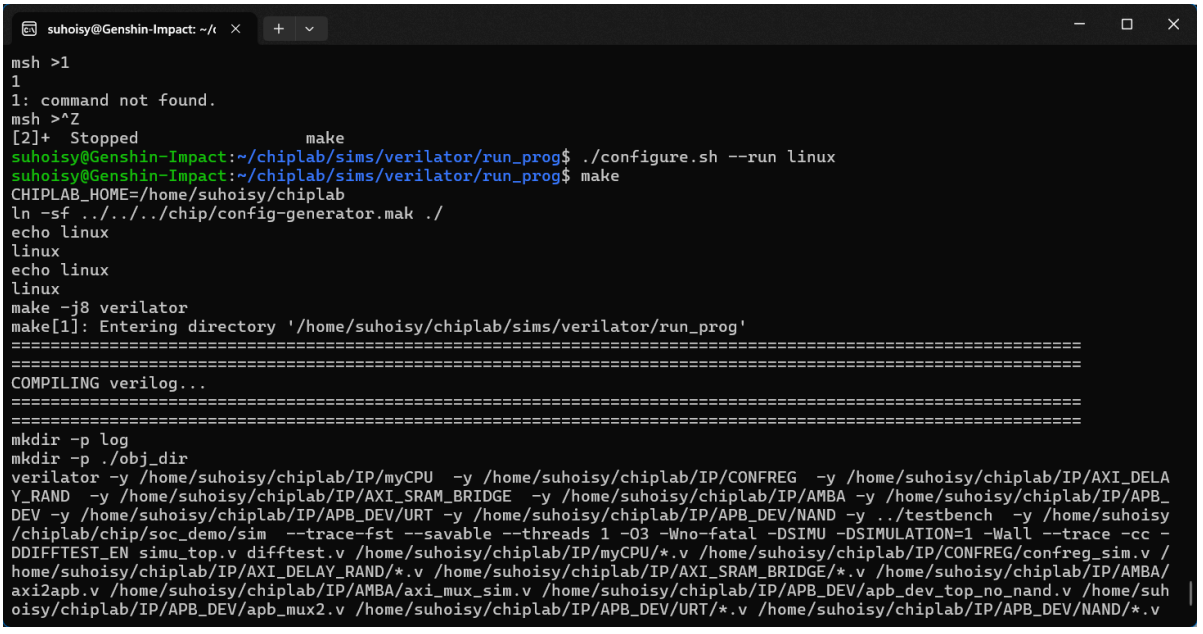


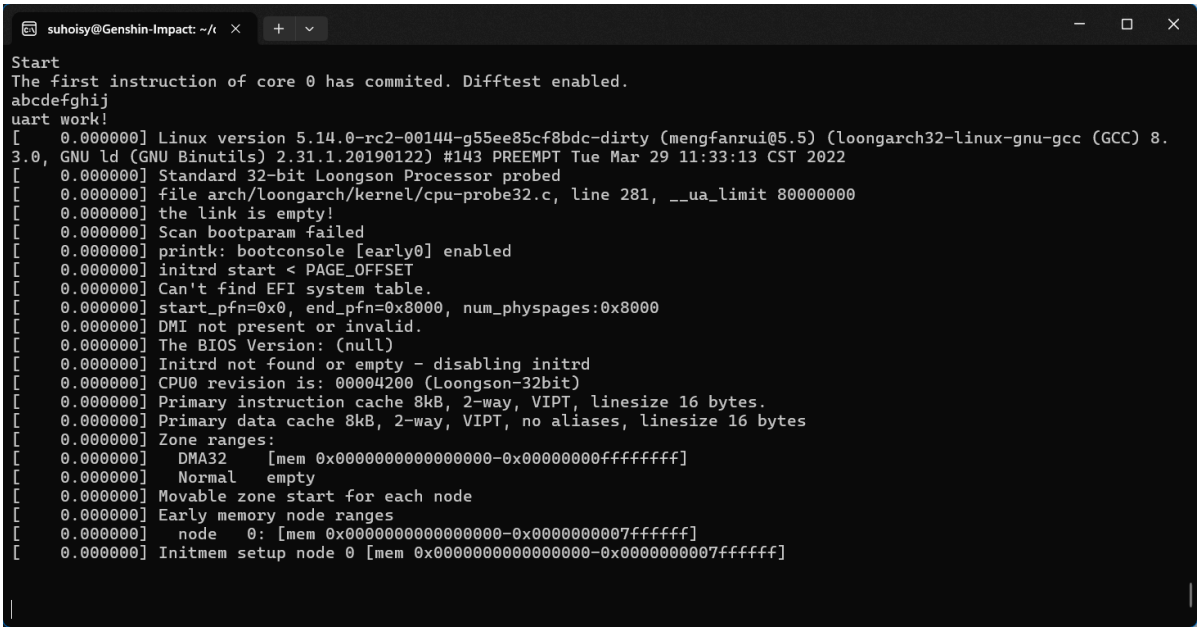
rtthread:

```
FSTLOAD | Building facility hierarchy tree.
FSTLOAD | Sorting facility hierarchy tree.
WM Destroy
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log/func/func_lab19_log$ cd ~/chiplab/sims/verilator/run_prog
/
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ls
Makefile      config-generator.mak  config.log    log         obj      output             run.py
Makefile_run  config-software.mak   configure.sh  log_script  obj_dir  qemu_system_run.sh
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ./configure.sh --run rtthread
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ make
CHIPLAB_HOME=/home/suhoisy/chiplab
ln -sf ../../../chip/config-generator.mak ./
echo rtthread
rtthread
echo rtthread
rtthread
make -j8 verilator
make[1]: Entering directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
==========================================================================================================
==========================================================================================================
COMPILING verilog...
==========================================================================================================
==========================================================================================================
mkdir -p log
mkdir -p ./obj_dir
verilator -y /home/suhoisy/chiplab/IP/myCPU  -y /home/suhoisy/chiplab/IP/CONFREG  -y /home/suhoisy/chiplab/IP/AXI_DELA
Y_RAND  -y /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE  -y /home/suhoisy/chiplab/IP/AMBA -y /home/suhoisy/chiplab/IP/APB_
DEV -y /home/suhoisy/chiplab/IP/APB_DEV/URT -y /home/suhoisy/chiplab/IP/APB_DEV/NAND -y ../testbench  -y /home/suhoisy
/chiplab/chip/soc_demo/sim  --trace-fst --savable --threads 1 -O3 -Wno-fatal -DSIMU -DSIMULATION=1 -Wall --trace -cc -
DDIFFTEST_EN simu_top.v difftest.v /home/suhoisy/chiplab/IP/myCPU/*.v /home/suhoisy/chiplab/IP/CONFREG/confreg_sim.v /
```

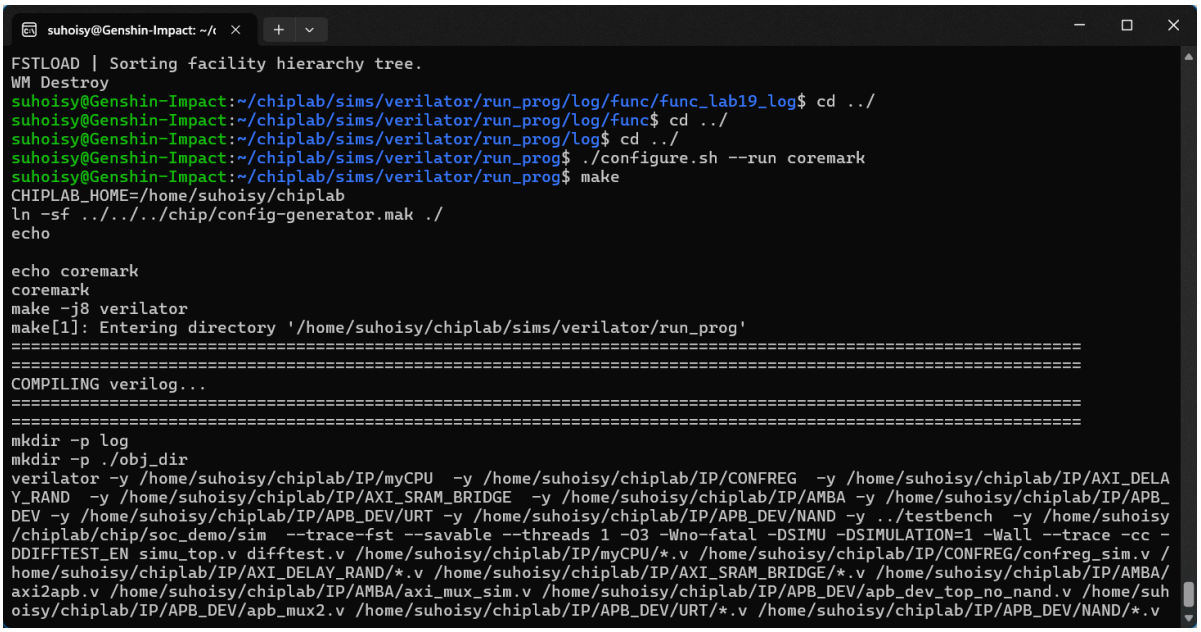

suhoisy@Genshin-Impact: ~/
==========
==========
RUN simulation...
==========
==========
cp: cannot stat './log/rtthread_log/golden_trace.txt': No such file or directory
make[2]: Entering directory '/home/suhoisy/chiplab/sims/verilator/run_prog/tmp'
../output --simu-bus-delay --simu-bus-delay-random-seed 5570815 --dump-delay 0 --dump-waveform 1 --time-limit 0 --save-bp-time 0 --ram-save-bp-file --top-save-bp-file --restore-bp-time 0 --ram-restore-bp-file --top-restore-bp-file --end-pc 1c000010 --fork-child 0
The image is ././ram.dat
Using simulated 4096MB RAM
Verilator Simulation Start.
Dump Start at 1 ns
--diff is not given, try to use $(CHIPLAB_HOME)/toolchains/nemu/la32r-nemu-interpreter-so by default
Using /home/suhoisy/chiplab/toolchains/nemu/la32r-nemu-interpreter-so for difftest
[NEMU] ####### INIT HERE ########
[NEMU] TLB_ENTRY = 32
[NEMU] PALEN = 32
Start
The first instruction of core 0 has commited. Difftest enabled.
abcdefghij
uart work!
current estat: 0x00000000, ecfg: 0x0000181c
\ | /
- RT - Thread Operating System
/ | \ 4.1.0 build Jun 6 2022 10:28:41
2006 - 2021 Copyright by rt-thread team

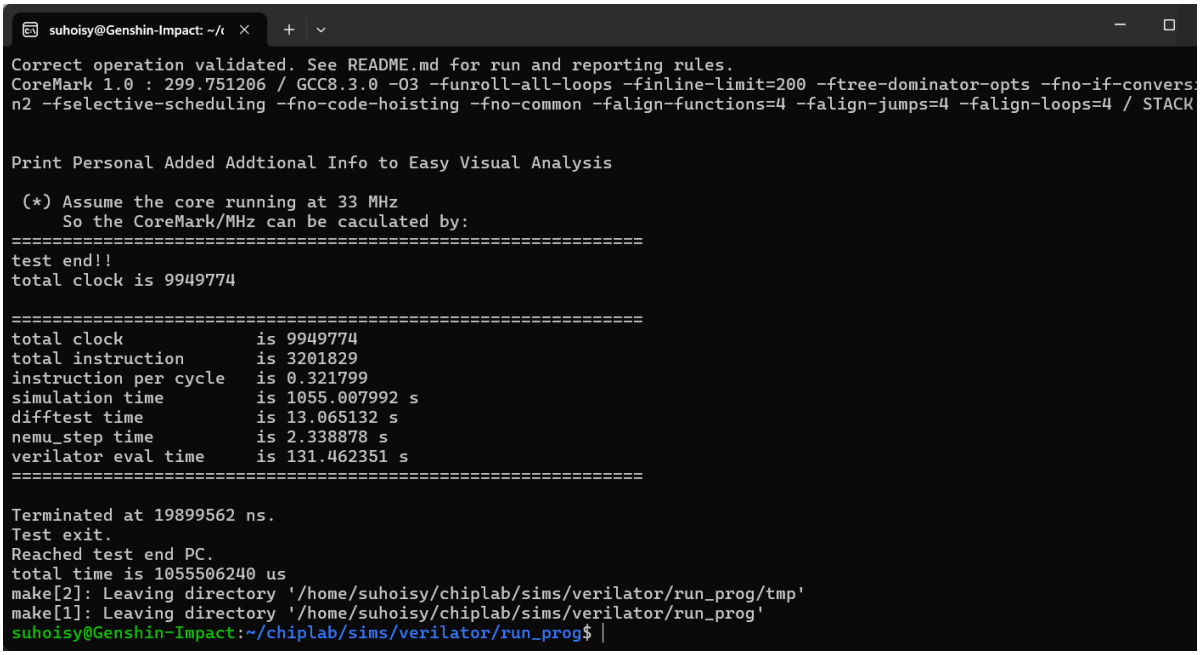
linux:

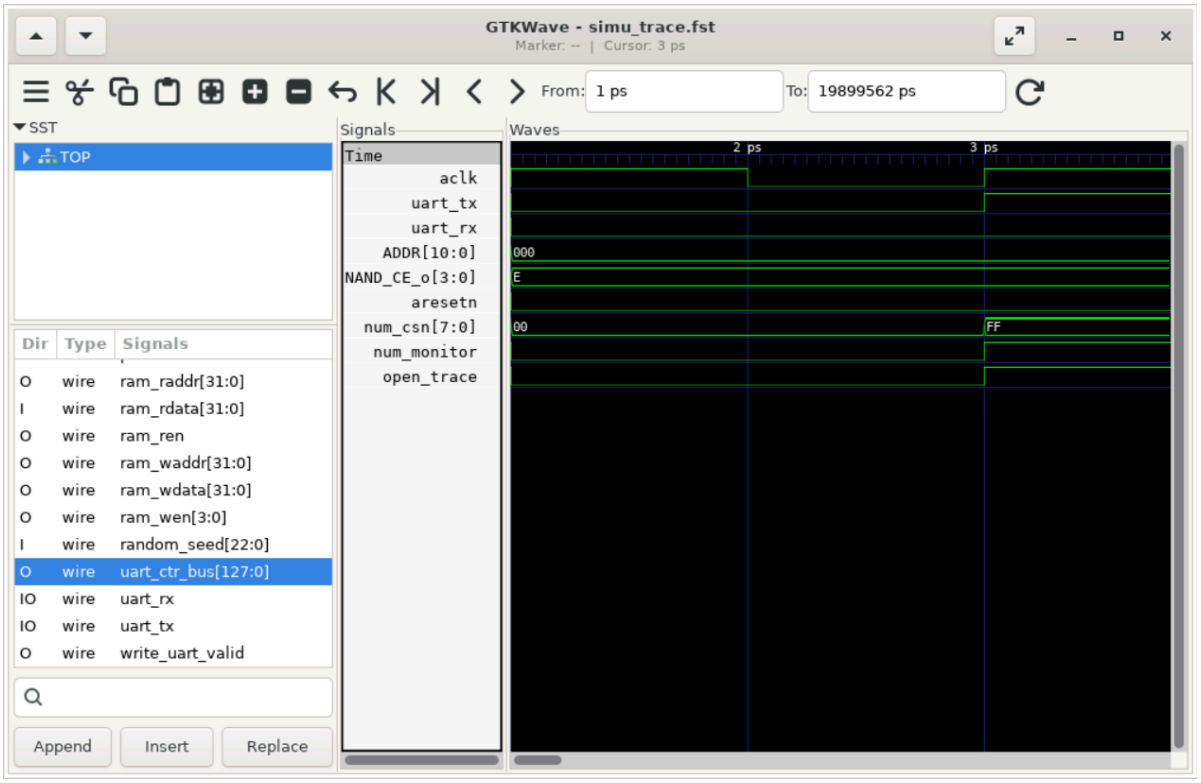

suhoisy@Genshin-Impact: ~/
msh >1
1
1: command not found.
msh >^Z
[2]+ Stopped make
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ./configure.sh --run linux
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ make
CHIPLAB_HOME=/home/suhoisy/chiplab
ln -sf ../../../chip/config-generator.mak ./
echo linux
linux
echo linux
linux
make -j8 verilator
make[1]: Entering directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
==========
==========
COMPILING verilog...
==========
==========
mkdir -p log
mkdir -p ./obj_dir
verilator -y /home/suhoisy/chiplab/IP/myCPU -y /home/suhoisy/chiplab/IP/CONFREG -y /home/suhoisy/chiplab/IP/AXI_DELAY_RAND -y /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE -y /home/suhoisy/chiplab/IP/AMBA -y /home/suhoisy/chiplab/IP/APB_DEV -y /home/suhoisy/chiplab/IP/APB_DEV/URT -y /home/suhoisy/chiplab/IP/APB_DEV/NAND -y ../testbench -y /home/suhoisy/chiplab/chip/soc_demo/sim --trace-fst --savable --threads 1 -O3 -Wno-fatal -DSIMU -DSIMULATION=1 -Wall --trace -cc -DDIFFTEST_EN simu_top.v difftest.v /home/suhoisy/chiplab/IP/myCPU/*.v /home/suhoisy/chiplab/IP/CONFREG/confreg_sim.v /home/suhoisy/chiplab/IP/AXI_DELAY_RAND/*.v /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE/*.v /home/suhoisy/chiplab/IP/AMBA/axi2apb.v /home/suhoisy/chiplab/IP/AMBA/axi_mux_sim.v /home/suhoisy/chiplab/IP/APB_DEV/apb_dev_top_no_nand.v /home/suhoisy/chiplab/IP/APB_DEV/apb_mux2.v /home/suhoisy/chiplab/IP/APB_DEV/URT/*.v /home/suhoisy/chiplab/IP/APB_DEV/NAND/*.v


suhoisy@Genshin-Impact: ~/
Start
The first instruction of core 0 has commited. Difftest enabled.
abcdefghij
uart work!
[0.000000] Linux version 5.14.0-rc2-00144-g55ee85cf8bdc-dirty (mengfanrui@5.5) (loongarch32-linux-gnu-gcc (GCC) 8.3.0, GNU ld (GNU Binutils) 2.31.1.20190122) #143 PREEMPT Tue Mar 29 11:33:13 CST 2022
[0.000000] Standard 32-bit Loongson Processor probed
[0.000000] file arch/loongarch/kernel/cpu-probe32.c, line 281, __ua_limit 80000000
[0.000000] the link is empty!
[0.000000] Scan bootparam failed
[0.000000] printk: bootconsole [early0] enabled
[0.000000] initrd start < PAGE_OFFSET
[0.000000] Can't find EFI system table.
[0.000000] start_pfn=0x0, end_pfn=0x8000, num_physpages:0x8000
[0.000000] DMI not present or invalid.
[0.000000] The BIOS Version: (null)
[0.000000] Initrd not found or empty - disabling initrd
[0.000000] CPU0 revision is: 00004200 (Loongson-32bit)
[0.000000] Primary instruction cache 8kB, 2-way, VIPT, linesize 16 bytes.
[0.000000] Primary data cache 8kB, 2-way, VIPT, no aliases, linesize 16 bytes
[0.000000] Zone ranges:
[0.000000] DMA32 [mem 0x0000000000000000-0x00000000ffffffff]
[0.000000] Normal empty
[0.000000] Movable zone start for each node
[0.000000] Early memory node ranges
[0.000000] node 0: [mem 0x0000000000000000-0x0000000007ffffff]
[0.000000] Initmem setup node 0 [mem 0x0000000000000000-0x0000000007ffffff]

coremark:


suhoisy@Genshin-Impact: ~/
FSTLOAD | Sorting facility hierarchy tree.
WM Destroy
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log/func/func_lab19_log$ cd ../
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log/func$ cd ../
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log$ cd ../
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ./configure.sh --run coremark
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ make
CHIPLAB_HOME=/home/suhoisy/chiplab
ln -sf ../../../chip/config-generator.mak ./
echo
echo coremark
coremark
make -j8 verilator
make[1]: Entering directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
COMPILING verilog...
mkdir -p log
mkdir -p ./obj_dir
verilator -y /home/suhoisy/chiplab/IP/myCPU -y /home/suhoisy/chiplab/IP/CONFREG -y /home/suhoisy/chiplab/IP/AXI_DELAY_RAND -y /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE -y /home/suhoisy/chiplab/IP/AMBA -y /home/suhoisy/chiplab/IP/APB_DEV -y /home/suhoisy/chiplab/IP/APB_DEV/URT -y /home/suhoisy/chiplab/IP/APB_DEV/NAND -y ../testbench -y /home/suhoisy/chiplab/chip/soc_demo/sim --trace-fst --savable --threads 1 -O3 -Wno-fatal -DSIMU -DSIMULATION=1 -Wall --trace -cc -DDIFFTEST_EN simu_top.v difftest.v /home/suhoisy/chiplab/IP/myCPU/*.v /home/suhoisy/chiplab/IP/CONFREG/confreg_sim.v /home/suhoisy/chiplab/IP/AXI_DELAY_RAND/*.v /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE/*.v /home/suhoisy/chiplab/IP/AMBA/axi2apb.v /home/suhoisy/chiplab/IP/AMBA/axi_mux_sim.v /home/suhoisy/chiplab/IP/APB_DEV/apb_dev_top_no_nand.v /home/suhoisy/chiplab/IP/APB_DEV/apb_mux2.v /home/suhoisy/chiplab/IP/APB_DEV/URT/*.v /home/suhoisy/chiplab/IP/APB_DEV/NAND/*.v

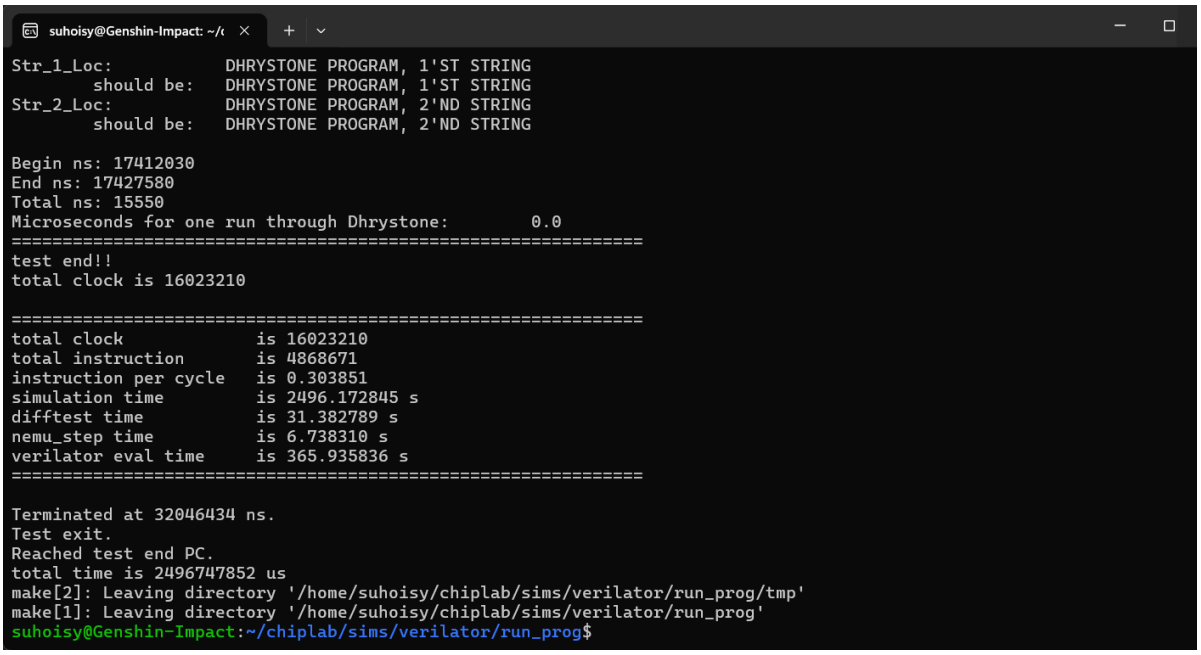

suhoisy@Genshin-Impact: ~/
Correct operation validated. See README.md for run and reporting rules.
CoreMark 1.0 : 299.751206 / GCC8.3.0 -O3 -funroll-all-loops -finline-limit=200 -ftree-dominator-opts -fno-if-conversion2 -fselective-scheduling -fno-code-hoisting -fno-common -falign-functions=4 -falign-jumps=4 -falign-loops=4 / STACK
Print Personal Added Addtional Info to Easy Visual Analysis
(*) Assume the core running at 33 MHz
So the CoreMark/MHz can be caculated by:
test end!!
total clock is 9949774
total clock is 9949774
total instruction is 3201829
instruction per cycle is 0.321799
simulation time is 1055.007992 s
difftest time is 13.065132 s
nemu_step time is 2.338878 s
verilator eval time is 131.462351 s
Terminated at 19899562 ns.
Test exit.
Reached test end PC.
total time is 1055506240 us
make[2]: Leaving directory '/home/suhoisy/chiplab/sims/verilator/run_prog/tmp'
make[1]: Leaving directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$

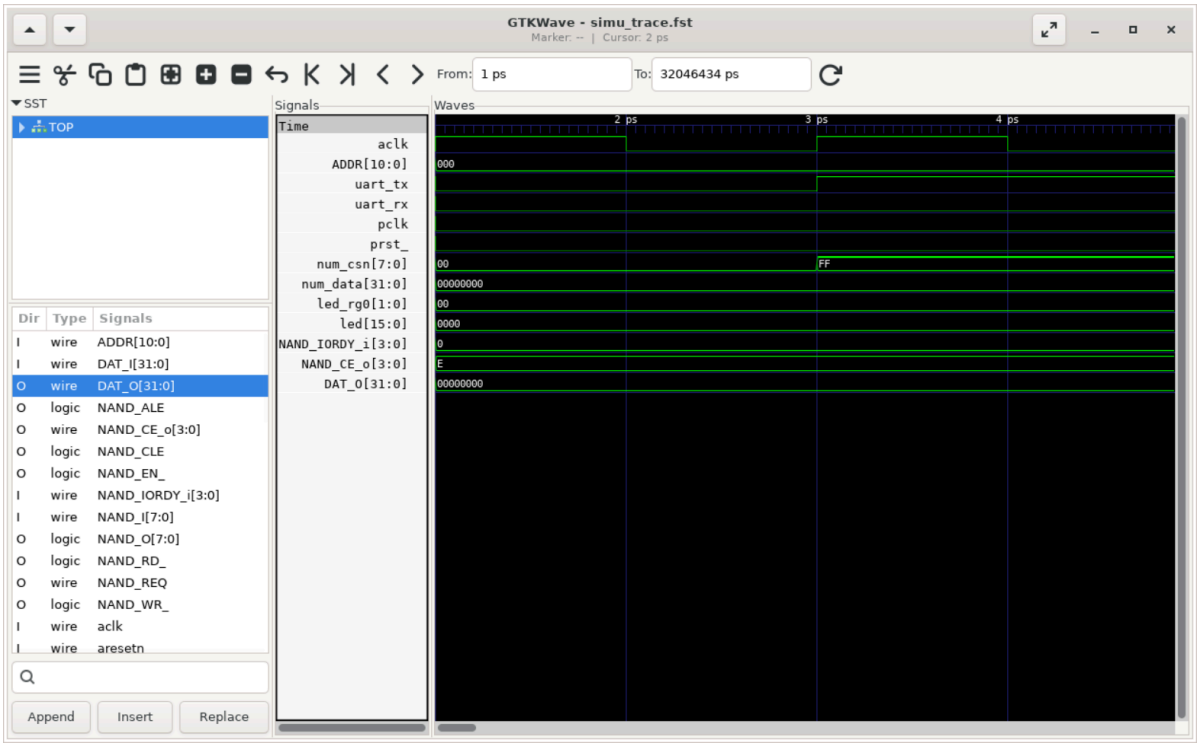


dhrystone:

```
suhoisy@Genshin-Impact: ~/(
  c_prg/inner_product
  c_prg/lookup_table
  c_prg/loop_induction
  c_prg/minmax_sequence
  c_prg/product_sequence
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ./configure.sh --run  dhrystone
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ make
CHIPLAB_HOME=/home/suhoisy/chiplab
ln -sf ../../../chip/config-generator.mak ./
echo

echo dhrystone
dhrystone
make -j8 verilator
make[1]: Entering directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
==========================================================================================================
==========================================================================================================
COMPILING verilog...
==========================================================================================================
==========================================================================================================
mkdir -p log
mkdir -p ./obj_dir
verilator -y /home/suhoisy/chiplab/IP/myCPU  -y /home/suhoisy/chiplab/IP/CONFREG  -y /home/suhoisy/chiplab/IP/AXI_DELA
Y_RAND  -y /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE  -y /home/suhoisy/chiplab/IP/AMBA -y /home/suhoisy/chiplab/IP/APB_
DEV -y /home/suhoisy/chiplab/IP/APB_DEV/URT -y /home/suhoisy/chiplab/IP/APB_DEV/NAND -y ../testbench  -y /home/suhoisy
/chiplab/chip/soc_demo/sim  --trace-fst --savable --threads 1 -O3 -Wno-fatal -DSIMU -DSIMULATION=1 -Wall --trace -cc -
DDIFFTEST_EN simu_top.v difftest.v /home/suhoisy/chiplab/IP/myCPU/*.v /home/suhoisy/chiplab/IP/CONFREG/confreg_sim.v /
home/suhoisy/chiplab/IP/AXI_DELAY_RAND/*.v /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE/*.v /home/suhoisy/chiplab/IP/AMBA/
axi2apb.v /home/suhoisy/chiplab/IP/AMBA/axi_mux_sim.v /home/suhoisy/chiplab/IP/APB_DEV/apb_dev_top_no_nand.v /home/suh
oisy/chiplab/IP/APB_DEV/apb_mux2.v /home/suhoisy/chiplab/IP/APB_DEV/URT/*.v /home/suhoisy/chiplab/IP/APB_DEV/NAND/*.v
```


suhoisy@Genshin-Impact: ~/
Str_1_Loc: DHRYSTONE PROGRAM, 1'ST STRING
should be: DHRYSTONE PROGRAM, 1'ST STRING
Str_2_Loc: DHRYSTONE PROGRAM, 2'ND STRING
should be: DHRYSTONE PROGRAM, 2'ND STRING
Begin ns: 17412030
End ns: 17427580
Total ns: 15550
Microseconds for one run through Dhrystone: 0.0
test end!!
total clock is 16023210
total clock is 16023210
total instruction is 4868671
instruction per cycle is 0.303851
simulation time is 2496.172845 s
difftest time is 31.382789 s
nemu_step time is 6.738310 s
verilator eval time is 365.935836 s
Terminated at 32046434 ns.
Test exit.
Reached test end PC.
total time is 2496747852 us
make[2]: Leaving directory '/home/suhoisy/chiplab/sims/verilator/run_prog/tmp'
make[1]: Leaving directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$


GTKWave - simu_trace.fst
Marker: -- | Cursor: 2 ps
From: 1 ps
To: 32046434 ps
SST
TOP
Dir Type Signals
I wire ADDR[10:0]
I wire DAT_I[31:0]
O wire DAT_O[31:0]
O logic NAND_ALE
O wire NAND_CE_o[3:0]
O logic NAND_CLE
O logic NAND_EN_
I wire NAND_IORDY_i[3:0]
I wire NAND_I[7:0]
O logic NAND_O[7:0]
O logic NAND_RD_
O wire NAND_REQ
O logic NAND_WR_
I wire aclk
I wire aresetn
Append
Insert
Replace
Signals
Time
aclk
ADDR[10:0]
uart_tx
uart_rx
pclk
prst_
num_csn[7:0]
num_data[31:0]
led_rg0[1:0]
led[15:0]
NAND_IORDY_i[3:0]
NAND_CE_o[3:0]
DAT_O[31:0]
Waves
2 ps
3 ps
4 ps
000
00
FF
00000000
00
0000
0
E
00000000