处理器设计实训-Lab1

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测试截图

```
[NEMU] This is syscall 0x11, end
[src/cpu/cpu-exec.c,338,cpu_exec] nemu: HIT GOOD TRAP at pc = 0x1c000230
[src/cpu/cpu-exec.c,78,monitor_statistic] host time spent = 44679 us
[src/cpu/cpu-exec.c,80,monitor_statistic] total guest instructions = 107612
[src/cpu/cpu-exec.c,81,monitor_statistic] simulation frequency = 2408558 instr/s
warning: ecode error, dut = 0, ref = b0000
    era different at pc = 0x1c000230, right= 0x1c000230, wrong = 0x00000000
END by Syscall
total clock is 903729

============================================================
total clock             is 903729
total instruction       is 107612
instruction per cycle   is 0.119076
simulation time         is 59.102313 s
difftest time           is 1.279522 s
nemu_step time          is 0.066685 s
verilator eval time     is 6.854739 s
============================================================

Terminated at 1807472 ns.
Test exit.
Reached test end PC.
Both Error(Code:0x4700)
total time is 59355757 us
make[1]: Leaving directory '/home/suhoisy/chiplab/sims/verilator/run_prog/tmp'
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ls
Makefile      config-generator.mak  config.log    log         obj      output              run.py
Makefile_run  config-software.mak   configure.sh  log_script  obj_dir  qemu_system_run.sh
```

```
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log/func/func_lab7_log$ gtkwave simu_trace.fst
error: XDG_RUNTIME_DIR is invalid or not set in the environment.

GTKWave Analyzer v3.3.116 (w)1999-2023 BSI

FSTLOAD | Processing 20637 facs.
FSTLOAD | Built 11884 signals and 8753 aliases.
FSTLOAD | Building facility hierarchy tree.
FSTLOAD | Sorting facility hierarchy tree.
```