处理器设计实训-Lab2

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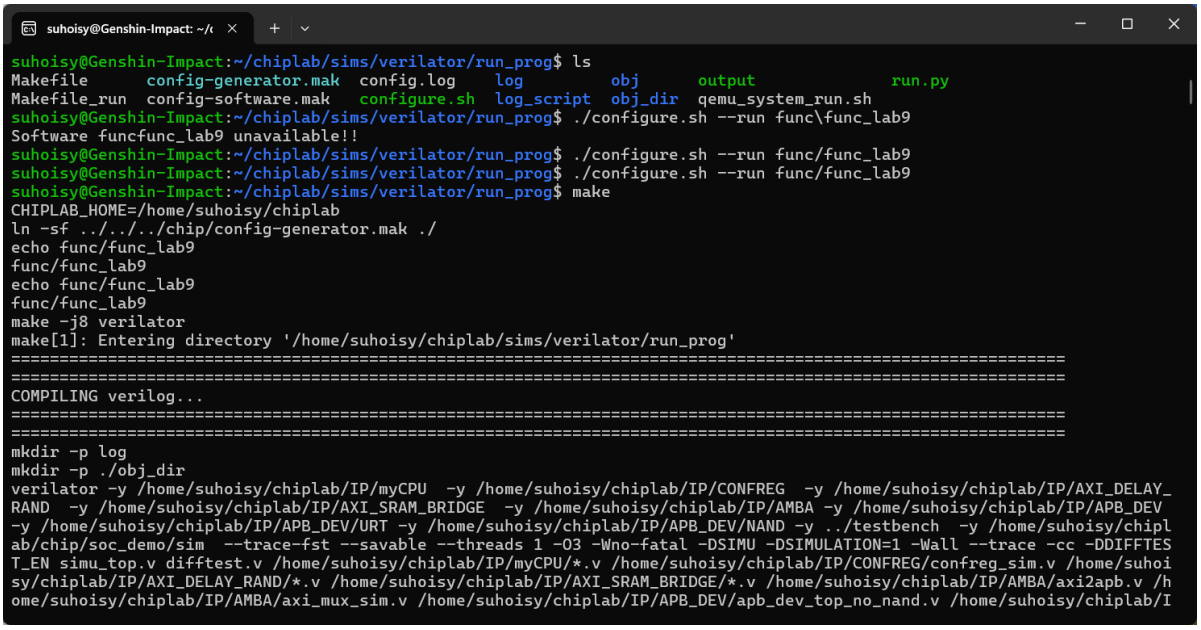
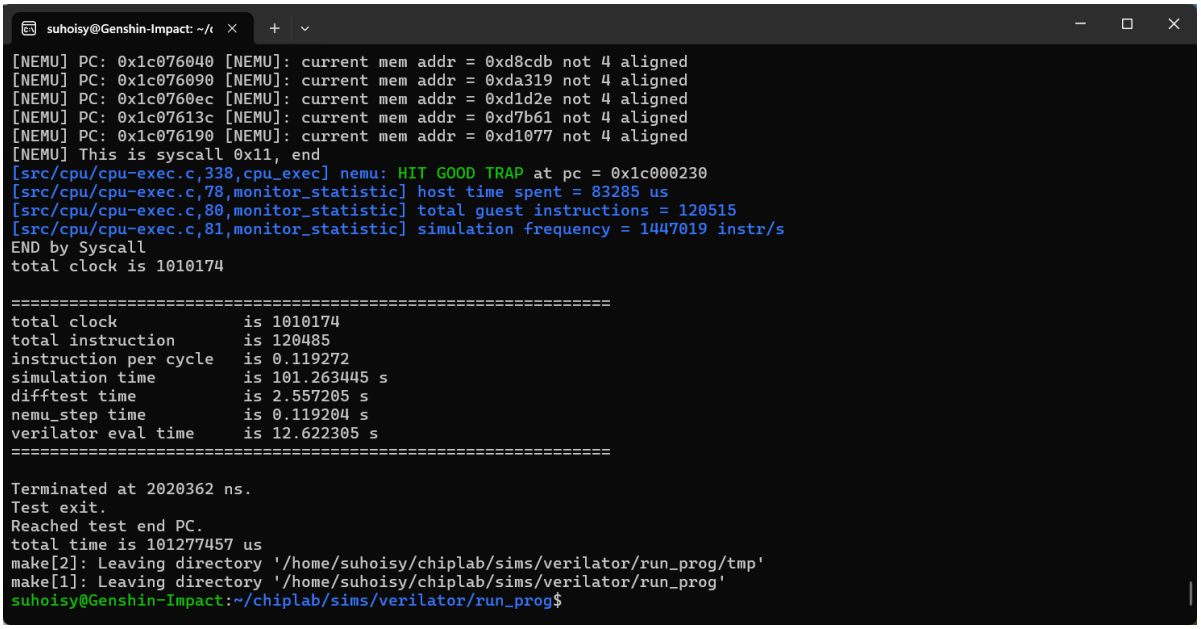
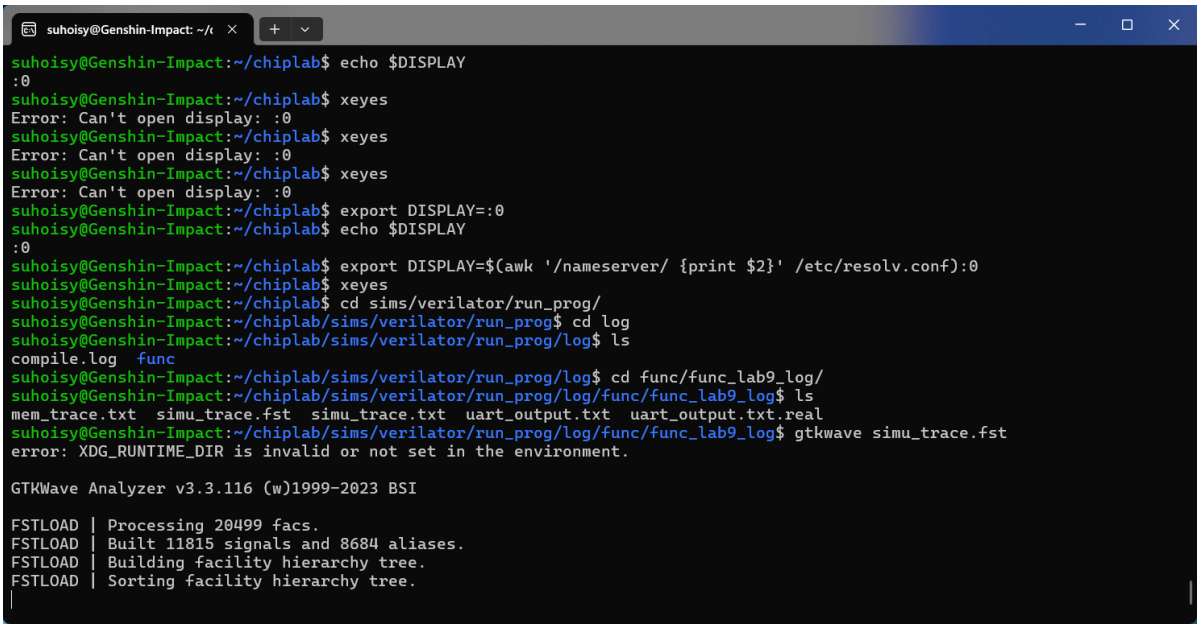
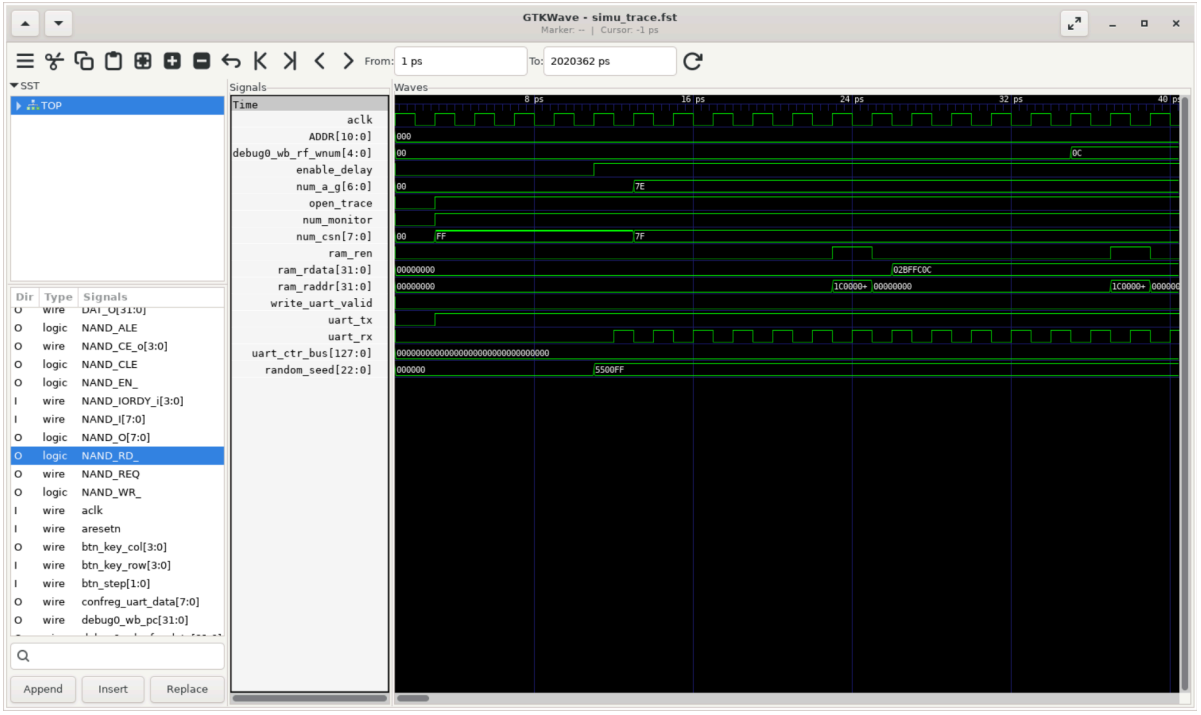
测试截图






suhoisy@Genshin-Impact: ~/c
suhoisy@Genshin-Impact:~/chiplab$ echo $DISPLAY
:0
suhoisy@Genshin-Impact:~/chiplab$ xeyes
Error: Can't open display: :0
suhoisy@Genshin-Impact:~/chiplab$ xeyes
Error: Can't open display: :0
suhoisy@Genshin-Impact:~/chiplab$ xeyes
Error: Can't open display: :0
suhoisy@Genshin-Impact:~/chiplab$ export DISPLAY=:0
suhoisy@Genshin-Impact:~/chiplab$ echo $DISPLAY
:0
suhoisy@Genshin-Impact:~/chiplab$ export DISPLAY=$(awk '/nameserver/ {print $2}' /etc/resolv.conf):0
suhoisy@Genshin-Impact:~/chiplab$ xeyes
suhoisy@Genshin-Impact:~/chiplab$ cd sims/verilator/run_prog/
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ cd log
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log$ ls
compile.log func
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log$ cd func/func_lab9_log/
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log/func/func_lab9_log$ ls
mem_trace.txt simu_trace.fst simu_trace.txt uart_output.txt uart_output.txt.real
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log/func/func_lab9_log$ gtkwave simu_trace.fst
error: XDG_RUNTIME_DIR is invalid or not set in the environment.
GTKWave Analyzer v3.3.116 (w)1999-2023 BSI
FSTLOAD | Processing 20499 facs.
FSTLOAD | Built 11815 signals and 8684 aliases.
FSTLOAD | Building facility hierarchy tree.
FSTLOAD | Sorting facility hierarchy tree.


GTKWave - simu_trace.fst
From: 1 ps
To: 2020362 ps
SST
TOP
Signals
Time
aclk
ADDR[10:0]
debug0_wb_rf_wnum[4:0]
enable_delay
num_a_g[6:0]
open_trace
num_monitor
num_csn[7:0]
ram_ren
ram_rdata[31:0]
ram_raddr[31:0]
write_uart_valid
uart_tx
uart_rx
uart_ctr_bus[127:0]
random_seed[22:0]
Waves
8 ps
16 ps
24 ps
32 ps
Dir Type Signals
O logic NAND_ALE
O wire NAND_CE_o[3:0]
O logic NAND_CLE
O logic NAND_EN_
I wire NAND_IORDY_i[3:0]
I wire NAND_I[7:0]
O logic NAND_O[7:0]
O logic NAND_RD_
O wire NAND_REQ
O logic NAND_WR_
I wire aclk
I wire aresetn
O wire btn_key_col[3:0]
I wire btn_key_row[3:0]
I wire btn_step[1:0]
O wire confreg_uart_data[7:0]
O wire debug0_wb_pc[31:0]
Append
Insert
Replace