处理器设计实训-Lab3

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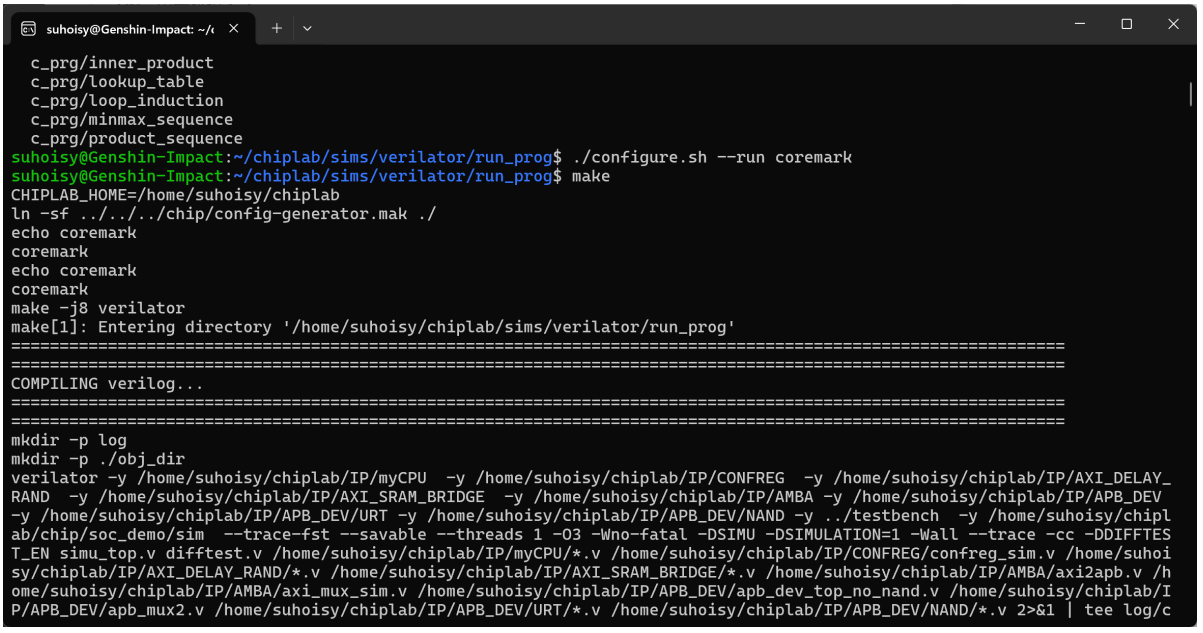
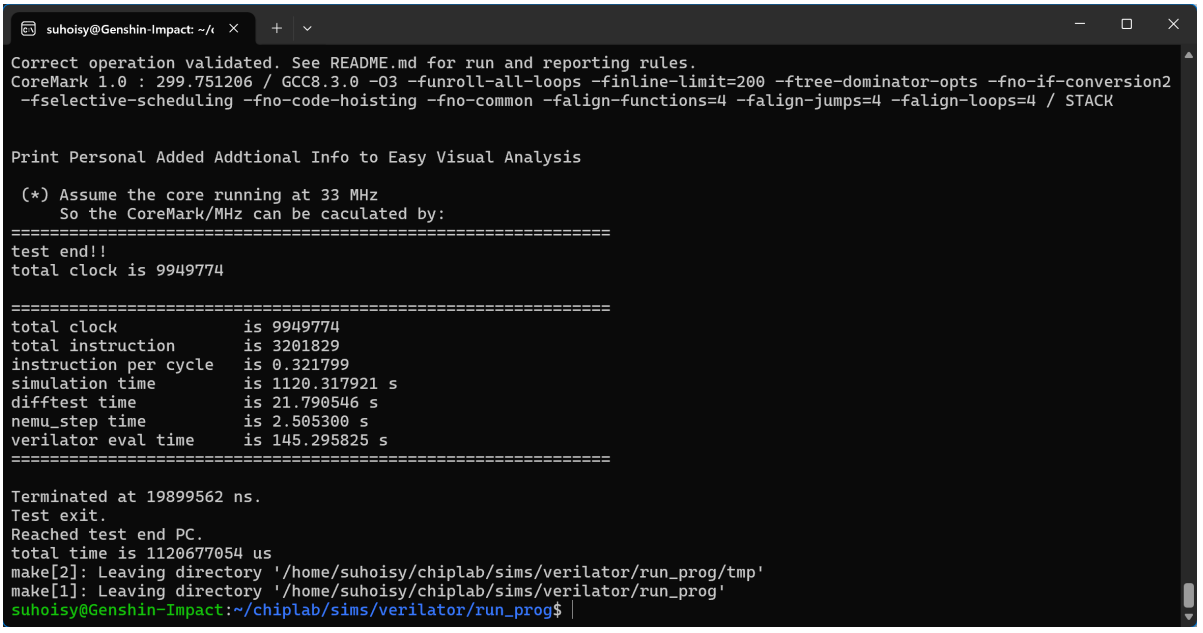
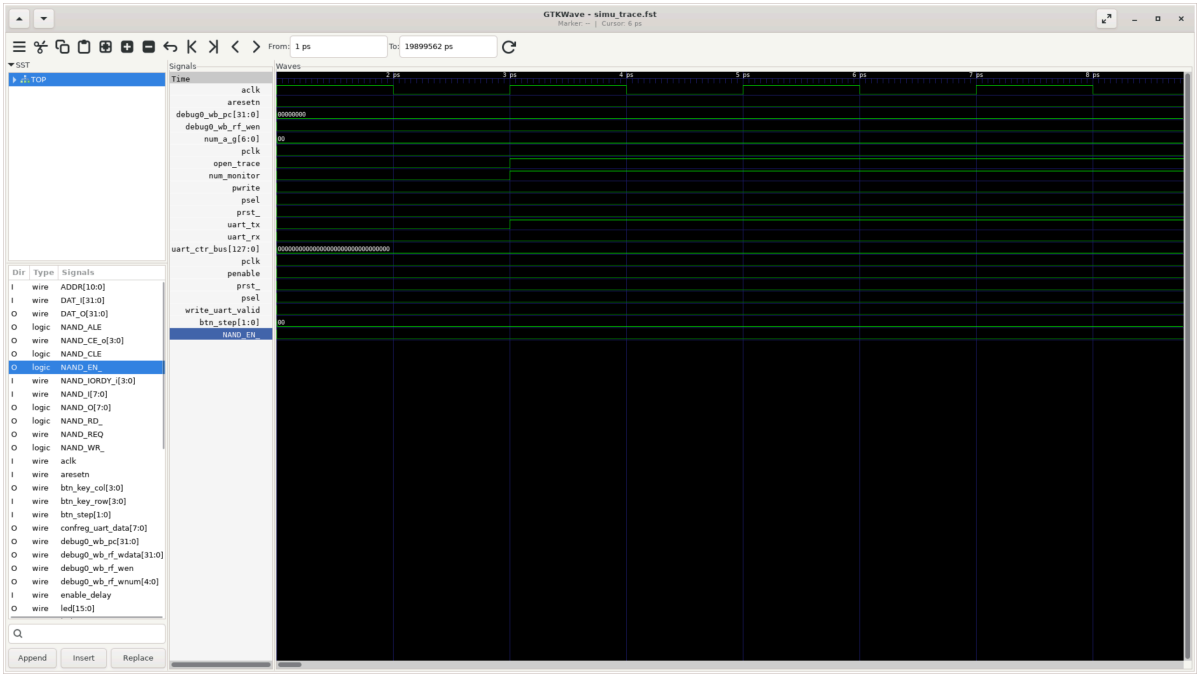
测试截图

coremark：







drystone:

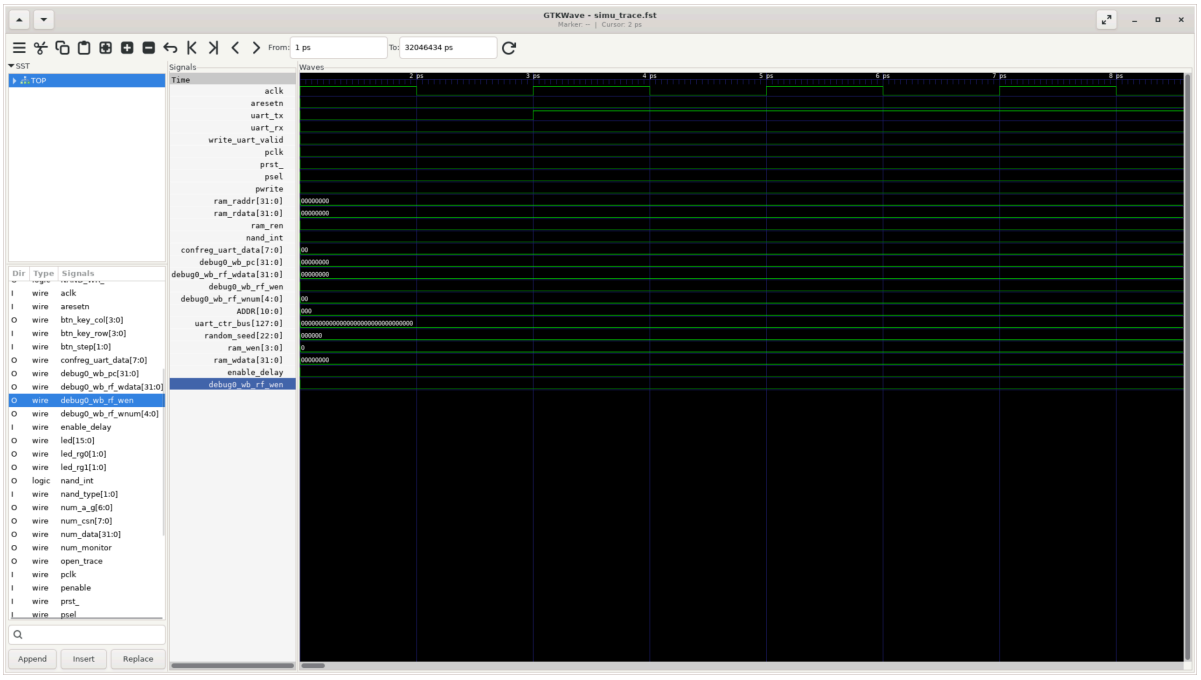
```
suhoisy@Genshin-Impact: ~/(
FSTLOAD | Sorting facility hierarchy tree.
WM Destroy
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log/coremark_log$ cd ../
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log$ cd ../
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ls
Makefile       config-generator.mak  config.log    log         obj      output              run.py
Makefile_run   config-software.mak   configure.sh  log_script  obj_dir  qemu_system_run.sh
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ./configure.sh --run dhrystone
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ make
CHIPLAB_HOME=/home/suhoisy/chiplab
ln -sf ../../../chip/config-generator.mak ./
echo dhrystone
dhrystone
echo dhrystone
dhrystone
make -j8 verilator
make[1]: Entering directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
==========================================================================================================================
==========================================================================================================================
COMPILING verilog...
==========================================================================================================================
==========================================================================================================================
mkdir -p log
mkdir -p ./obj_dir
verilator -y /home/suhoisy/chiplab/IP/myCPU  -y /home/suhoisy/chiplab/IP/CONFREG  -y /home/suhoisy/chiplab/IP/AXI_DELA
Y_RAND  -y /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE  -y /home/suhoisy/chiplab/IP/AMBA -y /home/suhoisy/chiplab/IP/APB_
DEV -y /home/suhoisy/chiplab/IP/APB_DEV/URT -y /home/suhoisy/chiplab/IP/APB_DEV/NAND -y ../testbench  -y /home/suhoisy
/chiplab/chip/soc_demo/sim  --trace-fst --savable --threads 1 -O3 -Wno-fatal -DSIMU -DSIMULATION=1 -Wall --trace -cc -
DDIFFTEST_EN simu_top.v difftest.v /home/suhoisy/chiplab/IP/myCPU/*.v /home/suhoisy/chiplab/IP/CONFREG/confreg_sim.v /
home/suhoisy/chiplab/IP/AXI_DELAY_RAND/*.v /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE/*.v /home/suhoisy/chiplab/IP/AMBA/
```

```
suhoisy@Genshin-Impact: ~/(
Str_2_Loc:           DHRYSTONE PROGRAM, 2'ND STRING
        should be:   DHRYSTONE PROGRAM, 2'ND STRING

Begin ns: 17412030
End ns: 17427580
Total ns: 15550
Microseconds for one run through Dhrystone:        0.0
============================================================
test end!!
total clock is 16023210

============================================================
total clock             is 16023210
total instruction       is 4868671
instruction per cycle   is 0.303851
simulation time         is 1872.746040 s
difftest time           is 24.023407 s
nemu_step time          is 4.684215 s
verilator eval time     is 256.118130 s
============================================================

Terminated at 32046434 ns.
Test exit.
Reached test end PC.
total time is 1873239688 us
make[2]: Leaving directory '/home/suhoisy/chiplab/sims/verilator/run_prog/tmp'
make[1]: Leaving directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ cd log
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log$ ls
compile.log  coremark_log  dhrystone_log  func
```



func/func_lab9:

```
suhoisy@Genshin-Impact: ~/(
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log/dhrystone_log$ cd ../
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog/log$ cd ../
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ ./configure.sh --run func/func_lab9
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$ make
CHIPLAB_HOME=/home/suhoisy/chiplab
ln -sf ../../../chip/config-generator.mak ./
echo

echo func/func_lab9
func/func_lab9
make -j8 verilator
make[1]: Entering directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
============================================================================================================
============================================================================================================
COMPILING verilog...
============================================================================================================
============================================================================================================
mkdir -p log
mkdir -p ./obj_dir
verilator -y /home/suhoisy/chiplab/IP/myCPU  -y /home/suhoisy/chiplab/IP/CONFREG  -y /home/suhoisy/chiplab/IP/AXI_DELA
Y_RAND  -y /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE  -y /home/suhoisy/chiplab/IP/AMBA -y /home/suhoisy/chiplab/IP/APB_
DEV -y /home/suhoisy/chiplab/IP/APB_DEV/URT -y /home/suhoisy/chiplab/IP/APB_DEV/NAND -y ../testbench  -y /home/suhoisy
/chiplab/chip/soc_demo/sim  --trace-fst --savable --threads 1 -O3 -Wno-fatal -DSIMU -DSIMULATION=1 -Wall --trace -cc -
DDIFFTEST_EN simu_top.v difftest.v /home/suhoisy/chiplab/IP/myCPU/*.v /home/suhoisy/chiplab/IP/CONFREG/confreg_sim.v /
home/suhoisy/chiplab/IP/AXI_DELAY_RAND/*.v /home/suhoisy/chiplab/IP/AXI_SRAM_BRIDGE/*.v /home/suhoisy/chiplab/IP/AMBA/
axi2apb.v /home/suhoisy/chiplab/IP/AMBA/axi_mux_sim.v /home/suhoisy/chiplab/IP/APB_DEV/apb_dev_top_no_nand.v /home/suh
oisy/chiplab/IP/APB_DEV/apb_mux2.v /home/suhoisy/chiplab/IP/APB_DEV/URT/*.v /home/suhoisy/chiplab/IP/APB_DEV/NAND/*.v
2>&1 | tee log/compile.log
make -C ./obj_dir -f "Vsimu_top.mk" || exit "$?"
make[2]: Entering directory '/home/suhoisy/chiplab/sims/verilator/run_prog/obj_dir'
```

```
[NEMU] PC: 0x1c076040 [NEMU]: current mem addr = 0xd8cdb not 4 aligned
[NEMU] PC: 0x1c076090 [NEMU]: current mem addr = 0xda319 not 4 aligned
[NEMU] PC: 0x1c0760ec [NEMU]: current mem addr = 0xd1d2e not 4 aligned
[NEMU] PC: 0x1c07613c [NEMU]: current mem addr = 0xd7b61 not 4 aligned
[NEMU] PC: 0x1c076190 [NEMU]: current mem addr = 0xd1077 not 4 aligned
[NEMU] This is syscall 0x11, end
[src/cpu/cpu-exec.c,338,cpu_exec] nemu: HIT GOOD TRAP at pc = 0x1c000230
[src/cpu/cpu-exec.c,78,monitor_statistic] host time spent = 67598 us
[src/cpu/cpu-exec.c,80,monitor_statistic] total guest instructions = 120515
[src/cpu/cpu-exec.c,81,monitor_statistic] simulation frequency = 1782819 instr/s
END by Syscall
total clock is 1010174

============================================================
total clock              is 1010174
total instruction        is 120485
instruction per cycle    is 0.119272
simulation time          is 91.512446 s
difftest time            is 1.874068 s
nemu_step time           is 0.099836 s
verilator eval time      is 11.548940 s
============================================================

Terminated at 2020362 ns.
Test exit.
Reached test end PC.
total time is 91587119 us
make[2]: Leaving directory '/home/suhoisy/chiplab/sims/verilator/run_prog/tmp'
make[1]: Leaving directory '/home/suhoisy/chiplab/sims/verilator/run_prog'
suhoisy@Genshin-Impact:~/chiplab/sims/verilator/run_prog$
```