ASSIGNMENT 2

Digital Design and Computer Organization

UE21CS251A

3rd Semester, Academic Year 2021-22

Date:30/09/2022

Name: SUJAL.S	SRN:PES2UG21CS548	Section I

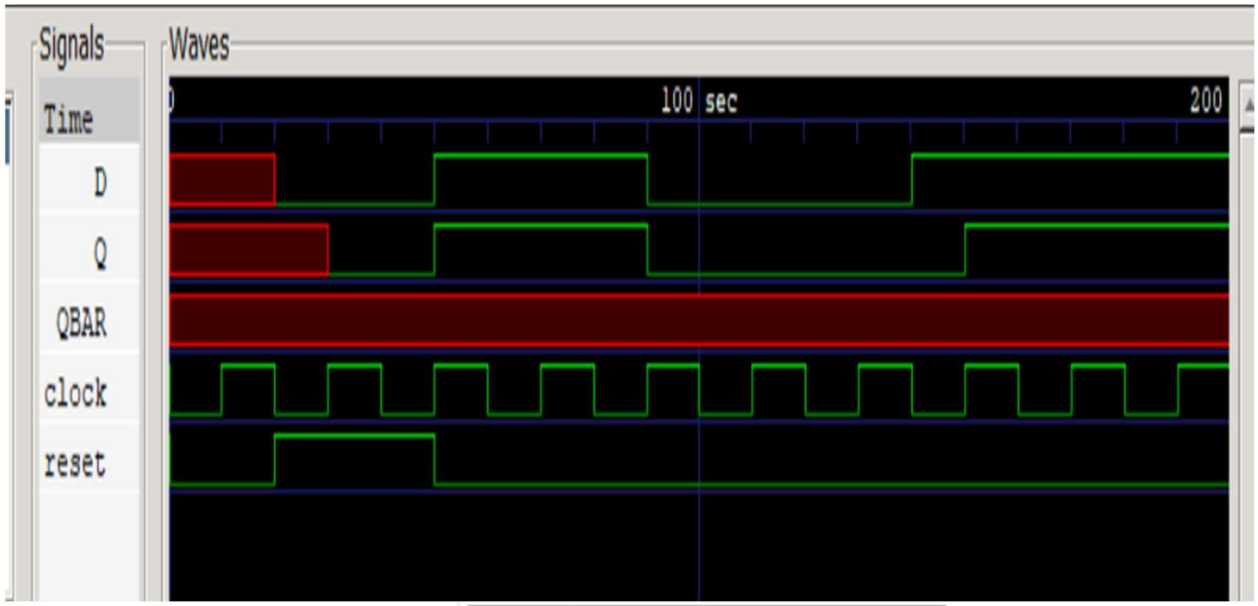
Program Number:____1_____

Title of the Program

AIM: DESIGN A D-FLIPFLOP AND VERIFY ITS TRUTH TABLE

```
module D_FLIPFLOP(d,clock,reset,q,q_comp);

input d, clock, reset;
output reg q, q_comp;

always@(posedge clock)

begin
if(reset == 1)
    q <= 0;
else
    q <= d;
end
endmodule
```

```
C:\iverilog\bin>iverilog.exe -o out DFLIPFLOP.v DFLIPFLOP_TB.v

C:\iverilog\bin>vvp out
VCD info: dumpfile dff.vcd opened for output.
                   0 D=x,clock =0,reset =0,output is Q = x
                  10 D=x,clock =1,reset =0,output is Q = x
                  20 D=0,clock =0,reset =1,output is Q = x
                  30 D=0,clock =1,reset =1,output is Q = 0
                  40 D=0,clock =0,reset =1,output is Q = 0
                  50 D=1,clock =1,reset =0,output is Q = 1
                  60 D=1,clock =0,reset =0,output is Q = 1
```



Clk	Q(t-1)	D	Q(t)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

ASSIGNMENT 2

Digital Design and Computer Organization

UE21CS251A

3rd Semester, Academic Year 2021-22

Date:30/09/2022

Name: SUJAL.S	SRN:PES2UG21CS548	Section I

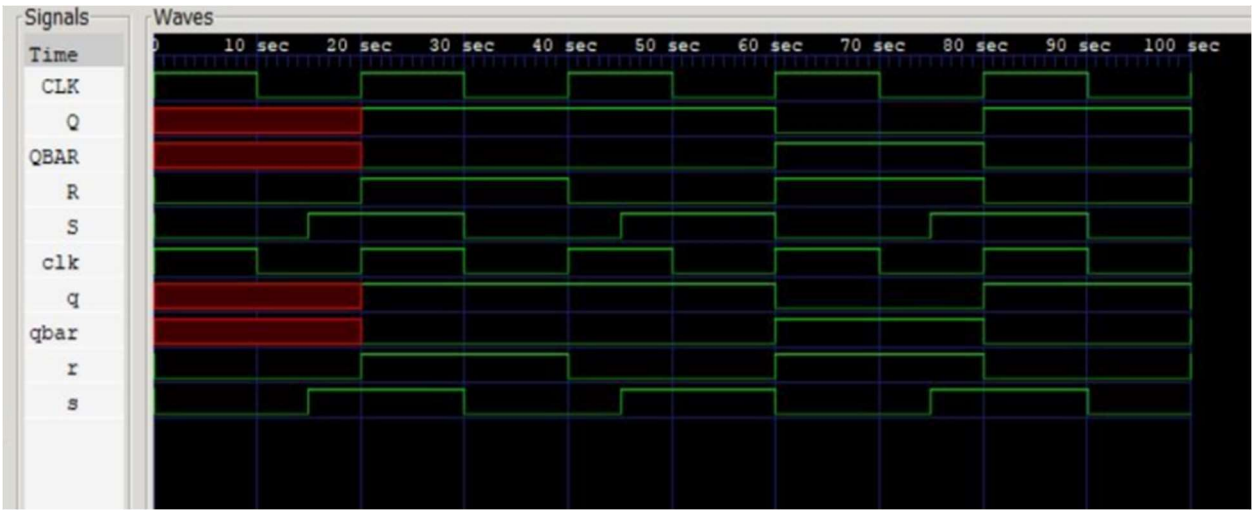
Program Number:____2_____

Title of the Program

AIM: DESIGN SR FLIPFLOP ..

```
module srff_dataflow(q,qbar,s,r,clk);

input s,r,clk;
output q, qbar;

assign q = clk? (s + ((~r) & q)) : q;
assign qbar = ~q;

endmodule
```

```
C:\iverilog\bin>iverilog -o test sr.v sr_tb.v

C:\iverilog\bin>vvp test
VCD info: dumpfile tb_srff1.vcd opened for output.
RSLT    s       r       q       qbar
PASS    0       0       0       1
PASS    0       1       0       1
PASS    1       0       1       0
FAIL    1       1       x       x
```



Inputs		Outputs	
S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	invalid	
1	1	invalid	

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Digital Design and Computer Organization

UE21CS251A

3rd Semester, Academic Year 2021-22

Date:30/09/2022

Name: SUJAL.S	SRN: PES2UG21CS548	Section I

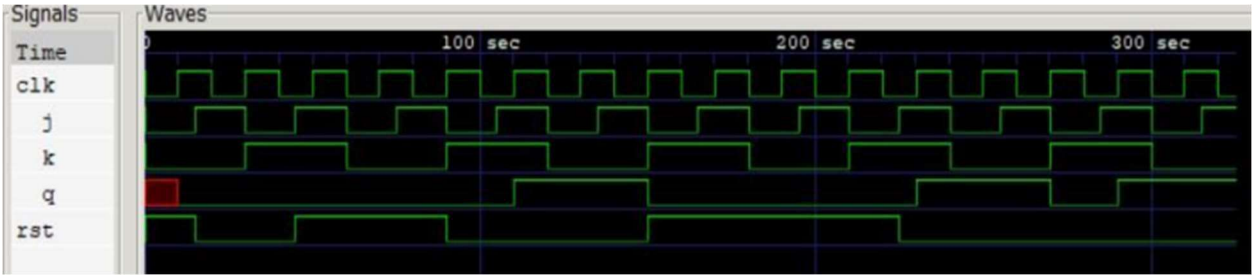
Program Number:____3_____

Title of the Program

AIM: DESIGN A JK FLIPFLOP …

```
module JK_FlipFlop( input j, input k, input clock, output q);

   reg q;

   always @ (posedge clock)
      case ({j,k})
         2'b00 :  q <= q;
         2'b01 :  q <= 0;
         2'b10 :  q <= 1;
         2'b11 :  q <= ~q;
      endcase
endmodule
```

```
C:\iverilog\bin>iverilog -o te jk_ff.v jk_tb.v

C:\iverilog\bin>vvp te
VCD info: dumpfile jkff_test.vcd opened for output.
time =10          INPUT VALUES    J =0 K=0 RST_n =1        OUTPUT VALUES Q =0
time =30          INPUT VALUES    J =0 K=1 RST_n =0        OUTPUT VALUES Q =0
time =50          INPUT VALUES    J =1 K=1 RST_n =1        OUTPUT VALUES Q =0
time =70          INPUT VALUES    J =0 K=0 RST_n =1        OUTPUT VALUES Q =0
time =90          INPUT VALUES    J =0 K=1 RST_n =0        OUTPUT VALUES Q =0
time =110         INPUT VALUES    J =1 K=1 RST_n =0        OUTPUT VALUES Q =1
```



J_n	K_n	Q_n	$\overline{Q_n}$	Q_{n+1}	Action
0	0	0	1	0	$= Q_n =$ No change
0	0	1	0	1	
0	1	0	1	0	$= 0 =$ Reset
0	1	1	0	0	
1	0	0	1	1	$= 1 =$ Set
1	0	1	0	1	
1	1	0	1	1	$= \overline{Q_n} =$ Toggle
1	1	1	0	0	

ASSIGNMENT 1

Digital Design and Computer Organization

UE20CS251A

3rd Semester, Academic Year 2021-22

Date:30/09/2022

Name: SUJAL.S	SRN:PES2UG21CS548	Section I

Program Number:____4_____

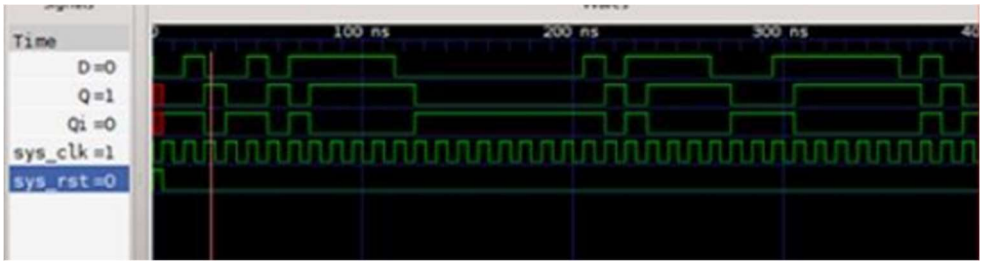
Title of the Program

AIM: DESIGN T-FLIPFLOP ….

Input	Outputs	
	Present State	Next State
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

```
module TFlipFlop(T,Clock,Q,Qbar );

input T,Clock;
output reg Q,Qbar;

always@(T,posedge(Clock))

begin
    if(T==0)
    begin
        Q =1'b1;
        Qbar=1'b0;
    end

else
    begin
        Q =1'b0;
        Qbar=1'b1;
    end

end
endmodule
```

```
VCD info: dumpfile tff_test.vcd opened for output.
time = 10        INPUT VALUES    T = 0 RST_n = 0          OUTPUT VALUES Q = x
time = 30        INPUT VALUES    T = 0 RST_n = 0          OUTPUT VALUES Q = x
time = 50        INPUT VALUES    T = 1 RST_n = 1          OUTPUT VALUES Q = 0
time = 70        INPUT VALUES    T = 0 RST_n = 1          OUTPUT VALUES Q = 0
time = 90        INPUT VALUES    T = 0 RST_n = 0          OUTPUT VALUES Q = 0
time = 110       INPUT VALUES    T = 1 RST_n = 0          OUTPUT VALUES Q = 1
time = 130       INPUT VALUES    T = 0 RST_n = 0          OUTPUT VALUES Q = 1
time = 150       INPUT VALUES    T = 0 RST_n = 1          OUTPUT VALUES Q = 0
time = 170       INPUT VALUES    T = 1 RST_n = 1          OUTPUT VALUES Q = 0
time = 190       INPUT VALUES    T = 0 RST_n = 1          OUTPUT VALUES Q = 0
time = 210       INPUT VALUES    T = 0 RST_n = 1          OUTPUT VALUES Q = 0
time = 230       INPUT VALUES    T = 1 RST_n = 0          OUTPUT VALUES Q = 1
time = 250       INPUT VALUES    T = 0 RST_n = 0          OUTPUT VALUES Q = 1
time = 270       INPUT VALUES    T = 0 RST_n = 0          OUTPUT VALUES Q = 1
time = 290       INPUT VALUES    T = 1 RST_n = 0          OUTPUT VALUES Q = 0
time = 310       INPUT VALUES    T = 0 RST_n = 0          OUTPUT VALUES Q = 0
```



ASSIGNMENT 1

Digital Design and Computer Organization

UE20CS251A

3rd Semester, Academic Year 2021-22

Date:30/09/2022

Name: SUJAL.S	SRN: PES2UG21CS548	Section I

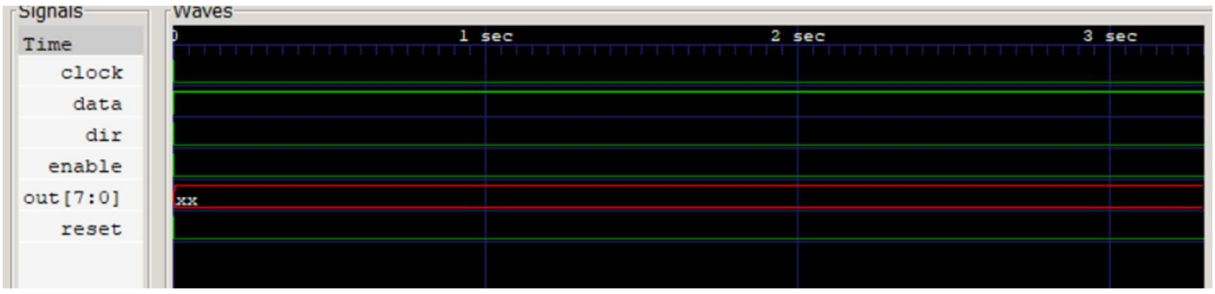
Program Number:____5_____

Title of the Program

AIM: DESIGN 8 Bit SHIFT REGISTER……

```
module shift_register (d,clock,enable,dir,reset,out);

input d,clock,enable,dir,reset;
output reg [7:0] out;

always @ (posedge clock)

if (! reset)
   out <= 0;

else
begin
   if (enable)
      case (dir)

   0: out <={out [6:0],d};
   1: out <={d, out [7:1]};
      endcase

   else
      out <= out;
end
endmodule
```

```
C:\iverilog\bin>iverilog.exe -o out siso.v sisotb.v

C:\iverilog\bin>vvp out
VCD info: dumpfile register.vcd opened for output.
reset = 0 data = 1 enable = 0 dir = 0 out = xxxxxxxx
reset = 0 data = 1 enable = 0 dir = 0 out = 00000000
reset = 1 data = 1 enable = 1 dir = 0 out = 00000000
reset = 1 data = 0 enable = 1 dir = 0 out = 00000001
reset = 1 data = 1 enable = 1 dir = 0 out = 00000010
reset = 1 data = 0 enable = 1 dir = 0 out = 00000101
reset = 1 data = 1 enable = 1 dir = 0 out = 00001010
reset = 1 data = 0 enable = 1 dir = 0 out = 00010101
reset = 1 data = 1 enable = 1 dir = 0 out = 00101010
reset = 1 data = 0 enable = 1 dir = 0 out = 01010101
reset = 1 data = 0 enable = 1 dir = 1 out = 01010101
reset = 1 data = 1 enable = 1 dir = 1 out = 00101010
reset = 1 data = 0 enable = 1 dir = 1 out = 10010101
reset = 1 data = 1 enable = 1 dir = 1 out = 01001010
reset = 1 data = 0 enable = 1 dir = 1 out = 10100101
reset = 1 data = 1 enable = 1 dir = 1 out = 01010010
reset = 1 data = 0 enable = 1 dir = 1 out = 10101001
reset = 1 data = 1 enable = 1 dir = 1 out = 01010100
reset = 1 data = 1 enable = 1 dir = 1 out = 10101010
reset = 1 data = 1 enable = 1 dir = 1 out = 11010101
reset = 1 data = 1 enable = 1 dir = 1 out = 11101010
reset = 1 data = 1 enable = 1 dir = 1 out = 11110101
reset = 1 data = 1 enable = 1 dir = 1 out = 11111010
reset = 1 data = 1 enable = 1 dir = 1 out = 11111101
reset = 1 data = 1 enable = 1 dir = 1 out = 11111110
```



Disclaimer:

- The programs and output submitted is duly written, verified and executed my me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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Section: I
Date: 30/09/2022