Digital Design and Computer Organisation Laboratory

UE20CS256

3rd Semester, Academic Year 2022-23

Date: 18-08-2022

Name: Sujal S	SRN: PES2UG21CS548	Section I

Week#____1_____ Program Number: ____1__

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT OR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE OR GATE TRUTH TABLE

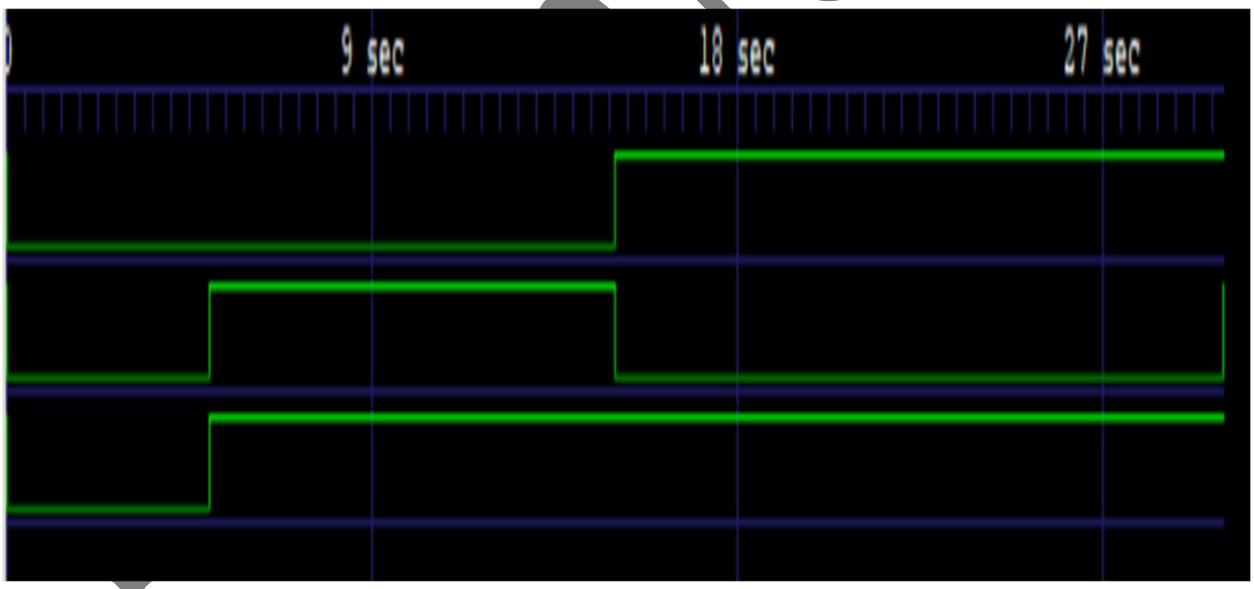
```
module Or(A,B,C);

input A,B;
output C;

assign C = A|B ;
endmodule
```

```
C:\iverilog\bin>iverilog.exe -o ORR or_mine.v and2_tb.v

C:\iverilog\bin>vvp ORR
VCD info: dumpfile OR_test.vcd opened for output.
                  0a=0, b=0, c=0
                  5a=0, b=1, c=1
                 15a=1, b=0, c=1
                 30a=1, b=1, c=1
```



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Date: 18-08-2022

Name: Sujal S	SRN: PES2UG21CS548	Section I

Week#____1_____ Program Number: ____2___

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A NOT GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOT GATE TRUTH TABLE

```
module Not( c,a );
input a;
output c;
assign c = ~a;
endmodule
```

```
C:\iverilog\bin>iverilog.exe -o NOTT not_mine.v and2_tb.v

C:\iverilog\bin>vvp NOTT
VCD info: dumpfile NOT_test.vcd opened for output.
                  0a=0, c=1
                 15a=1, c=0
```

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Name: Sujal S	SRN: PES2UG21CS548	Section I

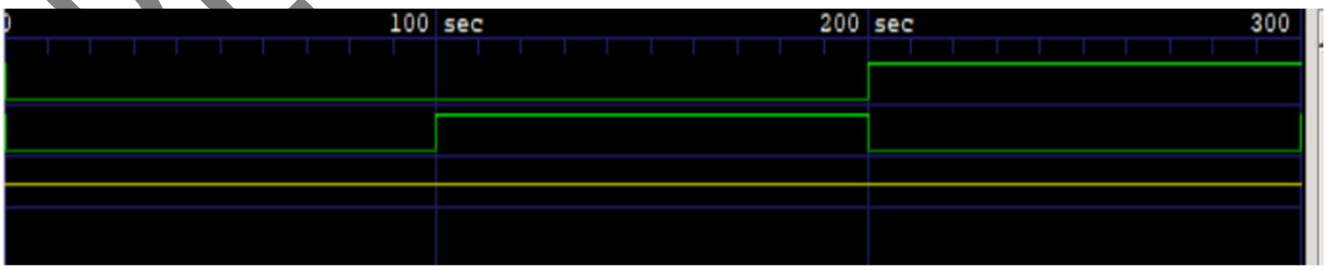
Week#____1_____ Program Number: ____3___

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NAND GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NAND GATE TRUTH TABLE

```
module Nand(a,b,c,Y);

input a,b,c;
output Y;

assign c = a & b;

assign Y = ~c ;

endmodule
```

```
C:\iverilog\bin>iverilog.exe -o NANDD nand_mine.v and2_tb.v

C:\iverilog\bin>vvp NANDD
VCD info: dumpfile Nand_test.vcd opened for output.
                  0a=0, b=0, Y=1
                100a=0, b=1, Y=1
                200a=1, b=0, Y=1
                300a=1, b=1, Y=x
```



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Date: 18-08-2022

Name: Sujal S	SRN: PES2UG21CS548	Section I

Week#____1_____ Program Number: ____4___

TITLE:

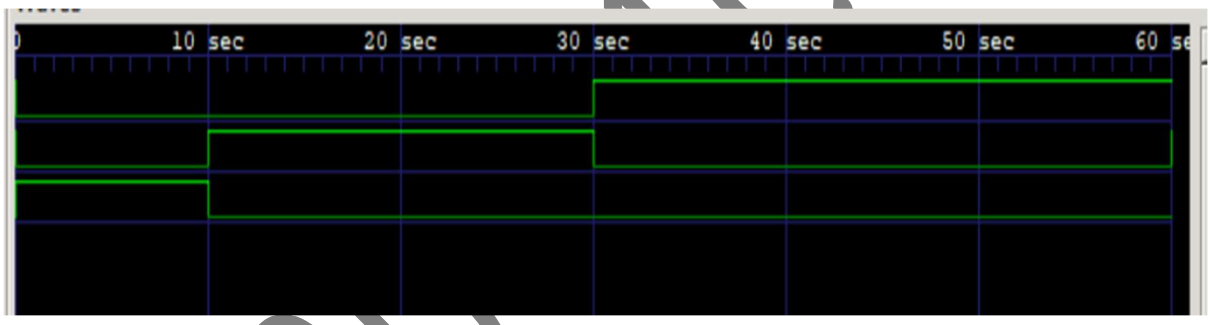
WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOR GATE TRUTH TABLE

```
1  module Nor(a,b,c,Y);
2
3  input a,b,c;
4  output Y;
5
6  assign c = a | b;
7  assign Y = ~c;
8
9  endmodule
```

```
C:\iverilog\bin>iverilog.exe -o norr nor_mine.v and2_tb.v

C:\iverilog\bin>vvp norr
VCD info: dumpfile Nor_test.vcd opened for output.
                   0a=0, b=0, c=1
                  10a=0, b=1, c=0
                  30a=1, b=0, c=0
                  60a=1, b=1, c=0

C:\iverilog\bin>
```



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Date: 18-08-2022

Name: Sujal S	SRN: PES2UG21CS548	Section I

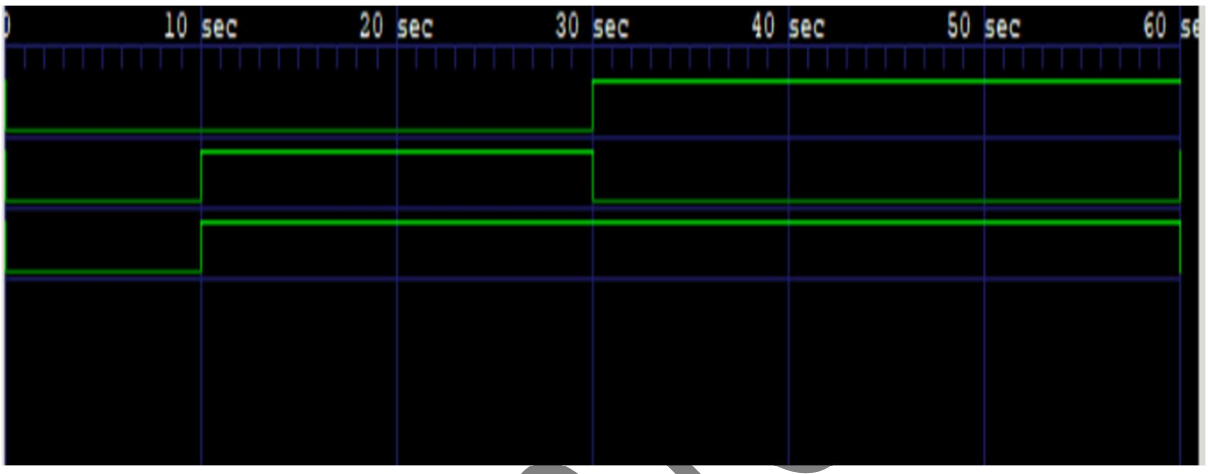
Week#____1_____ Program Number: ____5__

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

```
module Xor(a,b,c,d,Y);

input a,b,c,d;
output Y;

assign c = ~a&b;
assign d = ~b&a;
assign Y = c|d;

endmodule
```

```
C:\iverilog\bin>vvp xorr
VCD info: dumpfile Xor_test.vcd opened for output.
                   0a=0, b=0, c=0
                  10a=0, b=1, c=1
                  30a=1, b=0, c=1
                  60a=1, b=1, c=0

C:\iverilog\bin>
```



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Date: 18-08-2022

Name: Sujal S	SRN: PES2UG21CS548	Section I

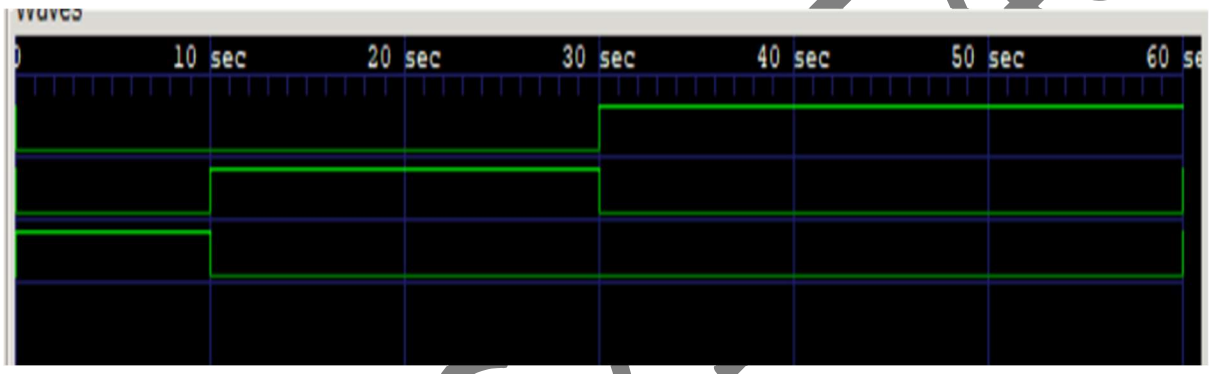
Week#____1_____ Program Number: ____6___

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XNOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

```
module Xnor( a,b,c,d,Y);

input a,b,c,d;
output Y;

assign c = a & b;
assign d = ~a & ~b;
assign Y = c | d;

endmodule
```

```
C:\iverilog\bin>iverilog.exe -o xnorr xnor_mine.v and2_tb.v

C:\iverilog\bin>vvp xnorr
VCD info: dumpfile Xnor_test.vcd opened for output.
                    0a=0, b=0, c=1
                   10a=0, b=1, c=0
                   30a=1, b=0, c=0
                   60a=1, b=1, c=1
```



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: Sujal S
Name: Sujal S
SRN: PES2UG21CS548
Section: I
Date: 18-08-2022