Digital Design and Computer Organization Laboratory

UE21CS251A

3rd Semester, Academic Year 2022-23

Date: 27/08/2022

Name: SUJAL S	SRN: PES2UG21CS548	Section I

Week#__2_____

Program Number :___1____

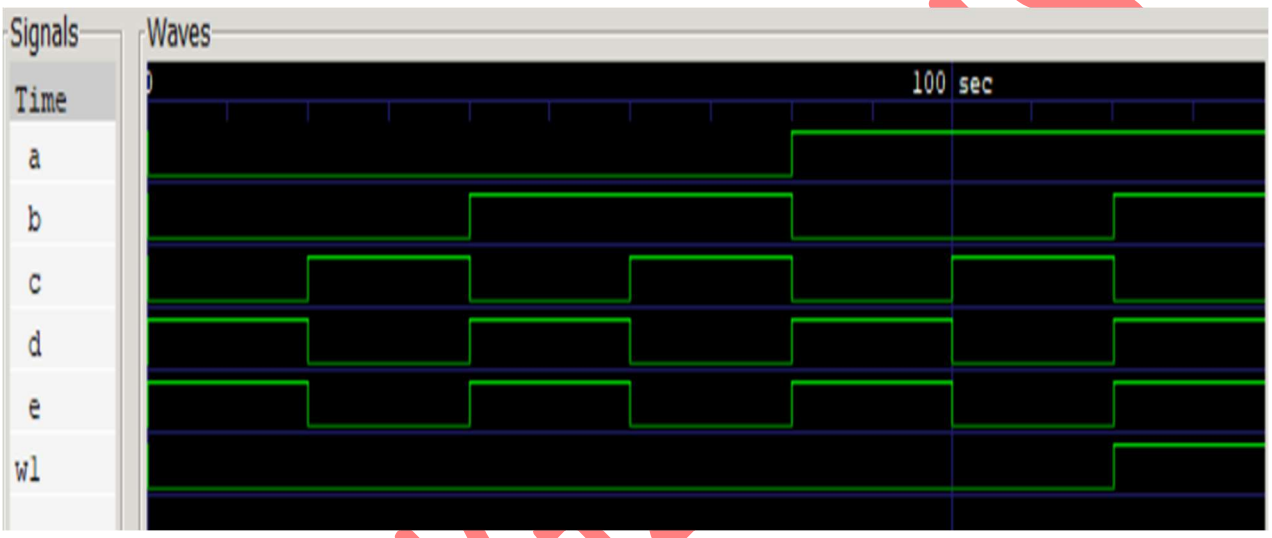
Title of the Program SIMPLE_CIRCUIT

Aim:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN SIMPLE CIRCUIT.GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE

```
module my_simple_circuit(a,b,c,d,e);

output d,e;
input a,b,c;

wire w1;

assign w1 =  a & b;

assign e =  ~c ;
assign d = e | w1;

endmodule
```

```
C:\iverilog\bin>iverilog.exe -o sujal mysimplecircuit.v simplecircuit_testbench.v

C:\iverilog\bin>vvp sujal
VCD info: dumpfile M.vcd opened for output.
                   0A=0, B=0, C=0, D=1 ,E=1
                  20A=0, B=0, C=1, D=0 ,E=0
                  40A=0, B=1, C=0, D=1 ,E=1
                  60A=0, B=1, C=1, D=0 ,E=0
                  80A=1, B=0, C=0, D=1 ,E=1
                 100A=1, B=0, C=1, D=0 ,E=0
                 120A=1, B=1, C=0, D=1 ,E=1
                 140A=1, B=1, C=1, D=1 ,E=0
```



a	b	c	d(output)	e(output)
0	0	0	1	1
0	0	1	0	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

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Program Number: ___2____

Title of the Program

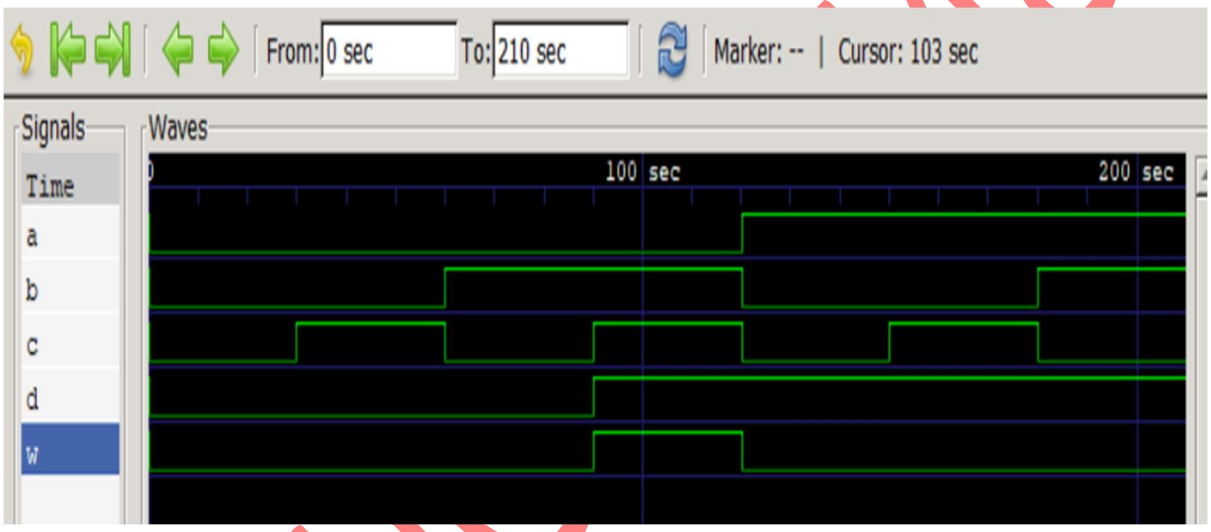
CIRCUIT1

Aim:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT1. GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE

```
module my_circuit1(a,b,c,d);

input a,b,c;
output d;

wire w;

assign w = c & b;
assign d = w | a;

endmodule
```

```
C:\iverilog\bin>iverilog.exe -o answer my_circuit1.v circuit1_testbench.v

C:\iverilog\bin>vvp answer
VCD info: dumpfile M1.vcd opened for output.
                    0A=0, B=0, C=0,Y=0
                   30A=0, B=0, C=1,Y=0
                   60A=0, B=1, C=0,Y=0
                   90A=0, B=1, C=1,Y=1
                  120A=1, B=0, C=0,Y=1
                  150A=1, B=0, C=1,Y=1
                  180A=1, B=1, C=0,Y=1
                  210A=1, B=1, C=1,Y=1
```



A	B	C	Y(Output)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

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Program Number: ___3____

Title of the Program

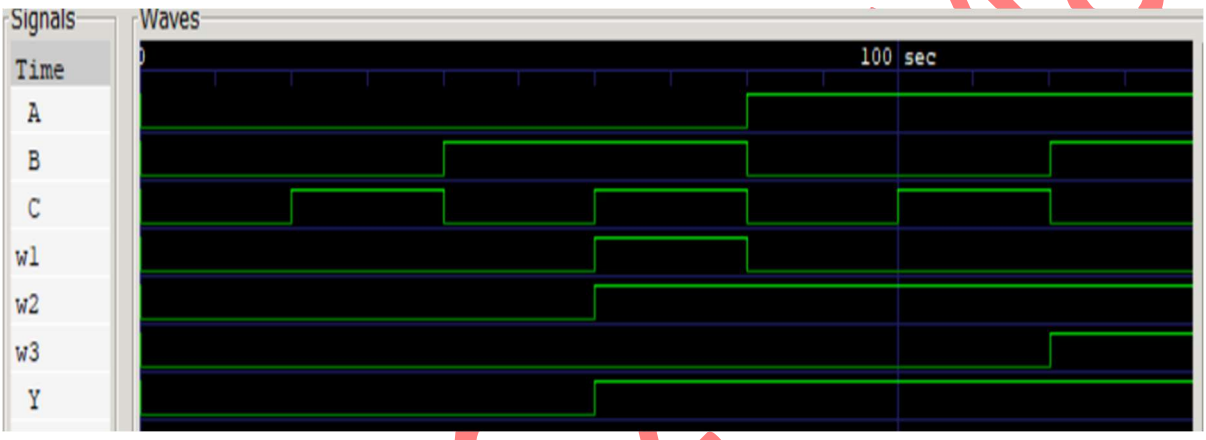
CIRCUIT2

Aim:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT2. GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE

```
module my_circuit2(A,B,C,Y);

output Y;
input A,B,C;

wire w1,w2,w3;

assign w1= C & B;
assign w2= w1 | A;
assign w3= A & B;
assign Y = w3 | w2;

endmodule
```

```
C:\iverilog\bin>iverilog.exe -o sujal my_circuit2.v circuit2_testbench.v

C:\iverilog\bin>vvp sujal
VCD info: dumpfile M2.vcd opened for output.
                   0A=0, B=0, C=0, Y=0
                  20A=0, B=0, C=1, Y=0
                  40A=0, B=1, C=0, Y=0
                  60A=0, B=1, C=1, Y=1
                  80A=1, B=0, C=0, Y=1
                 100A=1, B=0, C=1, Y=1
                 120A=1, B=1, C=0, Y=1
                 140A=1, B=1, C=1, Y=1
```



A	B	C	Y(Output)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

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Program Number: ___4___

Title of the Program

Half Adder

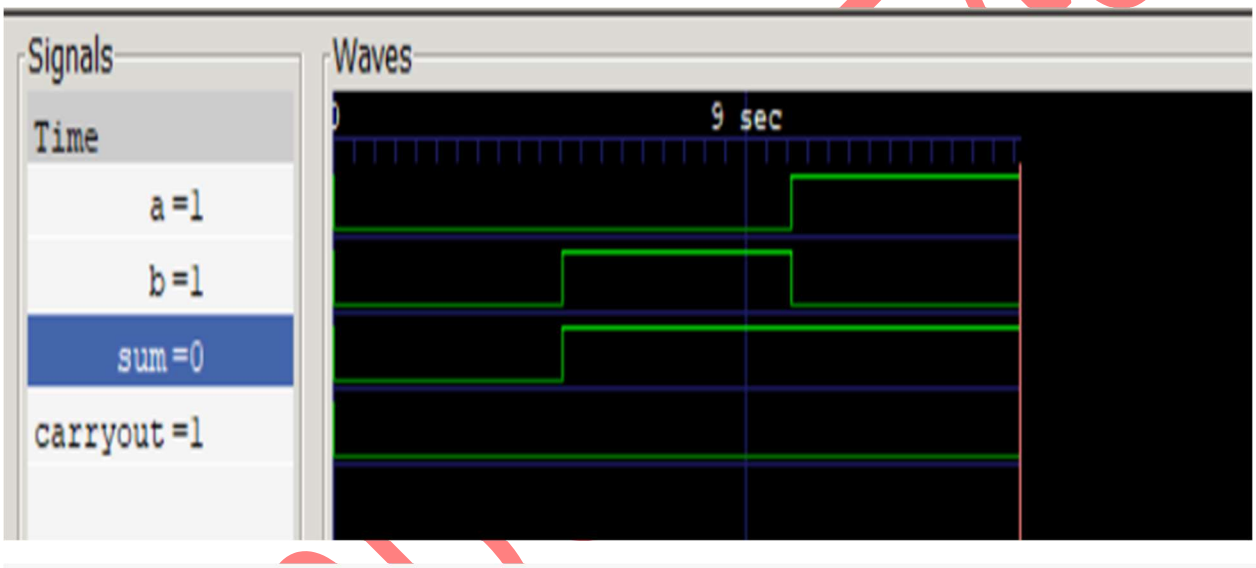
Aim:

WRITE A VERILOG PROGRAM TO MODEL THE HALF ADDER. GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE


```
1   module my_halfadder(a, b, sum, carryout);
2
3   input a,b;
4   output sum,carryout;
5
6   assign sum =  a & (~b) | (~a) & b;
7   assign carryout = a & b ;
8
9   endmodule
```

```
C:\iverilog\bin>iverilog.exe -o adder halfadder.v halfadder_testbench.v

C:\iverilog\bin>vvp adder
VCD info: dumpfile adder.vcd opened for output.
                  0a=0, b=0,sum=0,carry=0
                  5a=0, b=1,sum=1,carry=0
                 10a=1, b=0,sum=1,carry=0
                 15a=1, b=1,sum=0,carry=1
```



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

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Program Number: ___5____

Title of the Program

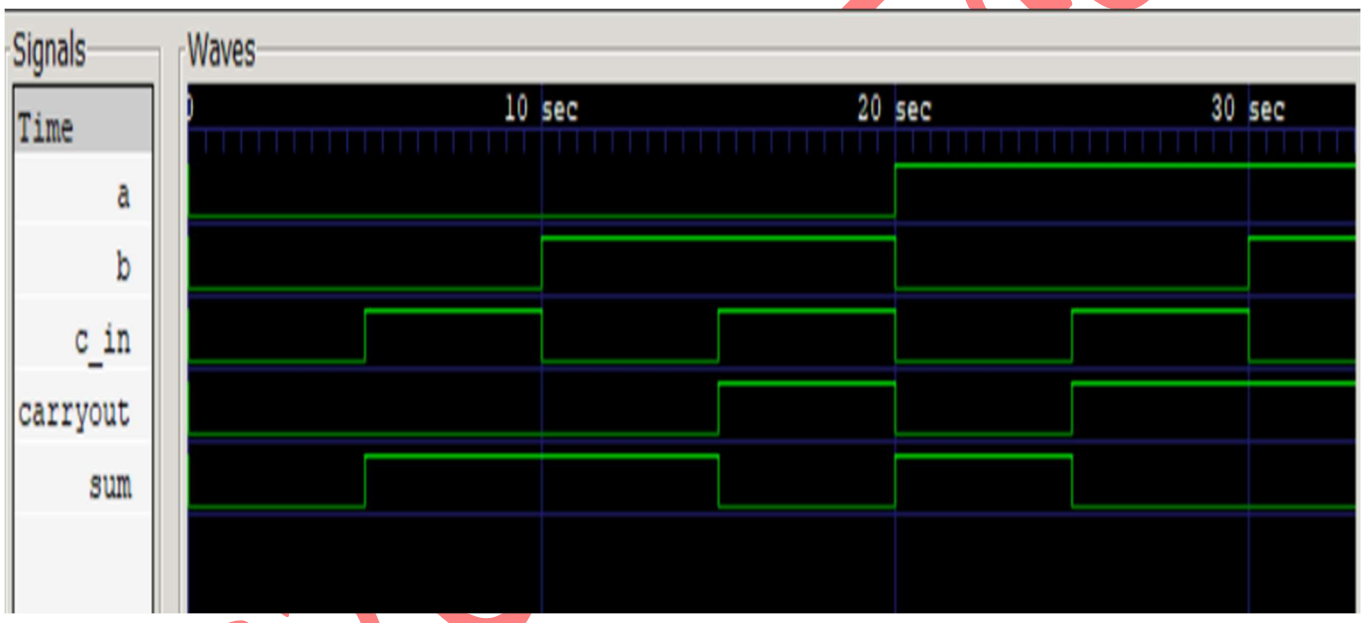
Full Adder

Aim:

WRITE A VERILOG PROGRAM TO MODEL THE FULL ADDER. GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE

```
module my_fulladder(a, b, c_in,sum,carryout);

input a,b,c_in;
output sum,carryout;

assign sum = (a)^(b)^(c_in);
assign carryout =  (a&b) | (c_in & (a^b));

endmodule
```

```
C:\iverilog\bin>iverilog.exe -o fulladder fulladder.v fulladdertestbench.v

C:\iverilog\bin>vvp fulladder
VCD info: dumpfile adder.vcd opened for output.
                    0a=0, b=0, c=0,sum=0,carry=0
                    5a=0, b=0, c=1,sum=1,carry=0
                   10a=0, b=1, c=0,sum=1,carry=0
                   15a=0, b=1, c=1,sum=0,carry=1
                   20a=1, b=0, c=0,sum=1,carry=0
                   25a=1, b=0, c=1,sum=0,carry=1
                   30a=1, b=1, c=0,sum=0,carry=1
                   35a=1, b=1, c=1,sum=1,carry=1
```



Inputs			Outputs	
A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Disclaimer:

- The programs and output submitted is duly written, verified and executed my me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: SUJAL S
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