ASSIGNMENT 3

Digital Design and Computer Organization

UE21CS251A

3rd Semester, Academic Year 2021-22

Date:14/09/2022

Name: Sujal.S	SRN:PES2UG21CS548	Section I

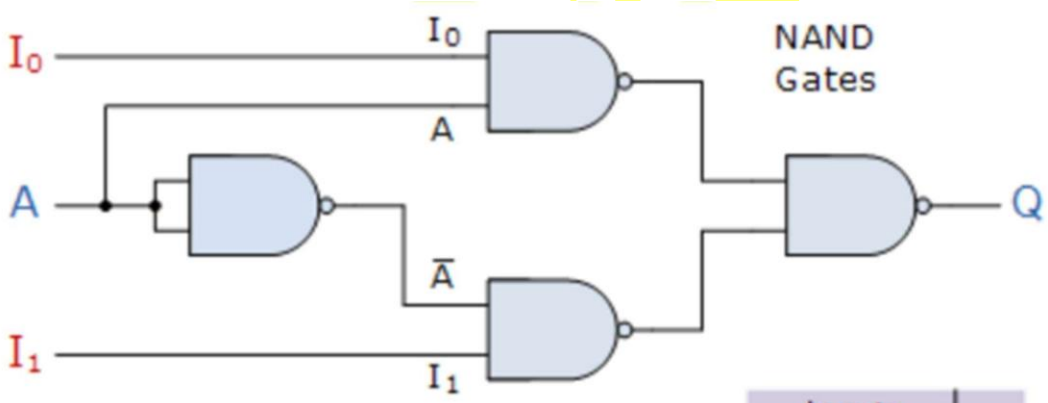
Program Number: ___1___

2:1 MUX

AIM: DESIGN A 2 TO 1 MULTIPLEXER AND VERIFY ITS TRUTH TABLE

```
module mux2_1(y,s,i0,i1);

input s,i0,i1;
output y;

wire t1,t2;

assign t1 = i0 & (~s);
assign t2 = s & i1;

assign y = t1 | t2;

endmodule
```

```
C:\iverilog\bin>iverilog.exe -o answer two_1mux.v two_1_tb.v

C:\iverilog\bin>vvp answer
VCD info: dumpfile mux2_1test.vcd opened for output.
At time =                    5, S=0, A=0, B=0, Output = 0
At time =                   10, S=0, A=0, B=1, Output = 0
At time =                   15, S=0, A=1, B=0, Output = 1
At time =                   20, S=0, A=1, B=1, Output = 1
At time =                   25, S=1, A=0, B=0, Output = 0
At time =                   30, S=1, A=0, B=1, Output = 1
At time =                   35, S=1, A=1, B=0, Output = 0
At time =                   40, S=1, A=1, B=1, Output = 1
```



Truth Table

Inputs			
A	I_1	I_0	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

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Program Number: ___2____

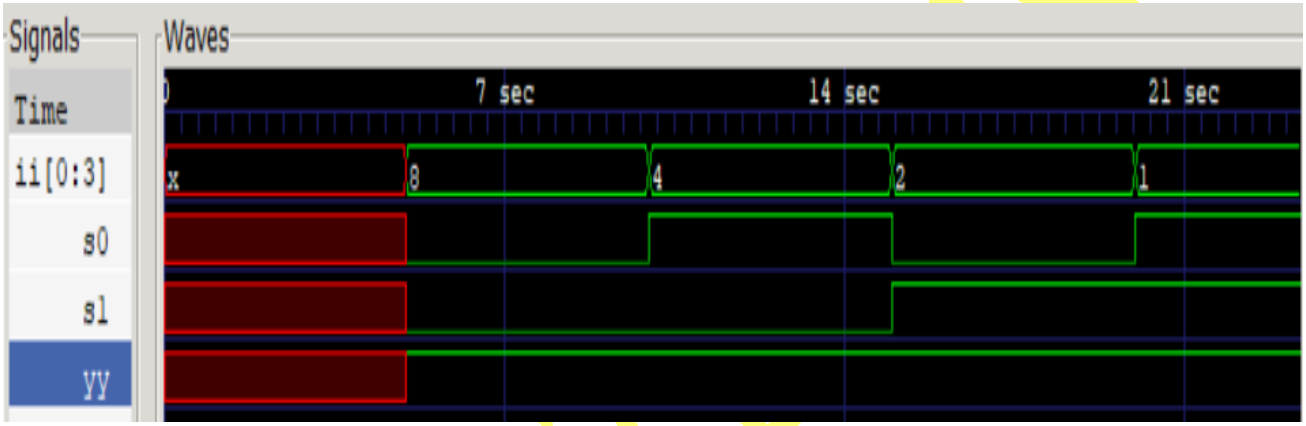
4_1 MUX

AIM: DESIGN A 4 TO 1 MULTIPLEXER AND VERIFY ITS TRUTH TABLE

```
module mux4_1(i,s1,s0,y);

input [0:3]i;
input s1,s0;
output y;

wire w1,w2;

mux2_1 a(w1,s0,i[0],i[1]);
mux2_1 b(w2,s0,i[2],i[3]);

mux2_1 c(y,s1,w1,w2);

endmodule
```

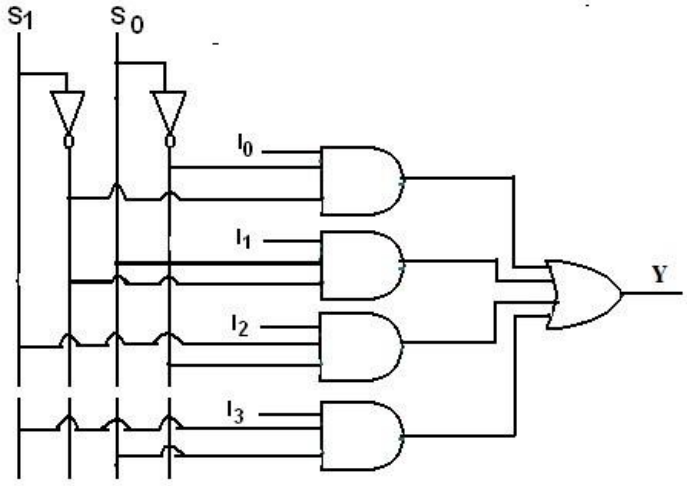
```
module mux2_1(y,s,i0,i1);

input s,i0,i1;
output y;

wire t1,t2;

assign t1 = i0 & (~s);
assign t2 = s & i1;

assign y = t1 | t2;

endmodule
```

```
C:\iverilog\bin>iverilog.exe -o out two_1mux.v 4_1.v 4_1_tb.v

C:\iverilog\bin>vvp out
VCD info: dumpfile mux4_1.vcd opened for output.
At time =                    5,Inputs=1000,s1=0,s0=0,Output = 1
At time =                   10,Inputs=0100,s1=0,s0=1,Output = 1
At time =                   15,Inputs=0010,s1=1,s0=0,Output = 1
At time =                   20,Inputs=0001,s1=1,s0=1,Output = 1
```



Input	S1	S0	Y
I_0	0	0	I_0
I_1	0	1	I_1
I_2	1	0	I_2
I_3	1	1	I_3

$$Y = S_1 S_0 I_3 + S_1 \overline{S_0} I_2 + \overline{S_1} S_0 I_1 + \overline{S_1}\,\overline{S_0} I_0$$



4 to 1 Multiplexer and its truth table

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Date:14/09/2022

Name: Sujal.S	SRN:PES2UG21CS548	Section I

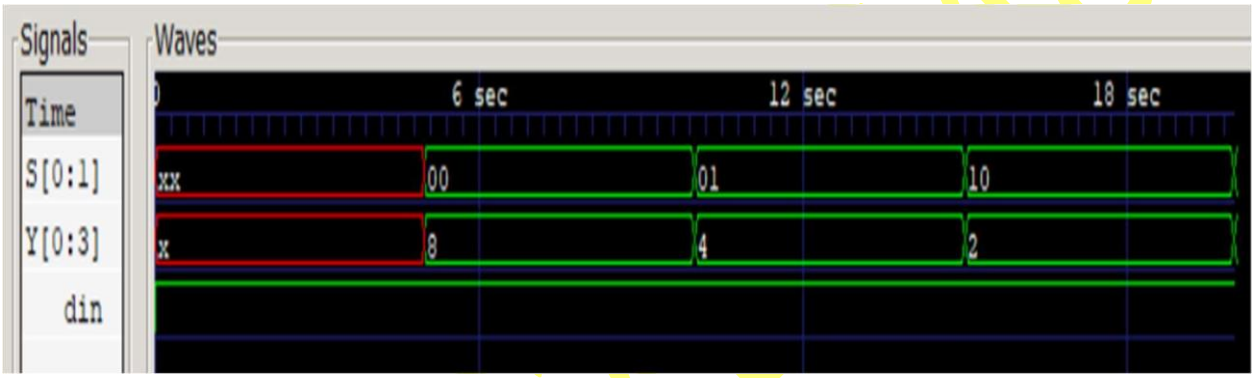
Program Number: ___3____

Title of the Program

1:4 De-MUX

```
module Demux1_4(Y,in,s);

input [0:1]s;
input in;
output [0:3]Y;

assign Y[0] =  ~s[0] & (~s[1]) & in
assign Y[1] =  ~s[0] &  s[1] & in ;
assign Y[2] =   s[0] &  (~s[1]) & in
assign Y[3] =   s[0] &  s[1] & in ;

endmodule
```

```
C:\iverilog\bin>iverilog.exe -o out 1_4.v 1_4_tb.v

C:\iverilog\bin>vvp out
VCD info: dumpfile demux.vcd opened for output.
                   0| Din = 1| S [0] = x| S[1] = x| Y [0] = x| Y [1] = x| Y [2] = x| Y [3] = x
                   5| Din = 1| S [0] = 0| S[1] = 0| Y [0] = 1| Y [1] = 0| Y [2] = 0| Y [3] = 0
                  10| Din = 1| S [0] = 0| S[1] = 1| Y [0] = 0| Y [1] = 1| Y [2] = 0| Y [3] = 0
                  15| Din = 1| S [0] = 1| S[1] = 0| Y [0] = 0| Y [1] = 0| Y [2] = 1| Y [3] = 0
                  20| Din = 1| S [0] = 1| S[1] = 1| Y [0] = 0| Y [1] = 0| Y [2] = 0| Y [3] = 1

C:\iverilog\bin>gtkwave demux.vcd
```



D	S_1	S_0	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

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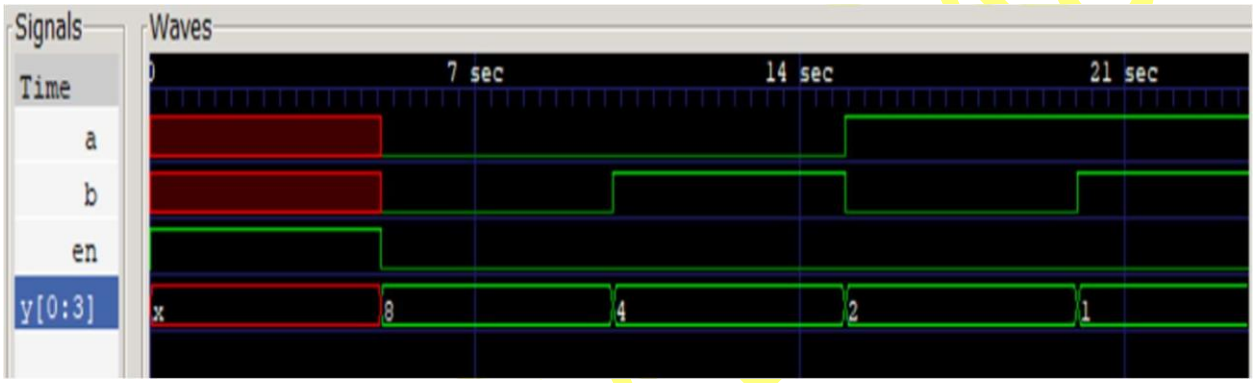
Name: Sujal.S	SRN:PES2UG21CS548	Section I

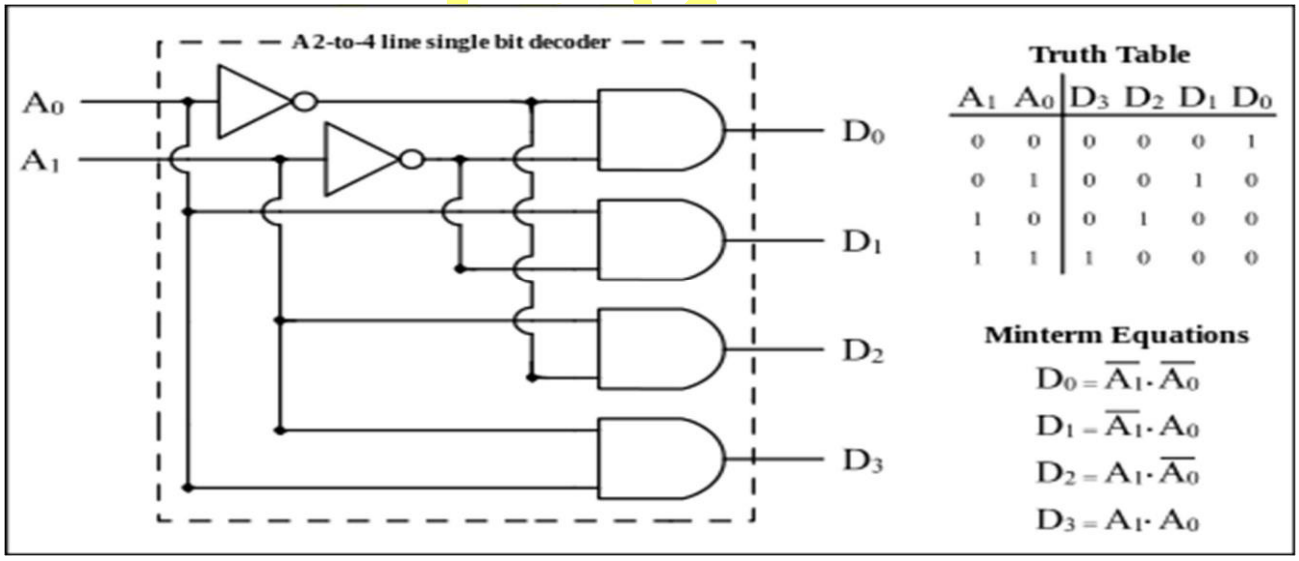
Program Number: ___4____

AIM: DESIGN A 2 TO 4 DECODER AND VERIFY ITS TRUTH TABLE

```
module Decoder2_4(enable,a,b,y);

    input enable,a,b;
    output [0:3]y;

    wire enb,na,nb;

    assign enb = ~enable;
    assign na = ~a;
    assign nb = ~b;

    assign y[0] = na & nb;
    assign y[1] = na & b;
    assign y[2] = a & nb;
    assign y[3] = a & b;

endmodule
```

```
C:\iverilog\bin>iverilog.exe -o out 2_4.v 2_4_tb.v

C:\iverilog\bin>vvp out
VCD info: dumpfile Decoder2_4test.vcd opened for output.
en=1 a=x b=x y=xxxx
en=0 a=0 b=0 y=1000
en=0 a=0 b=1 y=0100
en=0 a=1 b=0 y=0010
en=0 a=1 b=1 y=0001
```





Truth Table

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Minterm Equations

$D_0 = \overline{A_1} \cdot \overline{A_0}$

$D_1 = \overline{A_1} \cdot A_0$

$D_2 = A_1 \cdot \overline{A_0}$

$D_3 = A_1 \cdot A_0$

Disclaimer:

- The programs and output submitted is duly written, verified and executed my me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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