ASSIGNMENT 3

Digital Design and Computer Organization

UE21CS251A

3rd Semester, Academic Year 2021-22

Date:18/10/2022

Name: SUJAL.S	SRN:PES2UG21CS548	Section I

Program Number:____1_____

Title of the Program

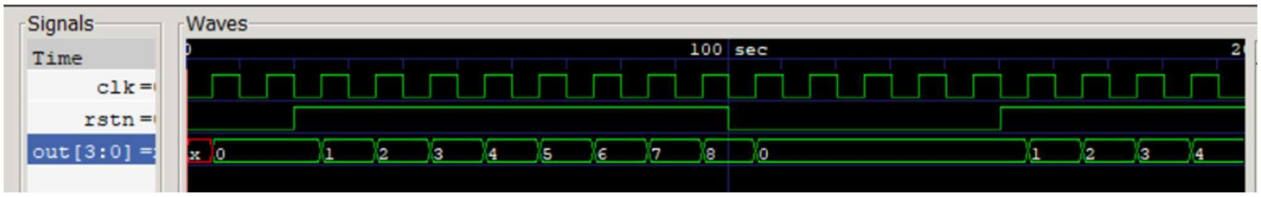
AIM: Write a Verilog code and test bench for 4 bit Binary up counter designed using D Flip Flops

C: > iverilog > bin > counter.v

```
1   module counter (clock ,reset ,out);
2
3   input clock;
4   input reset;
5   output reg[3:0] out;
6
7   always @ (posedge clock)
8   begin
9      if (! reset)
10        out <= 0;
11     else
12        out <= out + 1;
13  end
14
15  endmodule
```

```
module tb_counter;

reg clk;
reg rstn;
wire [3:0] out;

counter   c0 ( .clock (clk),.reset (rstn),.out (out));
 always #5 clk = ~clk;

  initial begin
    clk <= 0;
    rstn <= 0;

   $monitor ("Time = %0t  Output = %b", $time, out);
    #20   rstn <= 1;
   $monitor ("Time = %0t  Output = %b", $time, out);
    #80   rstn <= 0;
   $monitor ("Time = %0t  Output = %b", $time, out);
    #50   rstn <= 1;
   $monitor ("Time = %0t  Output = %b", $time, out);
    #50 $finish;
  end

initial
begin

$dumpfile("counter.vcd");
  $dumpvars(0, tb_counter);
```

```
C:\iverilog\bin>iverilog.exe -o output counter.v countertb.v

C:\iverilog\bin>vvp output
VCD info: dumpfile counter.vcd opened for output.
Time = 0  Output = xxxx
Time = 5  Output = 0000
Time = 20  Output = 0000
Time = 25  Output = 0001
Time = 35  Output = 0010
Time = 45  Output = 0011
Time = 55  Output = 0100
Time = 65  Output = 0101
Time = 75  Output = 0110
Time = 85  Output = 0111
Time = 95  Output = 1000
Time = 100  Output = 1000
```



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Date:18/10/2022

Name: SUJAL.S	SRN:PES2UG21CS548	Section I

Program Number:____2_____

Title of the Program

Write a Verilog code and test bench for 4-bit Ring Counter by D flipflop

C: > iverilog > bin > ring.v

```
1   module ring_counter(Clock,Reset,out);
2
3   input Clock;
4   input Reset;
5
6   output [3:0] out;
7   reg [3:0] Count_temp;
8
9   always @(posedge(Clock))
10  begin
11      if(Reset == 1'b0)
12      begin
13          Count_temp <= 4'b0001;
14      end
15
16      else
17      begin
18          Count_temp <= {Count_temp[2:0],Count_temp[3]};
19      end
20  end
21
22  assign Count_out = Count_temp;
23  endmodule
```

```
ring_counter uut(.Clock(Clock),.Reset(Reset),.out(Count_out));

initial Clock = 1'b1;
always #10 Clock = ~ Clock;

initial
begin
    Clock <= 1'b0;
    Reset <= 1'b1;

    $monitor ("T = %0t out = %b", $time, Count_out);
    repeat (2) @(posedge (Clock));

    Reset <= 1'b0;
    Clock <= 1'b1;
    $monitor ("T = %0t out = %b", $time, Count_out);
    repeat (15) @(posedge (Clock));
    $finish;
end

initial
begin

$dumpfile("ring_counter.vcd");
  $dumpvars(0,tb_ring);

end
endmodule
```

```
C:\iverilog\bin>vvp dsn
VCD info: dumpfile rc_test.vcd opened for output.
                 0clk=1,out=1000,reset=1
                 5clk=0,out=1000,reset=1
                10clk=1,out=0100,reset=0
                15clk=0,out=0100,reset=0
                20clk=1,out=0010,reset=0
                25clk=0,out=0010,reset=0
                30clk=1,out=0001,reset=0
                35clk=0,out=0001,reset=0
                40clk=1,out=1000,reset=0
                45clk=0,out=1000,reset=0
```

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UE21CS251A

3rd Semester, Academic Year 2021-22

Date:18/10/2022

Name: SUJAL.S	SRN: PES2UG21CS548	Section I

Program Number:____3_____

Title of the Program

Write a Verilog code and test bench for 4-bit Johnson Counter by D flipflop

```
module JohnSon_Counter #(parameter WIDTH=4)(clock,reset,out);

input clock;
input reset;
output [WIDTH-1 : 0] out;

always @ (posedge clock)
begin
   if (!reset)
      out <= 1;
   else
      begin
         out[WIDTH-1] <= ~out[0];

         for (int i = 0; i < (WIDTH-1); i=i+1)
         begin
            out[i] <= out[i+1];
         end
      end
end
endmodule
```

```
6   wire [WIDTH-1 : 0] out;
7
8   JohnSon_Counter  u0 (.clock (clk), .reset (rstn), .out(out));
9
10  initial clk = 0;
11  always #10 clk = ~clk;
12
13  initial
14  begin
15
16  {clk, rstn} <= 0;
17
18  $monitor ("Time = %0t  Output = %b", $time, out);
19     repeat (2) @(posedge clk);
20     $monitor ("Time = %0t  Output = %b", $time, out);
21     rstn <= 1;
22     $monitor ("Time = %0t  Output = %b", $time, out);
23     repeat (15) @(posedge clk);
24     $monitor ("Time = %0t  Output = %b", $time, out);
25     $finish;
26  end
27
28  initial
29  begin
30
31  $dumpfile("u0.vcd");
32    $dumpvars(0, tb);
33  end
34  endmodule
```

```
T=0 out=xxxx
T=10 out=0001
T=50 out=0000
T=70 out=1000
T=90 out=1100
T=110 out=1110
T=130 out=1111
T=150 out=0111
T=170 out=0011
T=190 out=0001
T=210 out=0000
T=230 out=1000
T=250 out=1100
T=270 out=1110
T=290 out=1111
T=310 out=0111
```

Disclaimer:

- The programs and output submitted is duly written, verified and executed my me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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