



Name : Sujal Agarwal
Roll.No : BT21ECE055
Course : CMOS design
Instructor : Dr.Paritosh Peshwa

Project Report

Title:

Design of Timer 555 in Astable Configuration.

1. Simulate schematic of 555 Timer in Astable Configuration in NgSpice.
2. Simulate layout of 555 Timer in Astable Configuration in Microwind.

Theory:

555 Timer:

The 555 timer IC is an integrated circuit (chip) used in a variety of timer, delay, pulse generation, and oscillator applications. The basic 555 timer gets its name from the fact that there are three internally connected $5K\Omega$ resistors which it uses to generate the two comparators reference voltages. Functional Diagram of 555 Timer:

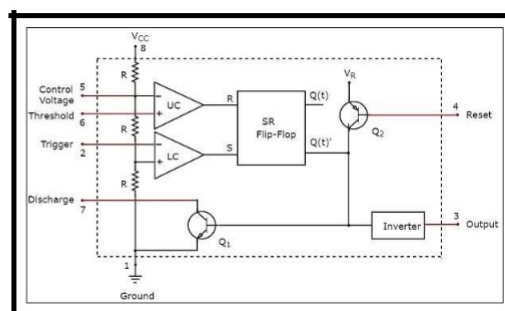


Figure 1: Functional Diagram of 555 Timer

Description of Functional Diagram:

Voltage Divider Network: The voltage divider network consists of a three $5k\Omega$ resistors that are connected in series between the supply voltage V_{DD} and ground.

The Network provides $2V_{DD}/3$ Voltage at the point after which two $5k\Omega$ resistors are connected to ground. Similarly it provides $V_{DD}/3$ at the point after which one $5k\Omega$ resistor is connected to grounds.

Comparator:

The functional diagram of a 555 Timer IC consists of two comparators: an Upper Comparator (UC) and a Lower Comparator (LC).

If the voltage present at the non-inverting terminal of an op-amp is greater than the voltage present at its inverting terminal, then the output of comparator will be $+V_{sat}$. This can be considered as Logic High ('1') in digital representation.

If the voltage present at the non-inverting terminal of op-amp is less than or equal to the voltage at its inverting terminal, then the output of comparator will be $-V_{sat}$. This can be considered as Logic Low ('0') in digital representation.

Flip-Flop:

An SR flip-flop stores the state of the timer and is controlled by the two comparators. The "Reset" pin overrides the other two inputs, thus the flip-flop (and therefore the entire timer) can be reset at any time.

Transistors and Inverter: The functional diagram of a 555 Timer IC consists of one npn transistor Q1 and one pnp transistor Q2. The npn transistor Q1 will be turned ON if its base to emitter voltage is positive and greater than cut-in voltage. Otherwise, it will be turned-OFF.

The pnp transistor Q2 is used as buffer in order to isolate the reset input from SR flip-flop and npn transistor Q1.

The inverter used in the functional diagram of a 555 Timer IC not only performs the inverting action but also amplifies the power level.

Astable Confriguation of 555 Timer

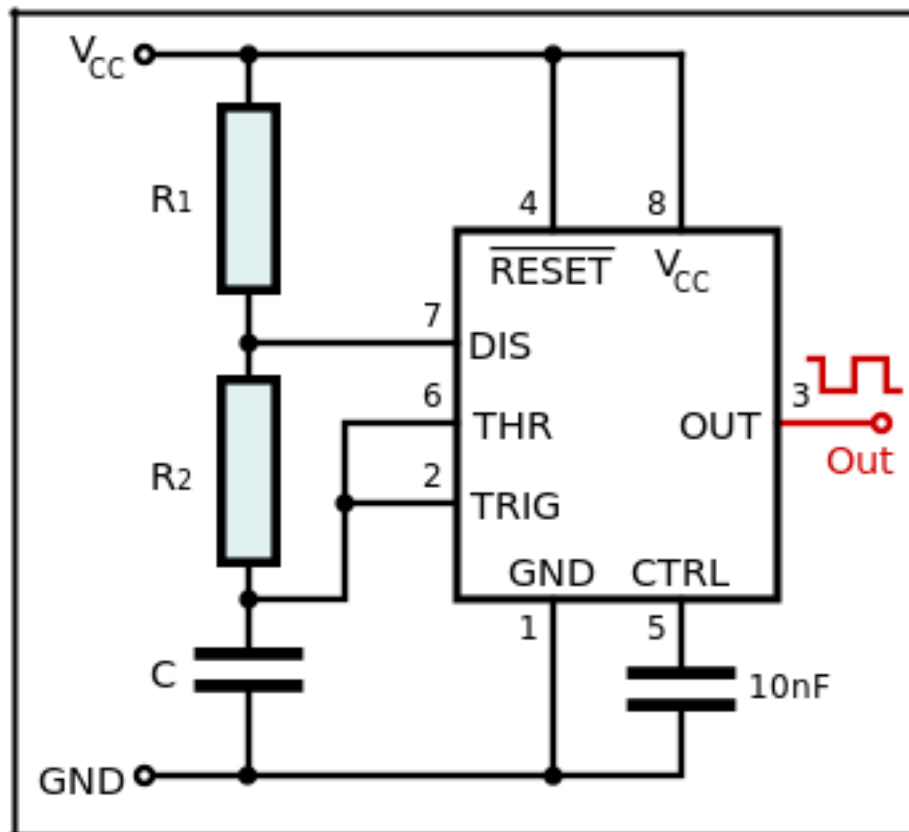


Figure 2: Astable Configuration of 555 Timer

In the astable configuration, the 555 timer puts out a continuous stream of rectangular pulses having a specific frequency. The astable configuration is implemented using two resistors, R_1 and R_2 and one capacitor C . In this configuration, the control pin is not used, thus it is connected to ground through a 10 nF decoupling capacitor to shunt electrical noise. The threshold and trigger pins are connected to the capacitor C ; thus they have the same voltage.

The Output Pulse Generated will have,

$$\begin{aligned}
 t_{\text{high}} &= \ln(2) * (R_1 + R_2) * C \\
 t_{\text{low}} &= \ln(2) * R_2 * C \\
 f &= \frac{t_{\text{high}}}{t_{\text{high}} + t_{\text{low}}} = \frac{\ln(2) * (R_1 + 2 * R_2) * C}{\ln(2) * (R_1 + 2 * R_2) * C + \ln(2) * R_2 * C} \\
 \text{dutyCycle}\% &= \frac{t_{\text{high}}}{t_{\text{high}} + t_{\text{low}}} * 100 = \frac{(R_1 + 2R_2)}{(R_1 + 2R_2) + R_2} * 100
 \end{aligned}$$

Theoretical Calculations:

Time period of Output wave for R_1 , R_2 and C equal to 8.2K Ω , 68K Ω and 500nF respectively is

$$f = \frac{10^6}{\ln(2) * (8.2 + 2 * 68) * 500} = 20$$

$$T = \frac{1}{f} = \frac{1}{20} = 0.05$$

CMOS Project

$$t_{\text{high}} = \ln(2) * (8.2 + 68) * 500 * 10^{-6} =$$

$$0.0264 \quad t_{\text{low}} = \ln(2) * (68) * 500 * 10^{-6} =$$

$$0.0235$$

$$\text{dutyCycle\%} = \frac{0.0264}{0.0264 + 0.0235} * 100 = \frac{0.0264}{0.0499} * 100 = 53\%$$

Circuit,Codes, Layouts and Outputs:

Note: In all the Circuit figure node number is displayed in red color.

555 Timer:

CMOS Circuit of 555 Timer in Astable Configuration:

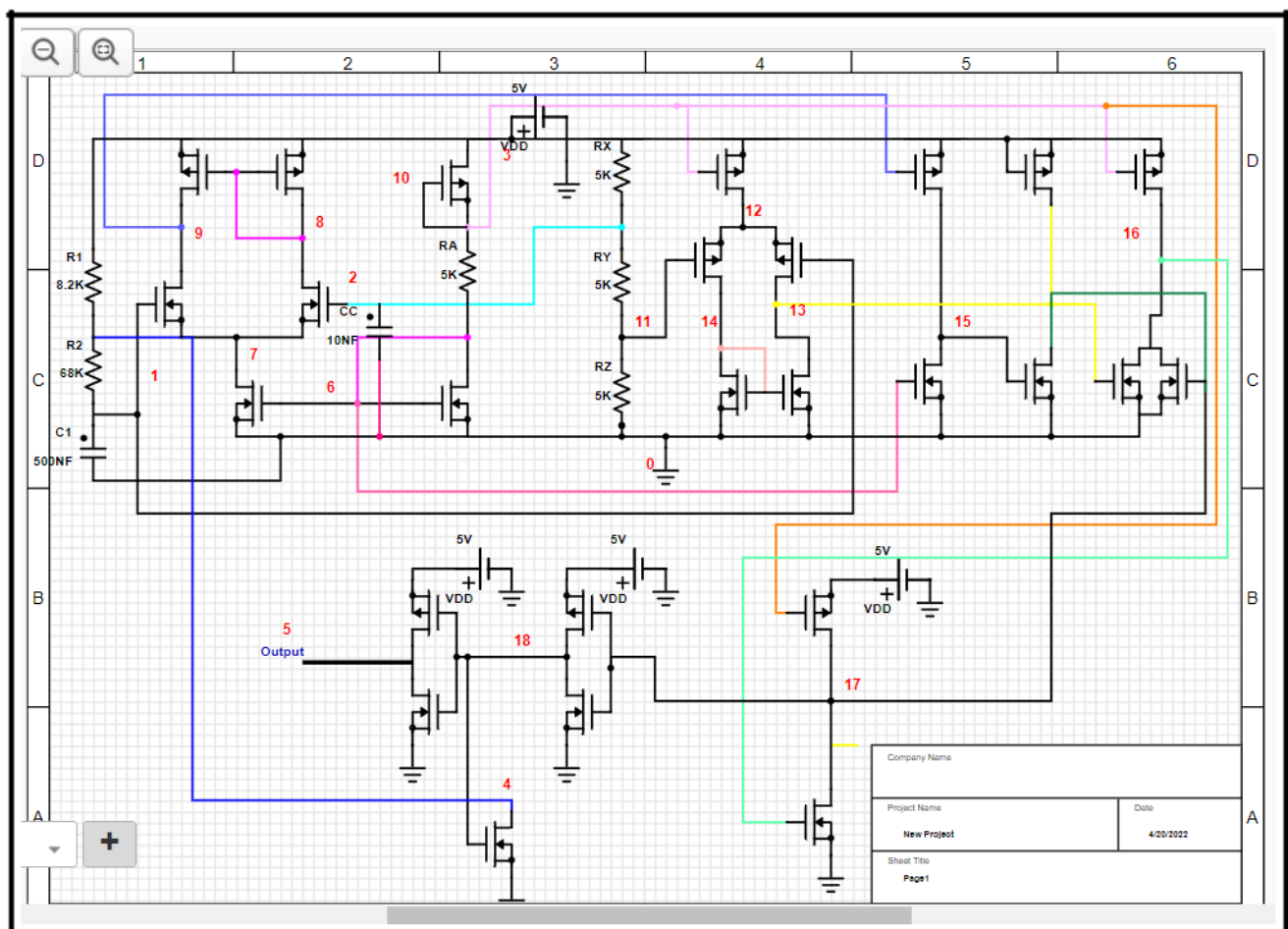


Figure 3: CMOS Circuit of 555 Timer in Astable Configuration

NgSpice Code:

```
*** Project    Timer 555
```

```
VDD 3 0 dc 2V
```

```
Rx 3 2 5k
```



```

Ry 2 11 5k
Rz 11 0 5k
Ra 10 6 5k
Cc 2 0 10n
R1 3 4 8.2K
R2 4 1 68 k
C 1 0 500n

.model nmod nmos level=54 verison=4.7
.model pmod pmos level=54 verison=4.7

M1 9 1 7 0nmod w = 100u | = 10u
M2 8 2 7 0nmod w = 100u | = 10u
M3 7 6 0 0nmod w = 100u | = 10u
M4 6 6 0 0nmod w = 100u | = 10u
M5 14 14 00 nmod w = 100u | = 10u
M6 13 14 00 nmod w = 100u | = 10u
M7 15 60 0 nmod w = 100u | = 10u
M8 17 15 00 nmod w = 100u | = 10u
M9 16 13 00 nmod w = 100u | = 10u
M10 16 17 0 0 nmod w = 100u | = 10u
M11 17 16 0 0 nmod w = 100u | = 10u
M12 4 18 00 nmod w = 100u | = 10u
M13 18 17 0 0 nmod w = 100u | = 10u
M14 5 18 00 nmod w = 100u | = 10u

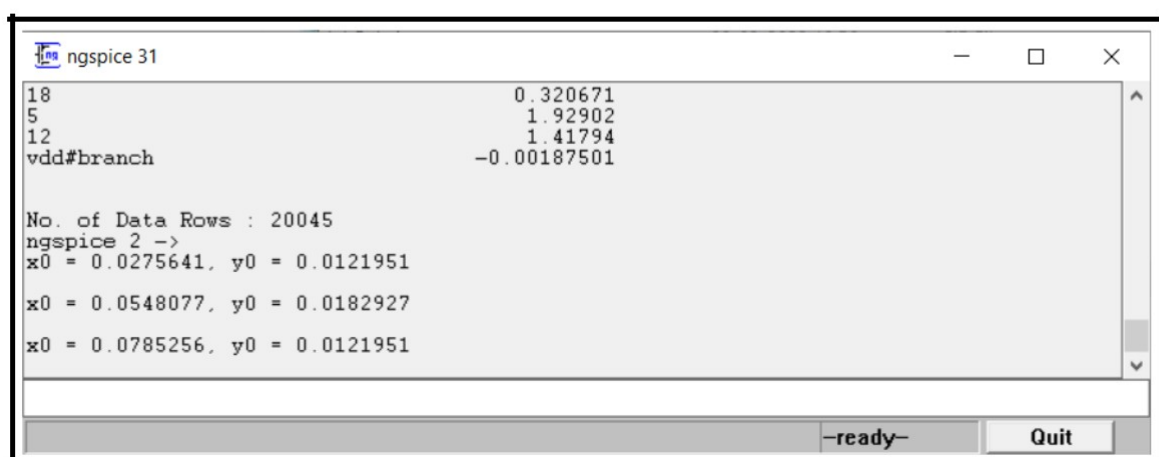
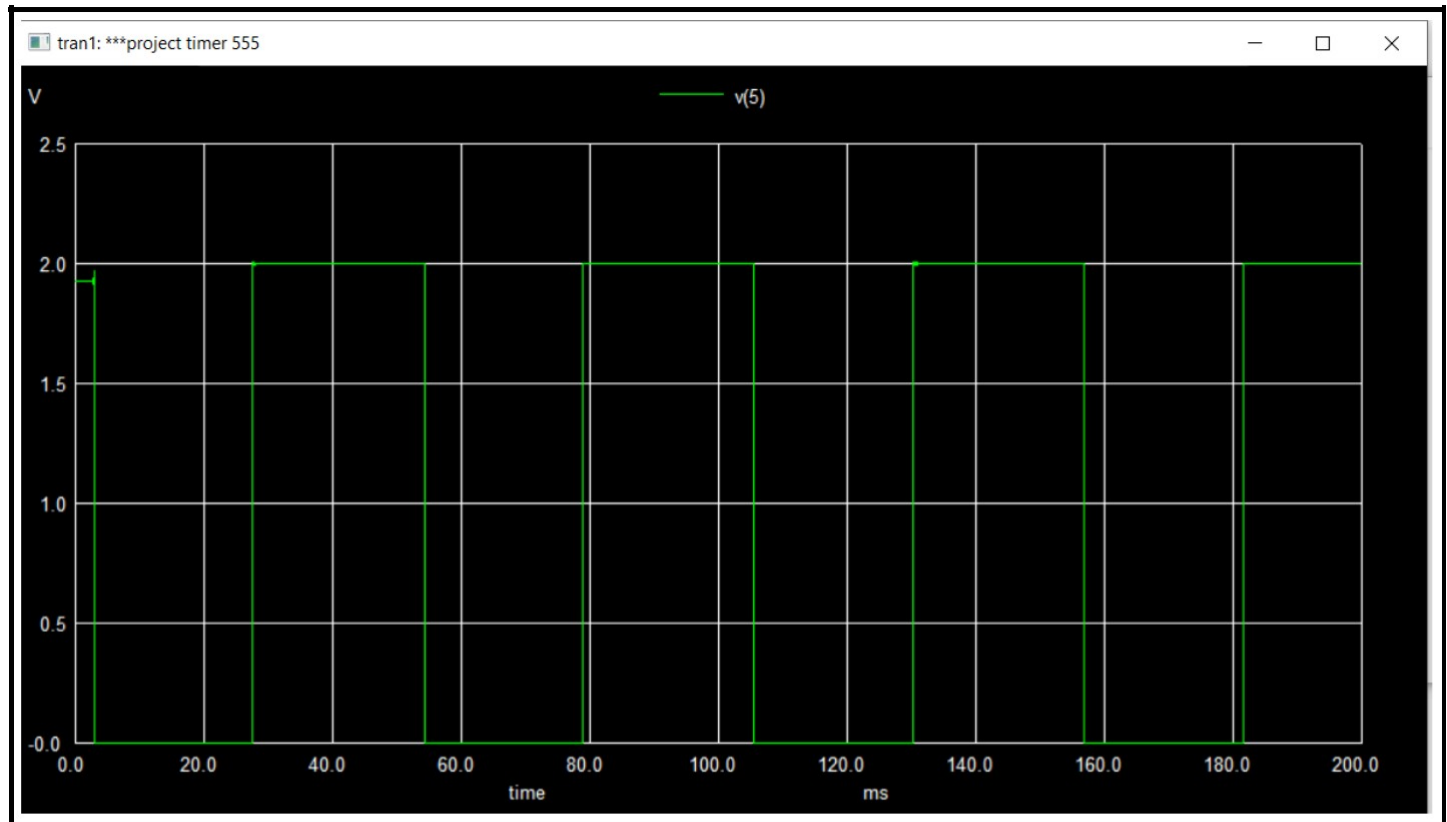
MA 9 8 3 3pmod w = 50u | = 10u
MB 8 8 3 3pmod w = 50u | = 10u
MC 10 10 33 pmod w = 50u | = 10u
MD 12 10 33 pmod w = 50u | = 10u
ME 14 11 12 12 pmod w = 50u | = 10u
MF 13 1 12 12 pmod w = 50u | = 10u
MG 15 93 3 pmod w = 50u | = 10u
MH 13 33 3 pmod w = 50u | = 10u
MI 16 10 33 pmod w = 50u | = 10u
MJ 17 10 33 pmod w = 50u | = 10u
MK 18 17 33 pmod w = 50u | = 10u
ML 5 183 3 pmod w = 50u | = 10u

.tran 0.01ms 200ms

```

```
.contr
olrun
plotV(5)
.endc
.end
```

Ngspice Output:



In above Output Images V(5) is Output.

Practical Calculations:

$$t_{\text{high}} = 0.0548077 - 0.0275641 = 0.027$$

$$t_{\text{low}} = 0.0785256 - 0.0548077$$

$$T = 0.05$$

Microwind Layout:

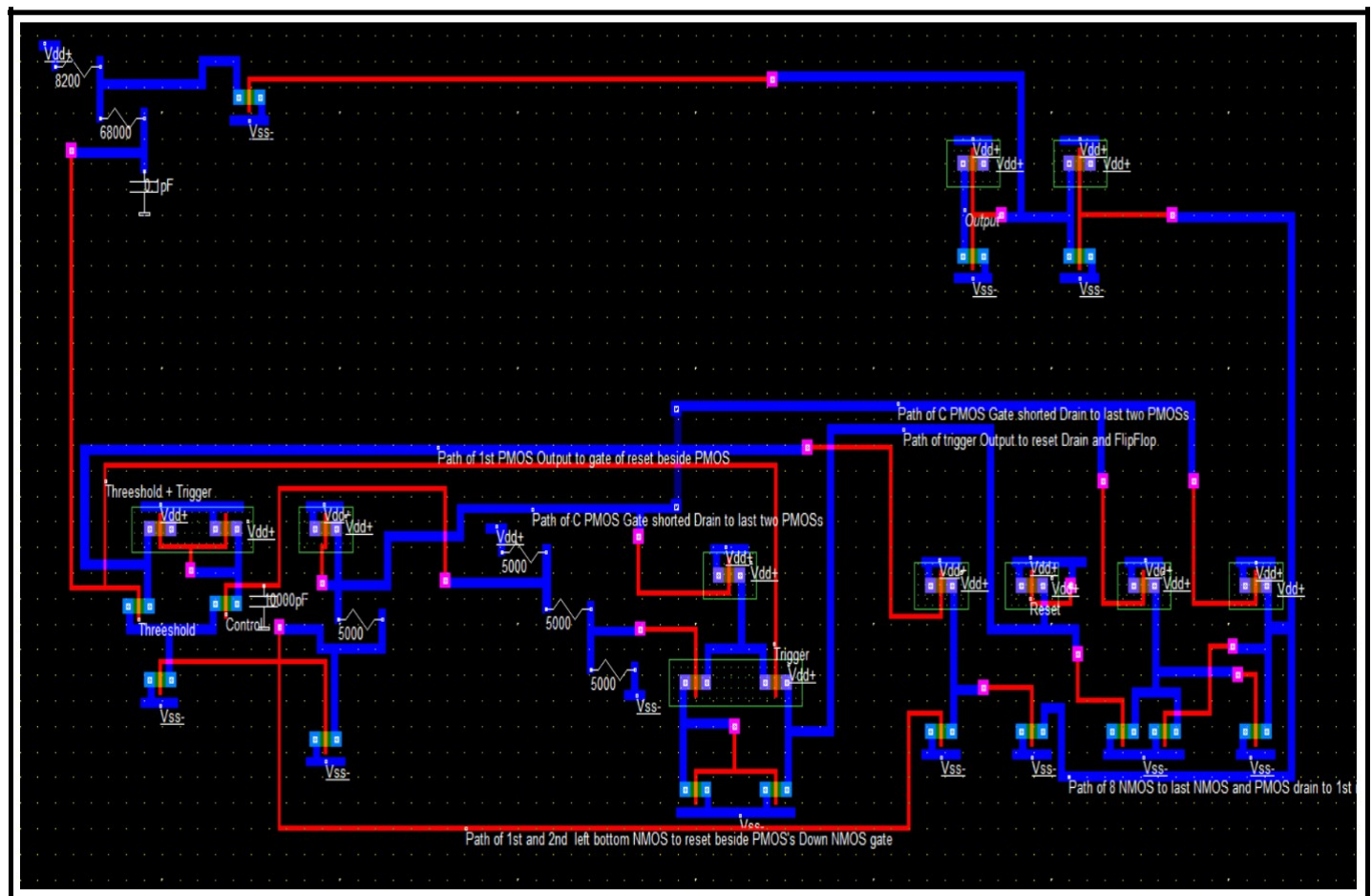


Figure 4: Microwind Layout of 555 Timer in Astable configuration

Simulation Output of Microwind Layout:

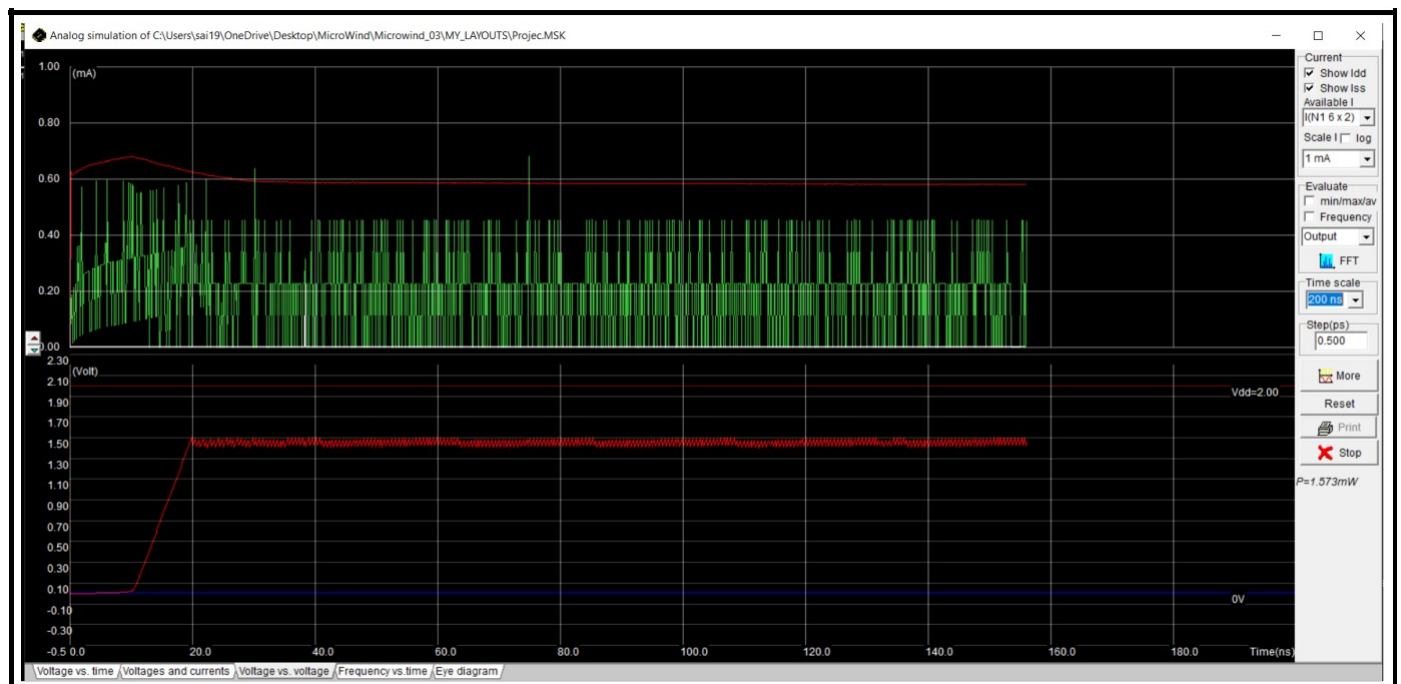


Figure 5: Microwind Layout Output of 555 Timer in Astable configuration

Conclusion:

In my project, I have Implemented the 555 timer in Astable Configuration, The theoritical calculations and Ngspice Calculations of Time Period of output pluse is same,and I designed the Layout of 555 Timer in MicroWind.some of the appli-cation of 555 Timer are Pulse Generation, Time Delay Generation,Precision Tim-ing,Sequential Timing,Pulse Width Modulation (PWM)