

# **Title of the Experiment: Hardware-based Security Primitives and Their Applications**

**Group Members' Names: Sujan Kumar Saha, Pankaj Bhowmik**

**Date: 10/23/2019**

---

## **Abstract**

In this experiment, we have implemented SRAM based Physical Unclonable Function (PUF), RO based PUF, SRAM based True Random Number generator (TRNG) and RO based TRNG. In the following experiment, two different types PUFs i.e. SRAM PUFs and RO-PUFs are analyzed and mapped on the FPGA of the Hardware Hacking board. As for the SRAM PUF, 64 bytes of the SRAM power-up states are read from the Microcontroller to generate a signature. Then, the signature is sent to the FPGA using the interconnections and extracted afterwards from an in-chip memory. In the second part of the experiment, a RO-PUF is implemented on the FPGA to generate a 128-bit key. The keys are collected at different operating voltages i.e. 2.7V and 3.3V. In the third part, a RO-based TRNG is developed using the RO-PUF modules. As per the instructions, the data are collected from the TRNG at varying voltages and different number stages of RO-based TRNG. All the data are processed afterwards using MATLAB.

## **Experimental Details**

**Goals:** This experiment has three goals.

1. Implementing two Physical Unclonable Functions (PUF): SRAM-based PUF and RO-based PUF.
2. Implementing two True Random Number Generators using PUFs.
3. Evaluating the PUFs and TRNGs.

**Experimental Setup:** We used Quartus, ATMEL Studio and Analog discovery to do the experiments. We used Matlab for data processing. Also, we have used NIST statistical tool to evaluate the performance of the TRNGs.

## **Part I:**

### **Experiment Steps:**

1. We have written the microcontroller code using assembly language and load that code to the microcontroller. In this part, we send the SRAM cell data through the PORTD and generate a clock signal using PORTC pin 7. We implemented a delay function to make the clock signal frequency as expected.
2. We programmed the FPGA to read the data from PORTD which is sent by the microcontroller and save the data in a RAM.
3. We also have written a Matlab code to calculate the mean value and hamming distance of the data signatures.

## **Part II:**

### **Experiment Steps:**

1. We implemented the top module in verilog using the given VHDL files. We followed the figure 2 of the given document to implement RO-based PUF. To make placement and routing of the ROs symmetric, we manually find the coordinates and put commands in the tcl command window.
2. The 128 bit key output of the PUF is kept in RAM. We took the results for three different voltages and calculated hamming distance.

### **Part III:**

#### **Experiment Steps:**

1. In this part, a SRAM based True Random Number Generator is implemented. We used the same implementation of part I. We took a couple of signatures and found a bit value which changes at different runs. So, the 8 bit value from those SRAM cells can be used as true random number generator.

### **Part IV:**

#### **Experiment Steps:**

1. A RO-based TRNG has been implemented with ten 5-stage ROs. We changed the number of stages and number of ROs according to the given conditions. We did the placement of ROs symmetric. Then, we took the 100000 bit number and save it in a RAM.

### **Part VI:**

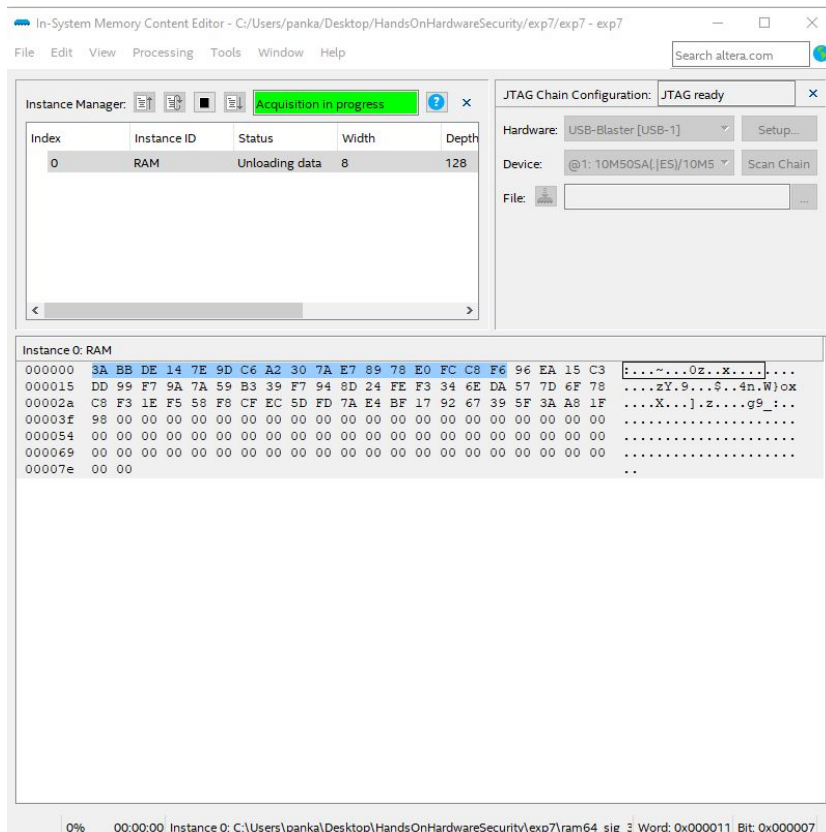
#### **Experiment Steps:**

1. We have done the optional follow-up which is randomness evaluation of the RO based TRNG. We downloaded the NIST source code, built it and use the binary bit data file to evaluate randomness of TRNG using 15 test suits.

## **Results and Observations**

### **Part I: SRAM PUF**

1. The size of the SRAM of Atmega16U4 is 1.25KB.
2. The address ranges from \$0100 to \$05FF for the SRAM. The lower addresses in that range are occupied by our program. We choose address from \$0500 to \$053F to get 64 byte signature
3. We generate a square wave by using PORTC bit PC7. We made the bit 1, added a delay and then set the bit to 0. This way we generate the square wave which is sent to the FPGA. The frequency of the square wave is 1.08Hz.
4. We have attached the assembly code with the report.
5. We have attached the FPGA code with the report. A screenshot of the In-system Memory content is given below.



6. We exported the signatures in hex file and processed those using Matlab. The S1 has 512 bits. The hex and binary values of S1 is given below.

S1

9267395F3AA81F983	1001001001100111001110010101111100111
ABBDE147E9DC6A2	010101010100000011111100110000011101010
307AE78978E0FCC8	1110111101111000010100011111101001110
F696EA15C3DD99F7	1110001101010001000110000011110101110
9A7A59B339F7948D	011110001001011110001110000011111001
24FEF3346EDA577D	1001000111101101001011011101010000101
6F78C8F31EF558F8C	0111000011110111011001100111110111100
FEC5DFD7AE4BF17	1101001111010010110011011001100111001
	1111011110010100100011010010010011111
	1101111001100110100011011101101101001
	0101110111110101101111011110001100100
	011110011000111101111010101010001111
	1000110011111111011000101110111111010
	1111010111001001011111100010111

7. 295 bits are 1 and 217 bits are 0. So , 42.38% bits are 0 and 57.61% bits are 1. The mean value is 0.5762
8. We took the S2 and S3 for voltage 3V and 2.7V. The values are given below.

S2

F79A7A59B339F7948	1111011110011010011110100101100110110
D24FEF3346EDA577	0110011100111110111100101001000110100
D6F78C8F31EF558F8	1001001111111011110011001101000110111

CFEC5DFD7AE4BF1	0110110100101011101111101011011110111
79267395F3AA81F98	1000110010001111001100011110111101010
3ABBDE147E9DC6A	1011000111110001100111111101100010111
2307AE78978E0FCC	0111111101011110101110010010111111000
8F696EA15C3DD99	1011110010010011001110011100101011111
	001110101010101000000111111001100000111
	0101011101111011110000101000111111010
	0111011100011010100010001100000111101
	0111001111000100101111000111000001111
	1100110010001111011010010110111010100
	00101011100001111011101100110011001

S3

948D24FEF3346EDA	1001010010001101001001001111111011110
577D6F78C8F31EF55	0110011010001101110110110100101011101
8F8CFEC5DFD7AE4B	1111010110111101111000110010001111001
F179267395F3AA81F	1000111101111010101011000111110001100
983ABBDE147E9DC6	1111111011000101110111111101011110101
A2307AE78978E0FC	1100100101111110001011110010010011001
C8F696EA15C3DD99	1100111001010111110011101010101000000
F79A7A59B339F7	1111110011000001110101011101111011110
	0001010001111110100111011100011010100
	0100011000001111010111001111000100101
	1110001110000011111100110010001111011
	0100101101110101000010101110000111101
	1101100110011111011110011010011110100
	1011001101100110011100111110111

- No, S2 and S3 are not the same as S1. S2 has 248 different bits compared with S1. So fractional hamming distance is 0.48. S3 has 244 different bits compared with S1. So, fractional hamming distance is 0.47.
- We have attached the Matlab code for calculating mean value and hamming distance with this report.

## Part II: RO-PUF

- The codes are attached with the report.
- Here is the K1 which has been taken for voltage value 3.3V.

K1

01010000000000011001001001101101100011111000110110010010
01110011100111000110111001111100000100110001111111010011
1110001100001000

- We took the results for voltage value 3V and 2.7V. The corresponding K2 and K3 are given below.

K2

10001100000011001101110011110011001000010000010000100001
0011100011111110001110000001111111111110010011111011111
0011101100011001

K3

01010011001011110010000000100111110111110010000000111111
001111100110100001101100011011011001111001110011100100111
0000011111001001

4. No, K2 and K3 are not the same as K1. K2 has 61 different bit with compared to K1. The fractional hamming distance is 0.4766. K3 has 65 different bits with compared to K1. The fractional hamming distance is 0.5078. As the hamming distance 0.5 is better, K3 has better hamming distance with K1 compared to K2.

### Part III: SRAM as a TRNG

1. We ran the part I several times with same voltage value and got the signature S1 values. We checked the values manually and observed that the value at SRAM address \$0504 changes randomly. So, we can use that 8 bit data for TRNG.
2. We send the address data of \$0504 to RAM using the same procedure in part I to find the 8-bit random number. The code is added with the report.

### Part IV: RO-based TRNG

1. We implemented the RO-based TRNG using ten 5-stage ROs. The 100000 bit numbers are collected for the given cases with voltage 3.3V and attached with the report.
2. We changed the stages of ROs to 9 and took the results.
3. The number of ROs have been changed to 20 and 30 and results have been taken.
4. The operating voltage has also been changed to 3V and 2.7V and results have been taken.
5. The robustness analysis is given in the table below. We measured the fractional hamming distance compared with the base design of 10 5 stage ROs with voltage 3.3V.

Voltage	# of ROs	# of Stages	#of Zeros	# of ones	Mean	Fractional Hamming Distance
3.3V	10	9	56906	43094	0.43094	0.4912
3.3V	20	5	58772	41228	0.41228	0.4634
3.3V	30	5	57570	42430	0.42430	0.4678
3.0V	10	5	57727	42273	0.42273	0.4899
2.7V	10	5	55113	44887	0.44887	0.4784

### Summary and discussion:

We learnt about PUF and TRNG and We faced difficulty to write microcontroller code and placement and routing of ROs to make those symmetric. But we were able to solve those. We also evaluated the robustness of the PUF and TRNG.