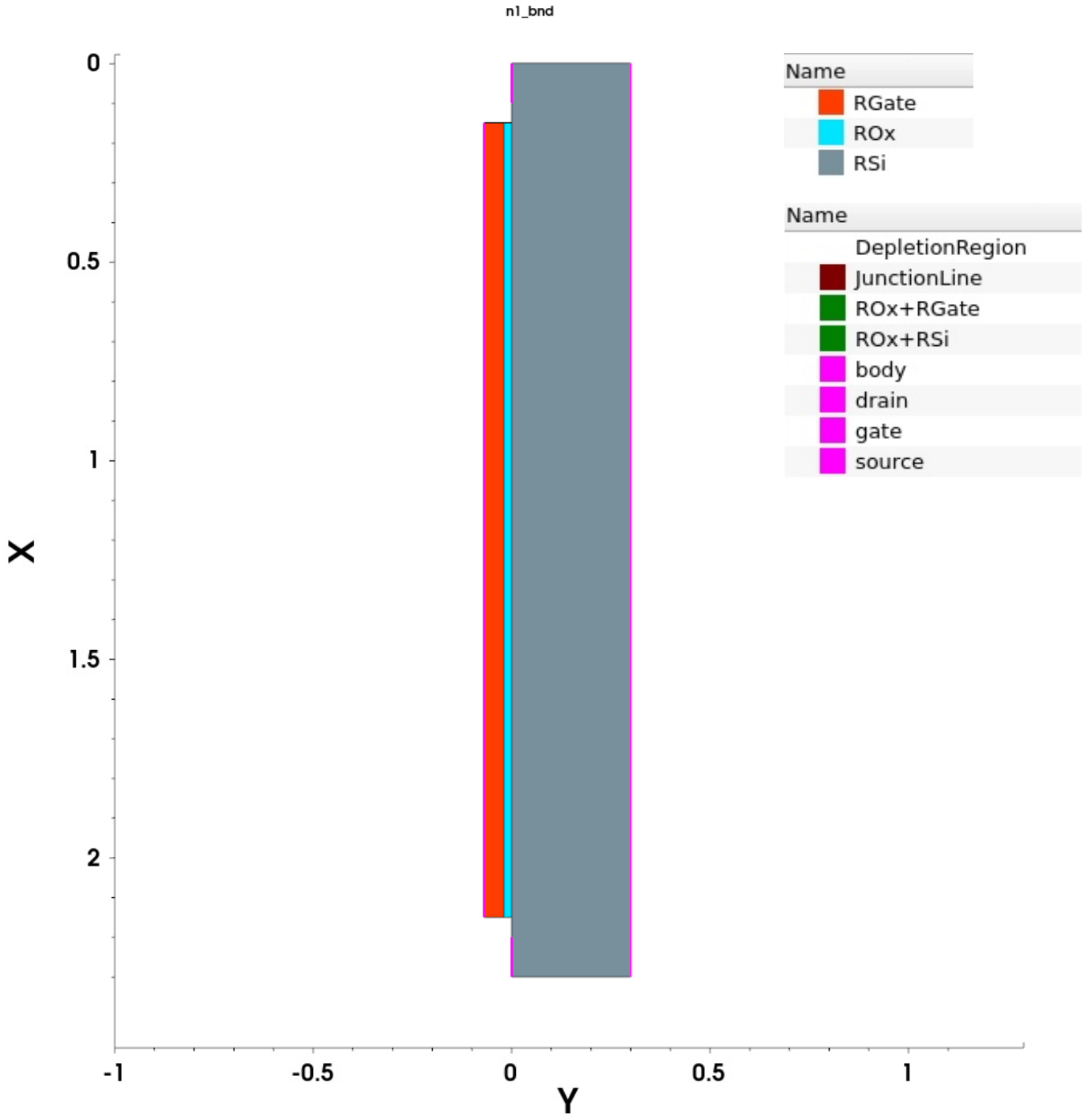
ECE 441: Physics and Modeling of Semiconductor Devices

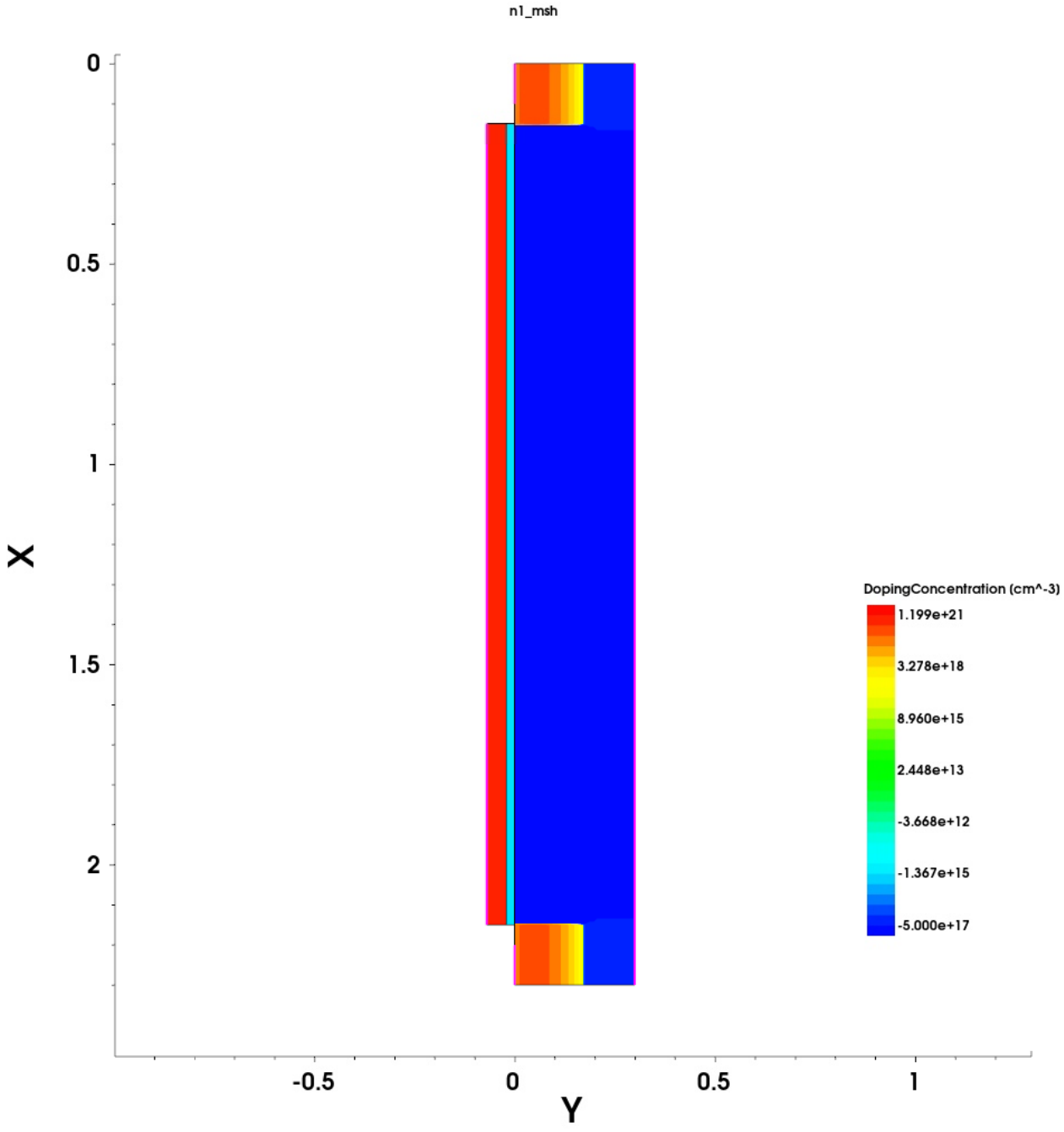
TCAD Project

1. Simulate long-channel nMOSFET

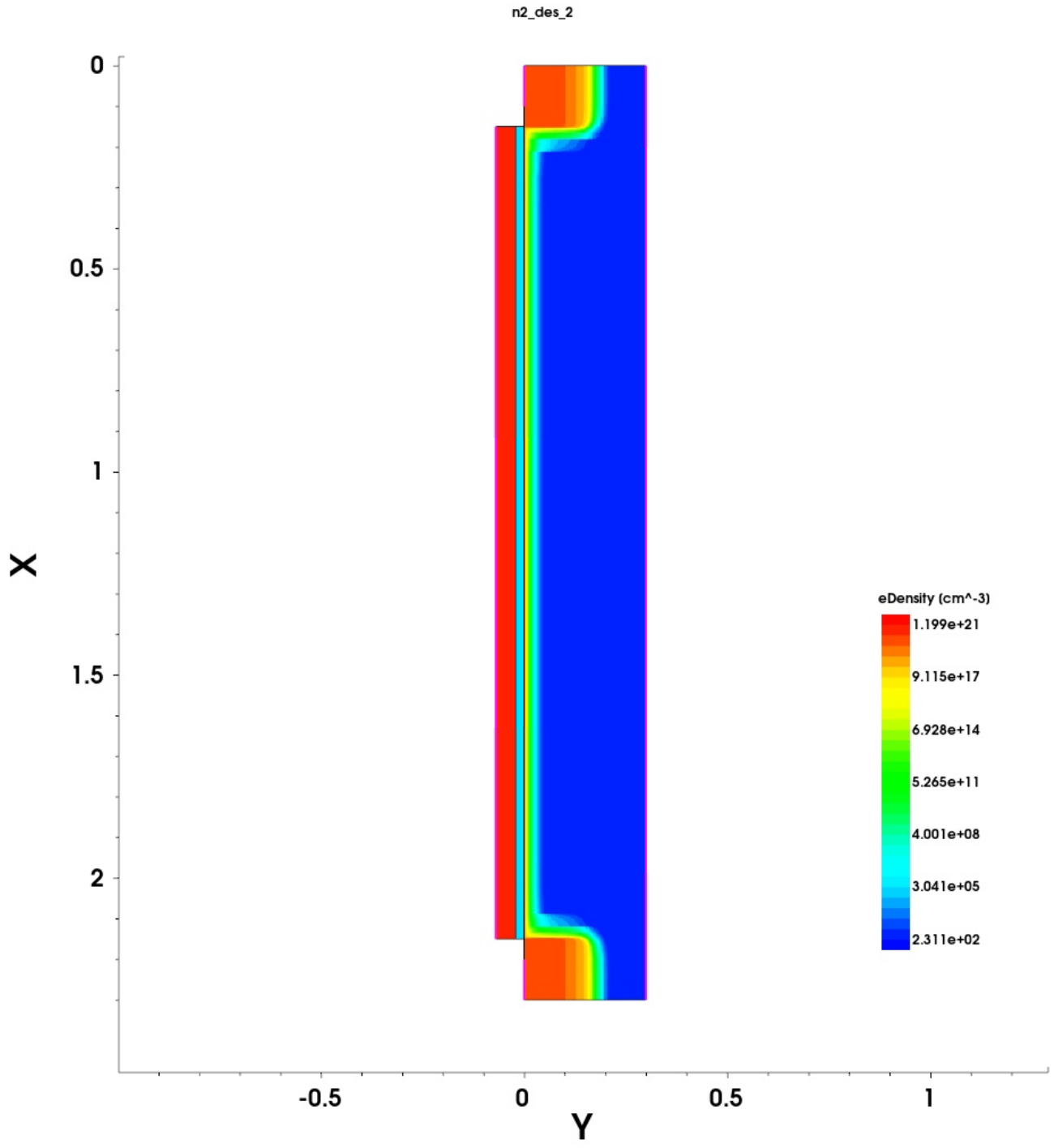
(i) Device Structure



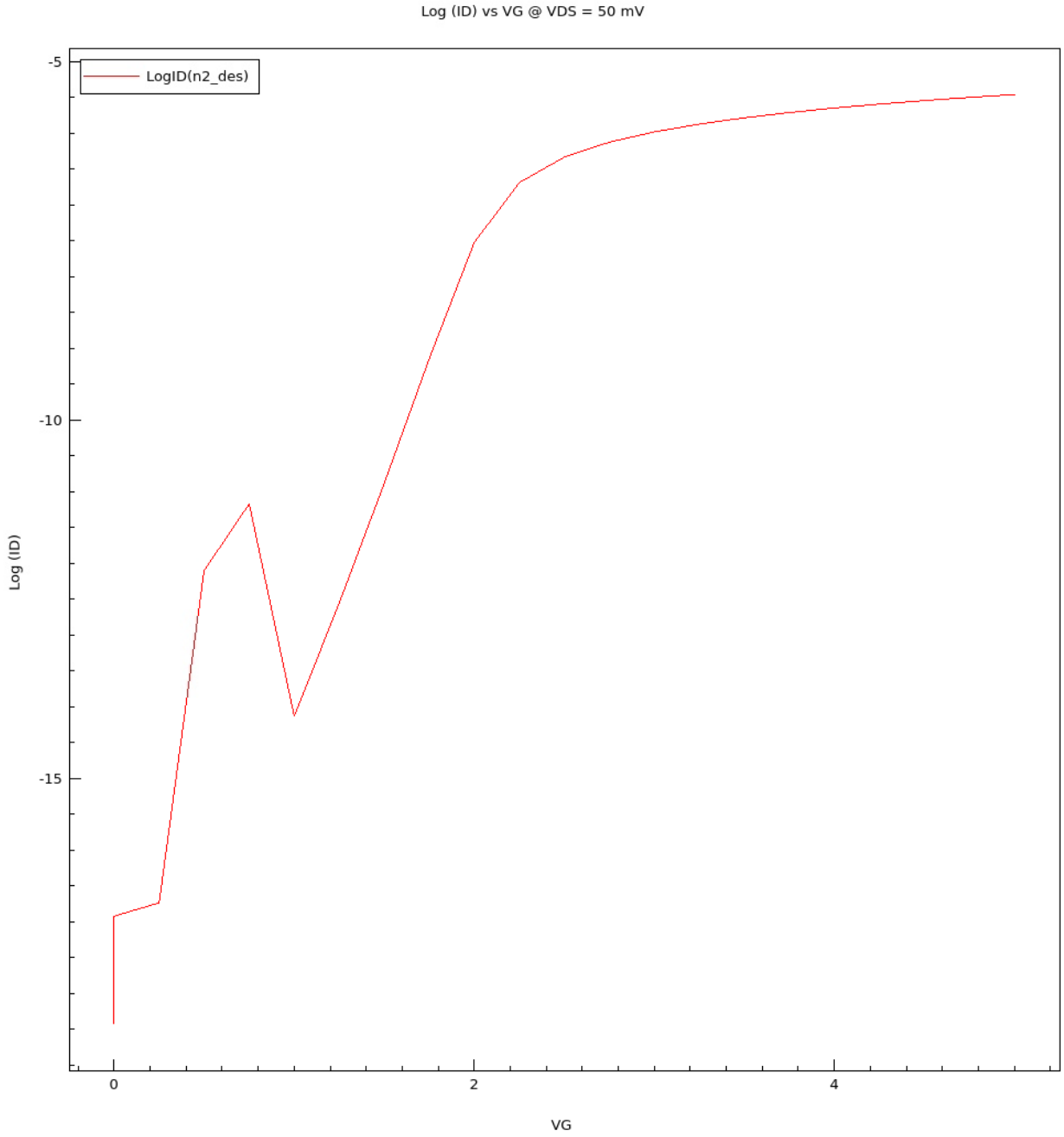
Doping Profile



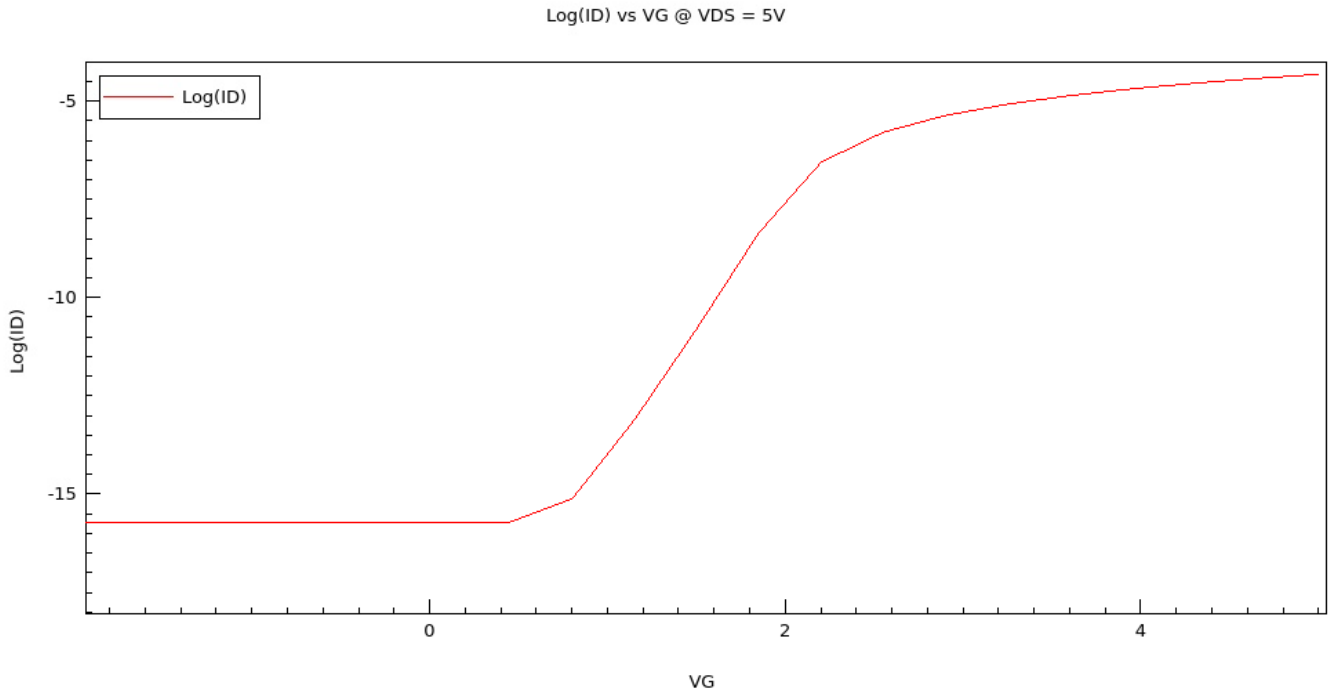
(ii) Electro density (inversion)



(iii) Log (ID)-VG @ VDS = 50 mV and VDD, extract the threshold voltages (V_{T_lin} and V_{T_sat}) at constant off current I_{off} = 1 x 10^{-7} A/um



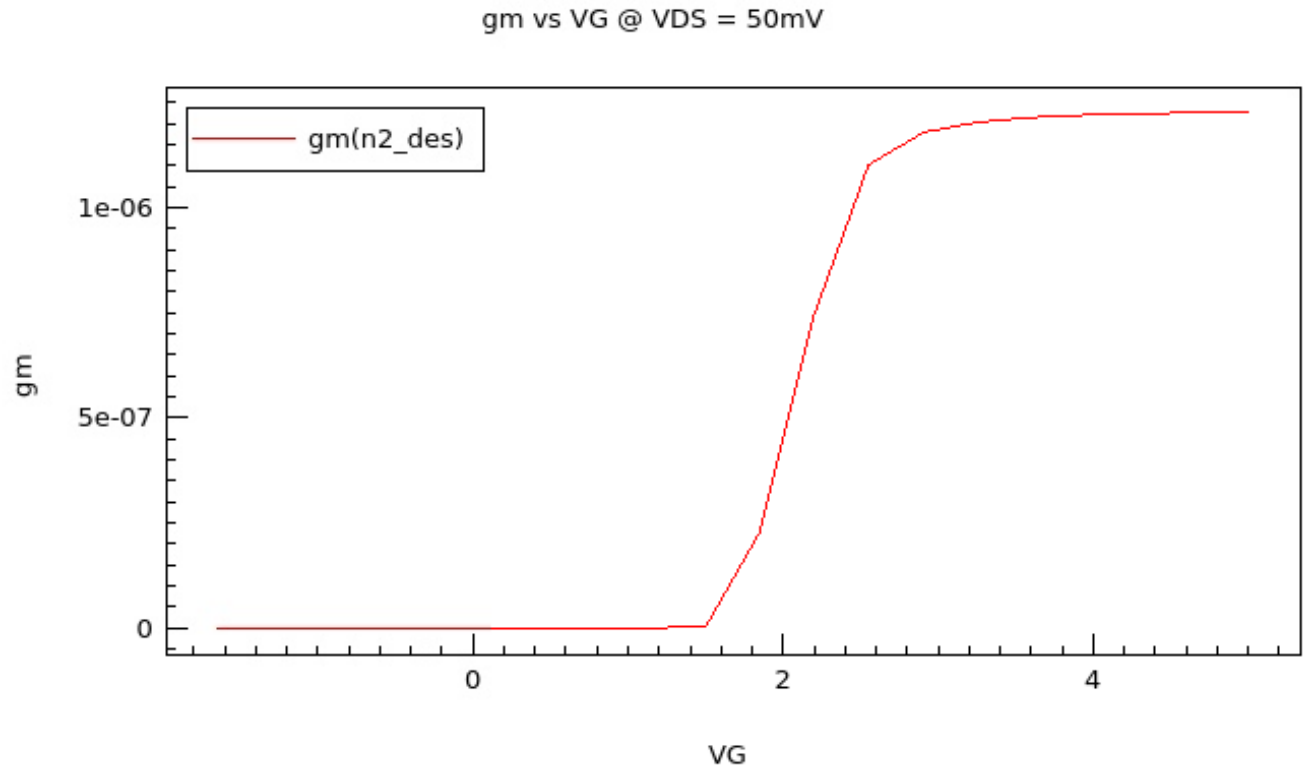
V_{T_lin} = 2.1547 V



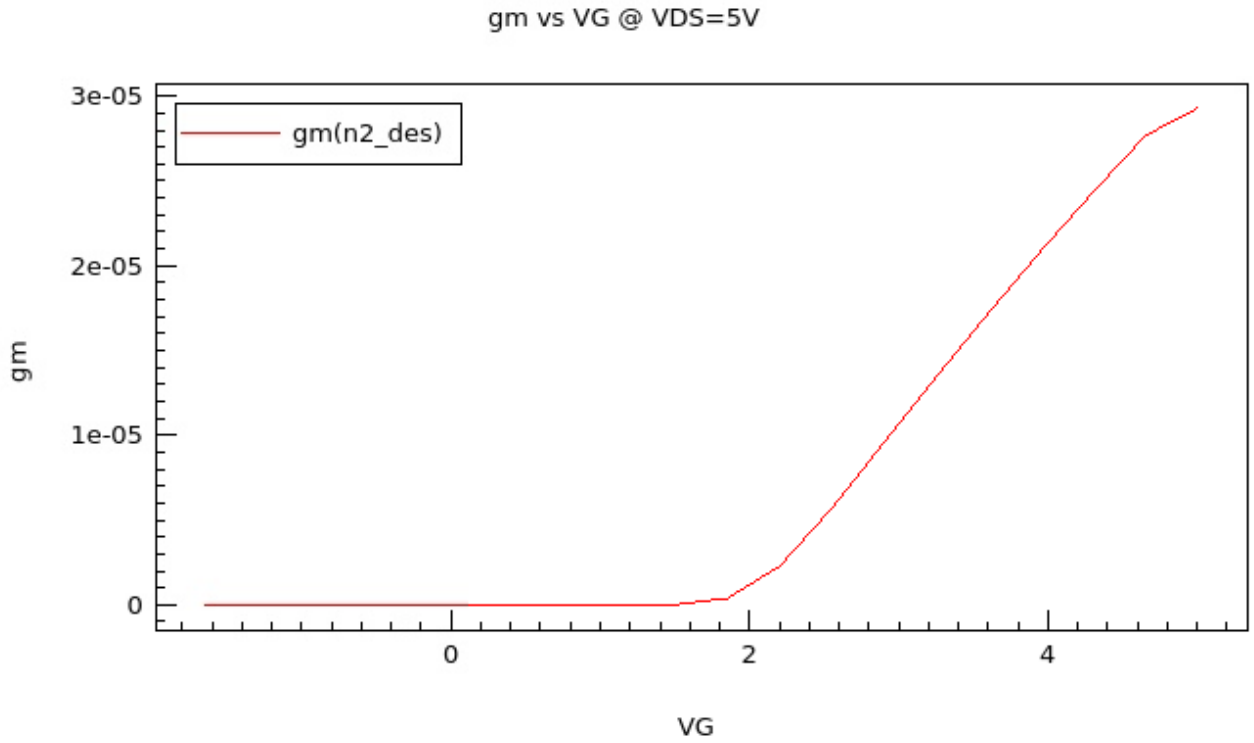
V_{T_sat} = 2.1126 V

(iv) Transconductance gm as a function of gate voltage @ VDS = 50mV and VDD

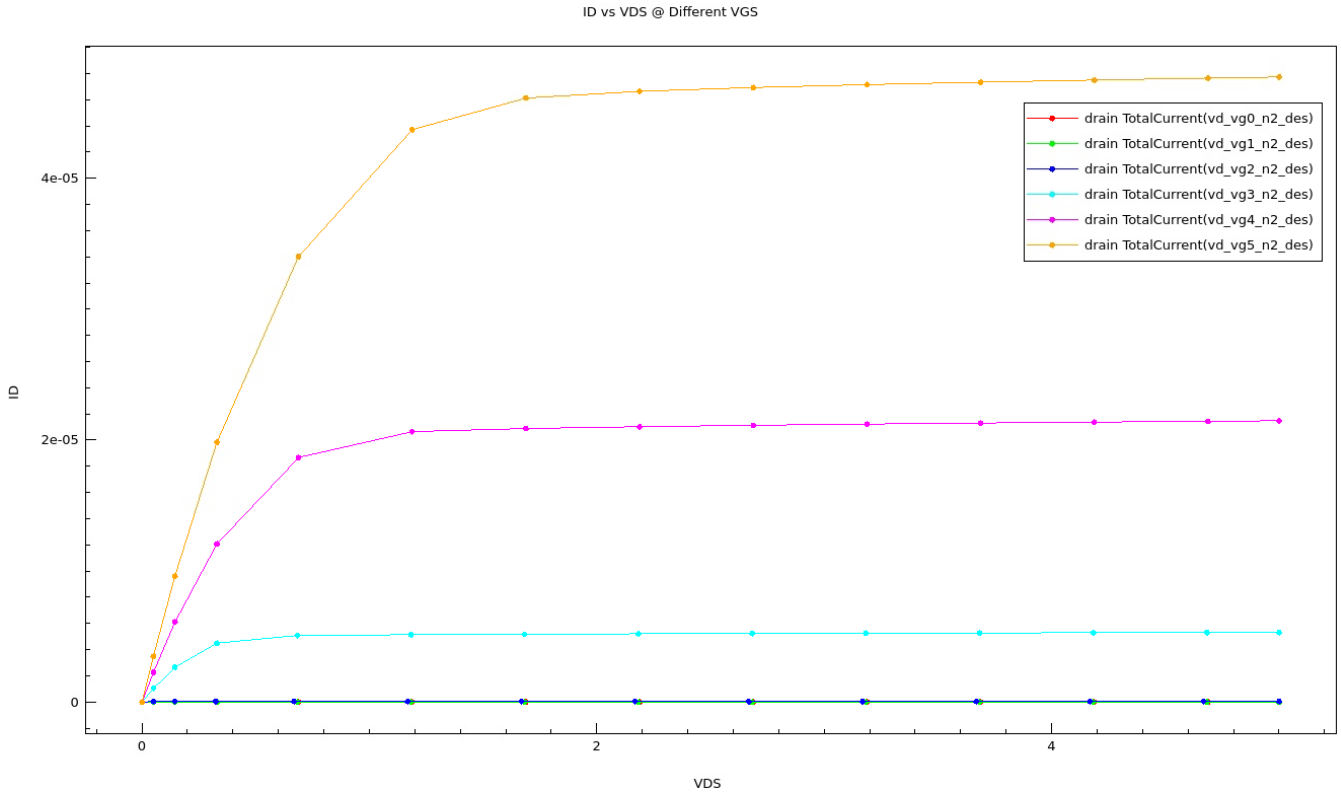
(a) VDS = 50mV



(b) VDS = VDD = 5V



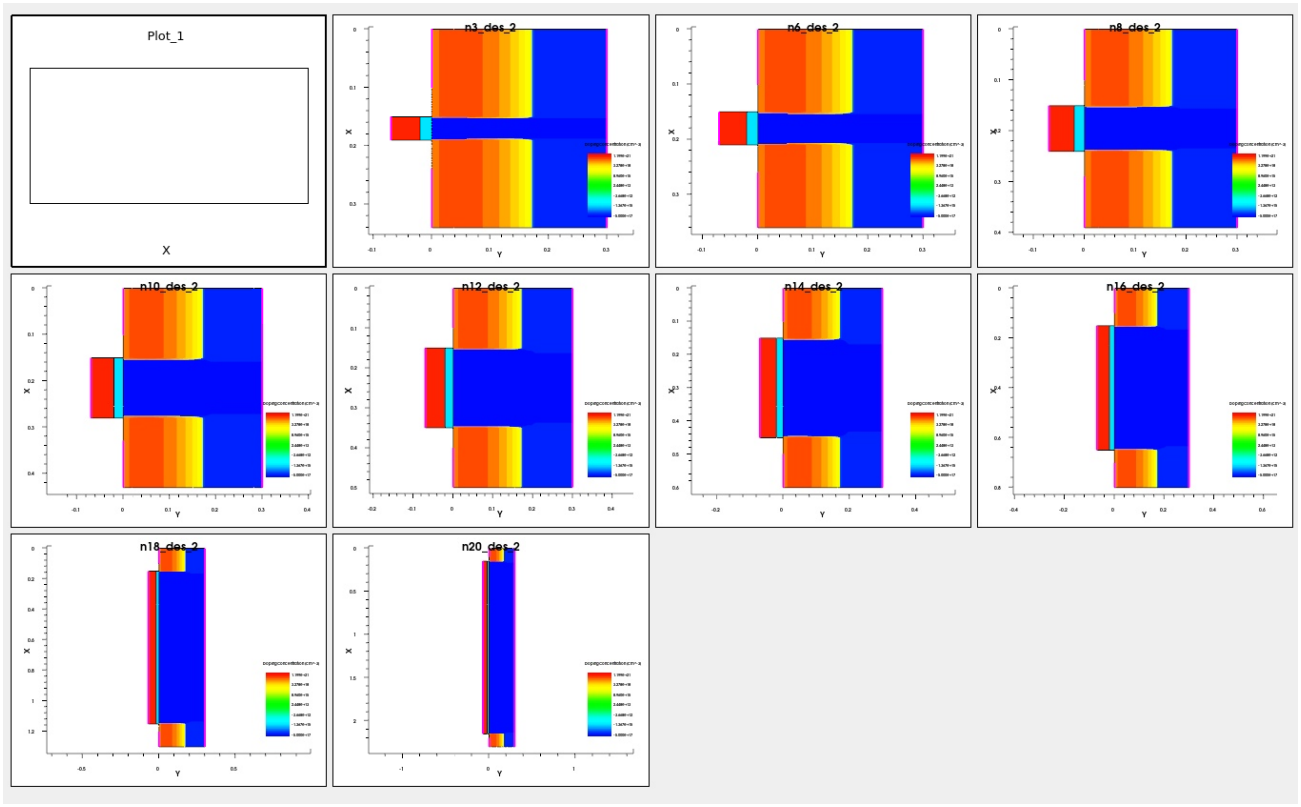
(v) ID vs VD for different VGS values between zero and VDD



2. Simulate short-channel effect

(i) V_{T_lin} and V_{T_sat} as a function of gate length LGATE.

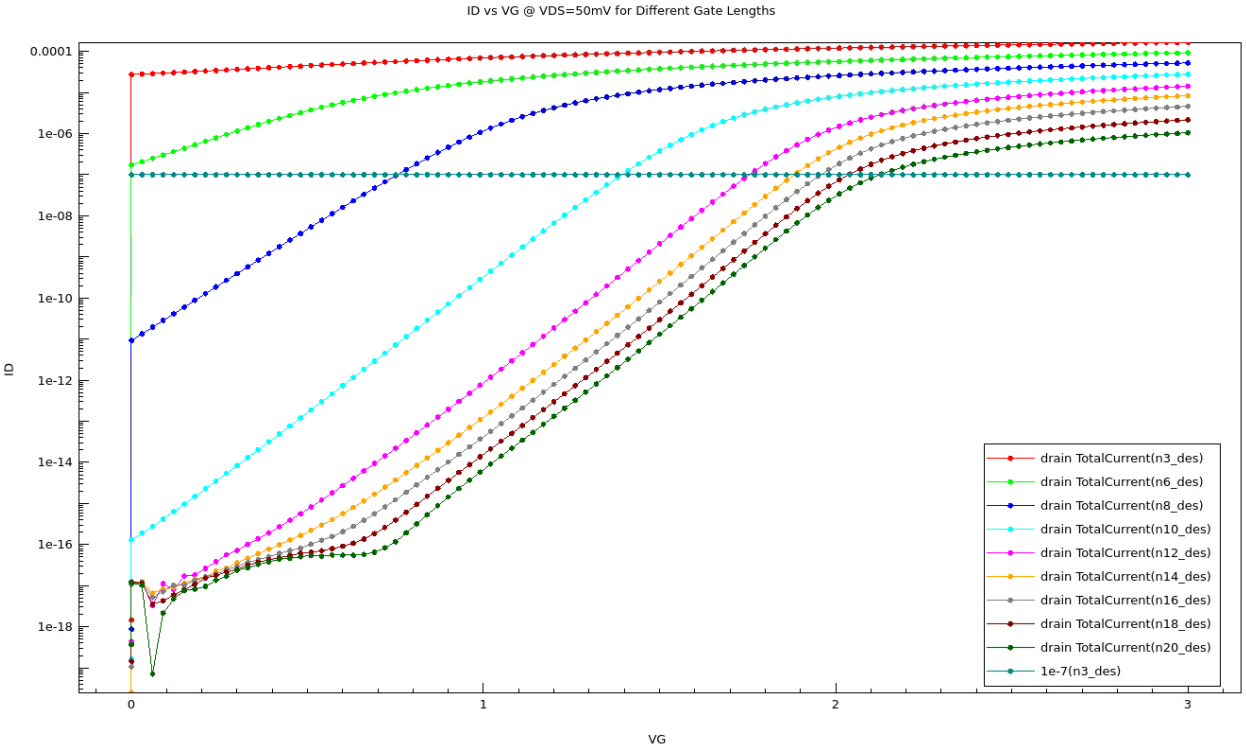
(a) Doping Profiles



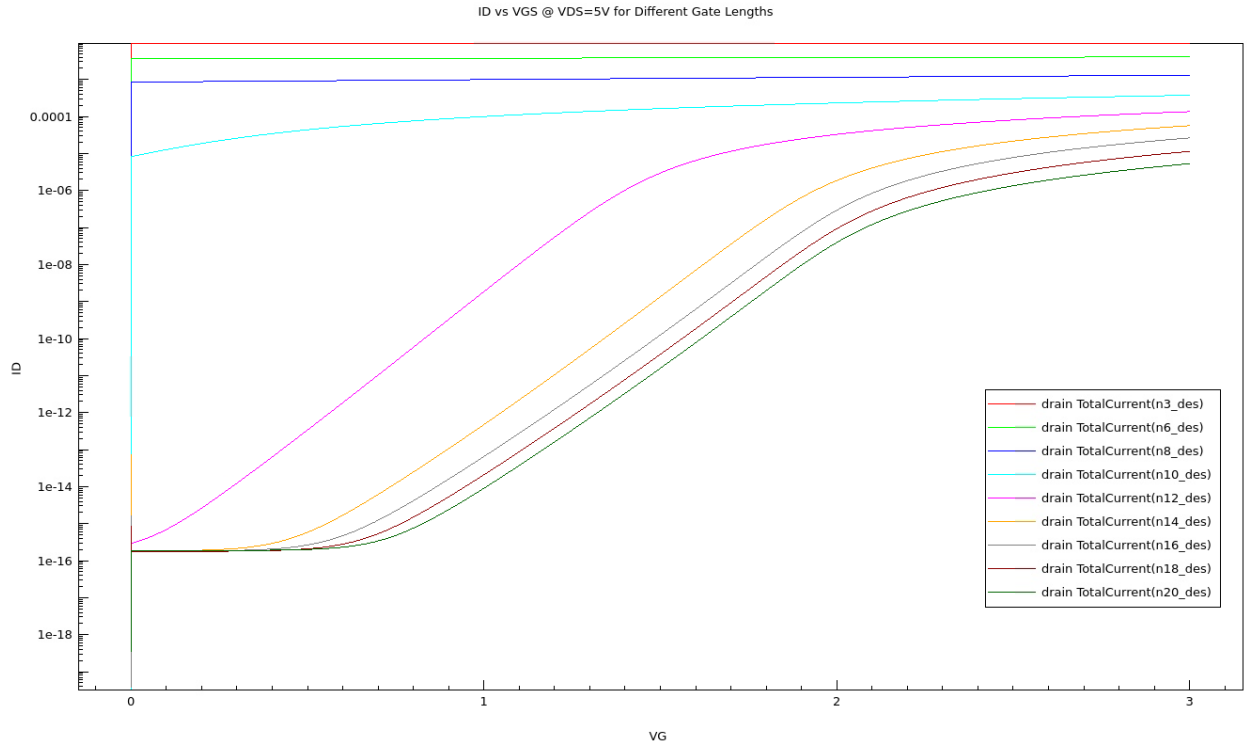
(b)

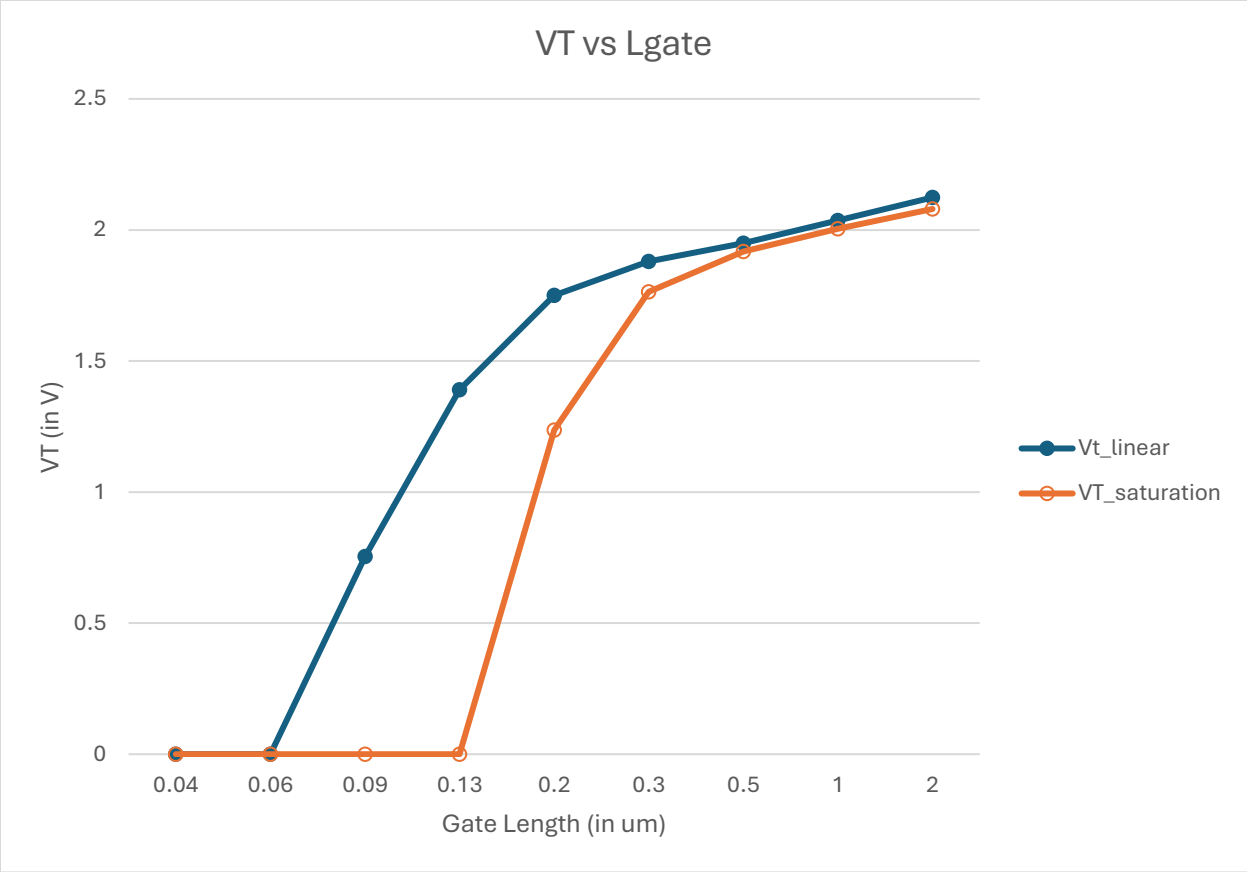
Node	Lgate (in um)	V_{T_lin}	V_{T_sat}
n3_des	0.04	0	0
n6_des	0.06	0	0
n8_des	0.09	0.754	0
n10_des	0.13	1.39	0
n12_des	0.2	1.75	1.236
n14_des	0.3	1.88	1.764
n16_des	0.5	1.95	1.918
n18_des	1	2.036	2.004
n20_des	2	2.124	2.08

V_{T_lin}


ID vs VG @ VDS=50mV for Different Gate Lengths
ID
VG
0.0001
1e-06
1e-08
1e-10
1e-12
1e-14
1e-16
1e-18
0
1
2
3
drain TotalCurrent(n3_des)
drain TotalCurrent(n6_des)
drain TotalCurrent(n8_des)
drain TotalCurrent(n10_des)
drain TotalCurrent(n12_des)
drain TotalCurrent(n14_des)
drain TotalCurrent(n16_des)
drain TotalCurrent(n18_des)
drain TotalCurrent(n20_des)
1e-7(n3_des)

V_{T_sat}


ID vs VGS @ VDS=5V for Different Gate Lengths
ID
VG
0.0001
1e-06
1e-08
1e-10
1e-12
1e-14
1e-16
1e-18
0
1
2
3
drain TotalCurrent(n3_des)
drain TotalCurrent(n6_des)
drain TotalCurrent(n8_des)
drain TotalCurrent(n10_des)
drain TotalCurrent(n12_des)
drain TotalCurrent(n14_des)
drain TotalCurrent(n16_des)
drain TotalCurrent(n18_des)
drain TotalCurrent(n20_des)

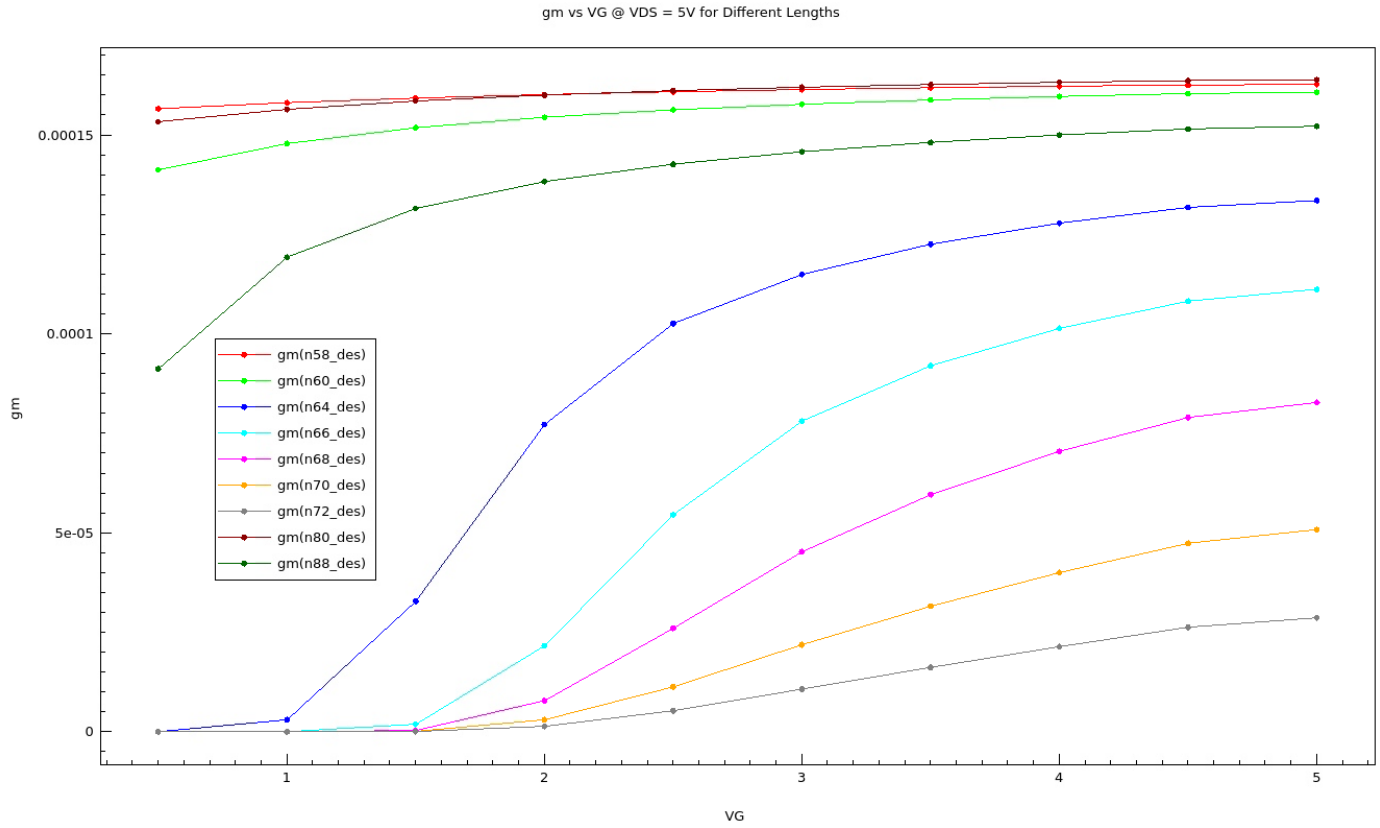


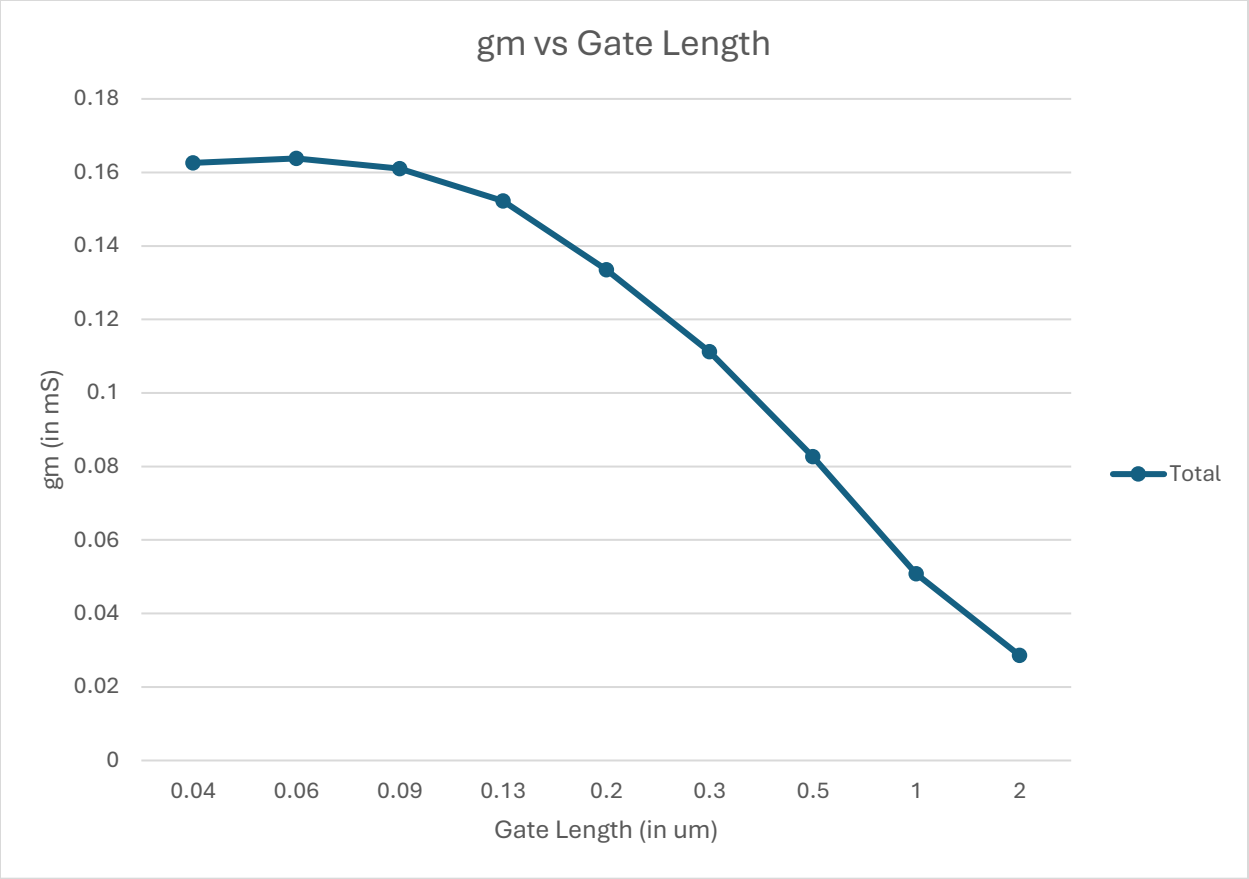
Observation: Yes, we do observe short-channel effect. As LGATE decreases we can see a roll off in threshold voltage and increase in DIBL. Threshold measured at high VDS (V_{T_sat}) is considerably lower than at low VDS, especially as LGATE decreases more.

Conclusion: The gate controls the channel potential by capacitive coupling through the oxide. For long channels the gate dominates. For short channels the source/drain depletion regions and drain potential penetrate the channel and perturb the barrier that the gate is trying to form. The gate loses electrostatic control as channel length decreases. Therefore, at high VDS, the required VG for a given current is lower.

(ii) Max transconductance g_{m_max} as a function of L_{GATE} . Here VDS = 5 V

Node	Lgate (in um)	V_{T_lin}	V_{T_sat}	gmmax
n58_des	0.04	0	0	0.1626
n80_des	0.06	0	0	0.1638
n60_des	0.09	0.754	0	0.161
n88_des	0.13	1.39	0	0.1522
n64_des	0.2	1.75	1.236	0.1335
n66_des	0.3	1.88	1.764	0.1112
n68_des	0.5	1.95	1.918	0.0827
n70_des	1	2.036	2.004	0.0508
n72_des	2	2.124	2.08	0.0286



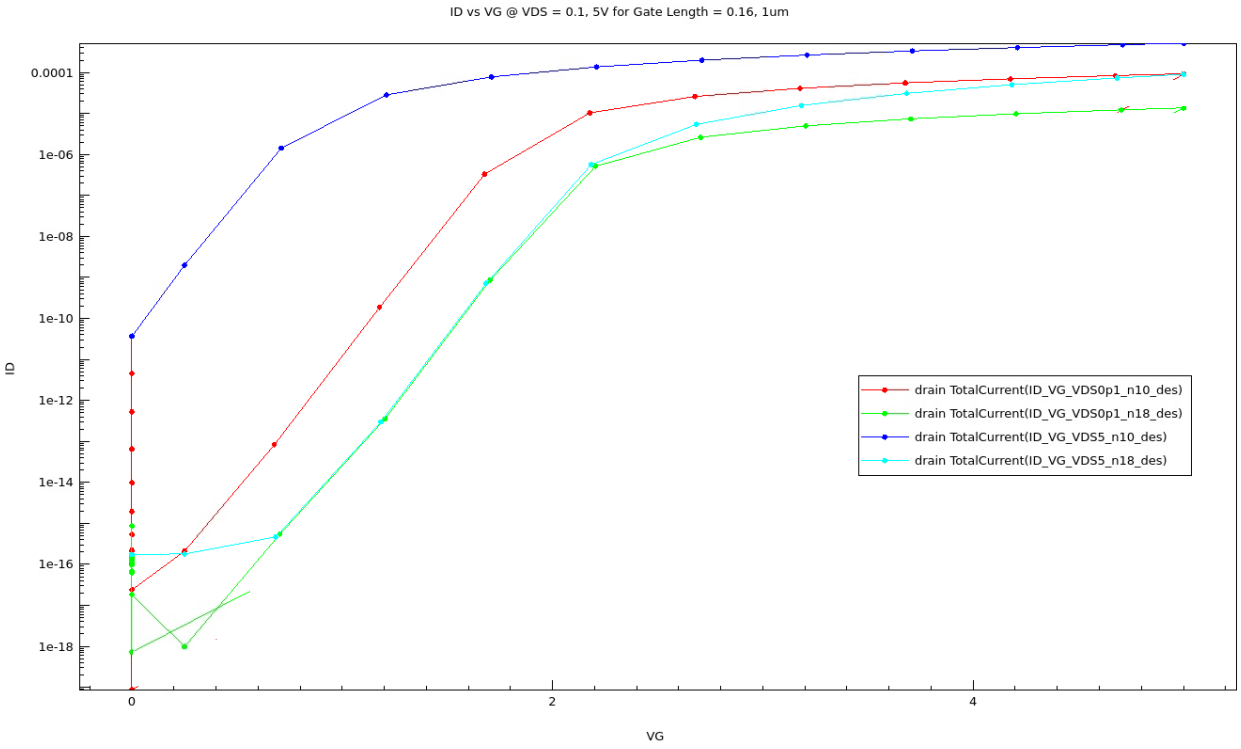


Observation: Increase in g_{m_max} as L reduces from 2 µm down to a few hundred nm, then flattening or roll-off for the shortest devices (~60 um).

Conclusion: For moderately long to moderate channel lengths, g_{m_max} increases as L decreases (because gm $\propto \frac{W}{L}$ for the strong-inversion, velocity-unsaturated regime).

For very short L, g_{m_max} will saturate and decrease due to velocity saturation. It limits the carrier velocity, so the drain current stops scaling as $1/L$. At very short L, there is also mobility degradation which reduce mobility and reduces g_{m_max}.

(iii) plot log (ID) -VG with various drain voltages (from 0.1V to VDD) and extract drain-induced-barrier-lowering (DIBL)



DIBL Calculation

Formula:

$$\text{DIBL} = \frac{V_T(V_{D,\text{low}}) - V_T(V_{D,\text{high}})}{V_{D,\text{high}} - V_{D,\text{low}}}$$

Here: $V_{D,\text{low}} = 0.1$ V, $V_{D,\text{high}} = 5$ V

Denominator = $5 - 0.1 = 4.9$ V

For L = 1 µm

$$V_T(0.1V) = 2.074$$
$$V_T(5V) = 2.052$$
$$\text{DIBL}_{1\mu m} = \frac{2.074 - 2.052}{4.9} = \frac{0.022}{4.9} = 0.00449$$
$$\text{DIBL}_{1\mu m} \approx 4.5\ \text{mV/V}$$

For L = 0.16 µm

$$V_T(0.1V) = 1.595$$

$$V_T(5V) = 0.523$$

$$\text{DIBL}_{0.16\mu m} = \frac{1.595 - 0.523}{4.9} = \frac{1.072}{4.9} = 0.2188$$

$$\text{DIBL}_{0.16\mu m} \approx 219\ \text{mV/V}$$

Channel Length	DIBL (mV/V)
1 µm	**4.5 mV/V**
0.16 µm	**219 mV/V**

DIBL much larger for the 0.16 µm device. Short-channel effects dominate in the 0.16 µm transistor. The depletion regions from source and drain get very close. Drain electric field can penetrate deep toward the channel. The source-channel barrier height is reduced when drain voltage increases. This reduces V_T significantly and leads to large DIBL.

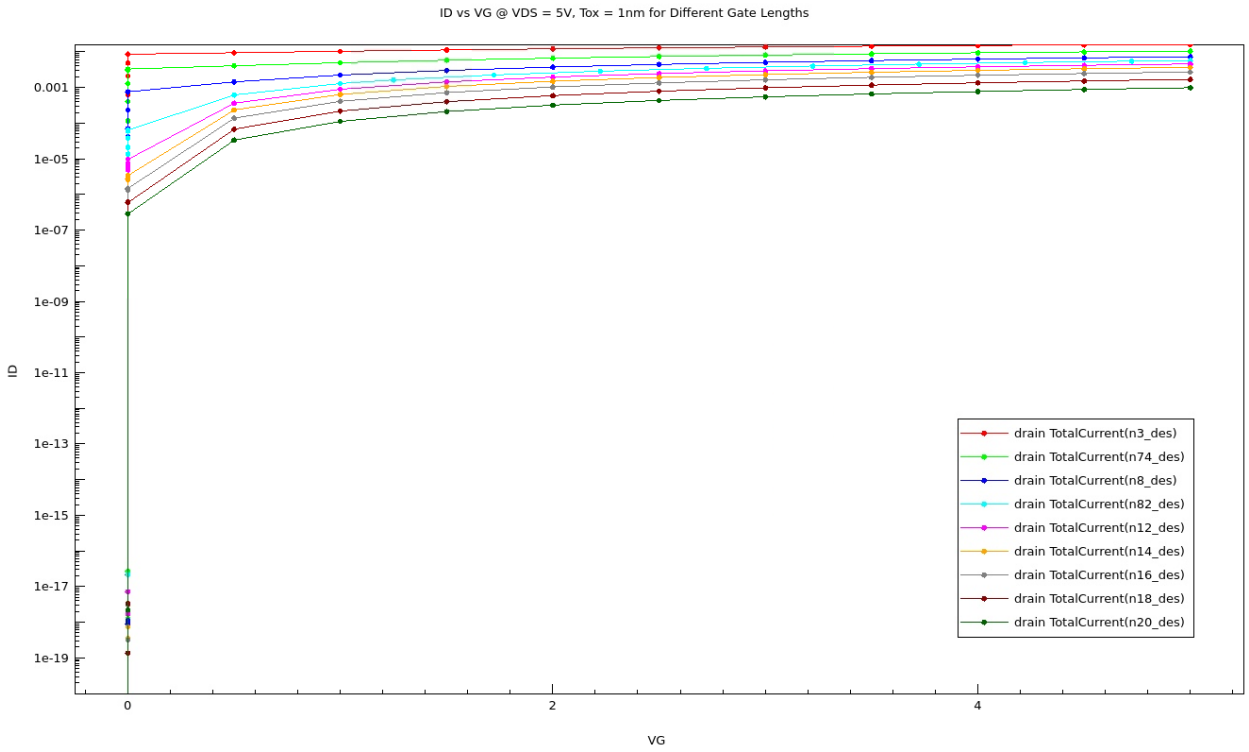
For the 1 µm device, the drain field is well screened. Channel is long enough so the potential barrier near the source is almost untouched. V_T barely changes and the DIBL is small.

3. Investigate the impact of process parameters on short-channel effect

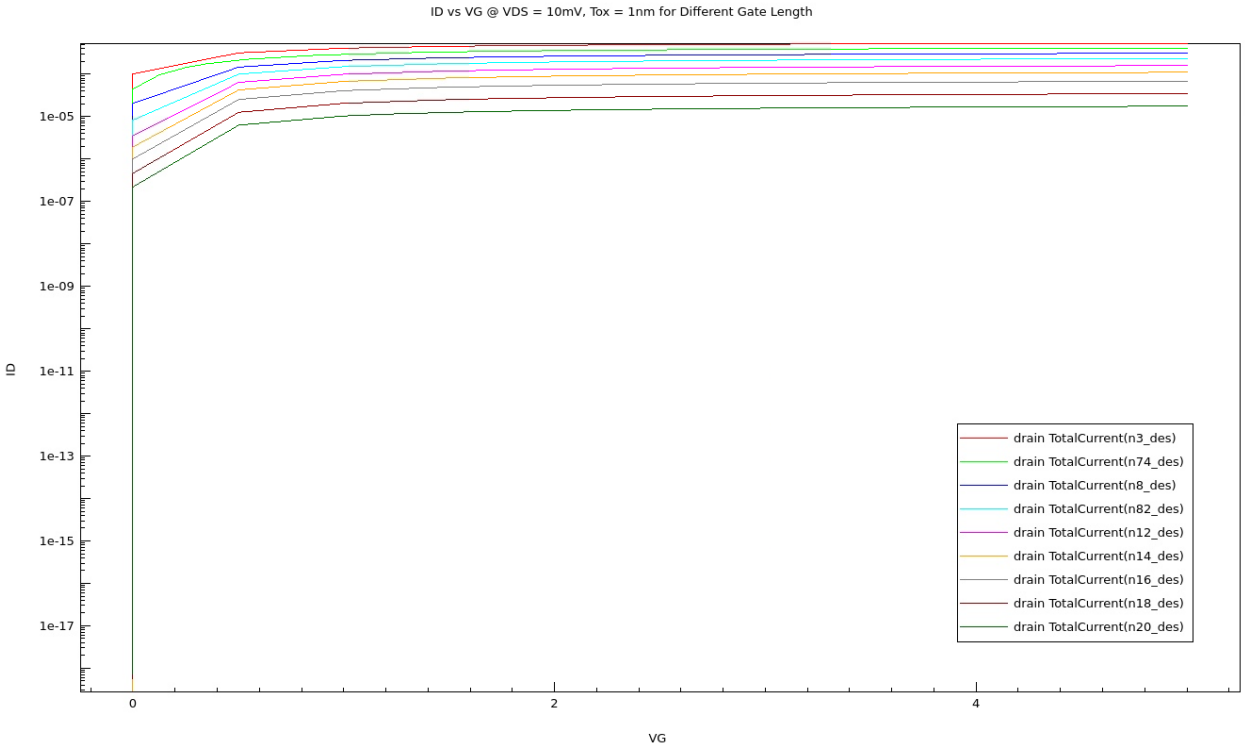
(a) Vary the gate oxide thickness (20nm, 10nm, 5 nm and 1nm) and perform the simulation of the NMOSFET with various channel length

(i) Tox = 1nm

V_{T_sat}

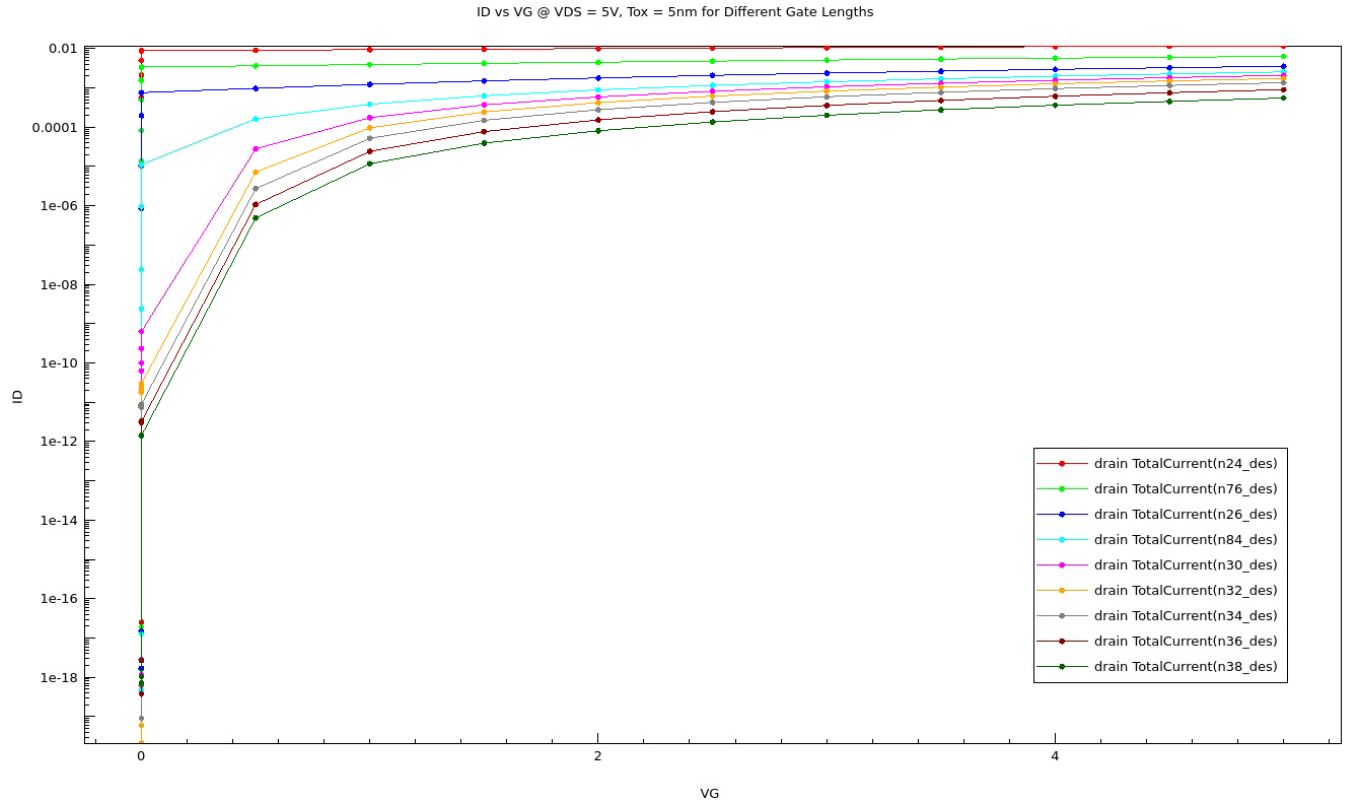


V_{T_lin}

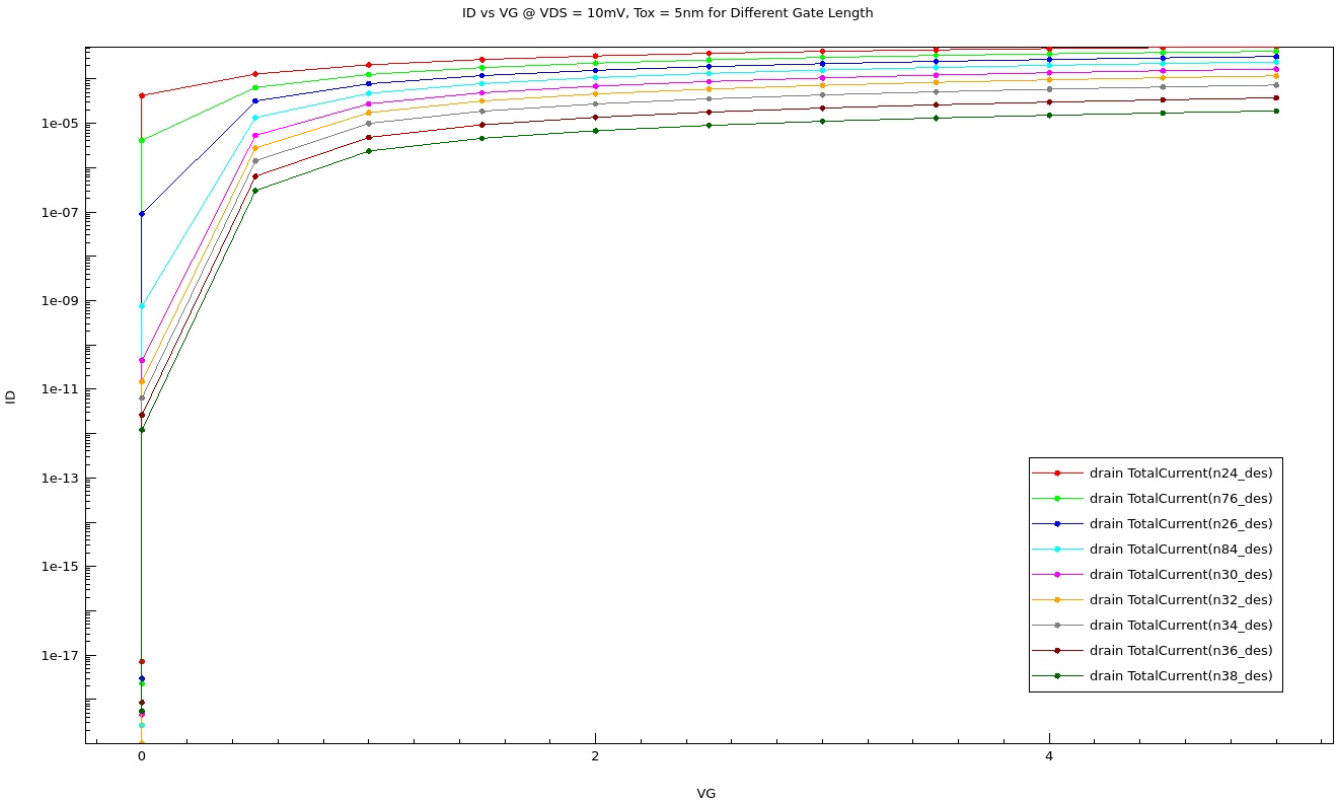


(ii) Tox = 5nm

V_{T_sat}

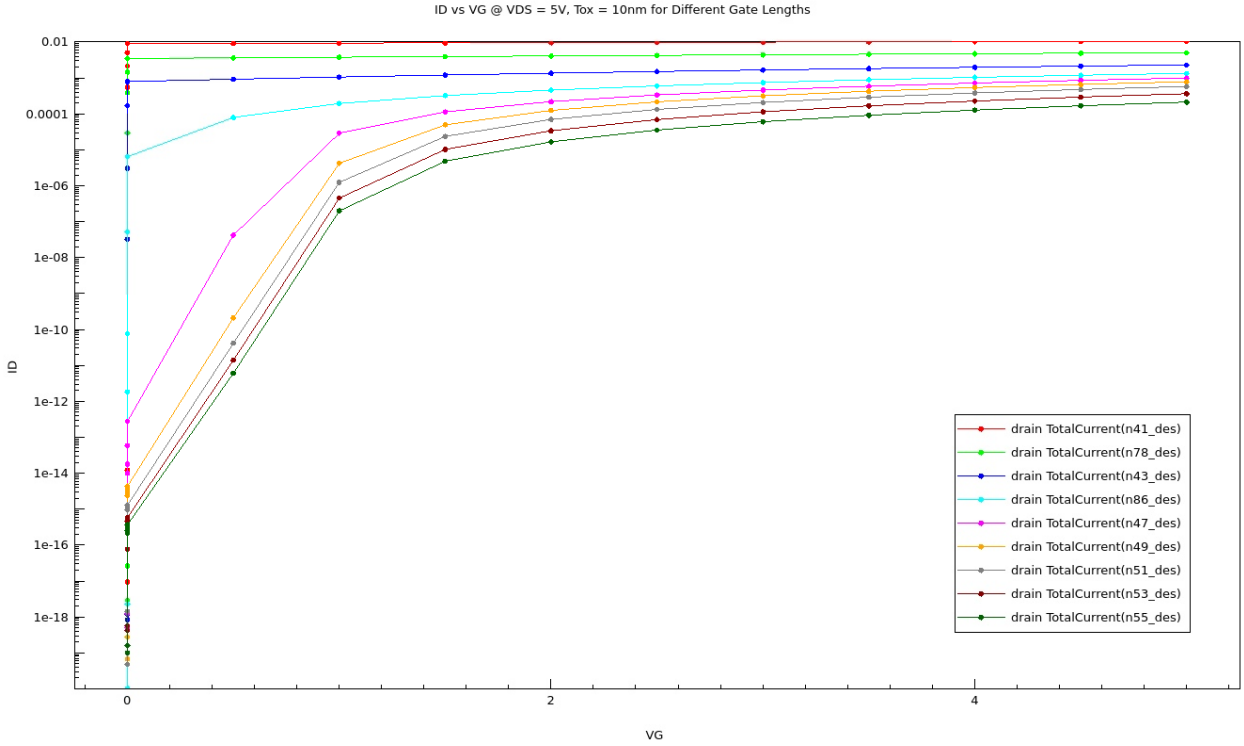

ID vs VG @ VDS = 5V, Tox = 5nm for Different Gate Lengths
ID
VG
0.01
0.0001
1e-06
1e-08
1e-10
1e-12
1e-14
1e-16
1e-18
0
2
4
drain TotalCurrent(n24_des)
drain TotalCurrent(n76_des)
drain TotalCurrent(n26_des)
drain TotalCurrent(n84_des)
drain TotalCurrent(n30_des)
drain TotalCurrent(n32_des)
drain TotalCurrent(n34_des)
drain TotalCurrent(n36_des)
drain TotalCurrent(n38_des)

V_{T_lin}

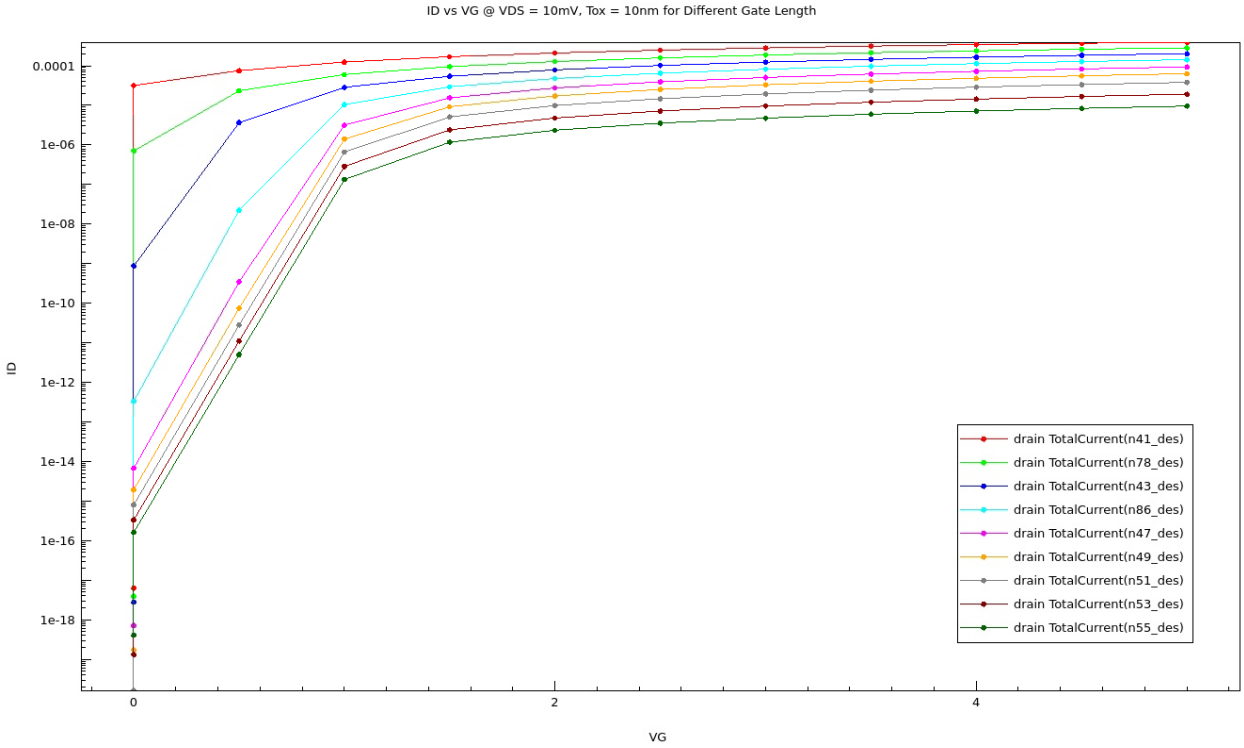

ID vs VG @ VDS = 10mV, Tox = 5nm for Different Gate Length
ID
VG
1e-05
1e-07
1e-09
1e-11
1e-13
1e-15
1e-17
0
2
4
drain TotalCurrent(n24_des)
drain TotalCurrent(n76_des)
drain TotalCurrent(n26_des)
drain TotalCurrent(n84_des)
drain TotalCurrent(n30_des)
drain TotalCurrent(n32_des)
drain TotalCurrent(n34_des)
drain TotalCurrent(n36_des)
drain TotalCurrent(n38_des)

(iii) Tox = 10nm

V_{T_sat}

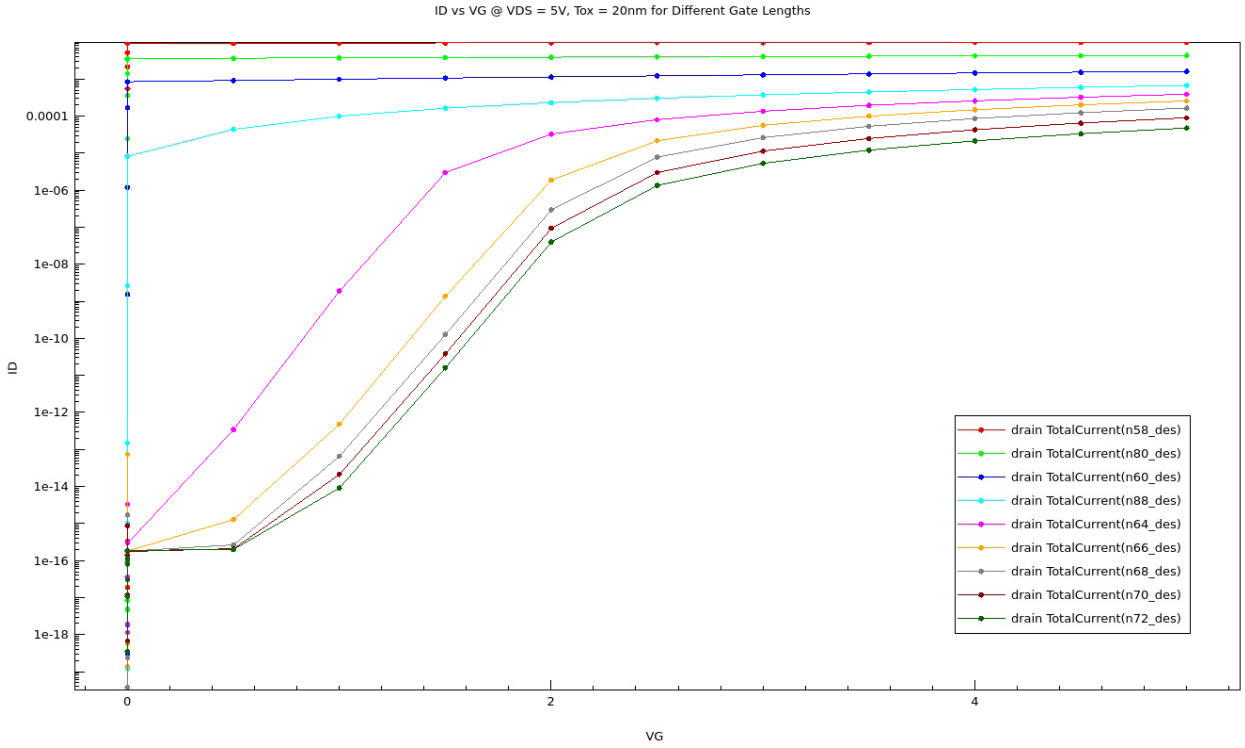


V_{T_lin}

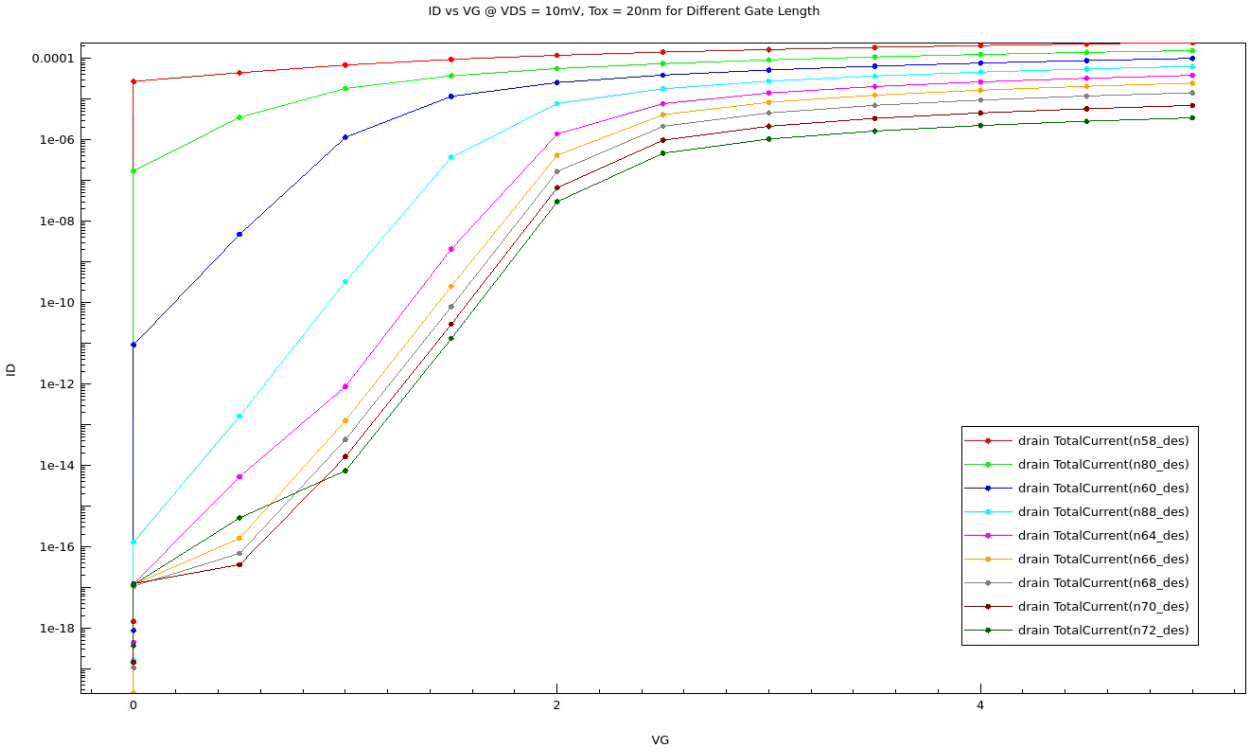


(iv) Tox = 20nm

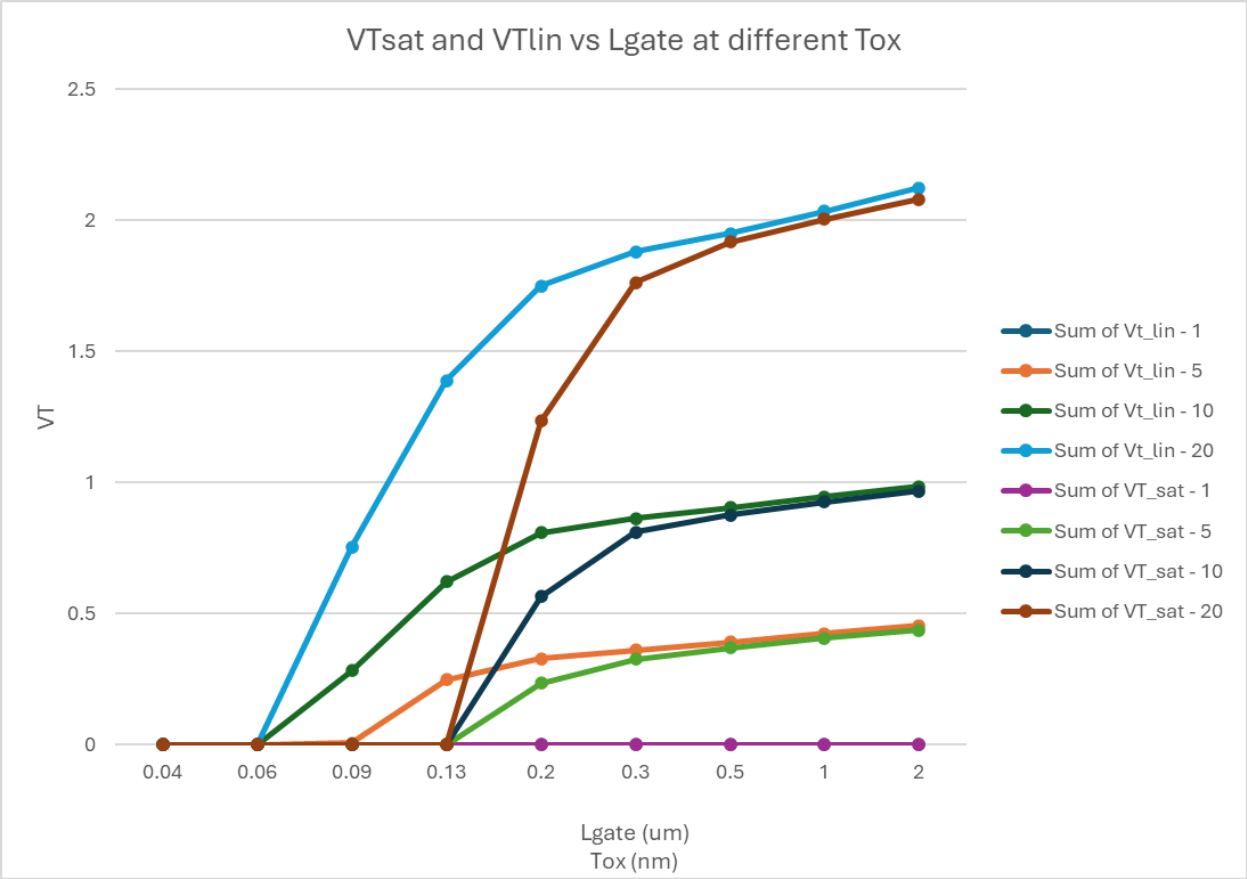
V_{T_sat}



V_{T_lin}



Node	Lgate (in um)	Tox (in nm)	V_{T_lin}	V_{T_sat}
n3	0.04	1	0	0
n74	0.06	1	0	0
n8	0.09	1	0	0
n82	0.13	1	0	0
n12	0.2	1	0	0
n14	0.3	1	0	0
n16	0.5	1	0	0
n18	1	1	0	0
n20	2	1	0	0
n24	0.04	5	0	0
n76	0.06	5	0	0
n26	0.09	5	0.0076	0
n84	0.13	5	0.249	0
n30	0.2	5	0.329	0.236
n32	0.3	5	0.362	0.327
n34	0.5	5	0.392	0.369
n36	1	5	0.425	0.407
n38	2	5	0.455	0.437
n41	0.04	10	0	0
n78	0.06	10	0	0
n43	0.09	10	0.283	0
n86	0.13	10	0.621	0
m47	0.2	10	0.809	0.565
m49	0.3	10	0.863	0.811
n51	0.5	10	0.904	0.877
n53	1	10	0.947	0.927
n55	2	10	0.985	0.967
n58	0.04	20	0	0
n80	0.06	20	0	0
n60	0.09	20	0.754	0
n88	0.13	20	1.39	0
n64	0.2	20	1.75	1.236
n66	0.3	20	1.88	1.764
n68	0.5	20	1.95	1.918
n70	1	20	2.036	2.004
n72	2	20	2.124	2.08



Observation: Thinner oxide has a stronger gate control which reduces V_T roll-off and reduced DIBL for a given L. The plot of V_T vs L for different t_{ox} shows that thinner oxides keep V_T more constant down to shorter L.

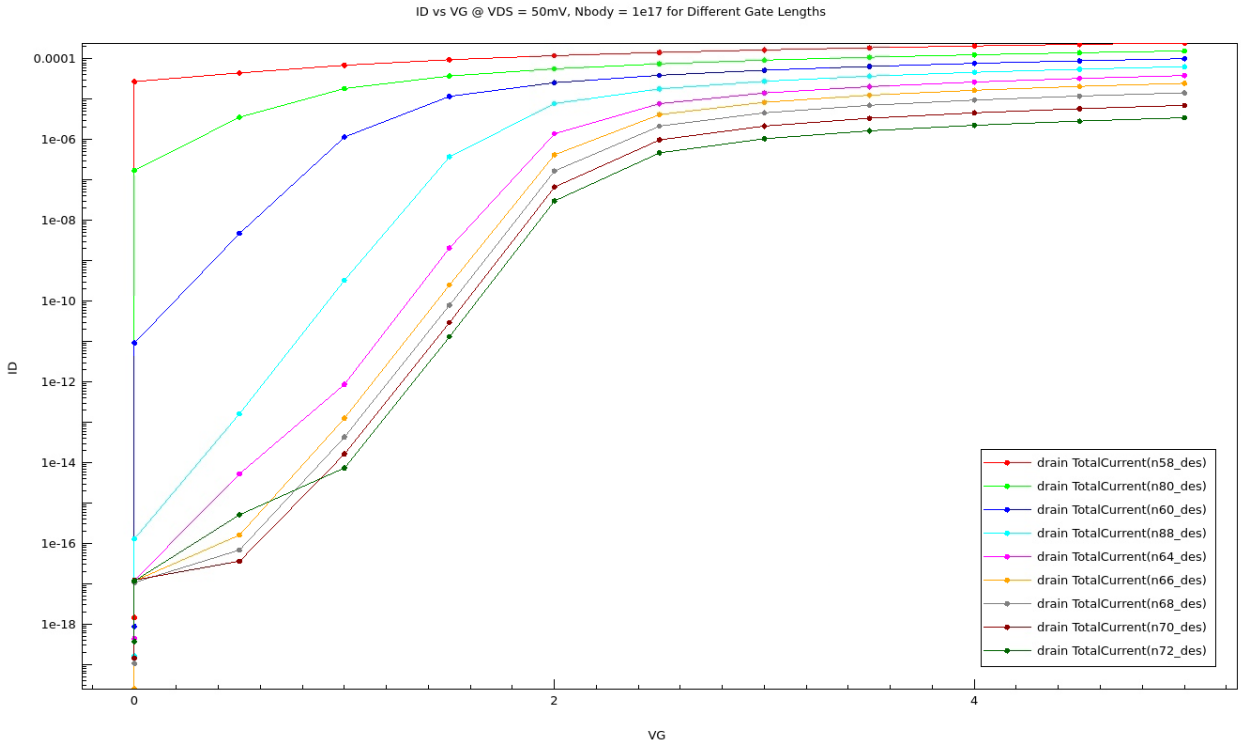
Conclusion: The gate's electrostatic control over channel potential is determined by the oxide capacitance $C_{ox} = \varepsilon_{ox}/t_{ox}$. A thinner oxide increases C_{ox}, so the gate dominates the electrostatics rather than the drain.

Yes, oxide scaling is an effective approach to suppress short channel effect upto a certain limit. It increases gate capacitance and improves gate electrostatic control. Reducing it too much (~1nm) will give a V_T below 0 and will lead to always on which would be bad for leakage. Therefore, practical limitations (leakage, reliability, quantum effects) limit how far you can scale SiO_2. In practice, high-κ dielectrics.

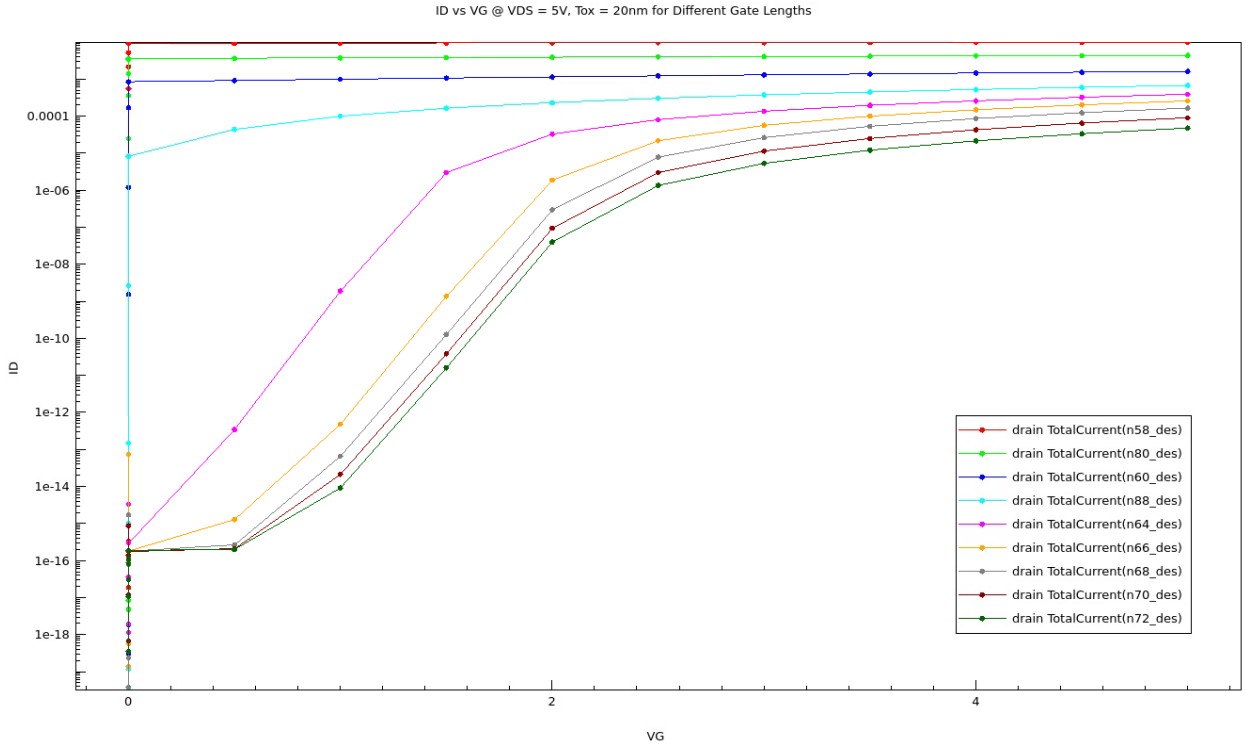
(b) Vary the substrate doping centration (Na = 5 x 10^{17} cm^{-3} and 5 x 10^{18} cm^{-3}) and perform the simulation of the NMOSFETs with various channel lengths.

(i) Nbody = 1e17

V_{T_lin}

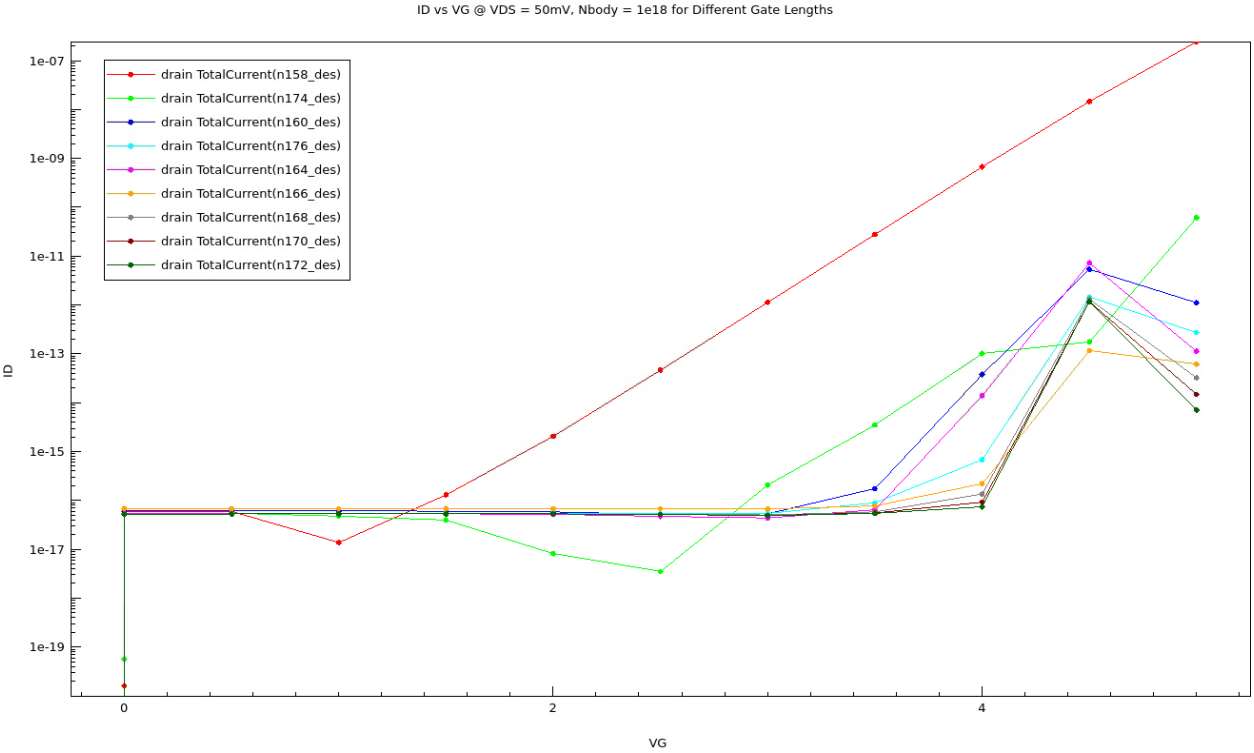


V_{T_sat}

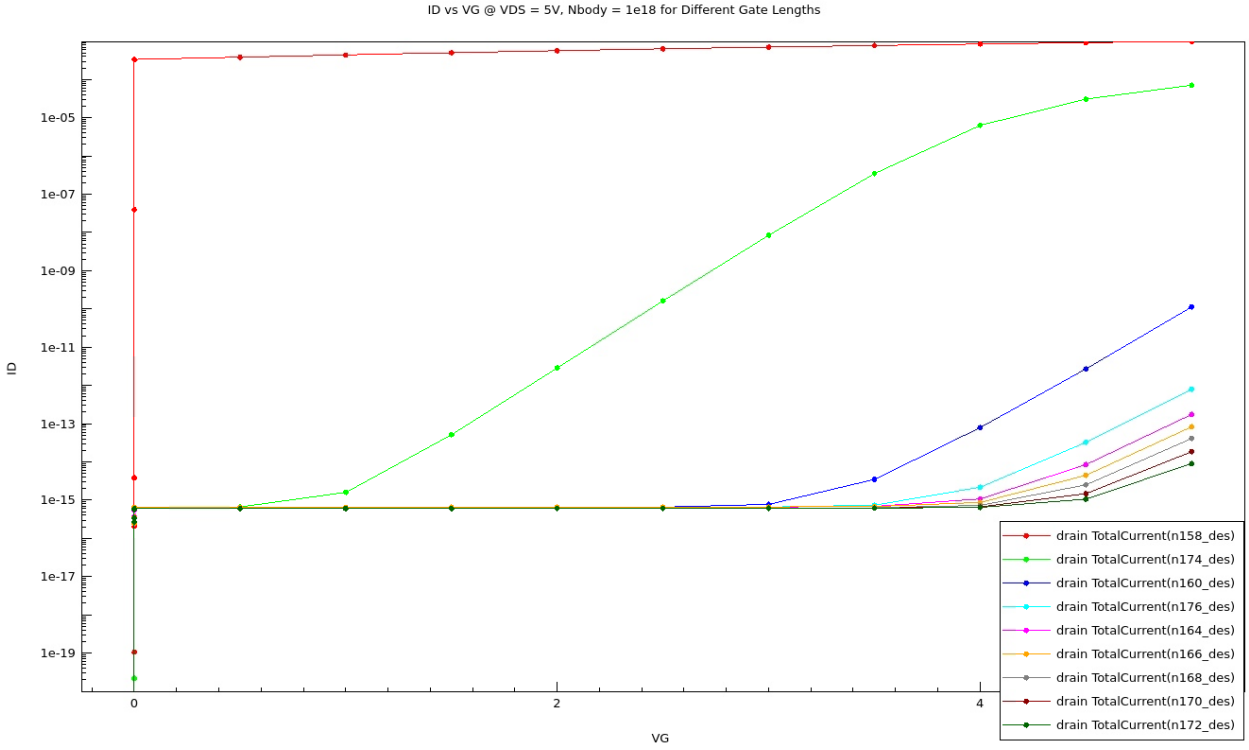


(ii) Nbody = 5e18

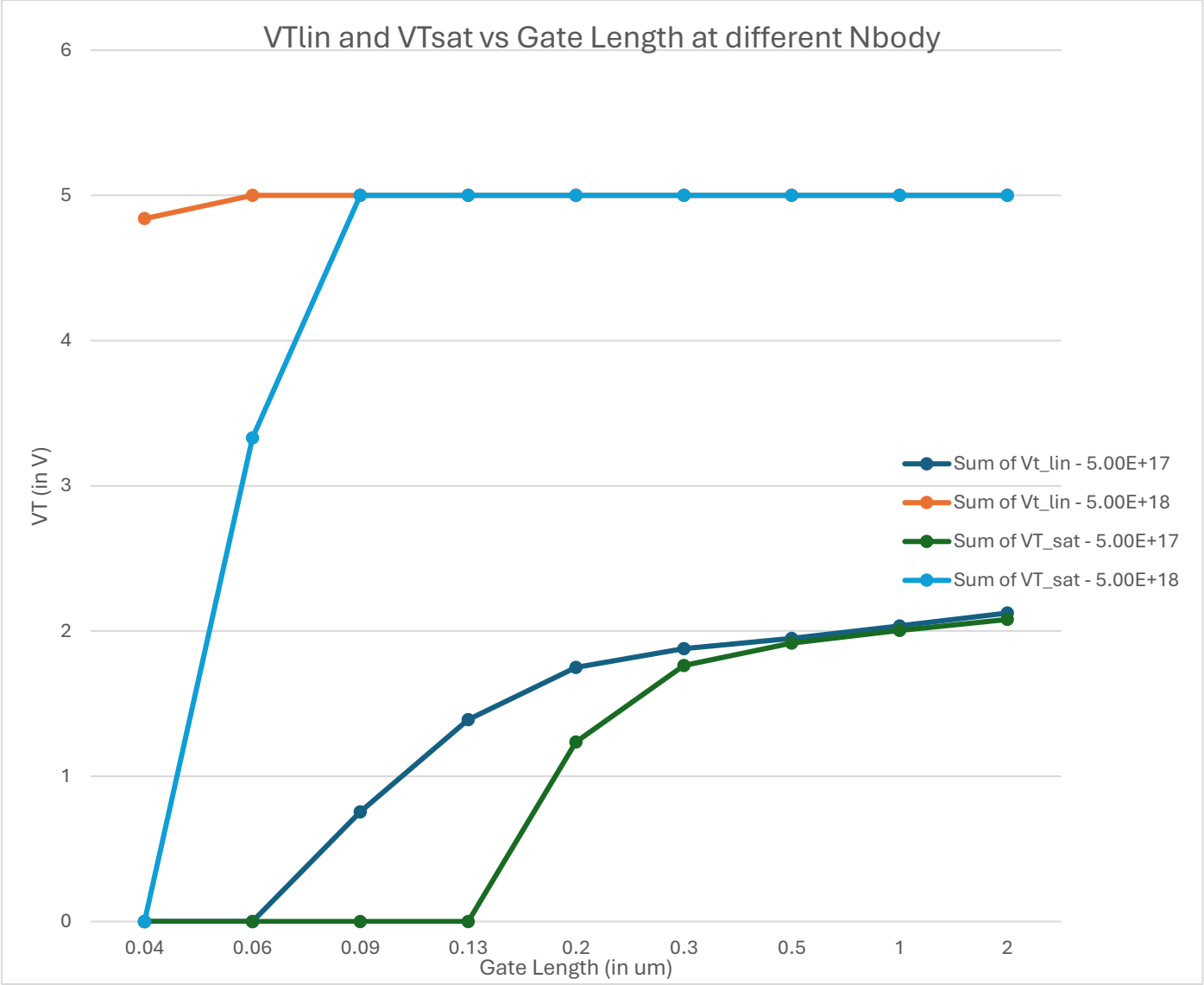
V_{T_lin}



V_{T_sat}



Node	Lgate (in um)	Nbody	Tox (in nm)	V_{T_lin}	V_{T_sat}
n58	0.04	5.00E+17	20	0	0
n80	0.06	5.00E+17	20	0	0
n60	0.09	5.00E+17	20	0.754	0
n88	0.13	5.00E+17	20	1.39	0
n64	0.2	5.00E+17	20	1.75	1.236
n66	0.3	5.00E+17	20	1.88	1.764
n68	0.5	5.00E+17	20	1.95	1.918
n70	1	5.00E+17	20	2.036	2.004
n72	2	5.00E+17	20	2.124	2.08
n158	0.04	5.00E+18	20	4.84	0
n174	0.06	5.00E+18	20	NA	3.33
n160	0.09	5.00E+18	20	NA	NA
n176	0.13	5.00E+18	20	NA	NA
n164	0.2	5.00E+18	20	NA	NA
n166	0.3	5.00E+18	20	NA	NA
n168	0.5	5.00E+18	20	NA	NA
n170	1	5.00E+18	20	NA	NA
n172	2	5.00E+18	20	NA	NA



Note: The values of V_T which were beyond the range of 5V (VDD), I have represented it as 5V

Observation: Higher substrate doping reduces V_T roll-off and reduces DIBL. Therefore, the short channel effects are mitigated. In plots of V_T vs L, the curve should show that the higher doping will show less reduction in $\mathbf{V_T}$ as L decreases.

Conclusion: Yes, increasing substrate doping is effective to suppress short channel effect to a degree. It reduces depletion width (depletion width $W_d \propto 1/\sqrt{N}$). Smaller depletion width means source/drain depletion regions encroach less into the channel and leads to lower DIBL and less roll-off. But as we can see very high substrate doping is undesirable in scaled devices as it leads to very high V_T.