ECE 441: Physics and Modeling of Semiconductor Devices

TCAD Project

Due: 6pm Wednesday Dec. 10th 2025

Fall Semester 2025

PLEASE UPLOAD YOUR PROJECT FILES ON CANVAS BEFORE 6PM (CST) WEDNESDAY DEC 10TH 2025. THE POLICY FOR LATE HOMEWORK IS POSTED IN THE SYLLABUS.

Simulation Assignments:

1. Simulate long-channel nMOSFET (30 points)

Design a long channel nMOSFET with channel length of 2 μm. The transistor will be built with n^+ polysilicon gate, SiO_2 gate dielectric and on a p-type silicon substrate. The SiO_2 thickness is 20 nm. The silicon substrate doping is $N_a = 5 \times 10^{17} cm^{-3}$. The source and drain have Gaussian doping profile with peak doping concentration of $N_d = 2 \times 10^{20} cm^{-3}$. The supply voltage is $V_{DD} = 5\,V$. Please simulate the DC characteristics of this transistor and provide the following plots.

- A snapshot of the device structure and doping profile.
- A snapshot showing the electron density when the device is biased in inversion.
- Log (I_D)-V_G @ V_{DS} = 50 mV and V_{DD}, extract the threshold voltages (V_{T_lin} and V_{T_sat}) at constant off current $I_{off} = 1 \times 10^{-7} A/\mu m$.
- Transconductance g_m as a function of gate voltage @ V_{DS} = 50 mV and V_{DD}
- I_D-V_D for several different V_{GS} values between zero and V_{DD}

Note the default width of the transistor in TCAD is 1 μm.

2. Simulate short-channel effect (30 points)

Please simulate the NMOSFET transistors with various channel length (maximum value: 2 μm, minimum value: 40 nm, number of values: 9). The doping concentration, oxide thickness and gate material are the same as the ones in Q1, Provide the following plots:

- V_{T_lin} and V_{T_sat} as a function of gate length L_{GATE}. Do you observe any short-channel effect? Please explain.
- Max transconductance g_{m_max} as a function of L_{GATE}. Here $V_{DS} = 5\,V$. Please discuss the trend you observe.
- For the transistors with channel length of 1μm and **160 nm**, plot log (I_D)-V_G with various drain voltages (from 0.1V to V_{DD}) and extract drain-induced-barrier-lowering (DIBL). Compare the DIBL values for these two transistors. Please explain why DIBL values are different in these two devices.

3. Investigate the impact of process parameters on short-channel effect (40 points)

(a) Vary the gate oxide thickness (20nm, 10nm, 5 nm and 1nm) and perform the simulation of the NMOSFET with various channel length. Here the doping concentrations are the same as the ones in Q1. Provide the plots of V_{T_lin} and V_{T_sat} as a function of gate length L_{GATE} with various gate oxide thickness. Is oxide scaling an effective approach to suppress the short-channel effect? Please explain. (20 points)

(b) Vary the substrate doping centration ($N_a = 5 \times 10^{17} cm^{-3}$ and $5 \times 10^{18} cm^{-3}$) and perform the simulation of the NMOSFETs with various channel lengths. Here the oxide thickness is the same as the one in Q1. Provide the plot of V_{T_lin} and V_{T_sat} as a function of gate length L_{GATE}

with various doping concentration. Is increasing the substrate doping an effective approach to suppress the short-channel effect? Please explain. (20 points)

Report and Project Hand-in

You need to submit a project report as a pdf file on Canvas. In your report, you need to attach the figures/plots indicated in the above assignment, provide essential annotation that supports your figures/plots, answer the questions and provide related discussions.

At the end of your report, for each of the questions above (Q1, Q2 and Q3), please attach any SWB file, device snapshots, intermediate results that is helpful to get to your results in the report. This will help you earn partial credit if the final answer is wrong.

You are required to upload a pdf version of your report on Canvas, **by 6pm Wednesday, Dec 10th, 2025**. See Syllabus for late homework policy.