

Packaging Workshop Report

Introduction

The workshop primarily focused on the evolution of semiconductor packaging, starting from the basics and progressing to advanced 3D packaging. It provided valuable insights into assembly and manufacturing processes, along with detailed explanations of testing methods and performance validation. A key highlight of the workshop was the hands-on experience through two ANSYS lab sessions, one focused on thermal simulation of semiconductor packages, and the other on package design and modeling from scratch. Design, wafer processing, packaging and testing, and assembly are the key stages in the semiconductor industry. This workshop primarily focused on the packaging and testing phases. The report is structured into five subsections, each outlining the key learnings I gained from the workshop.

I. Packaging Evolution from Basics To 3D Integration.

The appropriate package for a die is chosen based on factors such as I/O pin count, thermal dissipation requirements, cost, reliability and durability, form factor, and the intended application area.

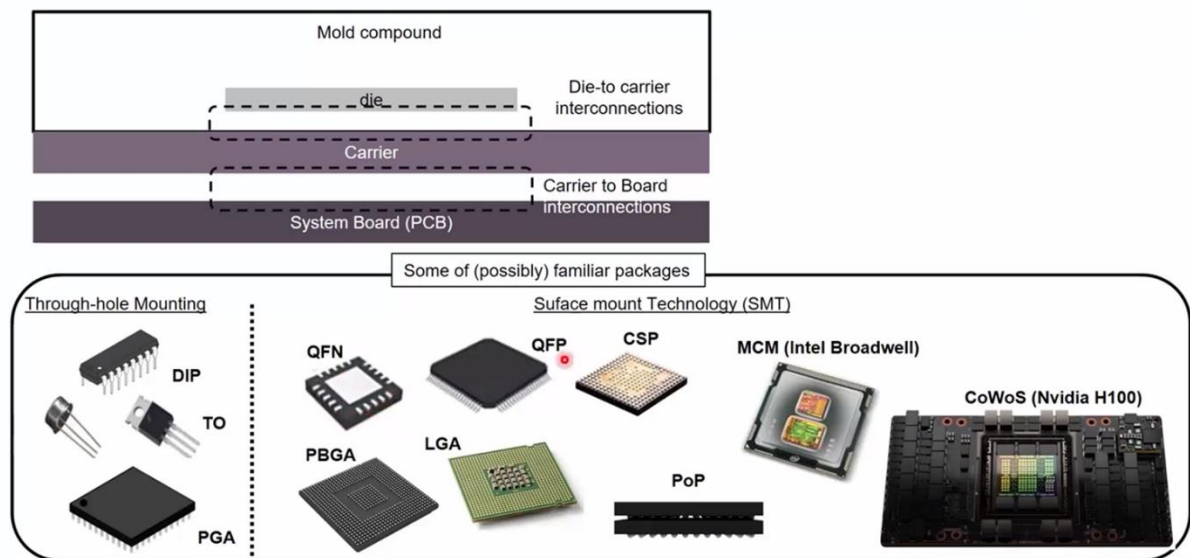


Figure 1. The basic structure of semiconductor packaging includes commonly used types such as through-hole mounting and surface mount packages.

Figure 1 shows the basic structure of semiconductor packages and commonly use packaging types such as through-hole mounting and surface mount packages. Chip scale packaging (CSP) can reduce the total area of the packaging, which is very close to the die size.

The section summarized the advantages and disadvantages of each type of packaging as follows,

a. Through-Hole Package

Through-hole packages are known for their low cost, ease of manual assembly, and durability. These characteristics make them suitable for basic and legacy applications. However, they come with limitations such as a larger physical size, low pin count, and incompatibility with modern automated assembly systems. Due to these constraints, they are commonly used in consumer electronics, industrial applications, and older system designs.

b. QFN (Quad Flat No-lead)

QFN packages are compact, lightweight, and offer good thermal performance, making them ideal for space-constrained applications. Despite their advantages, they present challenges in terms of testing accessibility and repairability. Additionally, they feature smaller I/O pins compared to QFP packages. QFNs are typically used in smartphones, tablets, automotive electronics, and telecommunication devices.

c. QFP (Quad Flat Package)

Quad Flat Packages provide a higher pin density and are easier to inspect and solder, which is beneficial in densely packed circuit designs. However, their exposed pins are susceptible to damage and can be difficult to repair if bent. These packages are widely used in microcontrollers, microprocessors, and application-specific integrated circuits (ASICs).

d. BGA (Ball Grid Array)

Ball Grid Array packages support a higher number of pins and deliver excellent electrical and thermal performance. On the downside, they are difficult to inspect and rework, have a limited shelf life, and tend to be more costly than QFN packages. BGAs

are ideal for high-performance integrated circuits where thermal and signal integrity are critical.

e. WLCSP (Wafer-Level Chip Scale Package)

Wafer-Level Chip Scale Packages significantly reduce the overall package size while maintaining high electrical performance at a lower cost. However, they are limited in terms of I/O pin count and may suffer from reliability issues such as solder joint failures and package warpage. These packages are commonly used in smartphones, Internet of Things (IoT) devices, and wearable electronics.

f. 2.5D IC Package

2.5D packaging technology offers a higher level of integration, improved performance, and better power efficiency. It connects multiple dies through an interposer or substrate in a planar configuration. Despite its performance benefits, one of its main drawbacks is the longer die-to-die connection path. This type of packaging is suited for data center chips, RF wireless modules, and aerospace or space-grade electronics.

g. 3D IC Package (with RDL Layer)

3D ICs with Redistribution Layer (RDL) offer higher I/O density and more efficient routing at a relatively lower cost. However, they can experience reliability issues related to the polymer RDL and generally have lower I/O density compared to 2.5D packages. These are used in high-performance computing segments where both performance and cost are balanced.

II. From Wafer to Package: Assembly and Manufacturing Essentials

First described about the supply chain of semiconductor industry, which is as follows. The **semiconductor supply chain** begins with the **design house**, where IC (Integrated Circuit) design is carried out using EDA (Electronic Design Automation) tools and foundry PDKs (Process Design Kits). This stage involves developing the test program and generating the GDSII layout, which serves as the blueprint for chip fabrication.

The next stage is **wafer fabrication**, where silicon wafers are processed using specialized equipment, gases, chemicals, and materials. This results in wafers populated with fabricated ICs, ready for packaging.

Following fabrication is the **package assembly and test** stage. Here, individual ICs are packaged using substrates, tools, chemicals, and lids. Each package is tested to ensure functionality and reliability.

In the **board assembly and test** phase, multiple packages are mounted onto a printed circuit board (PCB) using appropriate tools and materials. These assemblies are then tested as a unit to verify overall board performance.

The final step is **product assembly and test**, where all components are integrated into the final product using various tools. The fully assembled and tested products such as smartphones or computers are now ready for distribution and use.

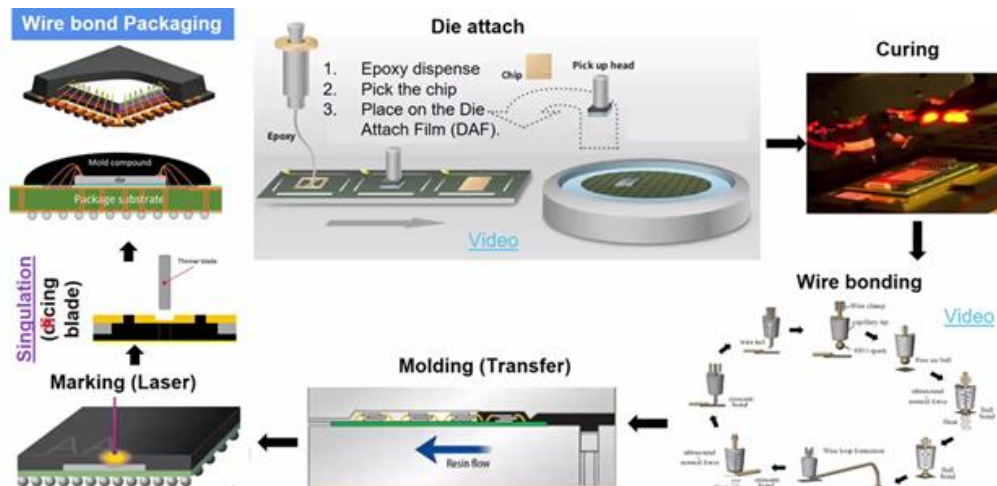


Figure 2. Steps involved in wire bond packaging.

Figure 2 illustrates the various steps involved in the wire bond packaging process. Wire bond packaging is one of the earliest and most widely adopted methods in semiconductor packaging. The process includes several key steps: die attach, curing, wire bonding, transfer molding, laser marking, and singulation, as depicted in the figure.

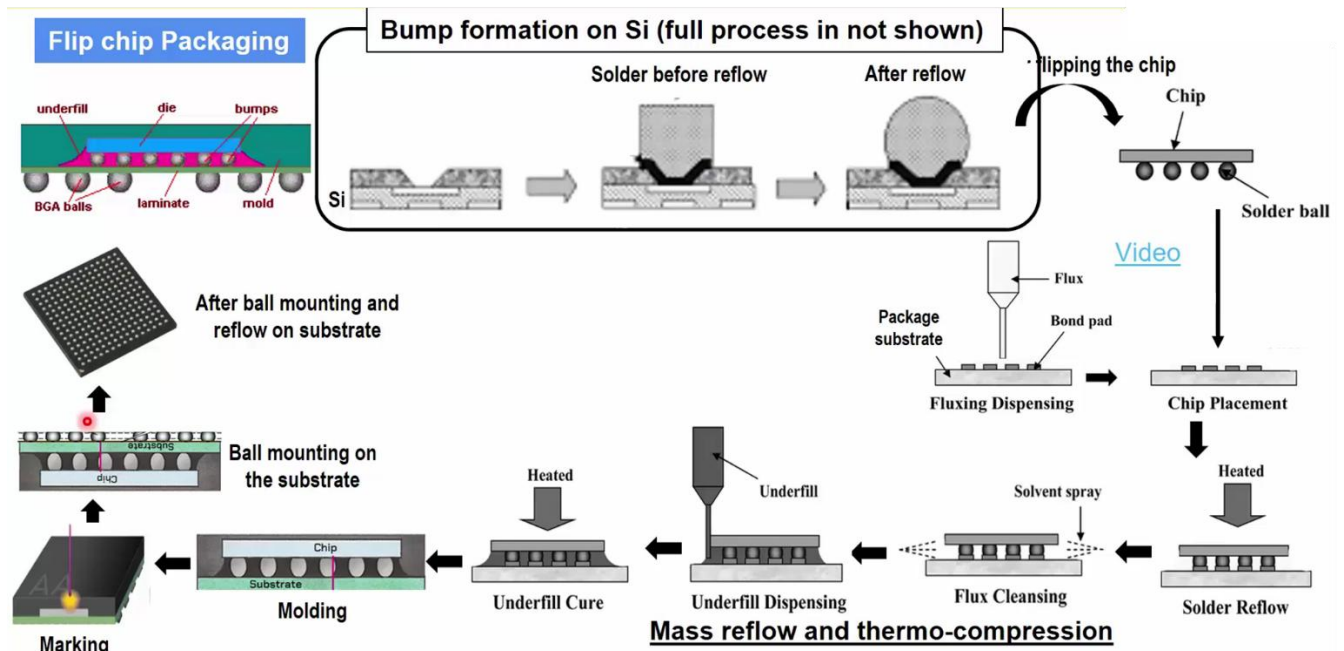


Figure 3. Different stages of flip chip packaging

Figure 3 shows the different stages of flip chip packaging. The process includes bump formation, flipping the chip, chip placement, solder reflow, flux cleansing, underfill dispensing, underfill cure, molding, marking, ball mounting on the substrate.

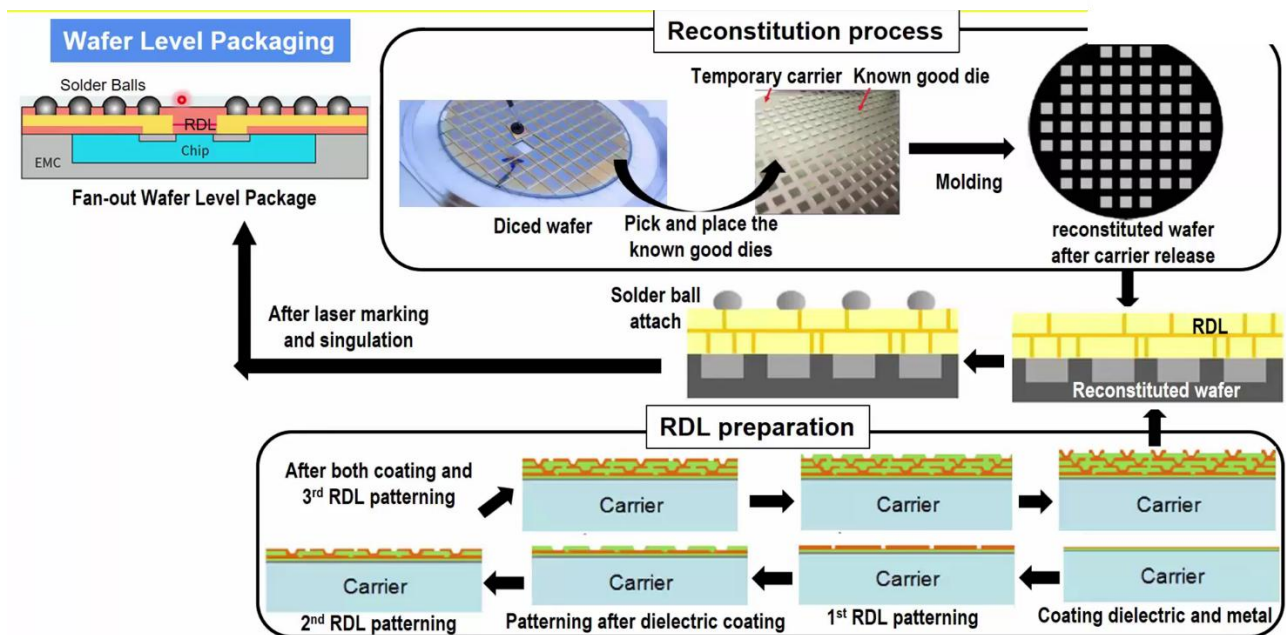


Figure 4. Steps involved in the wafer level packaging.

Figure 4. shows the steps involved in the wafer level packaging (WLP). The key step involved in the WLP is the formation of redistribution layers (RDLs). Redistribution Layers (RDLs) play a critical role in Wafer-Level Packaging (WLP) by enabling the rerouting of I/O pads from the densely packed bond pads on the die to a larger area, making external connections feasible. This is essential for creating fan-out structures, which allow for more I/O connections than the die itself would typically support. RDLs improve signal integrity, reduce electrical resistance, and support higher performance in miniaturized devices. They are key enabler for advanced packaging technologies such as fan-in WLP, fan-out WLP, and 2.5D/3D IC integration, contributing significantly to device scaling, form factor reduction, and cost efficiency.

III. Labs: Thermal Simulation of Semiconductor Package With ANSYS

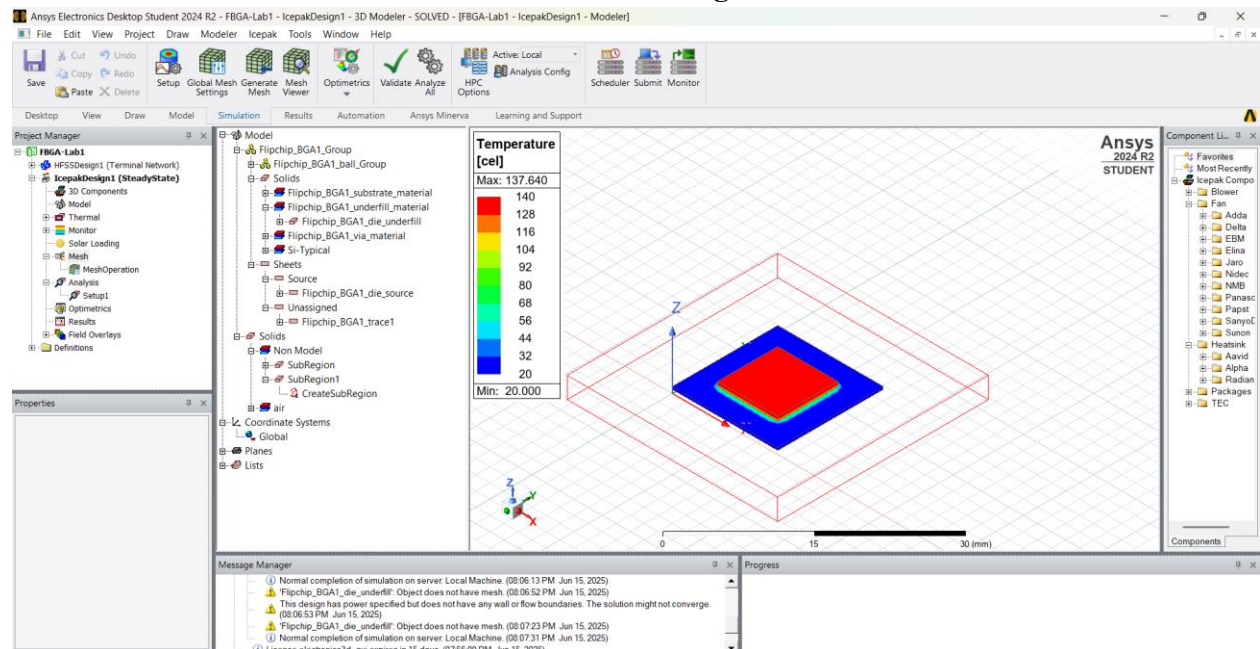


Figure 5. Thermal analysis of flip chip BGA package done by Lab-1

IV. Ensuring Package Reliability: Testing And Performance Validation

This section focused on the critical processes involved in verifying the reliability and performance of semiconductor packages. Reliability testing is a key stage in the packaging lifecycle, ensuring that each package meets both functional and environmental specifications before deployment in end-use applications. The testing process comprises several stages:

a. Assembly Open and Short Tests:

These are the initial electrical tests performed to detect basic assembly defects, such as open circuits (incomplete connections) or short circuits (unintended connections). These tests help identify issues introduced during wire bonding or substrate interconnections.

b. Burn-In Tests:

Burn-in testing involves subjecting the semiconductor package to elevated temperatures and voltages over an extended period. This is designed to accelerate the aging process and expose latent defects that could cause early-life failures in the field. One of the main goals of burn-in testing is to gather data relevant to the "bathtub curve," which illustrates the failure rate of a product over time—characterized by high initial failure (infant mortality), low constant failure rate during normal use, and increased failure rate as the product ages. Burn-in helps ensure that only stable and reliable devices proceed to market, thereby enhancing long-term product quality.

c. Final Testing (Cold and Hot Testing):

Final testing is conducted across a range of temperatures—typically at both low (cold) and high (hot) extremes—to validate the functional, parametric, and reliability specifications of the package. This includes verifying timing, current leakage, and thermal behavior to ensure that the device performs consistently under various environmental conditions. High-temperature testing, in particular, is crucial for confirming that the semiconductor package can operate within specified thermal limits without degradation or failure.

Collectively, these validation steps are essential for guaranteeing the robustness and longevity of semiconductor devices. They play a vital role in maintaining quality standards and customer confidence in high-performance, mission-critical electronic systems.

V. Package Design and Modelling: Building A Semiconductor Package from Scratch

In this section a wire bonding package is created with clear explanation and step by step guidance.

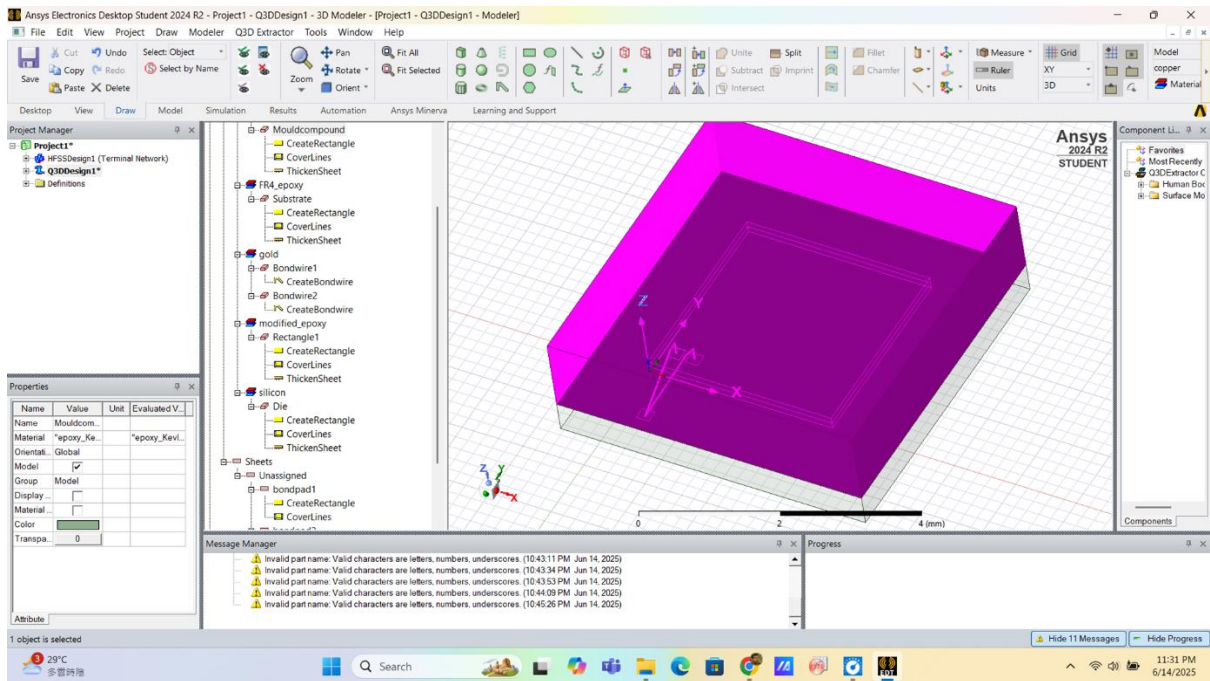


Figure 6. The wire bonding package was created using the step-by-step instructions in the workshop (Lab 2)

Conclusion

The Packaging Workshop provided a comprehensive understanding of semiconductor packaging technologies, from foundational methods to advanced 2.5D and 3D integration techniques. The sessions effectively bridged theoretical knowledge and practical application, emphasizing the importance of choosing appropriate packaging based on design, performance, cost, and reliability factors. Hands-on ANSYS lab exercises further reinforced key concepts in thermal analysis and package design, offering valuable insights into real-world applications. By exploring the entire lifecycle from wafer fabrication to final testing, the workshop highlighted the critical role of packaging in determining the overall functionality and reliability of semiconductor products. This experience has deepened my understanding of packaging technologies and their evolving role in meeting the demands of modern electronics.