

input A,B,C;  
 output O;  
 wire x;(x is an internal variable here)  
 1 OR gate(2 input)=6 MOSFET  
 1 AND gate(3 input)=8 MOSFET  
 1 NOT gate=2 MOSFET

```

module example_ckt(f, x1, x2, x3);

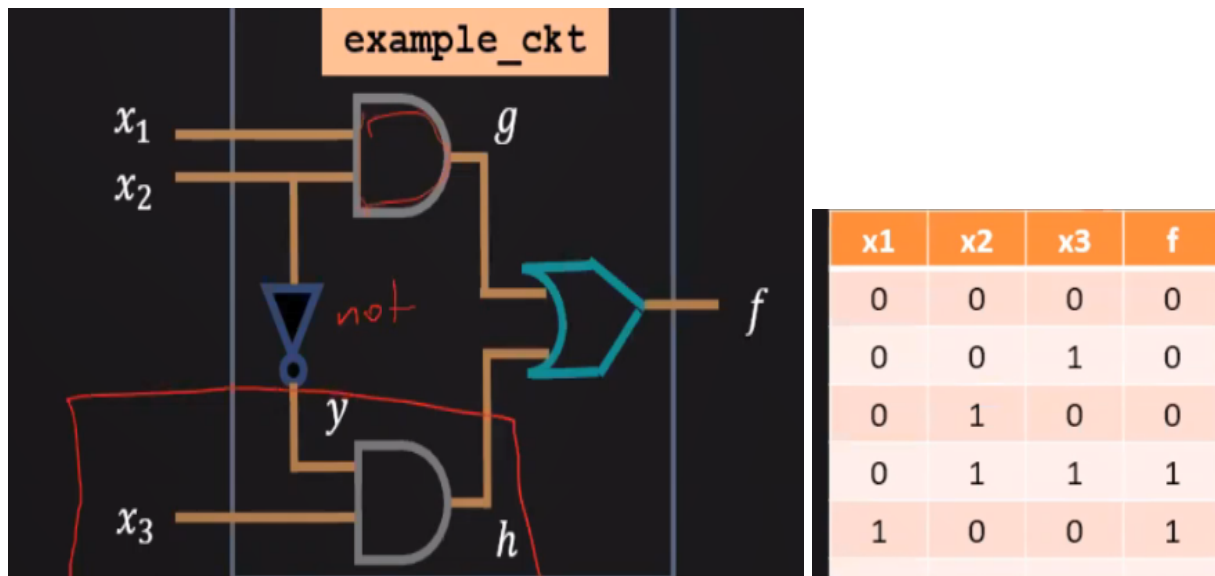
  input x1, x2, x3;
  output f;

  assign g = x1 & x2;
  assign y = ~x2;
  assign h = y & x3;
  assign f = g | h;

endmodule
  
```

*Handwritten notes:*  
 - A checkmark is next to the line `assign g = x1 & x2;`.  
 - An arrow points from the text "is complement" to the tilde symbol (~) in `assign y = ~x2;`.  
 - The variable `x3` in `assign h = y & x3;` is boxed.  
 - The expression `g | h` in `assign f = g | h;` is boxed, with the text "bitwise OR" written next to it.

$$f = x_1 \cdot x_2 + \overline{x_2} \cdot x_3$$



## How to work on quartus

File>New Project Wizard>Select Directory>Select Name>Next>Next>  
family=FLEX10KE>Next>

**Design entry:** Tool Name=Custom Format=VERILOG HDL

**Simulation:** Tool Name=Custom Format=VERILOG

**Timing Analysis:** Tool Name=Custom Format=VERILOG>Next>Finish

File>New>Design file:Verilog HDL file>OK

**Write your code now**

```

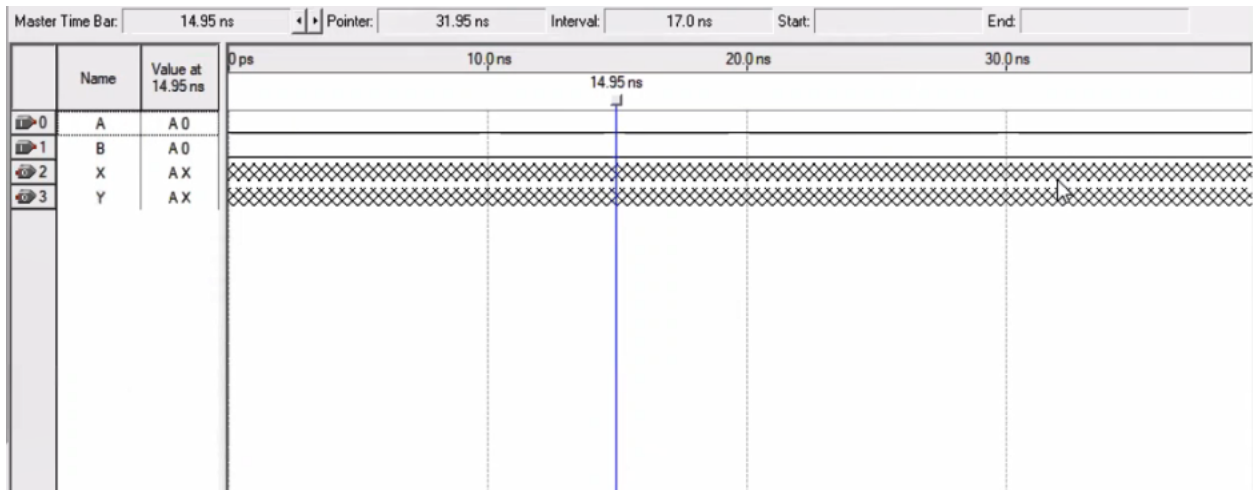
1  module ex1(A, B, X, Y);
2      input A, B;
3      output X, Y;
4
5      assign X = A&B;
6      assign Y = A|B;
7
8  endmodule

```

Start compilation button(violet play button)>save changes?yes>save>

**To see the output:(waveform output)**

File>New>Verification/Debugging file>Vector Waveform File>Ok>Click right mouse>Insert>Insert Node or Bus>Node Finder>Pins:all>List>Which pins I want to see select them>OK>OK



Click right mouse on A>Value>Clock>

**Clock**

Time range

Start time: 0 ns

End time: 100.0 ns

Base waveform on

☐ Clock settings:

☒ Time period:

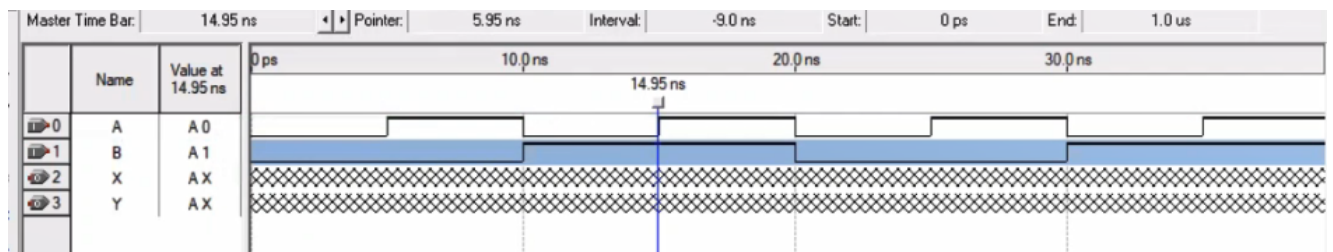
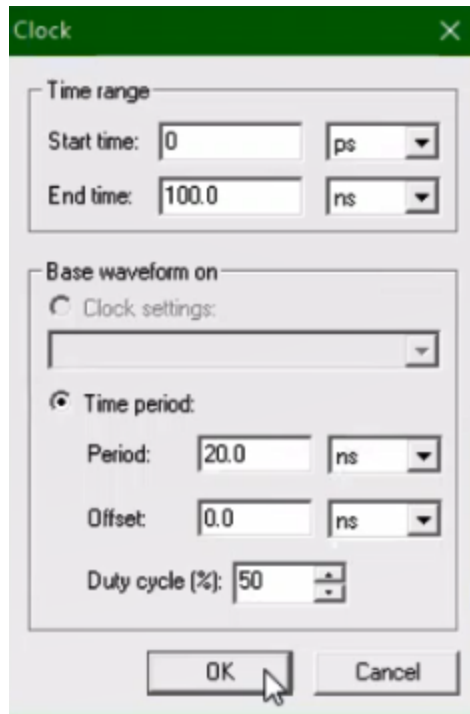
Period: 10.0 ns

Offset: 0.0 ns

Duty cycle (%): 50

OK Cancel

Click Right Mouse on B>Value>Clock>



If you want to zoom in or out this picture press CTRL+rotate mouse wheel

**Now,we want to see the output:**

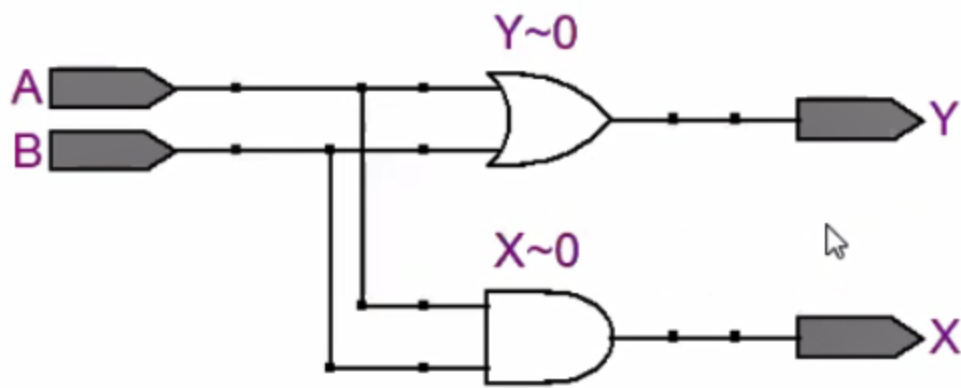
Assignment>Settings>Simulator setting>Simulation Mode>Functional>Ok

Processing>Generate Functional Simulation Netlist>Wanna  
save?YES>Save>Ok

Processing>Start Simulation>Ok

**Producing Circuit:(Schematic Diagram)**

Tools>Netlist Viewers>RTL Viewer



Operator	Operation
$\sim A$	This will produce <u>1's complement</u> of A <span style="color: red;">↓ 0 ↓ 1 ↓ 1 ↓ 0</span>
$X = A \& B$	Bitwise AND ✓
$A   B$	Bitwise OR ✓
$A \wedge B$	Bitwise XOR ✓
$A + B$	Addition of two single or multibit numbers
$A - B$	Subtraction of two single or multibit numbers
$A * B$	Multiplication of two single or multibit numbers
$A / B$	Division of two single or multibit numbers
$A \% B$	This returns the <u>remainder</u> of the integer division A/B