JYOTHY INSTITUTE OF TECHNOLOGY

TATAGUNI, BENGALURU
AFFILIATED TO VTU, BELAGAVI

Department of Computer Science and Engineering

Accredited by NBA,New Delhi

I INTERNAL ASSESSMENT, November 2020

Course: Advanced Computer Architecture ***Course Code: 17CS72*** ***Program & Semester: CSE-VII***

Max. Marks: 50 ***Date: 02-11-2020*** ***Time: 02:00-03:15 (75 minutes)***

Answer the following questions.12M Quiz and 3 questions 06M each

Q.No	*Question*	*Marks*	Course Outcomes
1	1. Pipelining technology came into existence during ____ generation. a) Second b) Third c) Fourth d) Fifth 2. Which among these is not a parallel computer? a) SISD b) SIMD c) MISD d) MIMD 3. Which among these development layers is machine independent? a) Addressing space b) Communication model c) Programming environment d) None of the above 4. _____ compiler is used in explicit parallelism. a) parallelizing b) Dependency preserving c) Concurrency preserving d) None of the above 5. A benchmark program contains 450000 arithmetic instructions, 320000 data transfer instructions and 230000 control transfer instructions. Each arithmetic instruction take 1 clock cycle to execute whereas each data transfer and control transfer instruction takes 2 clock cycles to execute on a 400MHz processors process. The effective CPI is a) 1.35 cycles / instruction b) 1.55 cycles / instruction c) 1.45 cycles / instruction d) None of the above 6. _____ is not a PRAM variant. a) EREW b) ERCW c) CRAW d) CRCW	6 * 1 M	CO1

	7. Statement S2 is _____ on statement S1 if S2 follows S1 in program order and if the output of S2 overlaps the input to S1. a) Flow Dependence b) Output Dependence c) Overlap Dependence d) Anti-Dependence 8. According to Amdahl's law, when N numbers of processors are used, speedup is calculated by ____. a) 1/((N/S)+P) b) 1/(P+N/S) c) 1/((P/N)+S) d) 1/((N/P)+S) 9. _____ is not a dynamic connection network. a) Hypercubes b) Omega c) Baseline d) Crossbar 10. In _____ refers to the situation where two or more instructions demand use of the same functional unit at the same time. a) Instruction conflict b) Function conflict c) Resource conflict d) IP conflict 11. A superscalar processor of degree m can issue__ instructions per cycle. a) 2m b) m^2 c) m d) m/2 12. Copies of same information item at successive memory levels be consistent is a _____ property of memory hierarchy. a) Temporal Locality b) Spatial Locality c) Coherence d) Inclusion		CO2
2 a **2 b**	Explain the elements of modern computers with relevant diagram. OR With a neat diagram, explain the operational model of SIMD.	6 M	CO1
3 a	Explain the Bernstein's condition for parallelism. Detect the parallelism in the following code using Bernstein's condition: **P1 : C = D * E** **P2 : M = G + C** **P3 : A = B + C** **P4: C = L + M** **P5: F = G / E**. OR	6 M	CO1

3 b	For the program given below, write the dataflow graph and show the parallel execution on a shared memory 4 processor system.
	
	input d, e, f
	$c_0 = 0$
	for i **from** 1 **to** 8 **do**
	begin
	$a_i := d_i + e_i$
	$b_i := a_i * f_i$
	$c_i := b_i + c_{i-1}$
	end
	output a, b, c		

4 a **4 b**	Differentiate between micro-programmed control and hardwired control architectures. OR Describe the typical VLIW processor and its pipeline operations.	6 M	CO2
Course outcomes ***Students will be able to:***			
CO 1: Acquire Knowledge on Parallel Computer Models, Network Properties and Scalable Performance CO 2: Illustrate Concepts of Computer (Processors, Memory Hierarchy, Bus, Cache, Shared Memory, Pipelining)			

Faculty Email id: - madhu.br@jyothyit.ac.in