RISC_V SIMULATOR with CACHES
Lab7_AI23BTECH11024_AI23BTECH11017

1 Intro

Lab7_AI23BTECH11024_AI23BTECH11017 is a tool designed to replicate the simulator like ripes.
The main goal is to run the given RV64I assembly code accordingly, updating the registers and memory with advanced implementation of caches.

2 Contents of the Archive

The compressed folder `Lab7_AI23BTECH11024_AI23BTECH11017.zip` has the following files:

1. **.c** : source code file written in C language.
2. **Makefile**: Compiles the C code and generates an executable named `riscv_sim`.
3. **README.pdf**: Provides brief information about the archive and usage instructions.
4. **report.pdf**: Contains details about the development process.

3 Usage

Follow these steps to use the project:

1. Download the `Lab7_AI23BTECH11024_AI23BTECH11017.zip` file.
2. Extract the folder into a directory/folder/path.
3. Add the corresponding files (ex: `input.s` and `config.txt`) containing the assembly code and the cache configurations to be followed to this folder/path.
4. Open a terminal and navigate to the extracted folder:
   `cd Lab7_AI23BTECH11024_AI23BTECH11017`
5. Compile the code using the following commands:
   > `make`
   > `./riscv_sim`
6. Now The commands like `cache_sim enable` ⟨`file_name`⟩`, cache_sim status, ....., load, regs, run, etc..` will be taken from the user, run the command, and gives the corresponding desired outputs.
7. Outputs are displayed in the terminal.
8. If cache simulation is enabled, after the execution of the code, there shall be almost 2 files created:
   - one having the status of each memory access made.
   - the other shall the snapshot of cache block in between of execution, if the command `cache_sim dump` ⟨`file_name`⟩ is provided to to the execution.