Roll No. | | | | | | | | | | | | **Total No. of Pages: 02**

Total No. of Questions: 09

B.Tech. (CSE) / (AI&ML) / (CE)/ B.Tech. CSE (Internet of Things and Cyber Security including Block Chain Technology) (Sem. – 4)

COMPUTER ORGANIZATION & ARCHITECTURE

Subject Code: BTES-401-18

M Code: 77627

Date of Examination : 05-01-2023

Time: 3 Hrs. **Max. Marks: 60**

INSTRUCTIONS TO CANDIDATES:

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Write briefly:

a) What are the advantages of pipelining?

b) What is an op code? How many bits are needed to specify 32 distinct operations?

c) What is the use of EEPROM?

d) How interrupt requests from multiple devices be handled?

e) Compare RISC and CISC architecture.

f) Explain a micro instruction format.

g) Distinguish between memory mapped and isolated I/O.

h) An address space is specified by 24 bits and the corresponding memory space by 16 bits.

How many words are there in the main memory and virtual memory?

i) What is meant by an interleaved memory?

j) State the difference between direct and indirect addressing mode?

SECTION-B

2. What is cache coherence and why is it important in a shared multi processors system? How can the problem be solved with a snooty cache controller?

3. Explain with an example how to multiply two unsigned binary numbers.

4. Explain about DMA controller with help of an example.

5. Elaborate different types of addressing modes with the help of an example.

6. Explain the design of micro programmed control unit in detail.

SECTION-C

7. Show how transfer from disk to memory is conducted under programmed I/O and interrupt driven I/O ?

8. Explain the various mappingtechniques associated with cache memories.

9. What is virtual memory? Explain the steps involved in virtual memory address translation.