Sheet: CPU

File: cpu.sch

Sheet: TED

File: ted.sch

Sheet: RAM

File: ram.sch

Sheet: ROMs

File: rom.sch

Sheet: Keyboard

File: keyboard.sch

Sheet: Datassette & Serial Bus

File: datasette.sch

Sheet: Expansion Port

File: exp_port.sch

Sheet: Power & Misc

File: misc.sch

Sheet: Joysticks

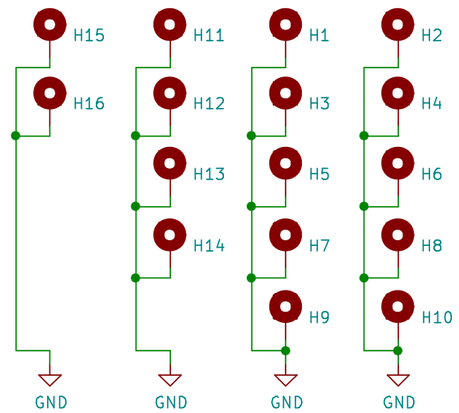
File: joysticks.sch

Sheet: PLA & Chip Selection

File: pla.sch

Sheet: Audio/Video Output

File: avout.sch



Sheet: User Port

File: userport.sch

Sheet: SID!

File: sid.sch

V0
LOGO

V1
PCBWAY_LOGO

V2
CC BY-NC-SA 4.0

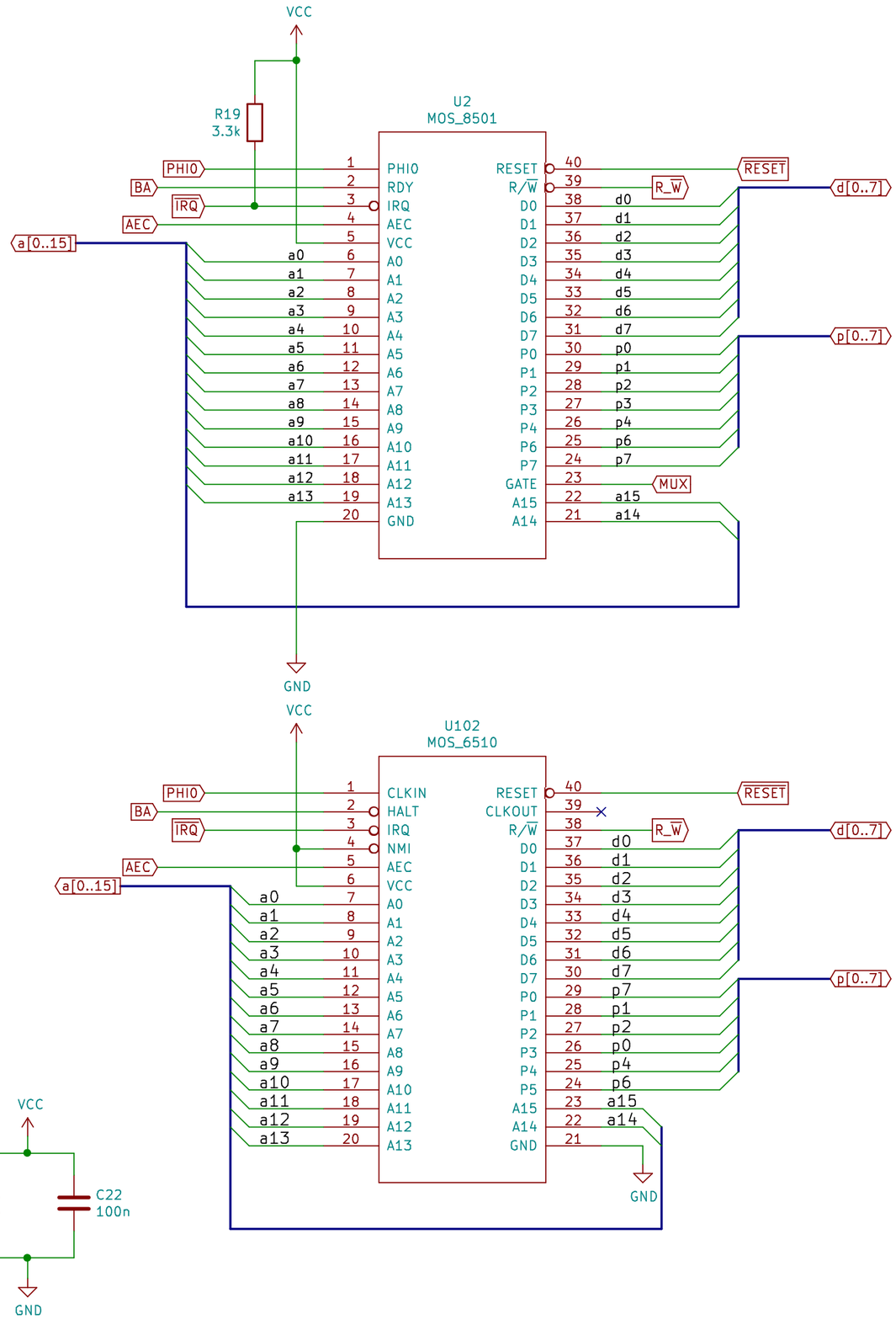
SukkoPera

Sheet: /

File: LittleSixteen.sch

Title: LittleSixteen

Size: A4	Date: 2023-02-15	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 1/14



The 7501/8501 CPU used in the x264 series is not much different from the 6510 that was used in the C64. Mapping of most pins is straightforward. Some signals change names but they are obviously the same.

6510s were working at 1MHz in the C64, while the x264 design is able to push them to nearly 2 MHz during video blanking. Since most 6510s seem to be pretty forgiving in this regard, we are left with two issues:

- GATE_IN: There is a lot of myth and inaccuracy about the purpose of this pin that is not available on the 6510. Here's a quote from the TED System Hardware Manual that should clarify things:

  "GATE IN: TTL level input, used to gate the R/W line to prevent the R/W line from going low during a read cycle, before RAS and CAS go high (resulting in a Read/Write cycle). Normally connected to the MUX line in a system configuration to synchronize the DRAM memory cycle to the processor clock cycle.

  If AEC is low when Gate In makes a low to high transition, the R/W line will go to a high impedence until the next transition of the Gate In line and AEC is high prior to the transition."

  This is confirmed by some guys who recently decapped an 8501 and analyzed its die, please see http://forum.6502.org/viewtopic.php?f=4&t=6617.

  A forum thread (http://www.softwolves.com/arkiv/cbm-hackers/16/16855.html) seems to suggest that when using DRAMs the signal is pretty useless, but it would be needed if SRAMs were used. I'm not sure this is correct and I really can't judge by myself, but since experience shows that leaving GATE_IN unconnected doesn't *seem* to hurt, we'll go with that for the moment, but for the future we might do something along the lines of this quote from Bil Herd himself:

  "[During the development of the x264 family, where we were using 6510 CPUs] I think I did the Gated Read/Write with a 74LS73 only I drove the R/W line high, not HiZ."

- I/O Port: The 8501 has a 7-bit I/O port while the 6510 only has a 6-bit, plus the exposed bits are numbered differently, so some remapping is needed, which implies that some modding to the KERNAL is required as well. I decided to follow what Andrew Challis did at http://hackjunk.com/2017/06/23/commodore-16-plus-4-8501-to-6510-cpu-conversion/. So, the 6510 socket is basically Andy's adapter built into the mainboard. If you go with a 6510 you will need to use his modified KERNAL and to solder the diode and resistor at D/R93. This comes at a compromise though:
  - Disk fastloaders will not work (unless they are modified themselves to match our pin shuffling).
  - The Datassette motor will spin whenever one of its keys is pressed, the computer will no longer be able to control it.

  I think these drawbacks are acceptable, as most fastloaders won't work anyway when using an SD2IEC, which is what most people do these days, I guess, while the loss of tape control isn't much of an issue in itself. Make sure to send a small donation to Andy if you go this way.

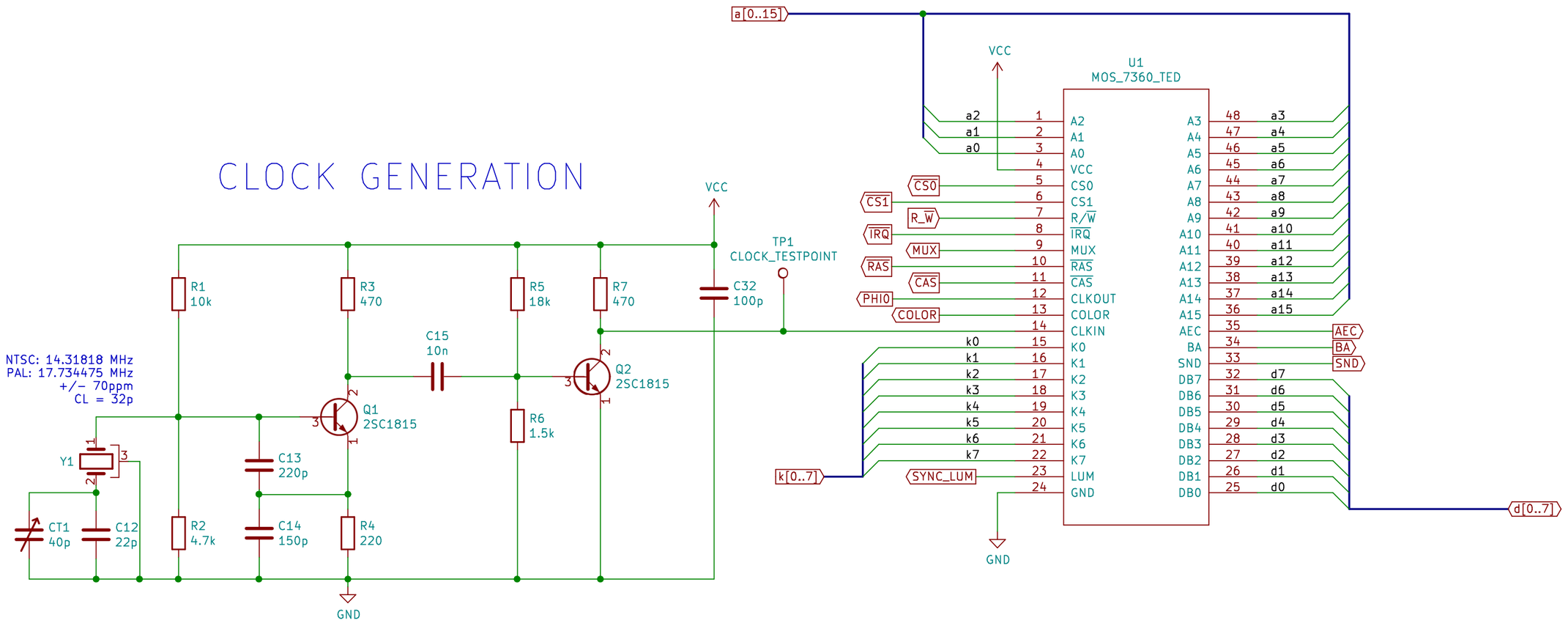
SukkoPera

Sheet: /CPU/
File: cpu.sch

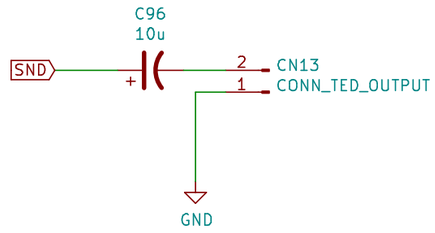
Title: LittleSixteen

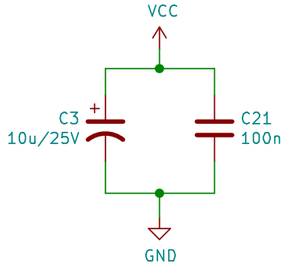
Size: A4	Date: 2021-11-17	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 2/14

CLOCK GENERATION



(EXPERIMENTAL)
DIRECT TED AUDIO OUTPUT





SukkoPera

Sheet: /TED/
File: ted.sch

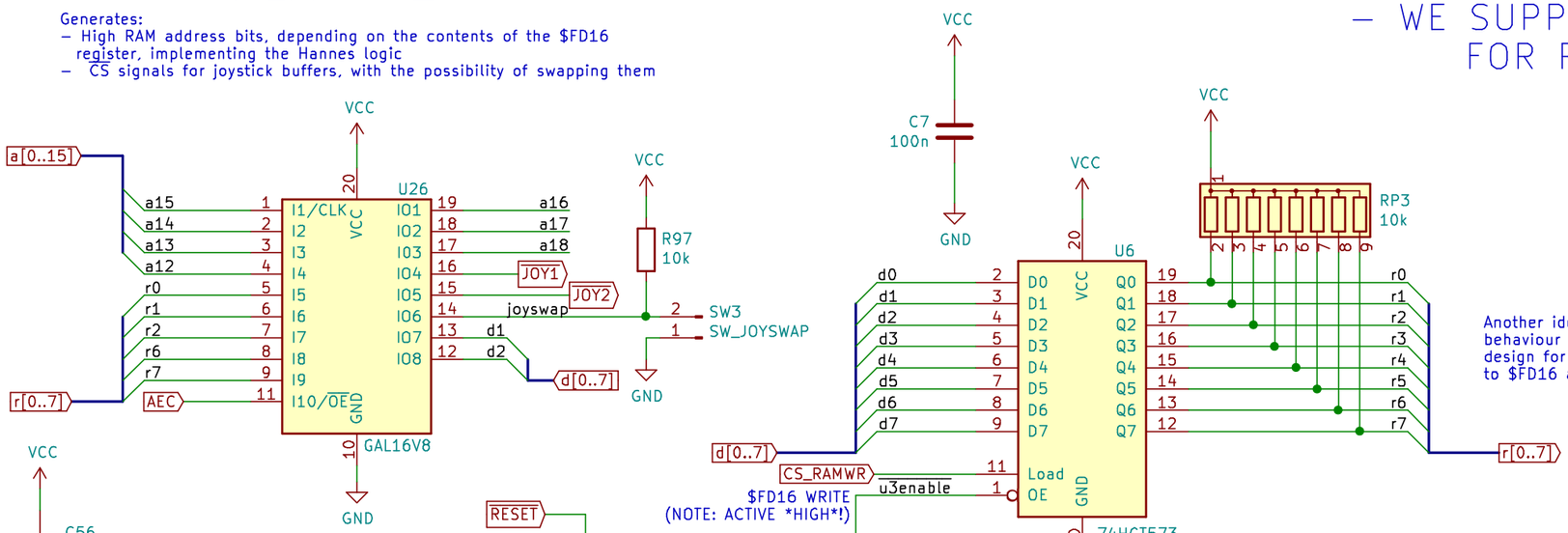
Title: LittleSixteen

Size: A4	Date: 2020-01-03	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 3/14

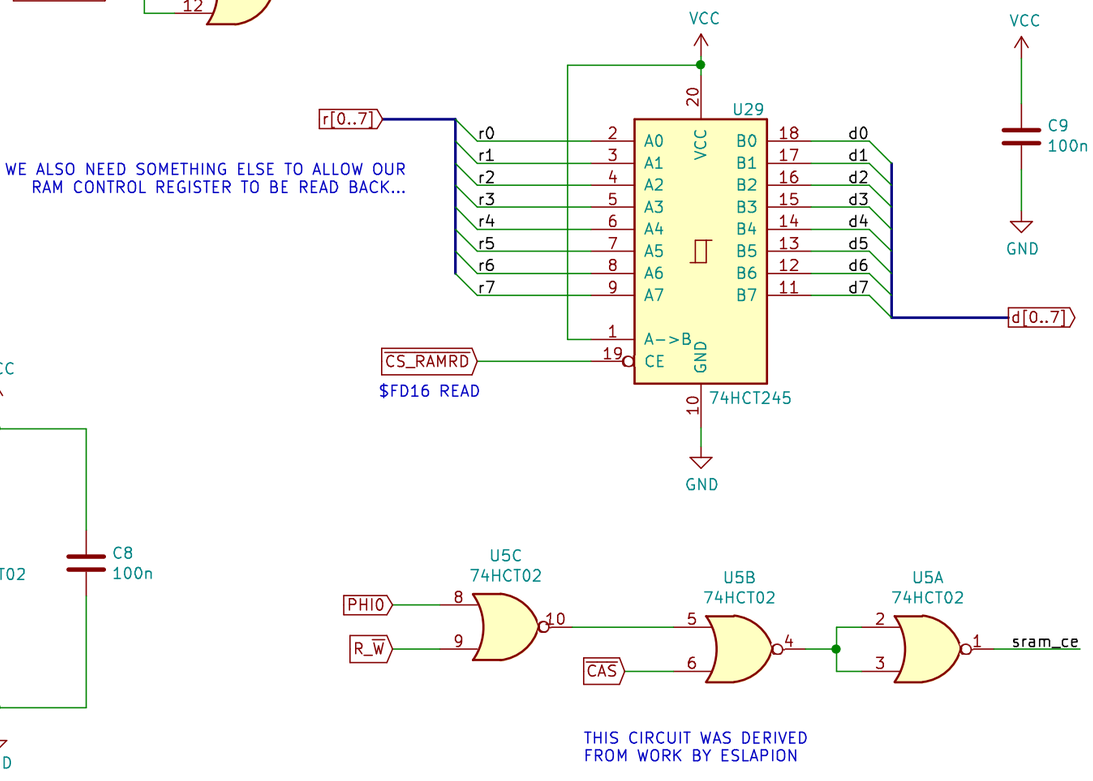
PLA – 2 –

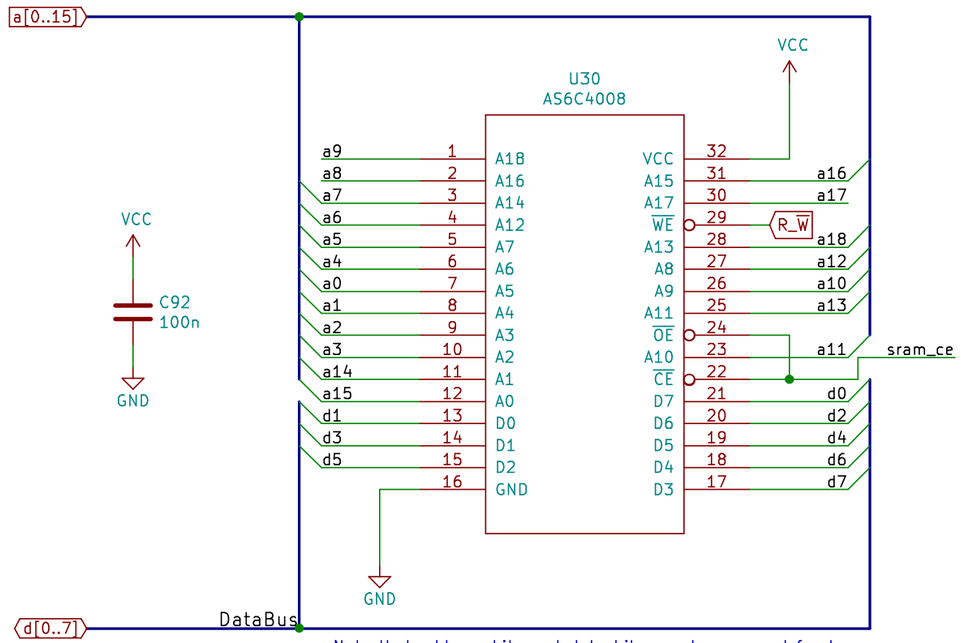
Generates:
- High RAM address bits, depending on the contents of the $FD16 register, implementing the Hannes logic
- CS signals for joystick buffers, with the possibility of swapping them

– WE USE A SINGLE STATIC RAM CHIP
– WE SUPPORT A HANNES–STYLE MECHANISM FOR RAM EXPANSION TO UP TO 512 KB



Another idea from Levente Hársfalvi in order to achieve the "high at reset" behaviour of the MOS 6529 that was originally used in Hannes/Solder's design for the control register: keep the 74x573 in Hi–Z until the first write to $FD16 and use pull–ups on its output. All hail TLC!



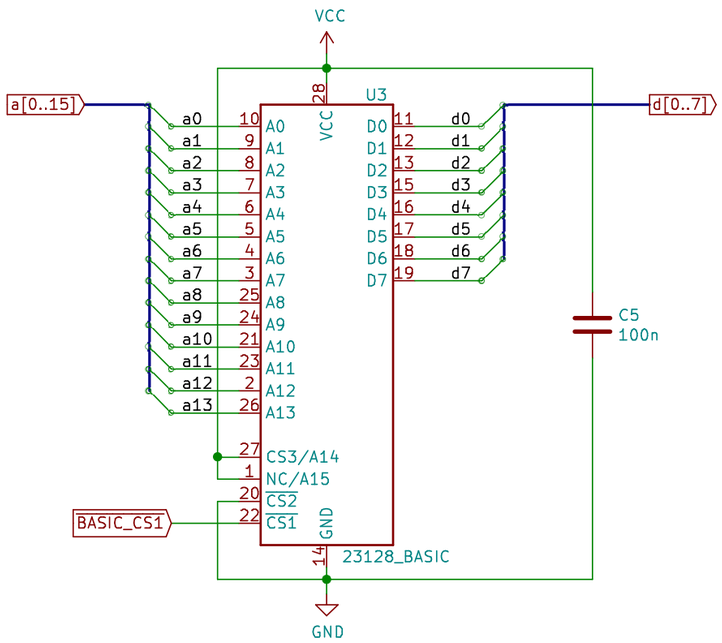


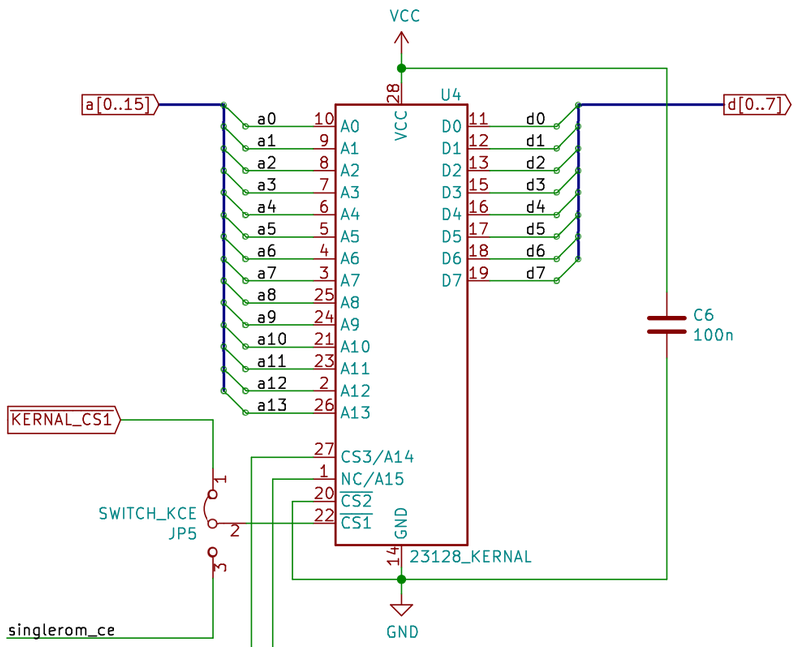
SukkoPera

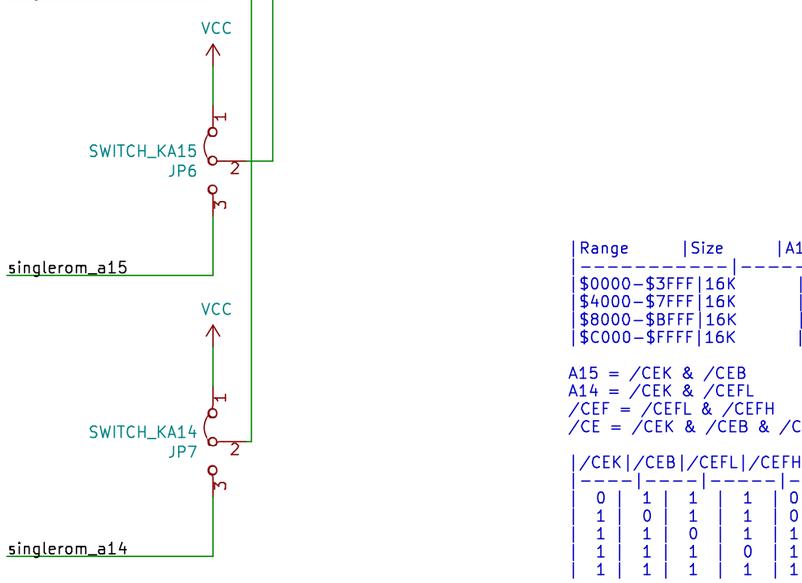
Sheet: /RAM/
File: ram.sch

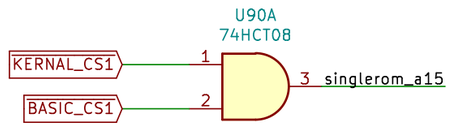
Title: LittleSixteen

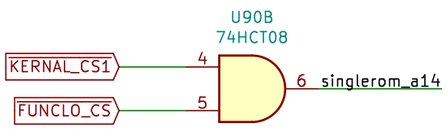
Size: A4	Date: 2023–07–10	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 4/14

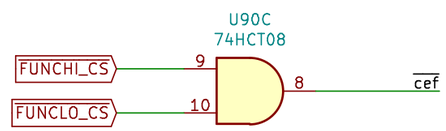


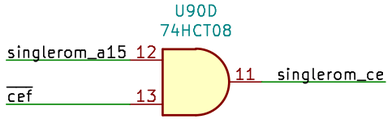


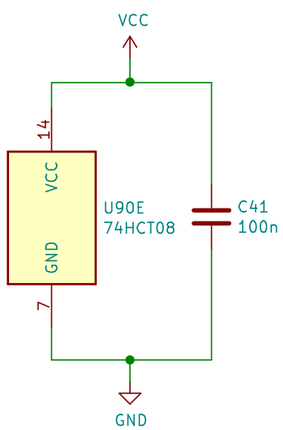












Range	Size	A15	A14	Content
$0000–$3FFF	16K	0	0	Kernal
$4000–$7FFF	16K	0	1	Basic
$8000–$BFFF	16K	1	0	FnLO
$C000–$FFFF	16K	1	1	FnHI

A15 = /CEK & /CEB
A14 = /CEK & /CEFL
/CEF = /CEFL & /CEFH
/CE = /CEK & /CEB & /CEF = A15 & /CEF

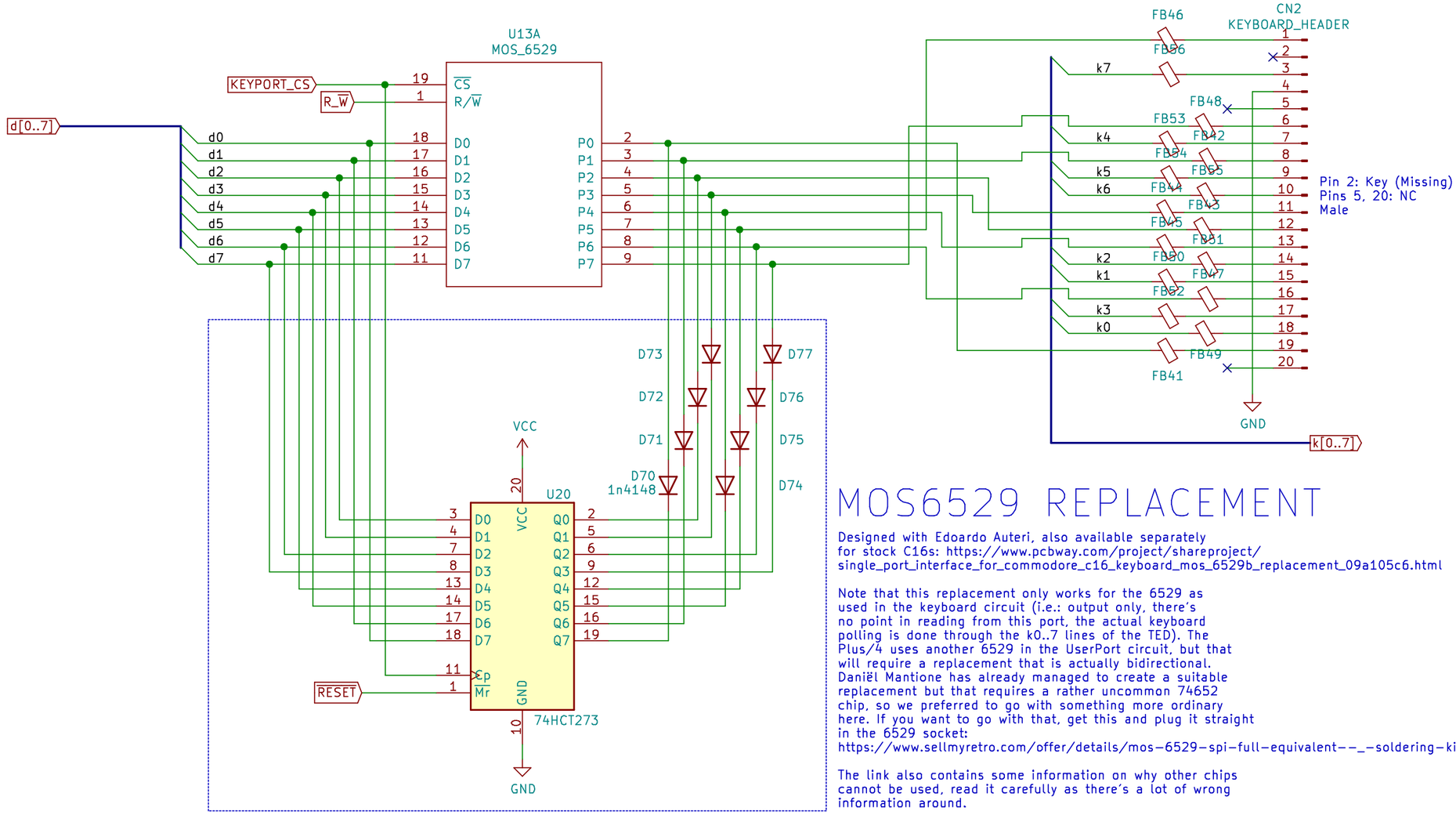
/CEK	/CEB	/CEFL	/CEFH	A15	A14	/CEF	/CE
0	1	1	1	0	0	1	0
1	0	1	1	0	1	1	0
1	1	0	1	1	0	0	0
1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	1

SukkoPera

Sheet: /ROMs/
File: rom.sch

Title: LittleSixteen

Size: A4	Date: 2021-11-14	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 5/14



MOS6529 REPLACEMENT

Designed with Edoardo Auteri, also available separately
for stock C16s: https://www.pcbway.com/project/shareproject/
single_port_interface_for_commodore_c16_keyboard_mos_6529b_replacement_09a105c6.html

Note that this replacement only works for the 6529 as
used in the keyboard circuit (i.e.: output only, there's
no point in reading from this port, the actual keyboard
polling is done through the k0..7 lines of the TED). The
Plus/4 uses another 6529 in the UserPort circuit, but that
will require a replacement that is actually bidirectional.
Daniël Mantione has already managed to create a suitable
replacement but that requires a rather uncommon 74652
chip, so we preferred to go with something more ordinary
here. If you want to go with that, get this and plug it straight
in the 6529 socket:
https://www.sellmyretro.com/offer/details/mos-6529-spi-full-equivalent--_-soldering-kit-43923

The link also contains some information on why other chips
cannot be used, read it carefully as there's a lot of wrong
information around.

SukkoPera

Sheet: /Keyboard/
File: keyboard.sch

Title: LittleSixteen

Size: A4	Date: 2022-08-17	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 6/14

DATASSETTE INTERFACE

These are protection diodes retrofitted after production on *some* C16s I've seen. These seem different from the 1n4148 that are retrofitted on p6/p7 on the same board, since those clearly say 1n4148 on their bodies, while these have a color coding of yellow (thick/cathode), brown, yellow, grey (or light blue?), which... erm, would make them 1n4148 ^___^. Multimeter says their Voltage drops are 0.555V and 0.561V, while it says 0.323 for the others (all measures in-circuit).

ADDITIONAL CURRENT-LIMITING RESISTOR

WARNING: The drawing of this connector does not match the real connector exactly!

CST_SENSE:
LOW if one of the keys PLAY, RECORD, F.FWD or REW is pressed, HIGH otherwise

This diode is the one Andrew Challis recommends in order to let the Datassette motor run only when one of its keys is pressed. We add a pull-up resistor just in case. Install both only when using a 6510 CPU. (He says FB15 on his page but it's a clear mistake.)

CST_MTR:
LOW = Motor on
HIGH = Motor off

CST_RD
CST_WRT
TAPE_SENSE
p[0..7]
p4
p3
VCC
GND
+9V
D95 1n4148
D94 1n4148
D93 1n4148
R94 4.7R 1W
R93 3.3k
R12 3.3k
R13 470
R29 100
C23 470p
C24 470p
C25 470p
C26 100n
FB14
FB15
FB16
FB17
FB18
FB19
tape_sense
tape_read2
tape_read
tape_+5v
tape_wr2
tape_mtr2
tape_gnd
CN3 CASSETTE
GND 8
READ 5
+5V 2
6 WRITE tape_wr
3 MOTOR tape_mtr
1 MOTOR_GND
SENSE 7
SHIELD 0
Q5 2SD880
D12 6.8V
U9C 74LS06

tape_sense 6
tape_wr 5
tape_read 4
tape_mtr 3
tape_+5v 2
tape_gnd 1
CN93
C64_STYLE_CASSETTE

SERIAL BUS (OR 1541 DISK DRIVE)

These (and the ones below) are more retrofitted protection diodes, these are present on most C16s I've seen. Note that these protection diodes have been added on all pins going straight to the CPU from the outside world.

These protection diodes are usually installed in place of ferrites FB3 and FB4.

D99 1n4148
D97 1n4148
D98 1n4148
D96 1n4148
p[0..7]
p7
p6
p2
p1
p0
SERIAL_RESET
RP1E RP1C RP1D RP1B 1k
U9D
U9E
U9F
U9B
74LS06
ATTN
BRESET
FB1
FB2
FB3
FB4
FB5
iec_atn
iec_clk CLK
iec_dat DATA
iec_rst
iec_srq
RESET
CN7 SERIAL_BUS ATN
FEMALE DIN-6
SHIELD
2 GND
1 SRQ
R102 330

NOTES:
- Fastloaders might use these signals differently!
- All signals are active-low
- All signals are open collector, since this is a *bus*

J90 CONN_IEC_INT
1
2 iec_dat
3 iec_clk
4 iec_rst
5 iec_atn
6 iec_srq
7

J91 CONN_TAPE_INT
1 2 tape_mtr
tape_read 3 4 tape_wr
tape_sense 5 6

These connectors have all the Tape and IEC signals and can be used to implement an internal SD2IEC and Tapuino.

U92 DT1042
tape_sense 1
tape_read 3
4
tape_wr 6
I/O1 I/O2 I/O3 I/O4 VCC GND

U91 DT1042
iec_rst 1
iec_clk 3
iec_dat 4
iec_atn 6
I/O1 I/O2 I/O3 I/O4 VCC GND

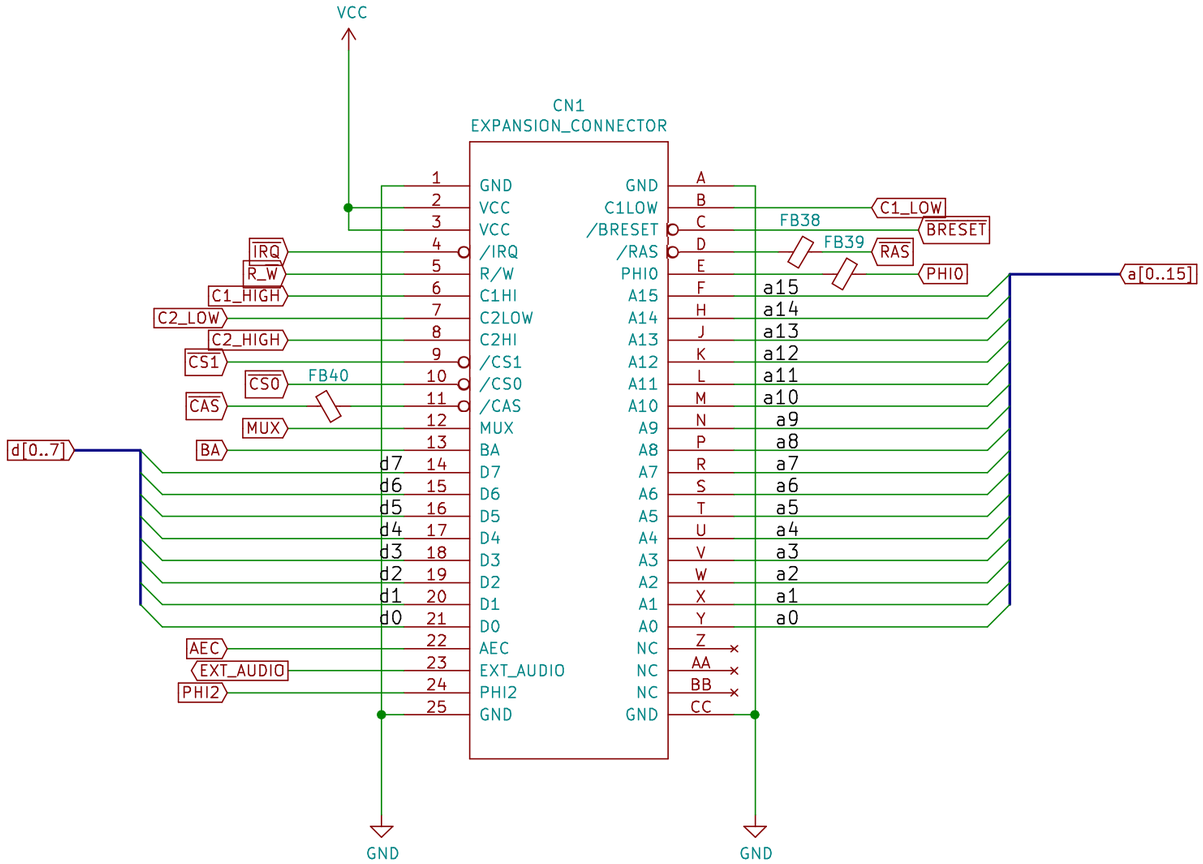
These offer better ESD protection than the retrofitted diodes, but use an SMT component. Mount only one or the other, at your preference.

SukkoPera

Sheet: /Datassette & Serial Bus/
File: datasette.sch

Title: LittleSixteen

Size: A4	Date: 2023-07-25	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 7/14



SukkoPera

Sheet: /Expansion Port/
File: exp_port.sch

Title: LittleSixteen

Size: A4	Date: 2021-12-05	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 8/14

POWER REGULATION

CN8
POWER_INPUT
+5VDC 1.7A
9VAC 1A
C100
100n/25V
C103
220n/25V
GND
LF100
CM4545Z131B-10
in_+5v
in_gnd
in_-9vac
in_+9avc
BLEEDING RESISTOR
TO DISCHARGE CAPS
ON POWER DOWN
R96
10 2.5W
SW1A
POWER_SWITCH
C101
100u/35V
C102
100n/25V
VCC
TP2
FIVEV_TESTPOINT
C105
220n/25V
C106
220n/25V
C104
220n/25V
RECOMMENDED
X5R/X7R
CERAMIC
THIS ODD CONNECTION
MAKES ROUTING EASIER
This power circuit has been
lifted as-is from the Plus/4
F100
1.5A
+9VAC
-9VAC
SW1B
POWER_SWITCH
CR100
NTE5304
+9V
UNREGULATED
TP4
NINEV_TESTPOINT
C107
2200u/25V
C109
100n/25V
SW1C
POWER_SWITCH
C95
470u
Additional cap
for smoother
VCC mid-board

VCC
PWR_FLAG
+9V
PWR_FLAG
PWR_FLAG
GND

POWER-ON RESET
+ RESET SWITCH

R21
100k
R20
47k
U10
NE555P
TR
CV
R
VCC
GND
Q
DIS
THR
U9A
74LS06
RP1A
1k
RESET
SERIAL_RESET
JP11
SW_RESET
C17
1u/16V
C16
10u/25V
This will be inverted
separately by U9B in
order to be exposed
on connectors to the
outside world

POWER LED

R14
470
CN9
LED_CONNECTOR
GND

SPARES

U12D
74HCT02

SID AUX VOLTAGE GENERATION

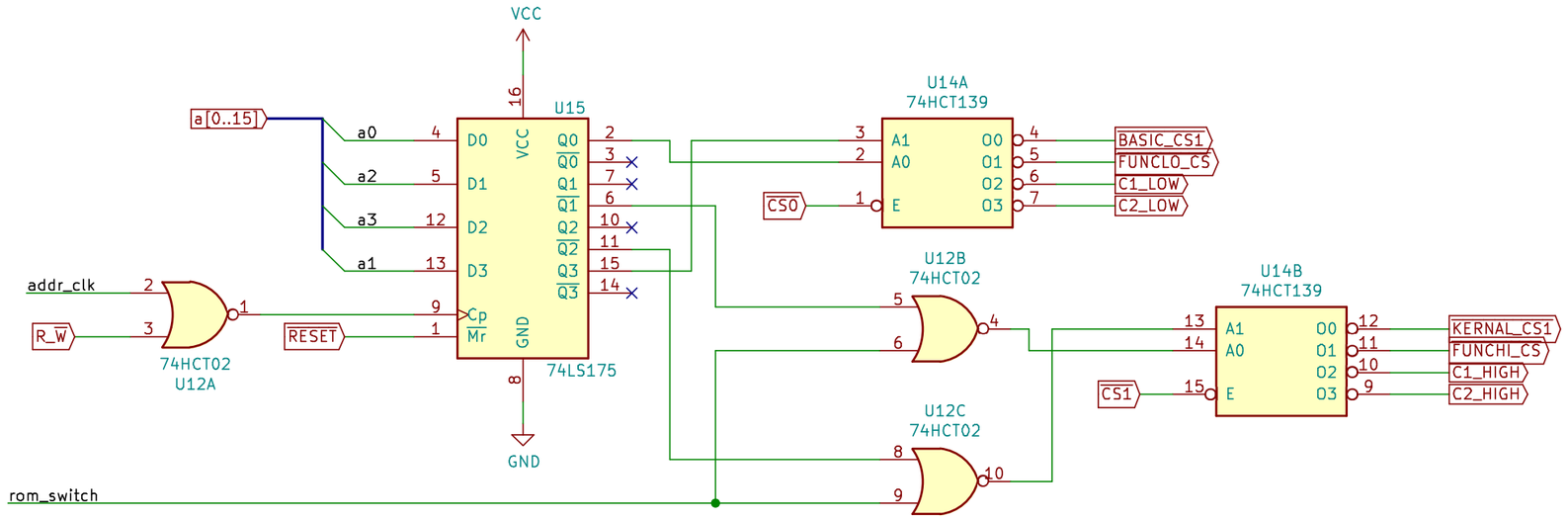
U9G
74LS06
C34
100n
C29
100n
Additional
decoupling cap
for U10
Charge pump, raises the
voltage input to the regulator
D87
1n4001
D88
1n4001
C110
470u
*** WARNING - WARNING - WARNING! ***
- Use 7812 for 6581 SID.
- Use 7809 for 8580 SID.
U7
L7812
IN
OUT
C111
470u/25V
C112
100n
C113
470u
C114
100n
L3
FERRITE
VTED
VTED_TESTPOINT
TP3

SukkoPera

Sheet: /Power & Misc/
File: misc.sch

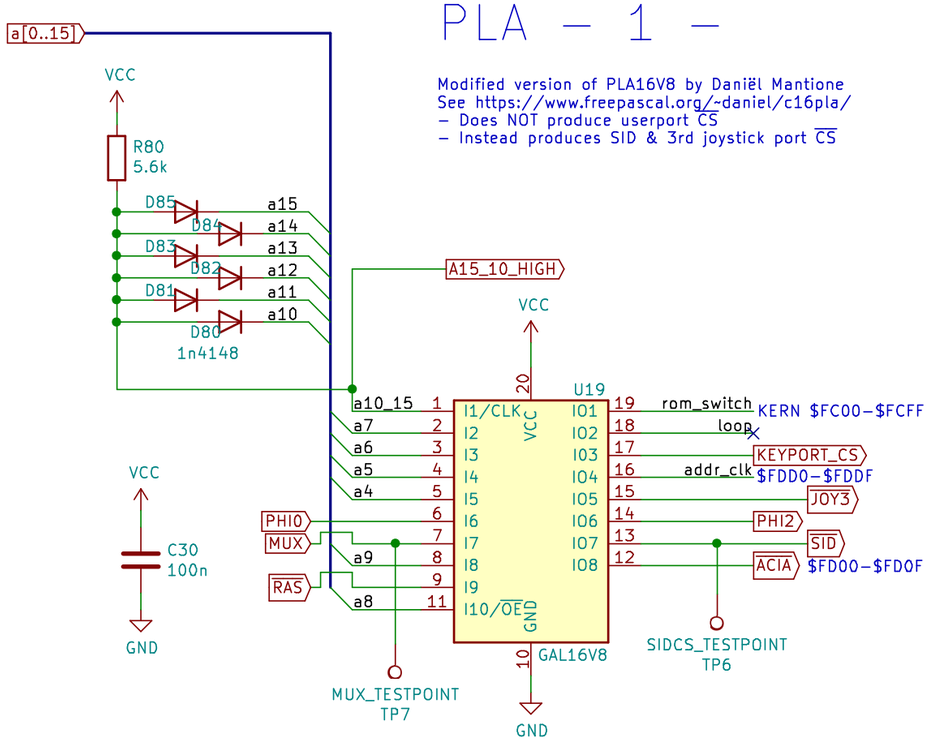
Title: LittleSixteen

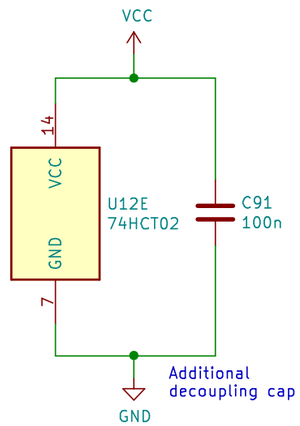
Size: A4	Date: 2023-07-12	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 9/14

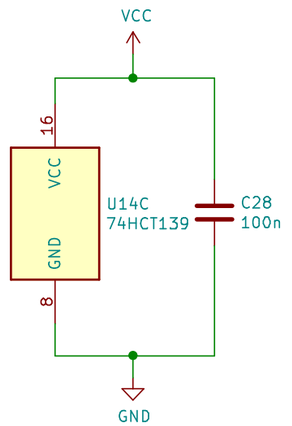


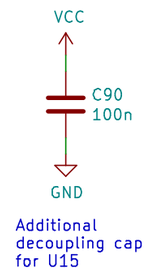
PLA – 1 –

Modified version of PLA16V8 by Daniël Mantione
See https://www.freepascal.org/~daniel/c16pla/
– Does NOT produce userport CS
– Instead produces SID & 3rd joystick port CS









SukkoPera

Sheet: /PLA & Chip Selection/
File: pla.sch

Title: LittleSixteen

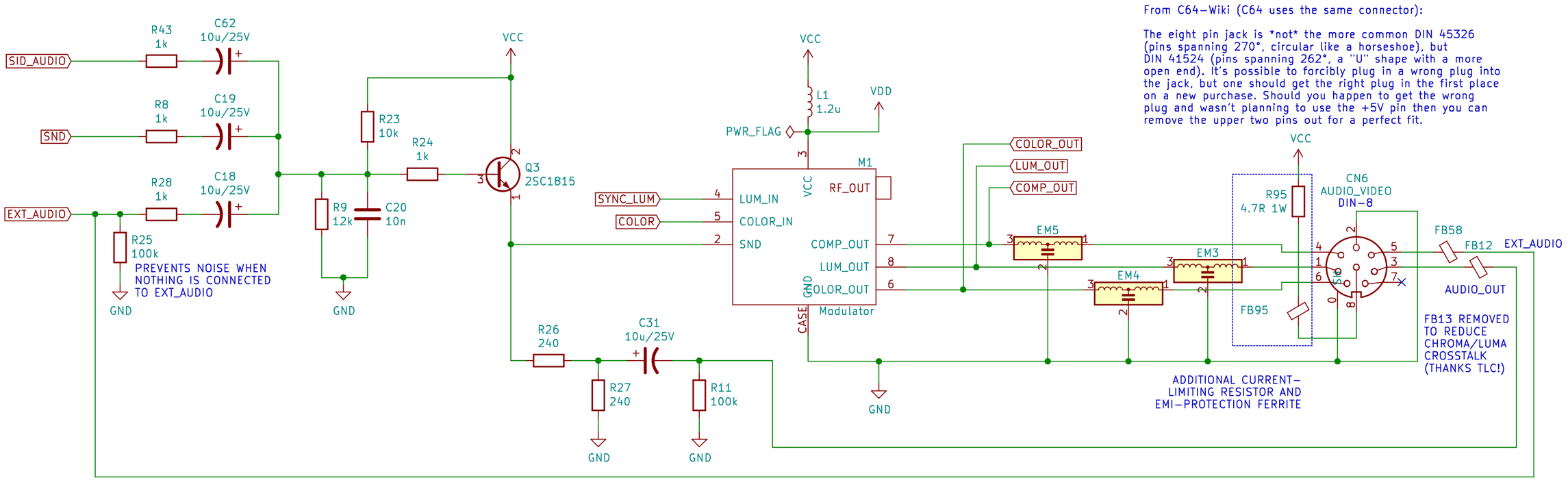
Size: A4	Date: 2021–11–05	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 10/14

This was one of the weakest spots of the C16, where the TED chip pins were directly exposed outside through the joystick ports.

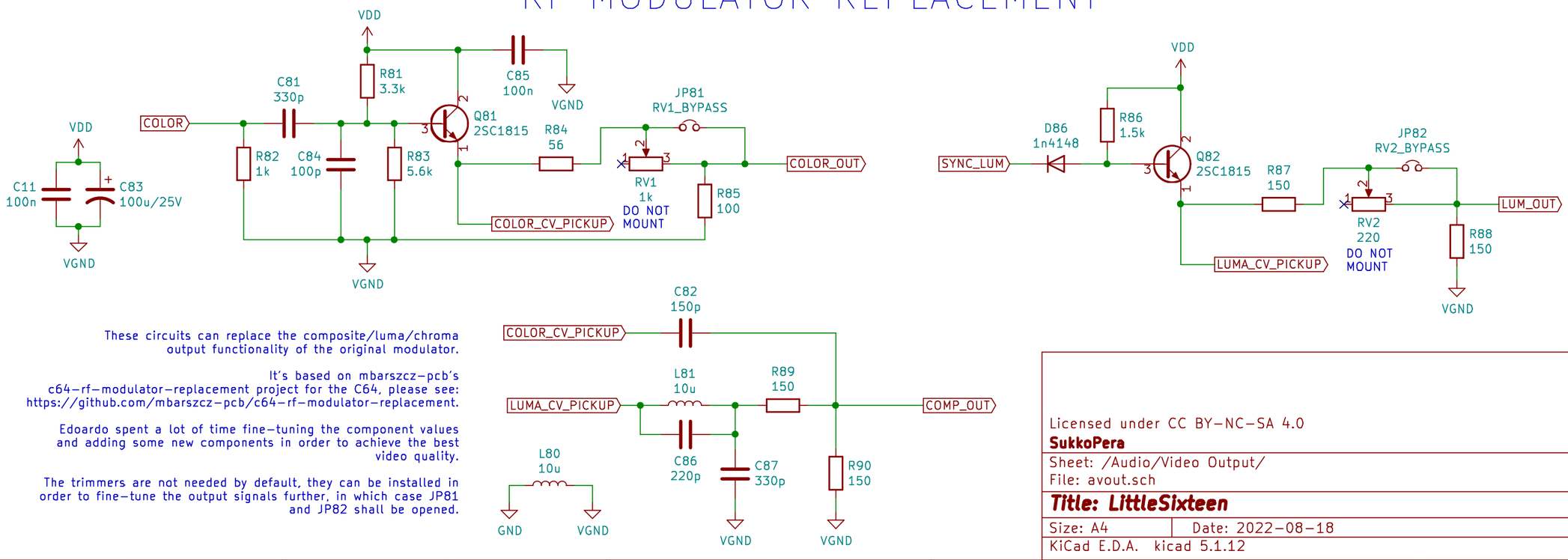
Adding a buffer will protect the TED from ESD, and TVS diodes could do even more. This is basically Levente Hársfalvi's design (changed to 74x245 just for our convenience) integrated into the C16. Please see:
http://www.zimmers.net/anonftp/pub/cbm/documents/projects/interfaces/plus4joy/plus4joy.html

VCC
R91 4.7R 1W
ADDITIONAL CURRENT-LIMITING RESISTOR
FB22
CN4 JOY1
JP9 JP_J1_POW5
5 f1r 8 3 f1l 7 2 f1d 6 f1f 1 f1u 0
FB24 FB25 FB26 FB27 FB28 FB29
1u 1d 1l 1r 1f
GND
JOY1
RP2 3.3k
VCC
U17
A0 A1 A2 A3 A4 A5 A6 A7 A->B CE
B0 B1 B2 B3 B4 B5 B6 B7 GND VCC
74HCT245
GND
The (apparently) odd connections here are to simplify routing!
100
RP90C RP90A RP90E RP90D RP90B
1N914
D5 D2 D1 D3 D4
b1f b1d b1u b1l b1r
k6 k1 k0 k2 k3
k[0..7]
k7
VCC
R92 4.7R 1W
ADDITIONAL CURRENT-LIMITING RESISTOR
FB30
CN5 JOY2
JP10 JP_J2_POW5
5 f2r 8 3 f2l 7 2 f2d 6 f2f 1 f2u 0
FB31 FB32 FB33 FB34 FB35 FB37
2u 2d 2l 2r 2f
GND
JOY2
RP5 3.3k
VCC
U18
A0 A1 A2 A3 A4 A5 A6 A7 A->B CE
B0 B1 B2 B3 B4 B5 B6 B7 GND VCC
74HCT245
GND
100
RP91C RP91A RP91E RP91D RP91B
1N914
D10 D7 D6 D8 D9
b2f b2d b2u b2l b2r
VCC
U93 DT1042
1 f2l 3 f2r 4 6
I/O1 I/O2 I/O3 I/O4 VCC GND
GND
VCC
U95 DT1042
f1f 1 f1u 3 f1l 4 f1d 6
I/O1 I/O2 I/O3 I/O4 VCC GND
GND
VCC
U94 DT1042
f2u 1 f1r 3 f2d 4 f2f 6
I/O1 I/O2 I/O3 I/O4 VCC GND
GND
VCC
C39 100n
GND
VCC
C40 100n
GND

SukkoPera
Sheet: /Joysticks/
File: joysticks.sch
Title: LittleSixteen
Size: A4 | Date: 2023-07-17 | **Rev: 4git**
KiCad E.D.A. kicad 5.1.12 | Id: 11/14



RF MODULATOR REPLACEMENT



These circuits can replace the composite/luma/chroma output functionality of the original modulator.

It's based on mbarszcz-pcb's c64-rf-modulator-replacement project for the C64, please see: https://github.com/mbarszcz-pcb/c64-rf-modulator-replacement.

Edoardo spent a lot of time fine-tuning the component values and adding some new components in order to achieve the best video quality.

The trimmers are not needed by default, they can be installed in order to fine-tune the output signals further, in which case JP81 and JP82 shall be opened.

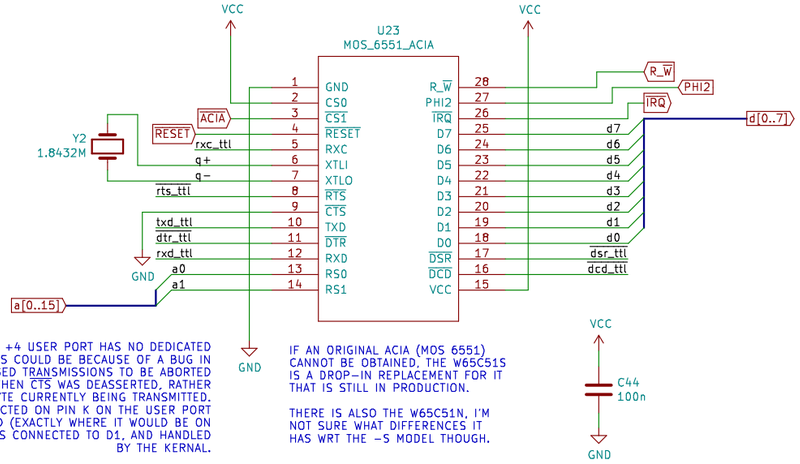
SukkoPera

Sheet: /Audio/Video Output/
File: avout.sch

Title: LittleSixteen

Size: A4	Date: 2022-08-18	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 12/14

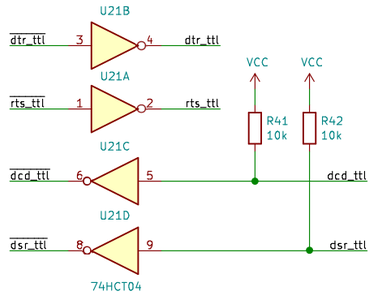
RS-232 INTERFACE (TTL LEVEL)



NOTE THAT THE +4 USER PORT HAS NO DEDICATED $\overline{\text{CTS}}$ PIN. THIS COULD BE BECAUSE OF A BUG IN THE 6551 THAT CAUSED TRANSMISSIONS TO BE ABORTED *IMMEDIATELY* WHEN $\overline{\text{CTS}}$ WAS DEASSERTED, RATHER THAN AFTER THE BYTE CURRENTLY BEING TRANSMITTED. THE SIGNAL IS EXPECTED ON PIN K ON THE USER PORT CONNECTOR INSTEAD (EXACTLY WHERE IT WOULD BE ON THE C64), WHICH IS CONNECTED TO D1, AND HANDLED BY THE KERNAL.

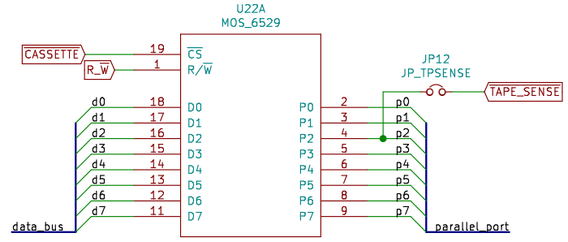
IF AN ORIGINAL ACIA (MOS 6551) CANNOT BE OBTAINED, THE W65C51S IS A DROP-IN REPLACEMENT FOR IT THAT IS STILL IN PRODUCTION.

THERE IS ALSO THE W65C51N, I'M NOT SURE WHAT DIFFERENCES IT HAS WRT THE -S MODEL THOUGH.

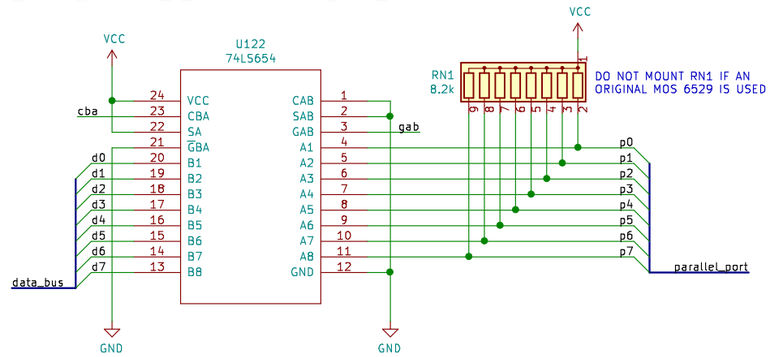


SOME CONTROL SIGNALS ARE INVERTED FOR HISTORICAL REASONS THAT DATE BACK TO THE VIC-1011A

''PARALLEL'' PORT

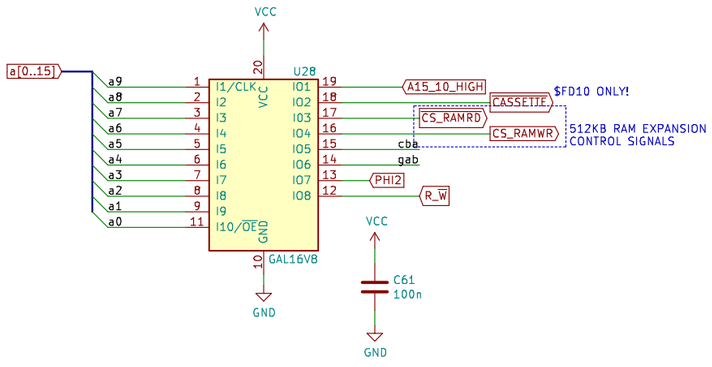


MOS 6529 REPLACEMENT CIRCUIT BY DANIËL MANTIONE



PLA - 3 -

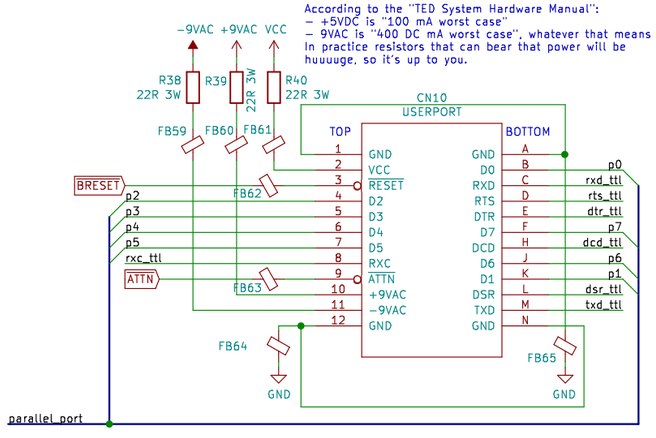
Generates:
- Control signals for the Hannes RAM Expansion register at $FD16
- $\overline{\text{CS}}$ for the User Port MOS 6529 (or replacement) at $FD10 only, named $\overline{\text{CASSETTE}}$ here
- Other control signals for the User Port MOS 6529 replacement circuit

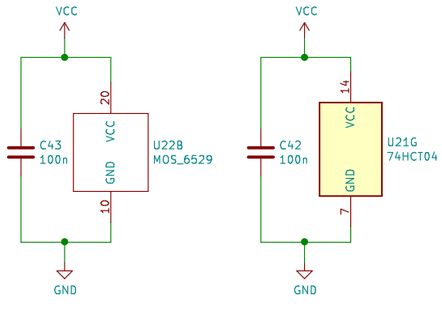


USER PORT CONNECTOR

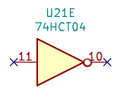
According to the ''TED System Hardware Manual'':
- +5VDC is ''100 mA worst case''
- 9VAC is ''400 DC mA worst case'', whatever that means

In practice resistors that can bear that power will be huuuuge, so it's up to you.





SPARES FOR LATER...



SukkoPera

Sheet: /User Port/
File: userport.sch

Title: LittleSixteen

Size: A3	Date: 2023-02-14	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 13/14

NOTE:

THE CIRCUIT ON THIS PAGE WAS HEAVILY DERIVED FROM THE RESEED PROJECT: https://github.com/SukkoPera/ReSeed.

PLEASE REFER TO THE PROJECT PAGE FOR DETAILS AND FURTHER INFORMATION.

AUDIO-STUFF IS USING A SEPARATE GROUND FOR NOISE ISOLATION

R1/2 APPROXIMATE THE ON-RESISTANCE OF THE CD4066 USED IN THE ORIGINAL C64 CIRCUIT IN ORDER TO HANDLE TWO PORTS

U24 MOS_8580

C45 22n

C46 22n

USE 470pF FOR 6581

RESET

sidclk

R_W

SID

a0 a1 a2 a3 a4

a[0..15]

CAP_1A CAP_1B CAP_2A CAP_2B RESET PHI2 R/W C5 A0 A1 A2 A3 A4 GND

VDD AUDIO_OUT AUDIO_IN VCC POTX POTY D7 D6 D5 D4 D3 D2 D1 D0

VTED VCC

C47 2.2n C48 2.2n

d[0..7]

R30 100 potx

R31 100 poty

audio_out

audio_in

R32 1k

MOUNT FOR MOS 6581 ONLY

R33 10k

C49 1n

C50 470p

VTED

C51 100n

Q6 2SC1815

R34 1k

RV3 10k

SID_AUDIO

THIS WILL BE MIXED WITH TED AUDIO, SO WE ALLOW VOLUME ADJUSTMENT

C52 10u

CN11 CONN_SID_OUTPUT

SID AUDIO OUTPUT CAN BE BROUGHT TO A DEDICATED JACK, BESIDES BEING MIXED WITH TED AUDIO

C53 100n

SW_DIGIFIX SW2

RV4 1M

R35 180k

R36 100k

CN12 CONN_SID_INPUT

AUDIO_IN CAN BE SHORTED TO GND IN ORDER TO AVOID NOISE OR BROUGHT TO AN EXTERNAL JACK IN ORDER TO PROVIDE ACTUAL AUDIO INPUT

L2 10u

PWR_FLAG

AUDIO GROUND CONNECTED TO POWER GROUND IN A SINGLE POINT THROUGH

C54 100n

C55 100n

AGND GND VTED VCC

SID CLOCK GENERATION

JP15 JMP_SIDCLK_SET

JP16 JMP_SIDCLK_RST

MUX

U21F 74HCT04

U25A 74LS74

R37 100

C57 470p

~886 kHz

sidclk

SIDCLK_TESTPOINT TP5

DELAY CIRCUIT

CLOCK GENERATION IS DONE DIFFERENTLY FROM RESEED, HERE WE USE A D-TYPE FLIP-FLOP IN A FREQUENCY DIVIDER CONFIGURATION. SINCE THE 74x74 IS TRIGGERED ON THE POSITIVE EDGE, WE NEED TO INVERT THE INPUT CLOCK IN ORDER TO HAVE THE OUTPUT SWITCH ON THE FALLING EDGE. THE FINAL RESULT IS THE SAME AS WITH THE CD4520 CIRCUIT WE USE ON RESEED AND WE SAVE ANOTHER FLIP-FLOP FOR OTHER PURPOSES.
IT'S HARD TO PREDICT IN ADVANCE WHERE THE RESET SIGNAL SHOULD GO, SO WE KEEP OPEN TO ALL POSSIBILITIES.
HINT: TO R SOUNDS BETTER.

C59 100n

U25C 74LS74

C60 470u/16V

ADDITIONAL DECOUPLING FOR IMPROVED STABILITY

ANALOG PADDLE/JOYSTICK PORT

ANY VALUE BETWEEN 3.3-10K SHOULD BE FINE

RN2 4.7k

RN3C RN3D RN3B RN3A RN3E 100

up left poty potx down right fire

CN14 CONN_JOY3

SERIES RESISTORS ADDED IN ORDER TO ALLOW SAFE WRITES TO THE PORT

U27 74HCT245

A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 A->B CE GND VCC

d0 d1 d2 d3 d4 d5 d6 d7

R_W JOY3

C58 100n

D5-7 ARE EXPECTED TO READ AS HIGH BY SOME SOFTWARE, EVEN THOUGH THEIR VALUE IS ACTUALLY MEANINGLESS...

SukkoPera

Sheet: /SID!/
File: sid.sch

Title: LittleSixteen

Size: A3	Date: 2023-02-16	Rev: 4git
KiCad E.D.A. kicad 5.1.12		Id: 14/14