Sheet: CPU

File: cpu.sch

Sheet: TED

File: ted.sch

Sheet: RAM

File: ram.sch

Sheet: ROMs

File: rom.sch

Sheet: Keyboard

File: keyboard.sch

Sheet: Datassette & Serial Bus

File: datasette.sch

Sheet: Expansion Port

File: exp_port.sch

Sheet: Power & Misc

File: misc.sch

Sheet: Joysticks

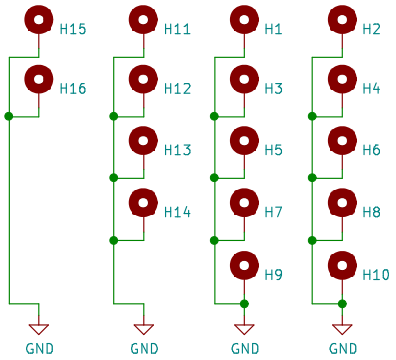
File: joysticks.sch

Sheet: PLA & Chip Selection

File: pla.sch

Sheet: Audio/Video Output

File: avout.sch



Sheet: User Port

File: userport.sch

Sheet: SID!

File: sid.sch

V0
LOGO

V1
PCBWAY_LOGO

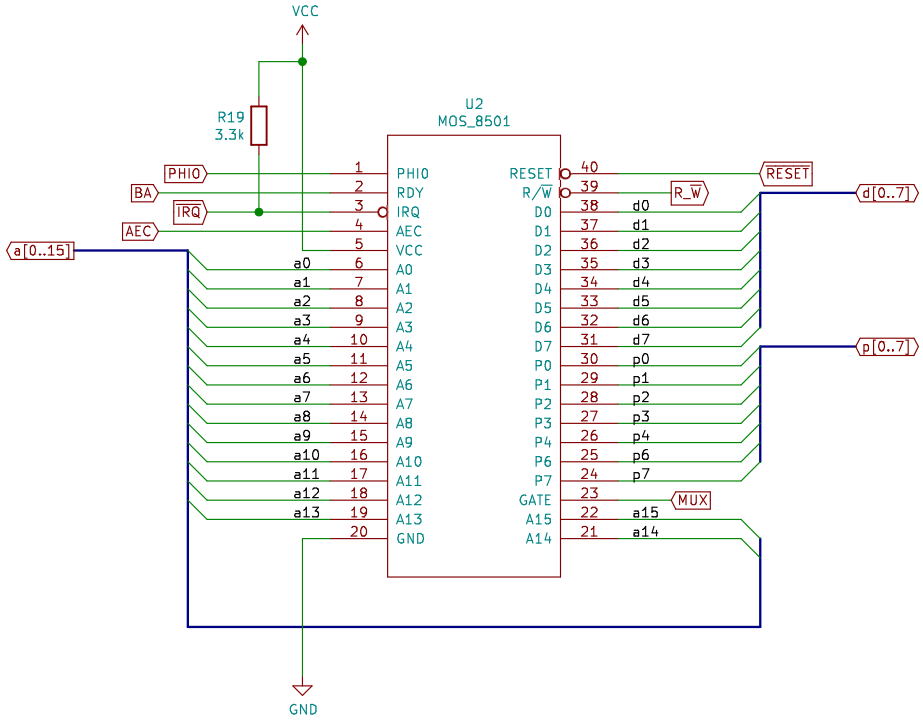
V2
CC BY-NC-SA 4.0

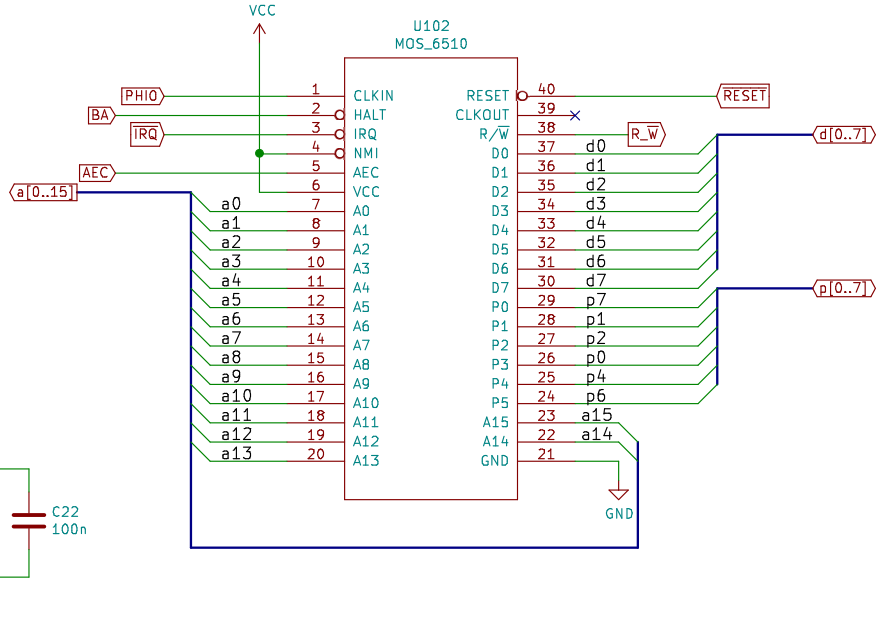
SukkoPera

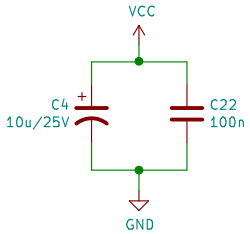
Sheet: /
File: LittleSixteen.sch

Title: LittleSixteen

Size: A4	Date: 2023-02-15	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 1/14







The 7501/8501 CPU used in the x264 series is not much different from the 6510 that was used in the C64. Mapping of most pins is straightforward. Some signals change names but they are obviously the same.

6510s were working at 1MHz in the C64, while the x264 design is able to push them to nearly 2 MHz during video blanking. Since most 6510s seem to be pretty forgiving in this regard, we are left with two issues:

- GATE_IN: There is a lot of myth and inaccuracy about the purpose of this pin that is not available on the 6510. Here's a quote from the TED System Hardware Manual that should clarify things:

  "GATE IN: TTL level input, used to gate the R/W line to prevent the R/W line from going low during a read cycle, before RAS and CAS go high (resulting in a Read/Write cycle). Normally connected to the MUX line in a system configuration to synchronize the DRAM memory cycle to the processor clock cycle.

  If AEC is low when Gate In makes a low to high transition, the R/W line will go to a high impedence until the next transition of the Gate In line and AEC is high prior to the transition."

  This is confirmed by some guys who recently decapped an 8501 and analyzed its die, please see http://forum.6502.org/viewtopic.php?f=4&t=6617.

  A forum thread (http://www.softwolves.com/arkiv/cbm-hackers/16/16855.html) seems to suggest that when using DRAMs the signal is pretty useless, but it would be needed if SRAMs were used. I'm not sure this is correct and I really can't judge by myself, but since experience shows that leaving GATE_IN unconnected doesn't *seem* to hurt, we'll go with that for the moment, but for the future we might do something along the lines of this quote from Bil Herd himself:

  "[During the development of the x264 family, where we were using 6510 CPUs] I think I did the Gated Read/Write with a 74LS73 only I drove the R/W line high, not HiZ."

- I/O Port: The 8501 has a 7-bit I/O port while the 6510 only has a 6-bit, plus the exposed bits are numbered differently, so some remapping is needed, which implies that some modding to the KERNAL is required as well. I decided to follow what Andrew Challis did at http://hackjunk.com/2017/06/23/commodore-16-plus-4-8501-to-6510-cpu-conversion/. So, the 6510 socket is basically Andy's adapter built into the mainboard. If you go with a 6510 you will need to use his modified KERNAL and to solder the diode and resistor at D/R93. This comes at a compromise though:
  - Disk fastloaders will not work (unless they are modified themselves to match our pin shuffling).
  - The Datassette motor will spin whenever one of its keys is pressed, the computer will no longer be able to control it.

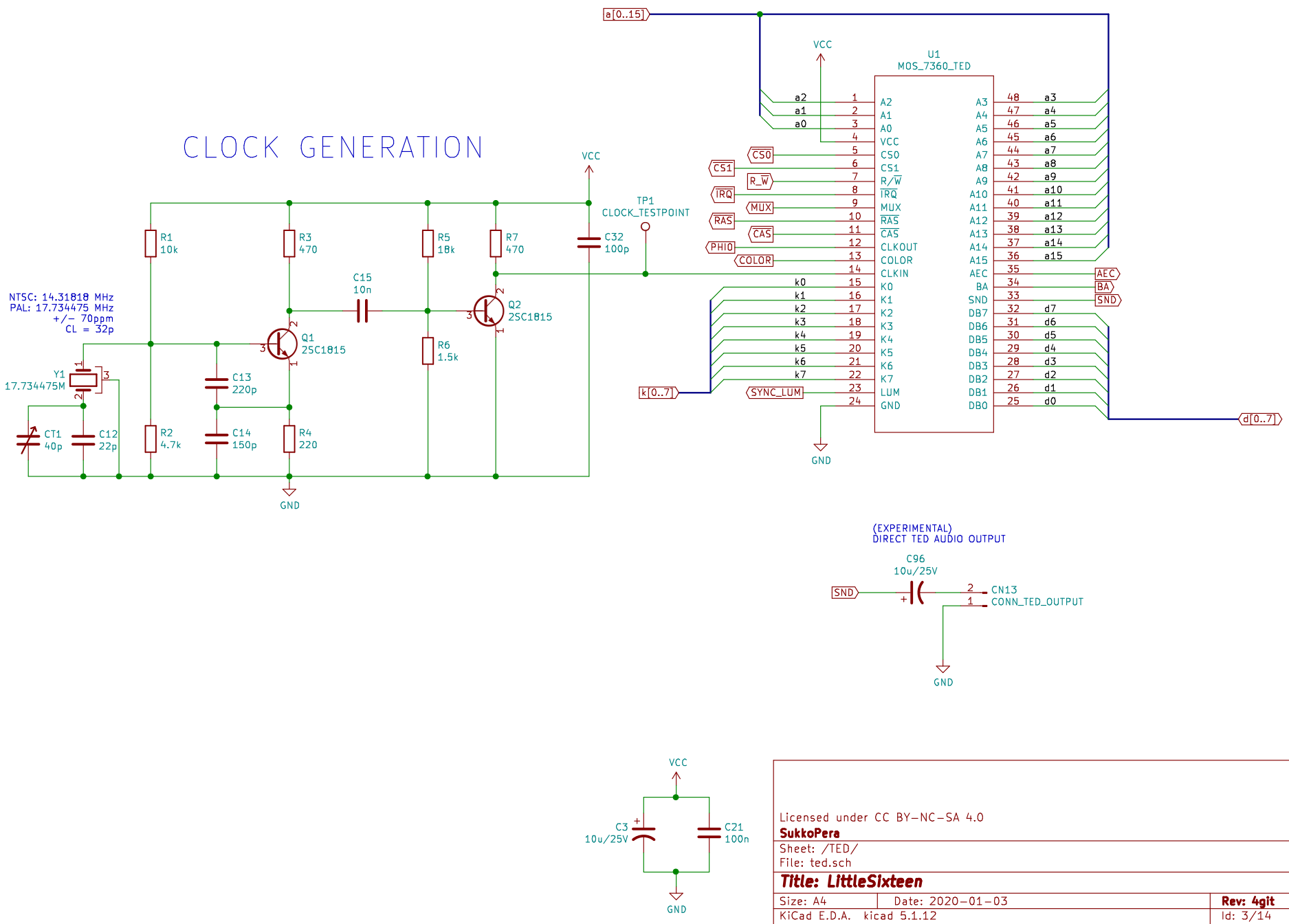
  I think these drawbacks are acceptable, as most fastloaders won't work anyway when using an SD2IEC, which is what most people do these days, I guess, while the loss of tape control isn't much of an issue in itself. Make sure to send a small donation to Andy if you go this way.

SukkoPera

Sheet: /CPU/
File: cpu.sch

Title: LittleSixteen

Size: A4	Date: 2021-11-17	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 2/14



SukkoPera

Sheet: /TED/
File: ted.sch

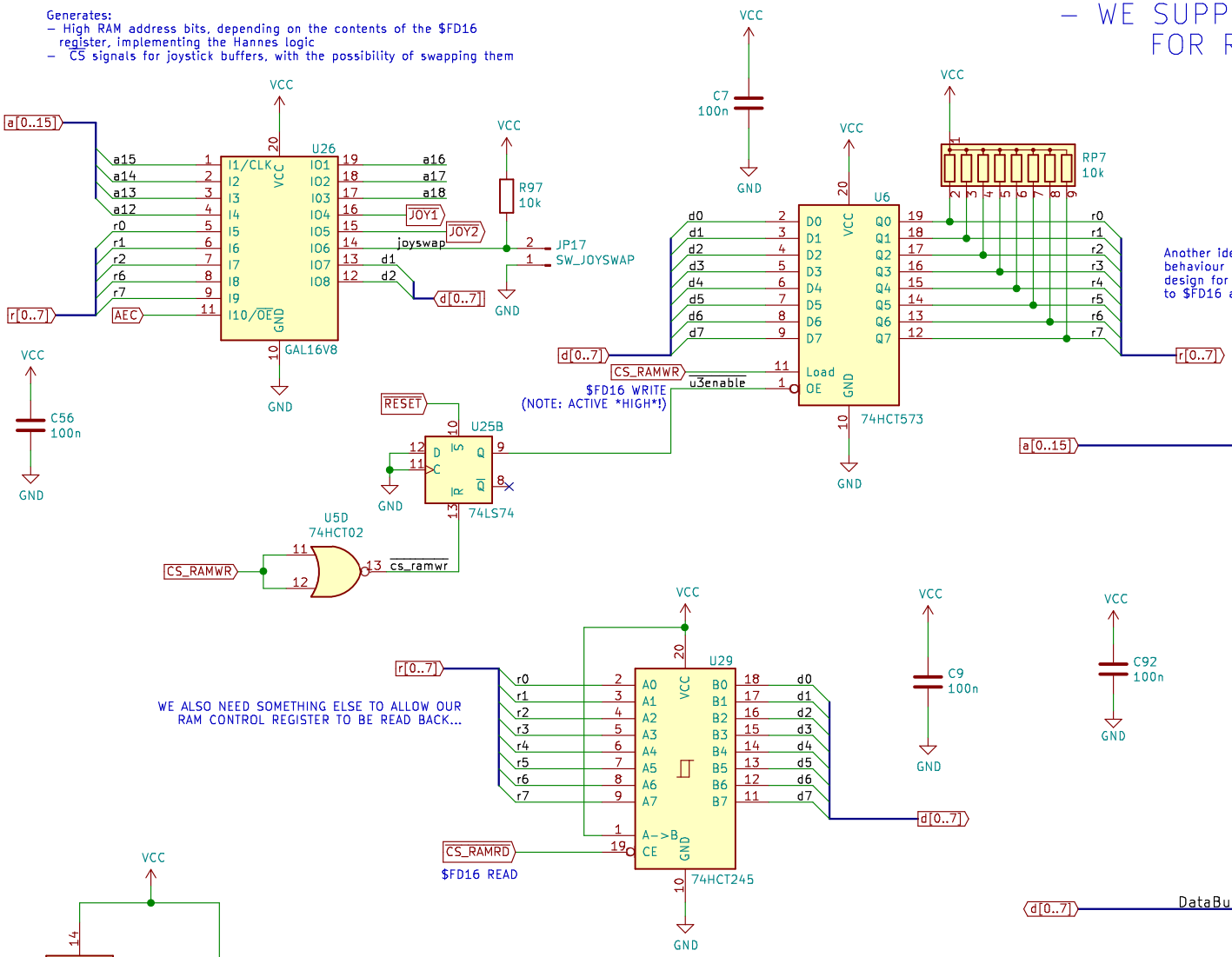
Title: LittleSixteen

Size: A4	Date: 2020-01-03	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 3/14

PLA – 2 –

Generates:
– High RAM address bits, depending on the contents of the $FD16 register, implementing the Hannes logic
– CS signals for joystick buffers, with the possibility of swapping them

– WE USE A SINGLE STATIC RAM CHIP
– WE SUPPORT A HANNES–STYLE MECHANISM FOR RAM EXPANSION TO UP TO 512 KB

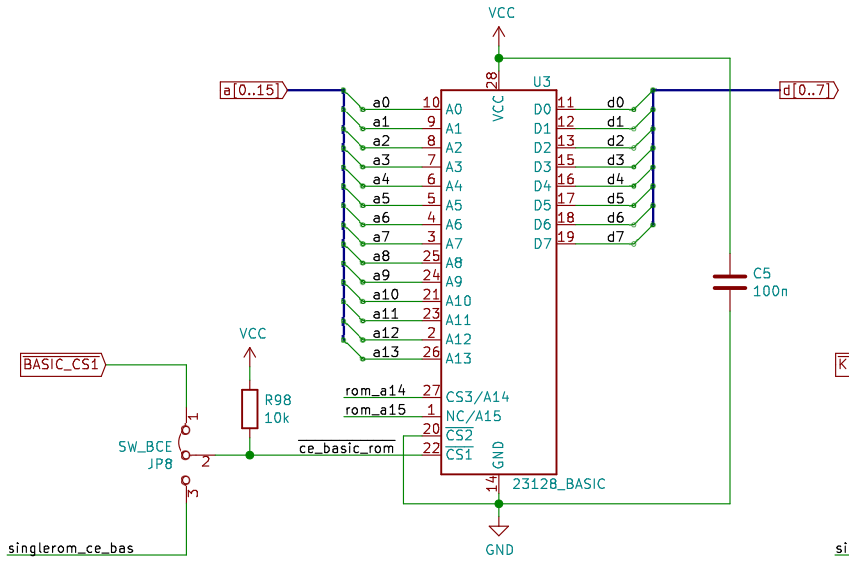


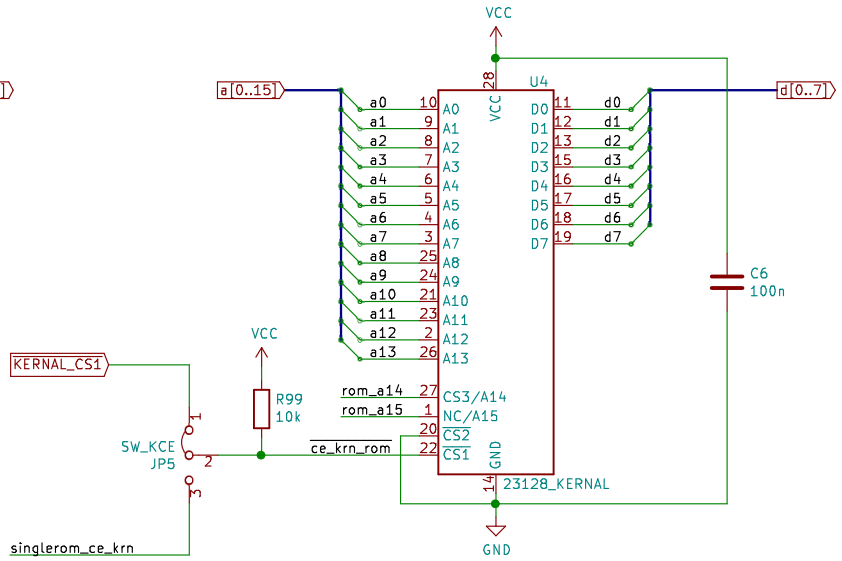
SukkoPera

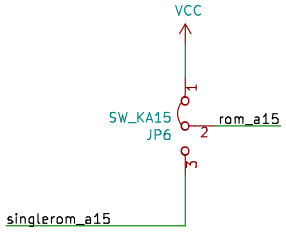
Sheet: /RAM/
File: ram.sch

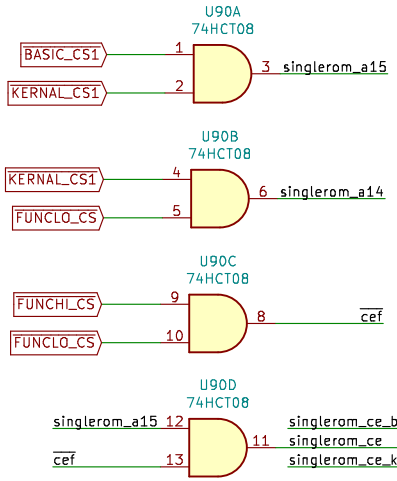
Title: LittleSixteen

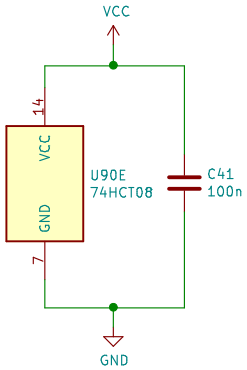
Size: A4	Date: 2023–07–10	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 4/14











Range	Size	A15	A14	Content
$0000–$3FFF	16K	0	0	Kernal
$4000–$7FFF	16K	0	1	Basic
$8000–$BFFF	16K	1	0	FnLO
$C000–$FFFF	16K	1	1	FnHI

A15 = /CEK & /CEB
A14 = /CEK & /CEFL
/CEF = /CEFL & /CEFH
/CE = /CEK & /CEB & /CEF = A15 & /CEF

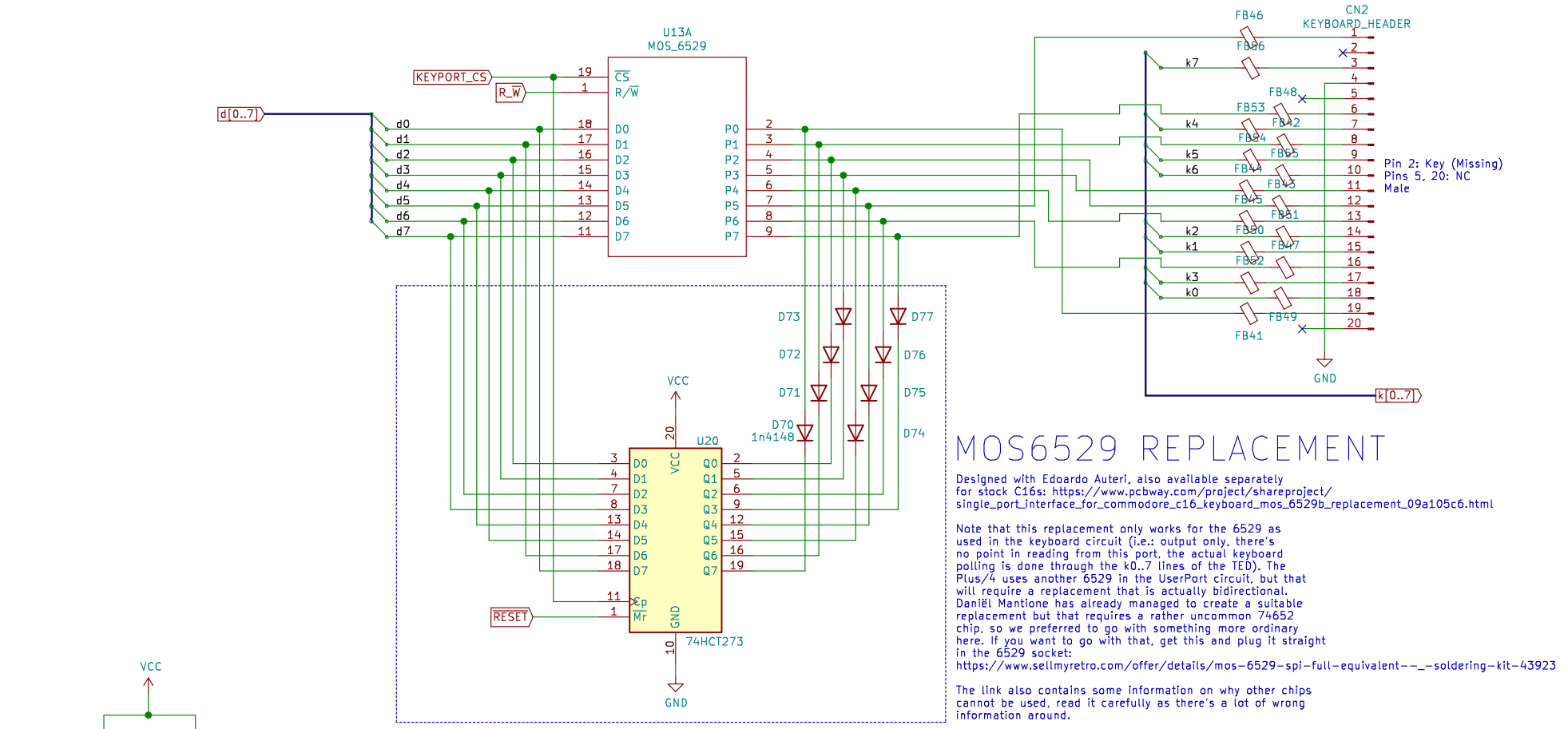
/CEK	/CEB	/CEFL	/CEFH	A15	A14	/CEF	/CE
0	1	1	1	0	0	1	0
1	0	1	1	0	1	1	0
1	1	0	1	1	0	0	0
1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	1

SukkoPera

Sheet: /ROMs/
File: rom.sch

Title: LittleSixteen

Size: A4	Date: 2023-07-30	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 5/14



MOS6529 REPLACEMENT

Designed with Edoardo Auteri, also available separately
for stock C16s: https://www.pcbway.com/project/shareproject/
single_port_interface_for_commodore_c16_keyboard_mos_6529b_replacement_09a105c6.html

Note that this replacement only works for the 6529 as
used in the keyboard circuit (i.e.: output only, there's
no point in reading from this port, the actual keyboard
polling is done through the k0..7 lines of the TED). The
Plus/4 uses another 6529 in the UserPort circuit, but that
will require a replacement that is actually bidirectional.
Daniël Mantione has already managed to create a suitable
replacement but that requires a rather uncommon 74652
chip, so we preferred to go with something more ordinary
here. If you want to go with that, get this and plug it straight
in the 6529 socket:
https://www.sellmyretro.com/offer/details/mos-6529-spi-full-equivalent---_-soldering-kit-43923

The link also contains some information on why other chips
cannot be used, read it carefully as there's a lot of wrong
information around.

SukkoPera

Sheet: /Keyboard/
File: keyboard.sch

Title: LittleSixteen

Size: A4	Date: 2022-08-17	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 6/14

DATASSETTE INTERFACE

These are protection diodes retrofitted after production on *some* C16s I've seen. These seem different from the 1n4148 that are retrofitted on p6/p7 on the same board, since those clearly say 1n4148 on their bodies, while these have a color coding of yellow (thick/cathode), brown, yellow, grey (or light blue?), which... erm, would make them 1n4148 ^___^. Multimeter says their Voltage drops are 0.555V and 0.561V, while it says 0.323 for the others (all measures in-circuit).

ADDITIONAL CURRENT-LIMITING RESISTOR

WARNING: The drawing of this connector does not match the real connector exactly!

CST_SENSE: LOW if one of the keys PLAY, RECORD, F.FWD or REW is pressed, HIGH otherwise

This diode is the one Andrew Challis recommends in order to let the Datassette motor run only when one of its keys is pressed. We add a pull-up resistor just in case. Install both only when using a 6510 CPU. (He says FB15 on his page but it's a clear mistake.)

CST_MTR: LOW = Motor on HIGH = Motor off

CN93 C64_STYLE_CASSETTE

SERIAL BUS (OR 1541 DISK DRIVE)

These (and the ones below) are more retrofitted protection diodes, these are present on most C16s I've seen. Note that these protection diodes have been added on all pins going straight to the CPU from the outside world.

These protection diodes are usually installed in place of ferrites FB3 and FB4.

These offer better ESD protection than the retrofitted diodes, but use an SMT component. Mount only one or the other, at your preference.

NOTES:
- Fastloaders might use these signals differently!
- All signals are active-low
- All signals are open collector, since this is a *bus*

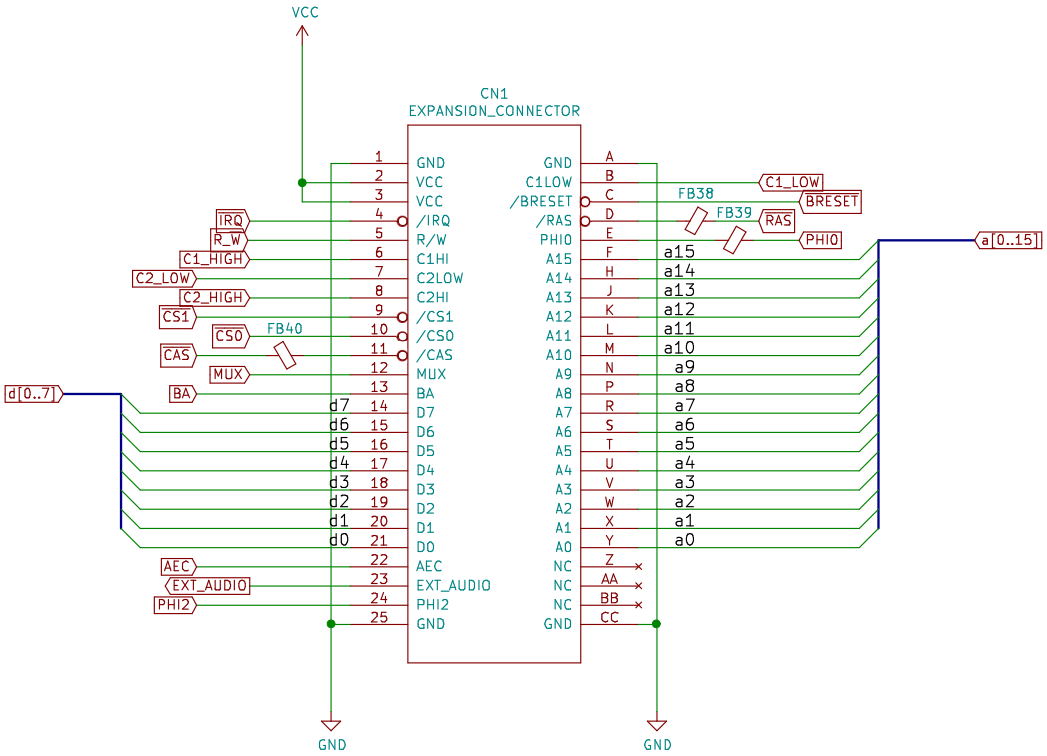
These connectors have all the Tape and IEC signals and can be used to implement an internal SD2IEC and Tapuino.

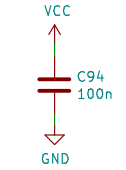
SukkoPera

Sheet: /Datassette & Serial Bus/
File: datasette.sch

Title: LittleSixteen

Size: A4	Date: 2023-07-25	Rev: 4git
KiCad E.D.A. kicad 5.1.12		Id: 7/14



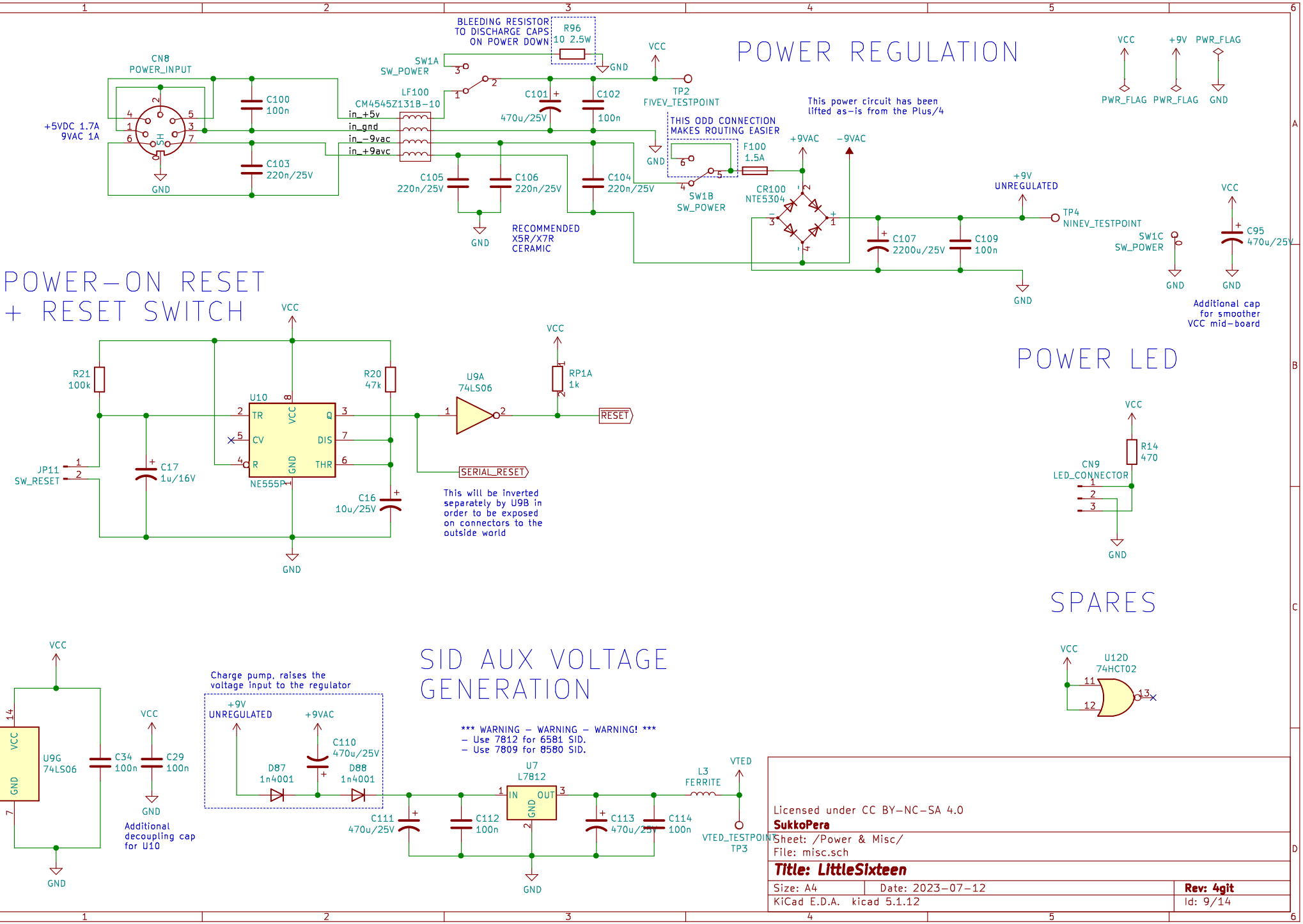


SukkoPera

Sheet: /Expansion Port/
File: exp_port.sch

Title: LittleSixteen

Size: A4	Date: 2021-12-05	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 8/14

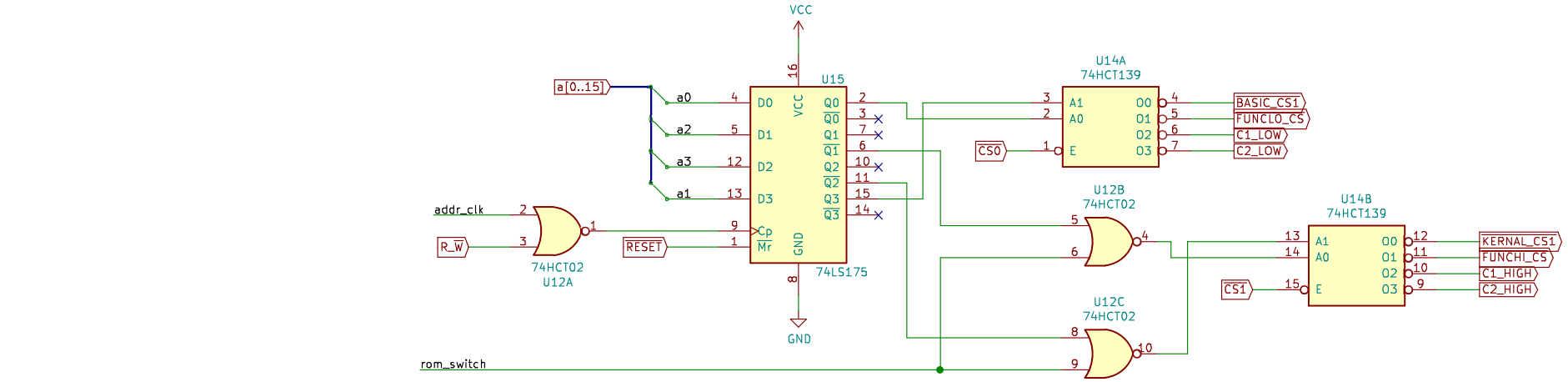


SukkoPera

Sheet: /Power & Misc/
File: misc.sch

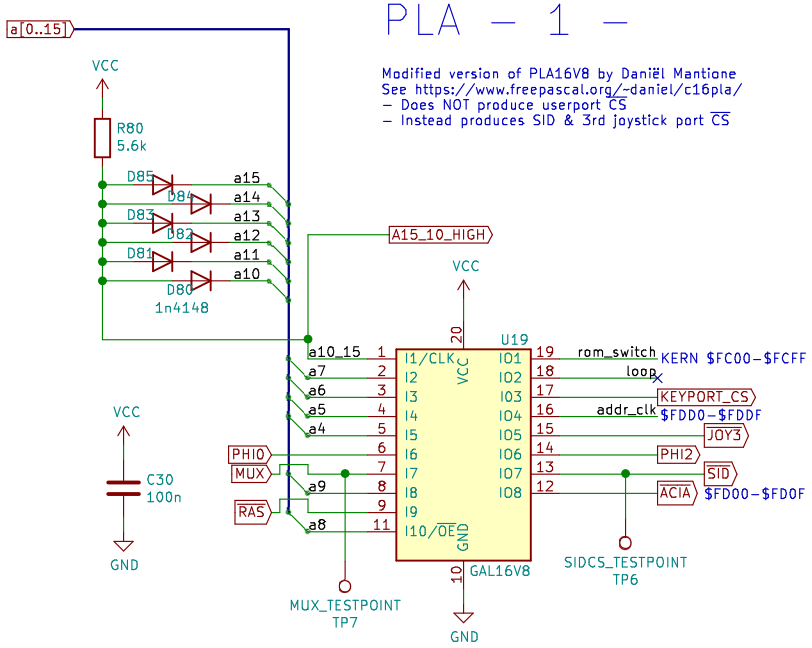
Title: LittleSixteen

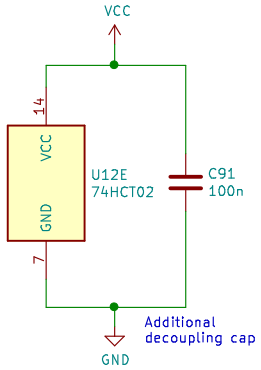
Size: A4	Date: 2023−07−12	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 9/14

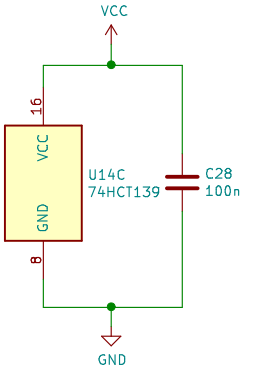


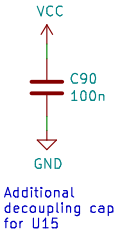
PLA – 1 –

Modified version of PLA16V8 by Daniël Mantione
See https://www.freepascal.org/~daniel/c16pla/
– Does NOT produce userport CS
– Instead produces SID & 3rd joystick port CS







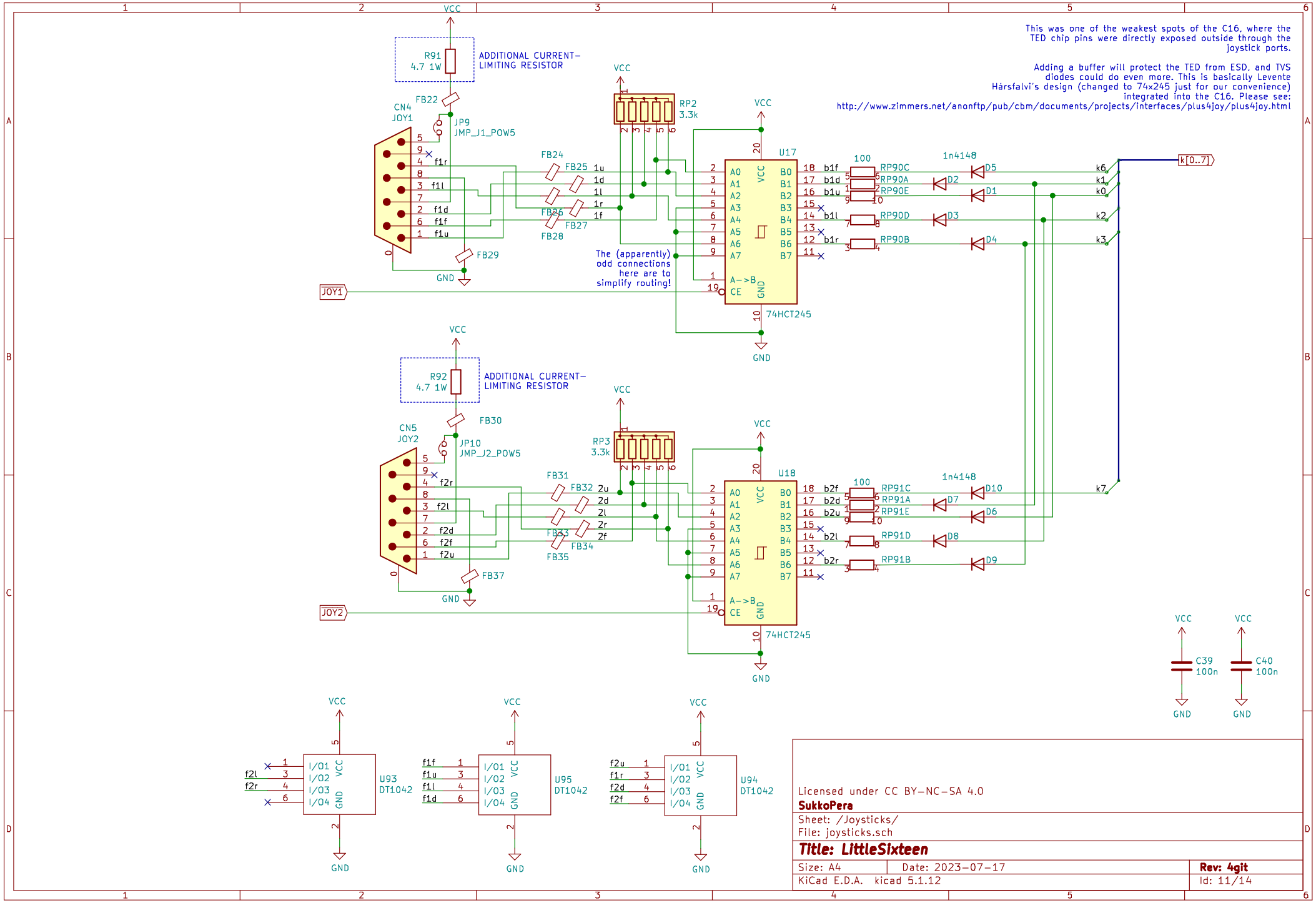


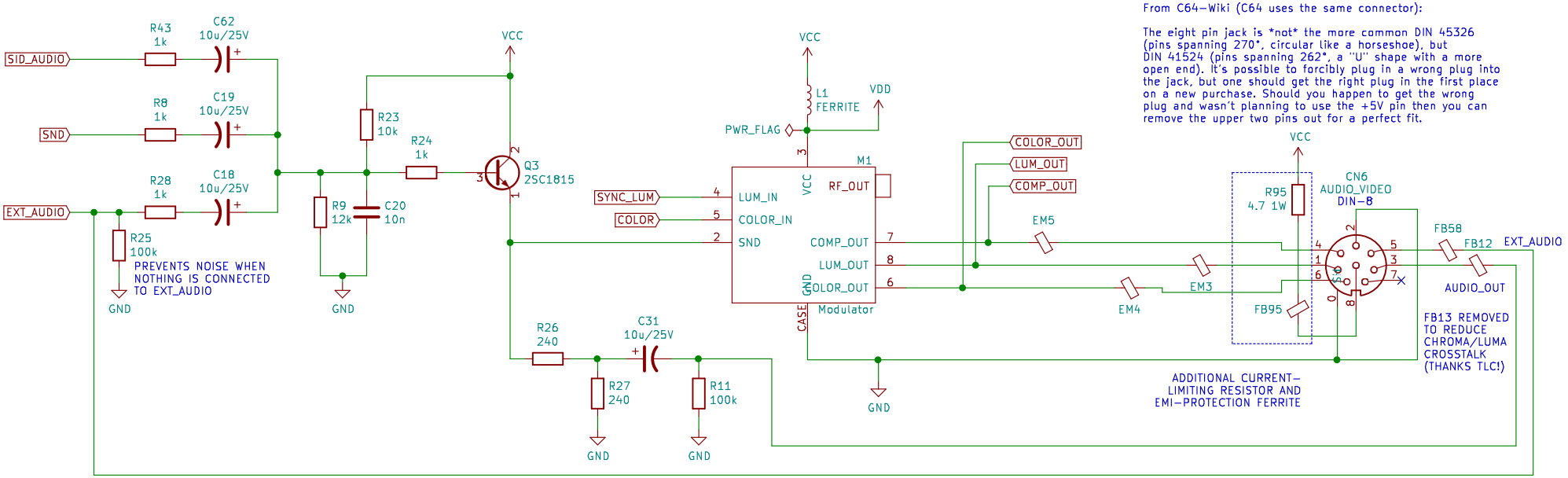
SukkoPera

Sheet: /PLA & Chip Selection/
File: pla.sch

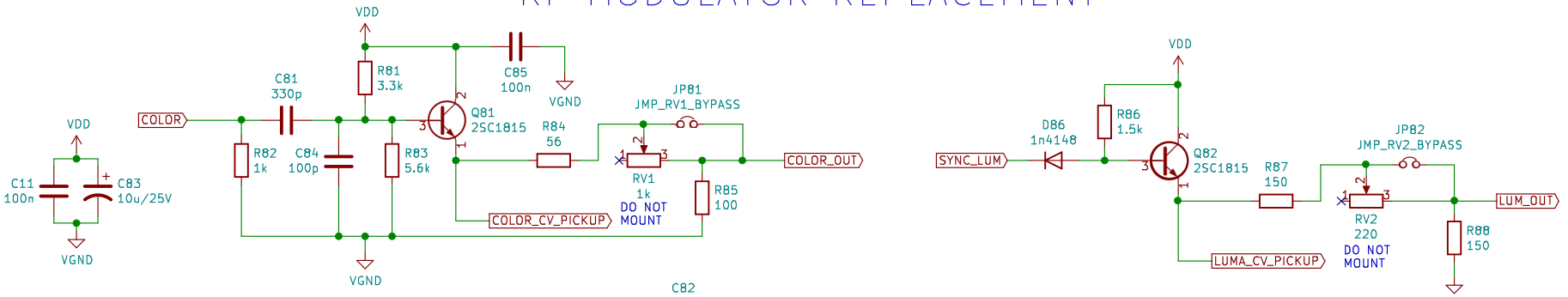
Title: LittleSixteen

Size: A4	Date: 2021–11–05	**Rev: 4git**
KiCad E.D.A. kicad 5.1.12		Id: 10/14


This was one of the weakest spots of the C16, where the TED chip pins were directly exposed outside through the joystick ports.
Adding a buffer will protect the TED from ESD, and TVS diodes could do even more. This is basically Levente Hársfalvi's design (changed to 74x245 just for our convenience) integrated into the C16. Please see:
http://www.zimmers.net/anonftp/pub/cbm/documents/projects/interfaces/plus4joy/plus4joy.html
VCC
R91
4.7 1W
ADDITIONAL CURRENT-LIMITING RESISTOR
CN4
JOY1
JP9
JMP_J1_POW5
FB22
RP2
3.3k
U17
74HCT245
100
1n4148
RP90C
RP90A
RP90E
RP90D
RP90B
D5
D2
D1
D3
D4
k[0..7]
k6
k1
k0
k2
k3
FB24
FB25
FB26
FB27
FB28
FB29
1u
1d
1l
1r
1f
b1f
b1d
b1u
b1l
b1r
The (apparently) odd connections here are to simplify routing!
JOY1
GND
R92
4.7 1W
ADDITIONAL CURRENT-LIMITING RESISTOR
CN5
JOY2
JP10
JMP_J2_POW5
FB30
RP3
3.3k
U18
74HCT245
RP91C
RP91A
RP91E
RP91D
RP91B
D10
D7
D6
D8
D9
k7
FB31
FB32
FB33
FB34
FB35
FB37
2u
2d
2l
2r
2f
b2f
b2d
b2u
b2l
b2r
JOY2
C39
100n
C40
100n
U93
DT1042
U95
DT1042
U94
DT1042
I/O1
I/O2
I/O3
I/O4
Licensed under CC BY-NC-SA 4.0
SukkoPera
Sheet: /Joysticks/
File: joysticks.sch
Title: LittleSixteen
Size: A4
Date: 2023-07-17
Rev: 4git
KiCad E.D.A. kicad 5.1.12
Id: 11/14



RF MODULATOR REPLACEMENT



These circuits can replace the composite/luma/chroma output functionality of the original modulator.

It's based on mbarszcz-pcb's c64-rf-modulator-replacement project for the C64, please see: https://github.com/mbarszcz-pcb/c64-rf-modulator-replacement.

Edoardo spent a lot of time fine-tuning the component values and adding some new components in order to achieve the best video quality.

The trimmers are not needed by default, they can be installed in order to fine-tune the output signals further, in which case JP81 and JP82 shall be opened.

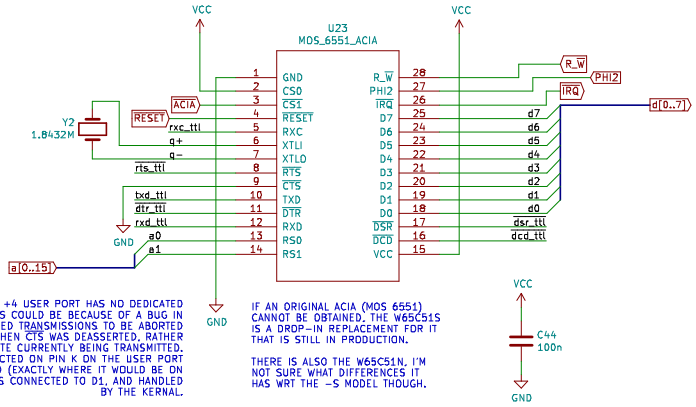
SukkoPera

Sheet: /Audio/Video Output/
File: avout.sch

Title: LittleSixteen

Size: A4	Date: 2022-08-18	Rev: 4git
KiCad E.D.A. kicad 5.1.12		Id: 12/14

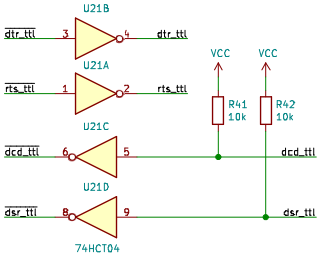
RS-232 INTERFACE (TTL LEVEL)



NOTE THAT THE +4 USER PORT HAS NO DEDICATED CTS PIN. THIS COULD BE BECAUSE OF A BUG IN THE 6551 THAT CAUSED TRANSMISSIONS TO BE ABORTED *IMMEDIATELY* WHEN CTS WAS DEASSERTED, RATHER THAN AFTER THE BYTE CURRENTLY BEING TRANSMITTED. THE SIGNAL IS EXPECTED ON PIN K ON THE USER PORT CONNECTOR INSTEAD (EXACTLY WHERE IT WOULD BE ON THE C64), WHICH IS CONNECTED TO D1, AND HANDLED BY THE KERNAL.

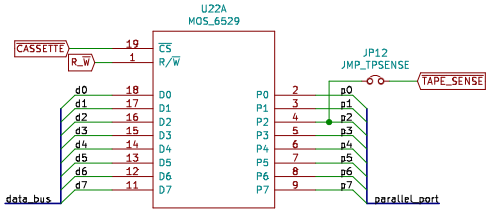
IF AN ORIGINAL ACIA (MOS 6551) CANNOT BE OBTAINED, THE W65C51S IS A DROP-IN REPLACEMENT FOR IT THAT IS STILL IN PRODUCTION.

THERE IS ALSO THE W65C51N, I'M NOT SURE WHAT DIFFERENCES IT HAS WRT THE -S MODEL THOUGH.

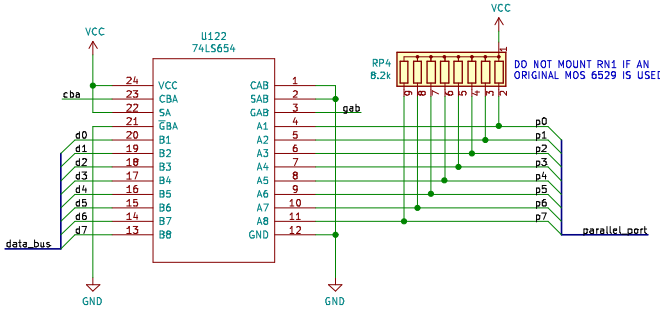


SOME CONTROL SIGNALS ARE INVERTED FOR HISTORICAL REASONS THAT DATE BACK TO THE VIC-1011A

"PARALLEL" PORT

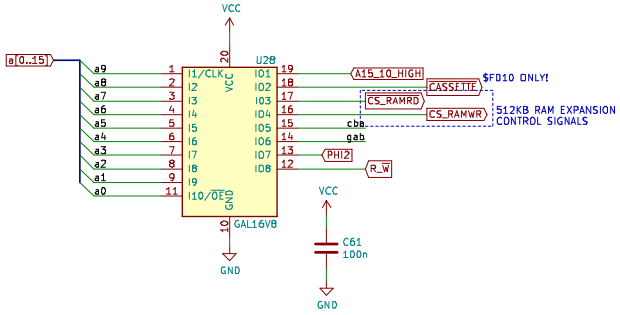


MOS 6529 REPLACEMENT CIRCUIT BY DANIËL MANTIONE



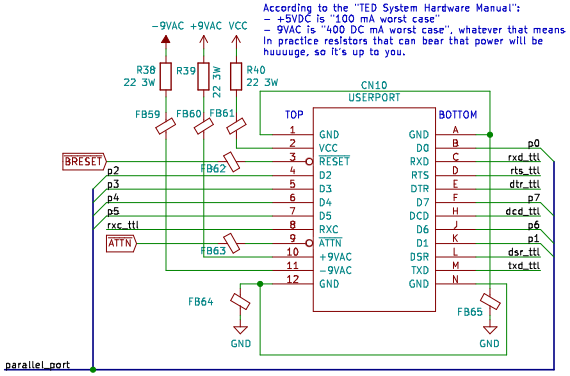
PLA — 3 —

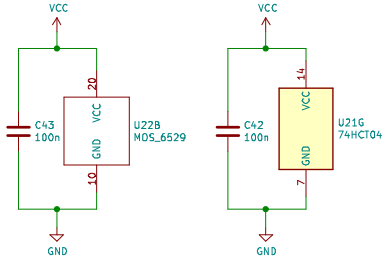
Generates:
- Control signals for the Hannes RAM Expansion register at $FD16
- CS for the User Port MOS 6529 (or replacement) at $FD10 only, named CASSETTE here
- Other control signals for the User Port MOS 6529 replacement circuit



USER PORT CONNECTOR

According to the "TED System Hardware Manual":
- +5VDC is "100 mA worst case"
- 9VAC is "400 DC mA worst case", whatever that means in practice resistors that can bear that power will be huuuuge, so it's up to you.





SPARES FOR LATER...

SukkoPera

Sheet: /User Port/
File: userport.sch

Title: LittleSixteen

Size: A3	Date: 2023-02-14	Rev: 4g1t
KiCad E.D.A. kicad 5.1.12		Id: 13/14

NOTE:

THE CIRCUIT ON THIS PAGE WAS HEAVILY DERIVED FROM THE RESEED PROJECT: https://github.com/SukkoPera/ReSeed.

PLEASE REFER TO THE PROJECT PAGE FOR DETAILS AND FURTHER INFORMATION.

AUDIO-STUFF IS USING A SEPARATE GROUND FOR NOISE ISOLATION

R1/2 APPROXIMATE THE ON-RESISTANCE OF THE CD4066 USED IN THE ORIGINAL C64 CIRCUIT IN ORDER TO HANDLE TWO PORTS

USE 470pF FOR 6581

MOUNT FOR MOS 6581 ONLY

THIS WILL BE MIXED WITH TED AUDIO, SO WE ALLOW VOLUME ADJUSTMENT

SID AUDIO OUTPUT CAN BE BROUGHT TO A DEDICATED JACK, BESIDES BEING MIXED WITH TED AUDIO

AUDIO_IN CAN BE SHORTED TO GND IN ORDER TO AVOID NOISE OR BROUGHT TO AN EXTERNAL JACK IN ORDER TO PROVIDE ACTUAL AUDIO INPUT

AUDIO GROUND CONNECTED TO POWER GROUND IN A SINGLE POINT THROUGH

SID CLOCK GENERATION

CLOCK GENERATION IS DONE DIFFERENTLY FROM RESEED, HERE WE USE A D-TYPE FLIP-FLOP IN A FREQUENCY DIVIDER CONFIGURATION. SINCE THE 74x74 IS TRIGGERED ON THE POSITIVE EDGE, WE NEED TO INVERT THE INPUT CLOCK IN ORDER TO HAVE THE OUTPUT SWITCH ON THE FALLING EDGE. THE FINAL RESULT IS THE SAME AS WITH THE CD4520 CIRCUIT WE USE ON RESEED AND WE SAVE ANOTHER FLIP-FLOP FOR OTHER PURPOSES.
IT'S HARD TO PREDICT IN ADVANCE WHERE THE RESET SIGNAL SHOULD GO, SO WE KEEP OPEN TO ALL POSSIBILITIES.
HINT: TO R SOUNDS BETTER.

ADDITIONAL DECOUPLING FOR IMPROVED STABILITY

ANALOG PADDLE/JOYSTICK PORT

ANY VALUE BETWEEN 3.3-10K SHOULD BE FINE

SERIES RESISTORS ADDED IN ORDER TO ALLOW SAFE WRITES TO THE PORT

D5-7 ARE EXPECTED TO READ AS HIGH BY SOME SOFTWARE, EVEN THOUGH THEIR VALUE IS ACTUALLY MEANINGLESS...

SukkoPera	
Sheet: /SID!/	
File: sid.sch	
Title: LittleSixteen	
Size: A3	Date: 2023-02-16
KiCad E.D.A. kicad 5.1.12	Rev: 4g1t
	Id: 14/14