Project Report

Adiabatic Logic: An Alternative Approach To Low Power Application Circuits

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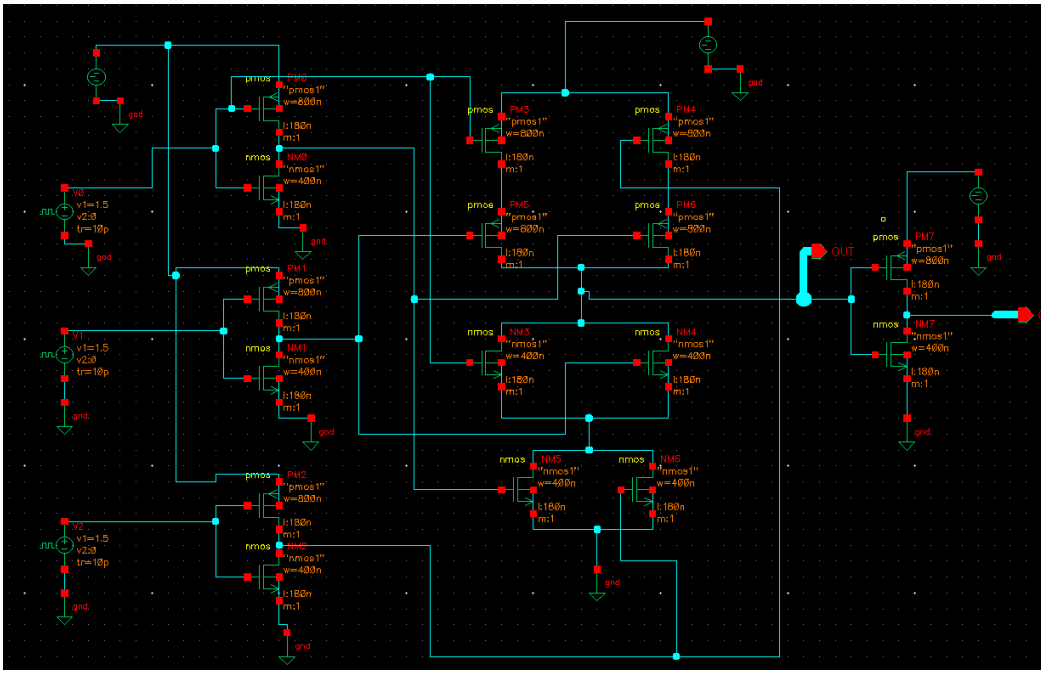
1. ABSTRACT

Over the last few decades, integrated circuit technology has fuelled enormous development in the electronics industry. Power dissipation has become a serious concern as the use of portable electronic devices has grown. It may become increasingly difficult to supply cooling as the density and size of the chips in the system rise, resulting in a considerable increase in the system's cost. That is why, even when numerous components are integrated on a single chip, we require circuitry that reduces power dissipation. In a digital CMOS circuit, we want to decrease power dissipation. To decrease power dissipation, several approaches are employed. The circuit is energy is regenerated in adiabatic logic, whereas energy is squandered in other techniques.

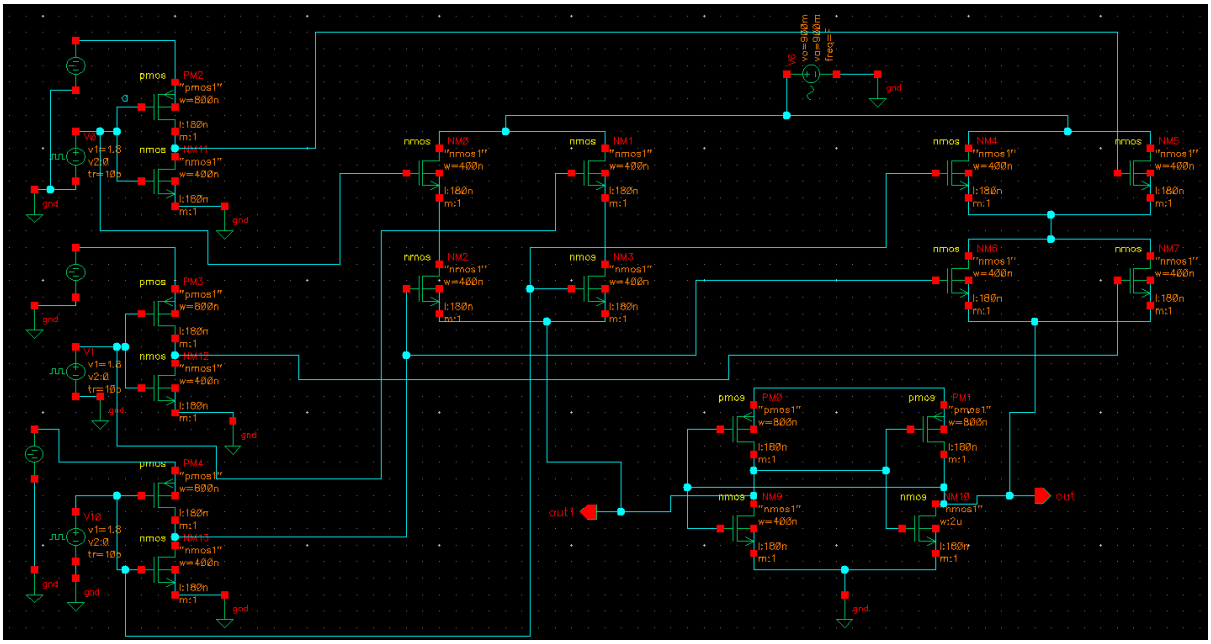
There are two types of adiabatic logic: partly adiabatic and fully adiabatic. Some of the circuits are power is squandered in partly adiabatic logic circuits. Energy is regenerated in completely adiabatic circuits (all charges are recovered). We use PFAL (positive feedback adiabatic logic), a partly adiabatic logic, to mimic mux, sum, and adder in this project.

2. CIRCUIT SCHEMATICS :



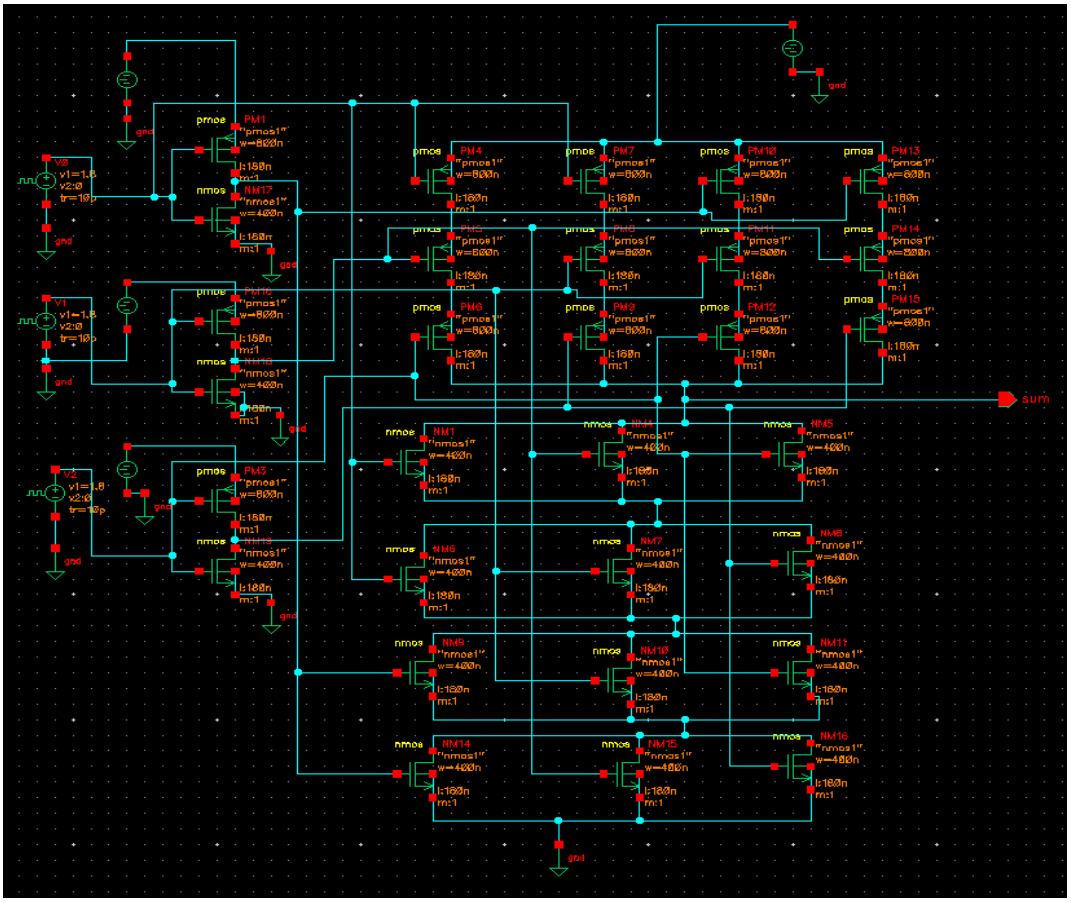
2x1 MUX USING CMOS LOGIC

(180 nm)



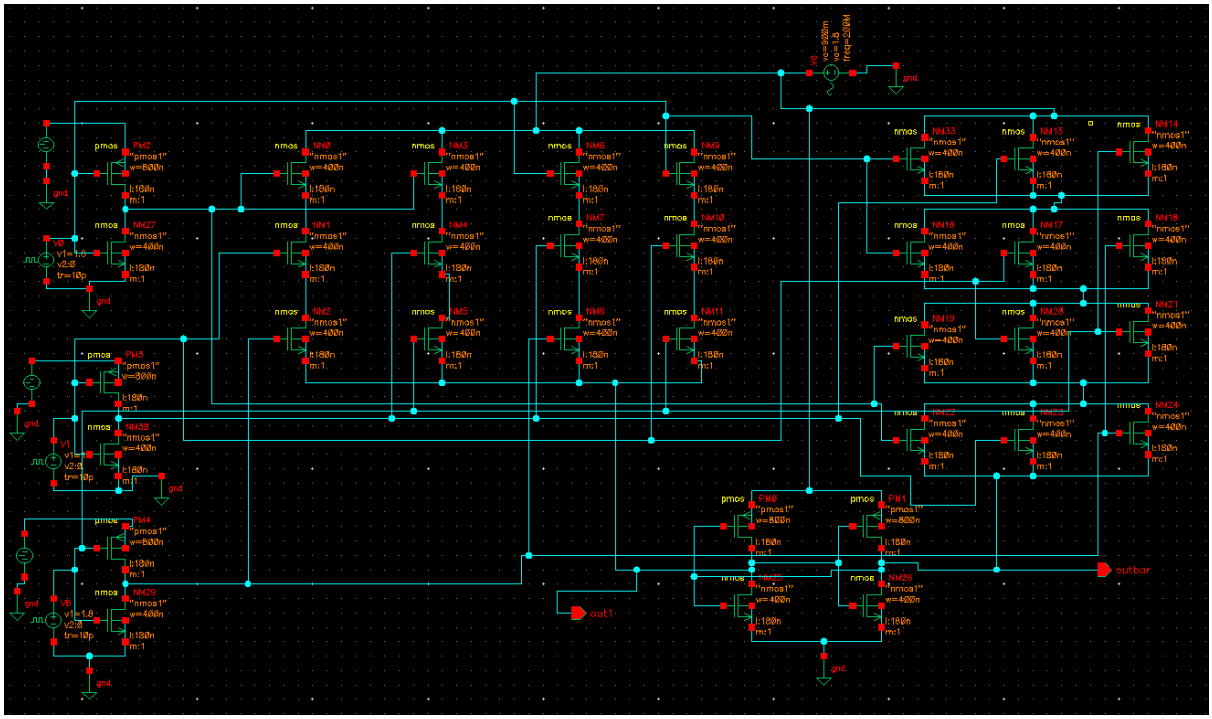
2x1 MUX USING PFAL LOGIC

(180 nm)



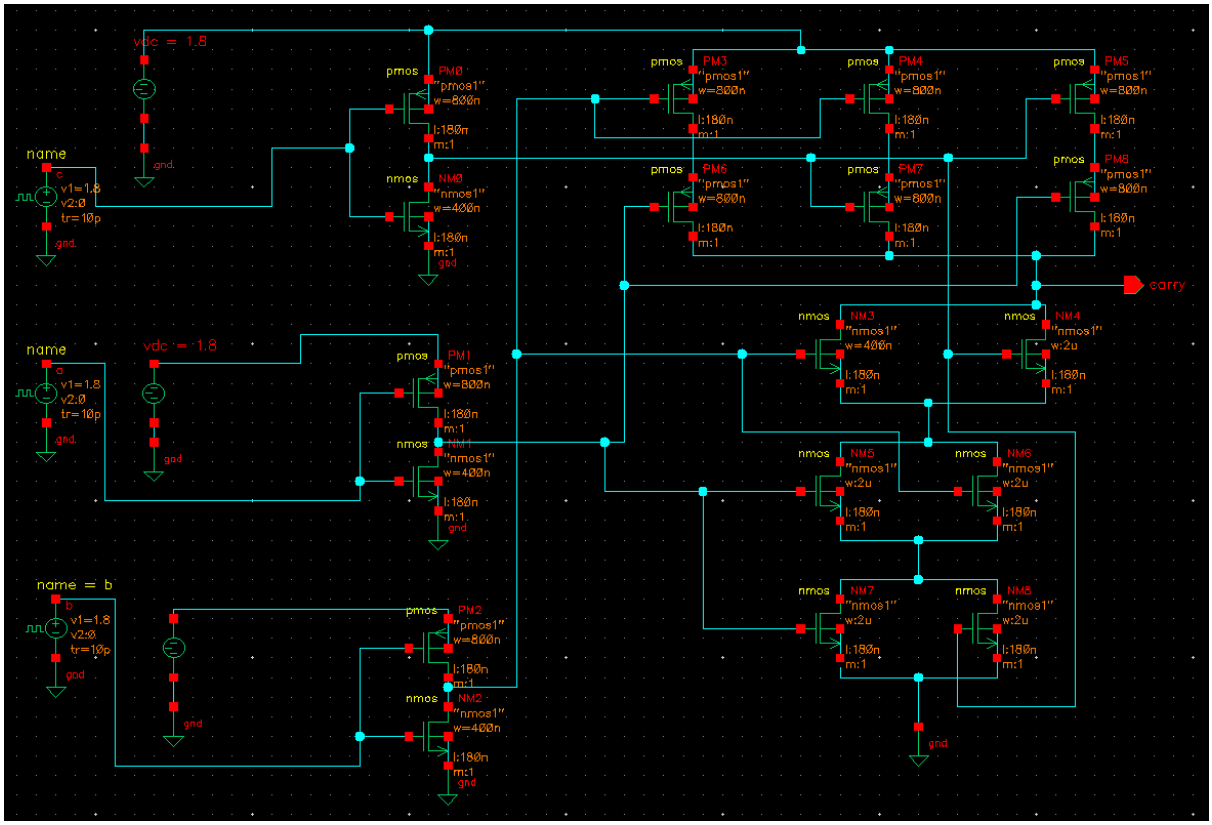
Full adder Sum using CMOS logic

(180 nm)



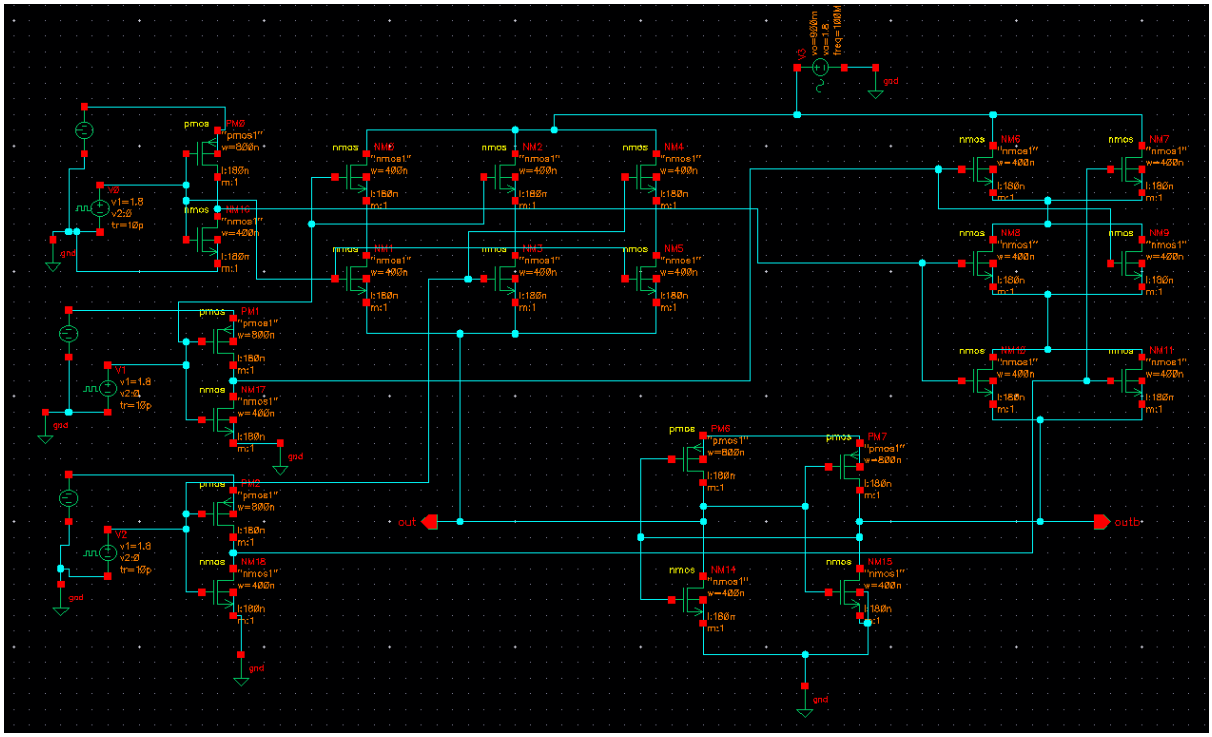
Full adder Sum using PFAL logic

(180 nm)



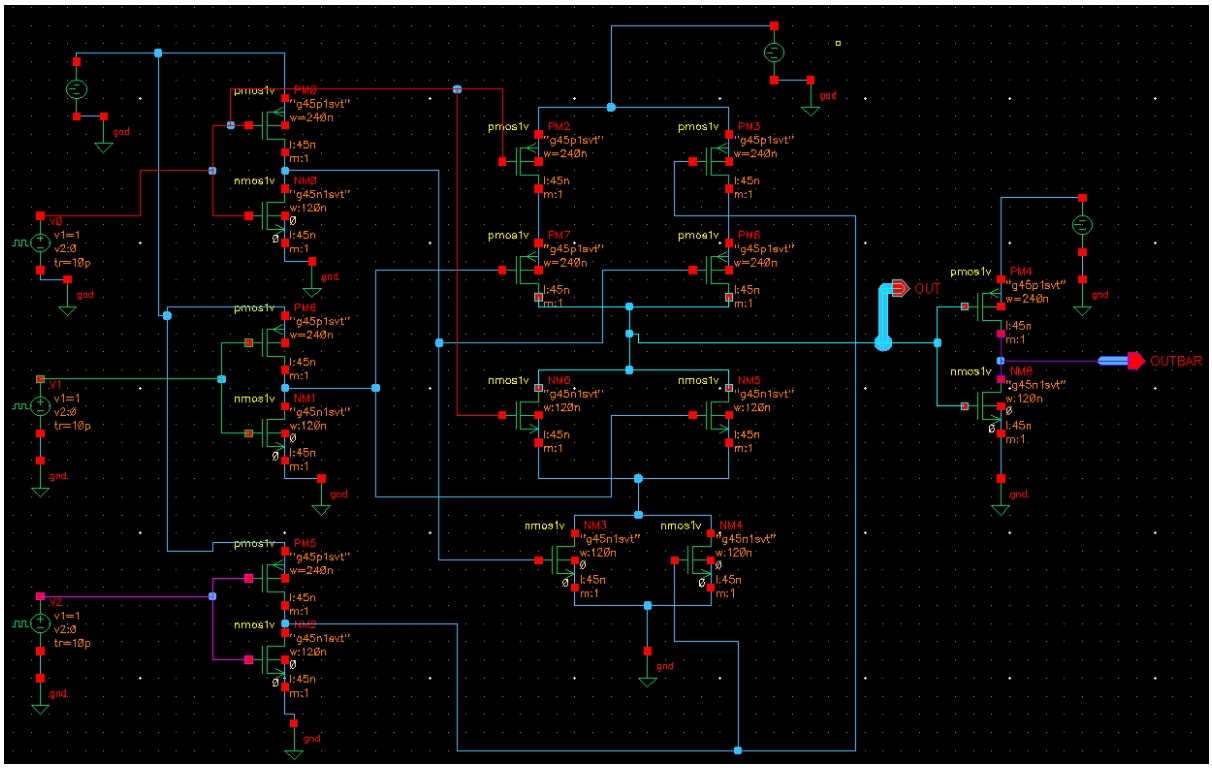
Full adder carry using CMOS logic

(180nm)



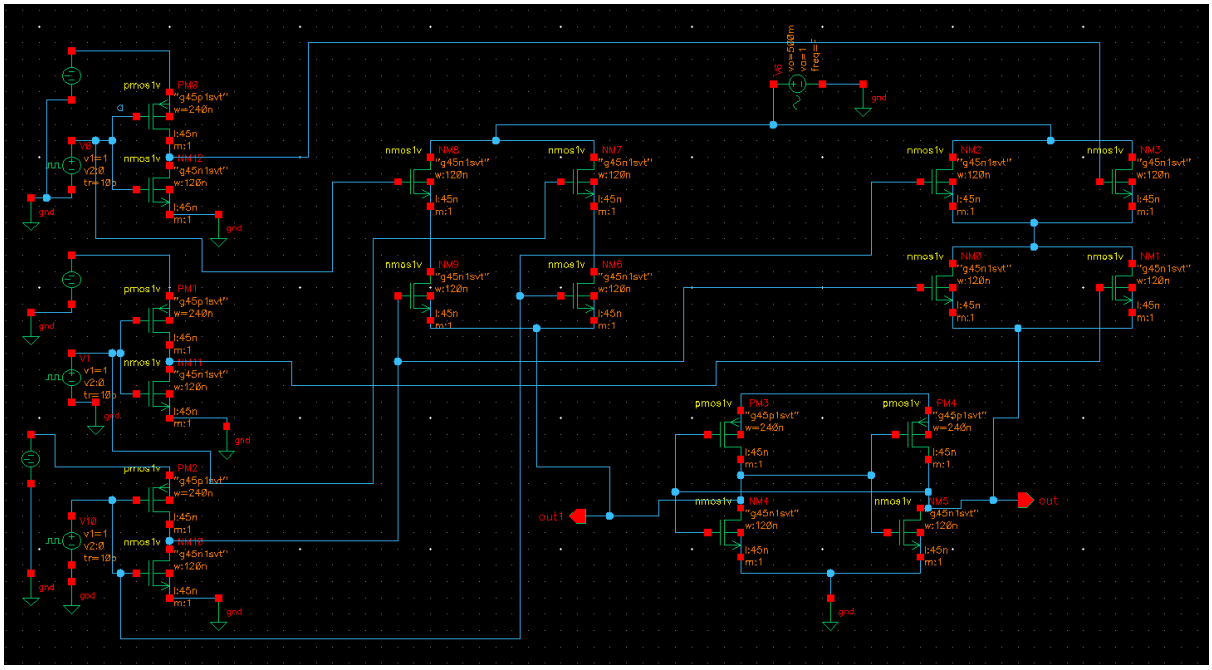
Full adder carry using PFAL logic

(180 nm)



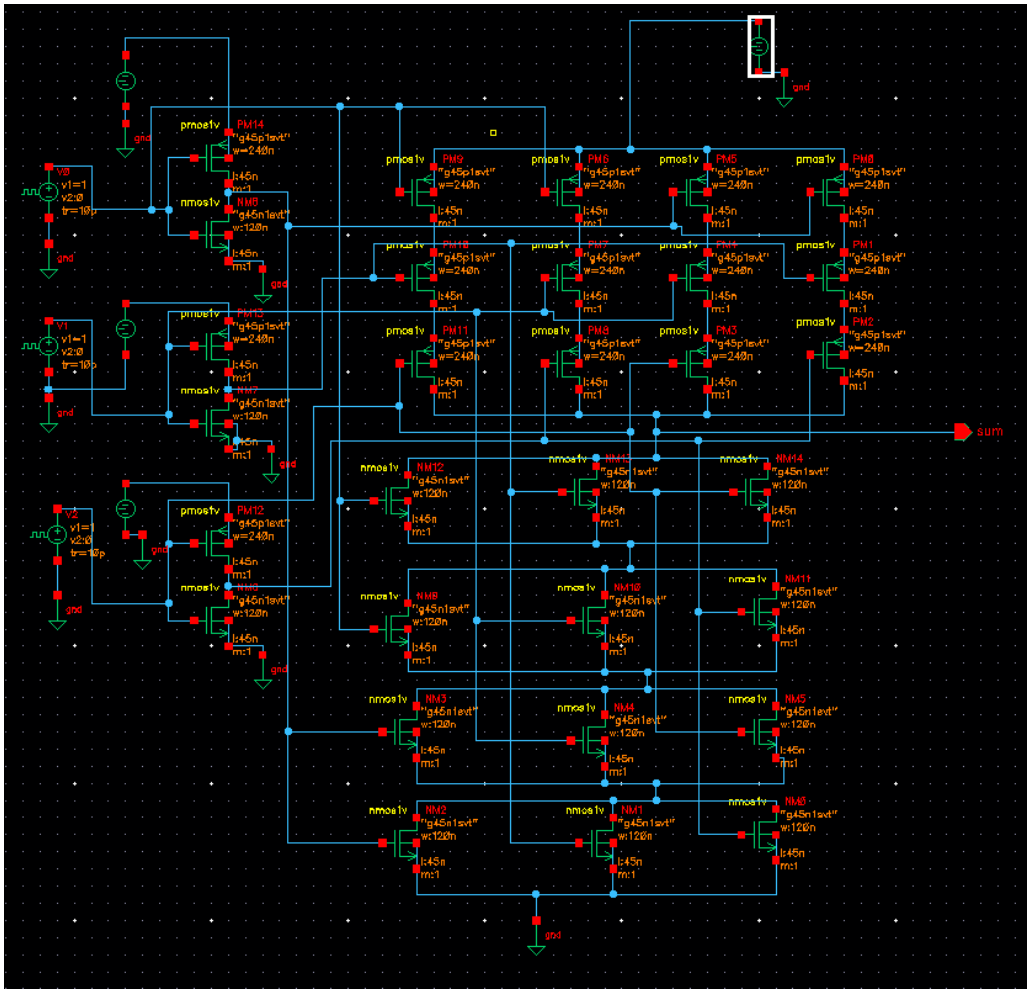
2x1 mux using CMOS LOGIC

(45 nm)

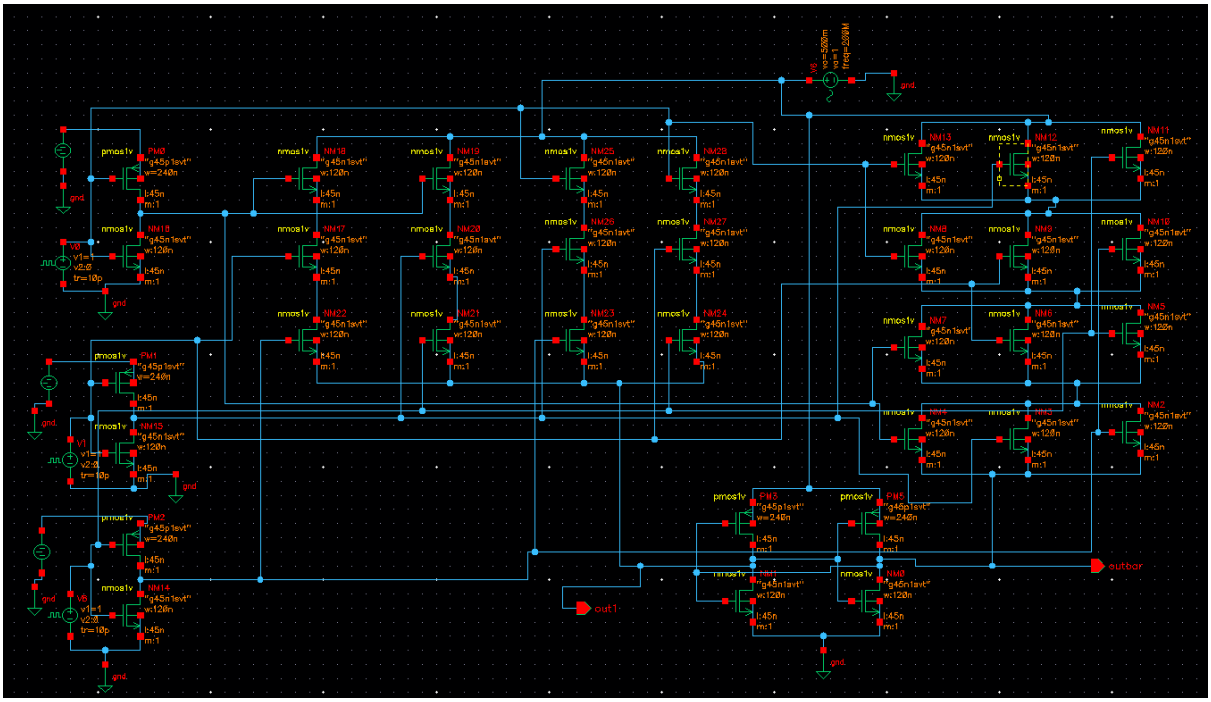


2x1 MUX using PFAL LOGIC

(45 nm)

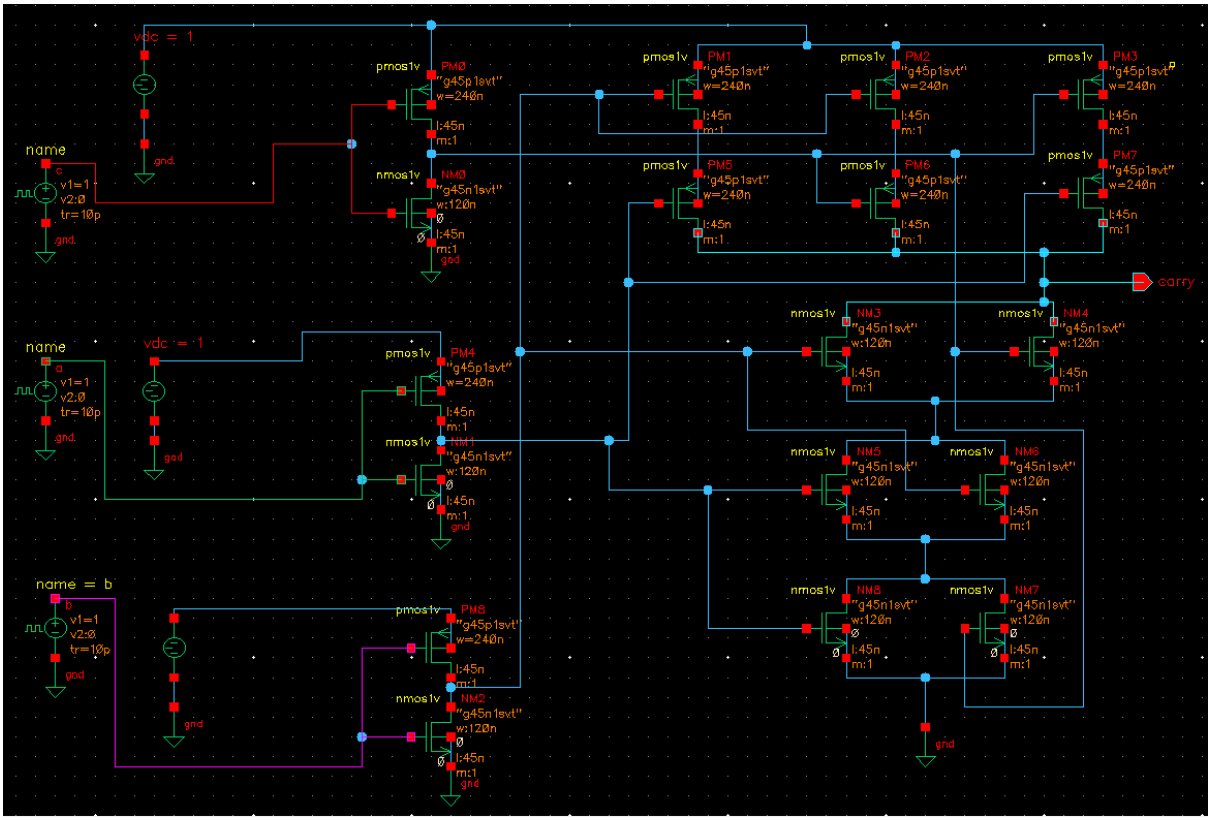


Full adder sum using CMOS logic (45 nm)



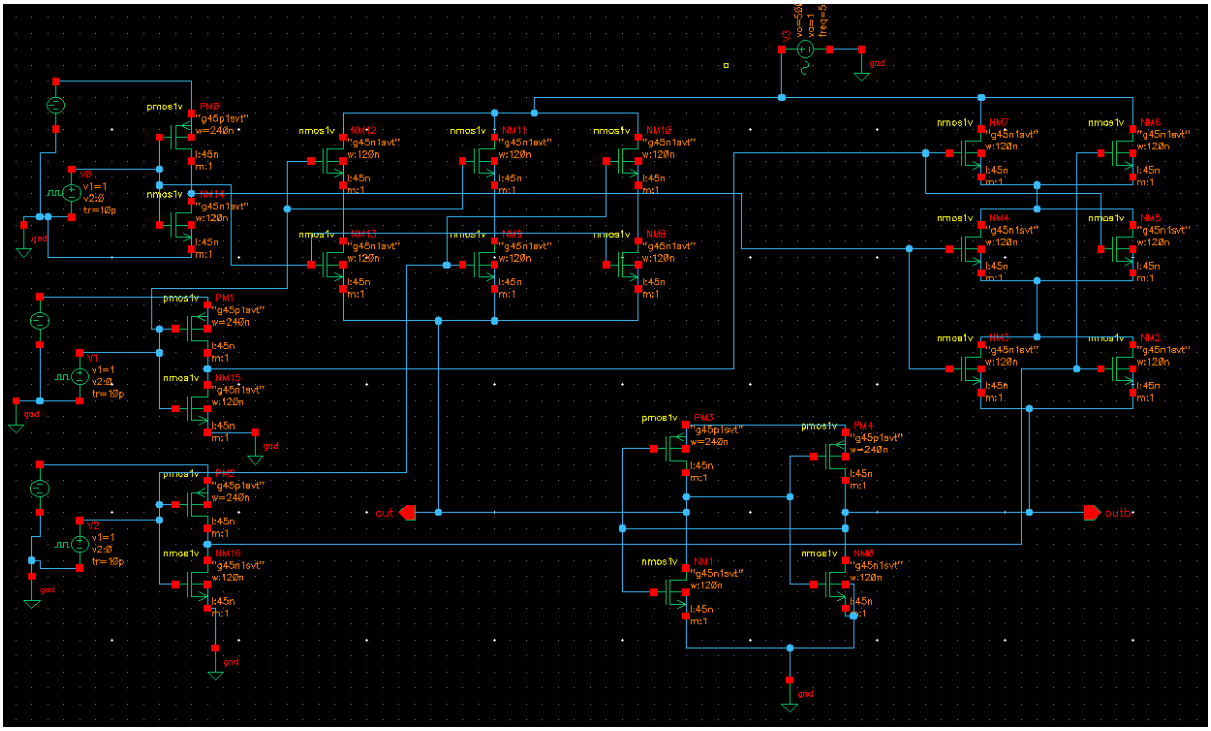
Full adder Sum using PFAL Logic

(45 nm)



Full adder carry using CMOS logic

(45 nm)



Full adder carry using PFAL logic

(45 nm)

3. EXPLANATION:

We used CMOS and PFAL circuitry to create 2x1 MUX, Full Adder Sum, and Carry. The general operation of a 2x1 MUX is shown in the table below.

Input 1	Input 2	Select Line	Output
A	B	0	A
A	B	1	B

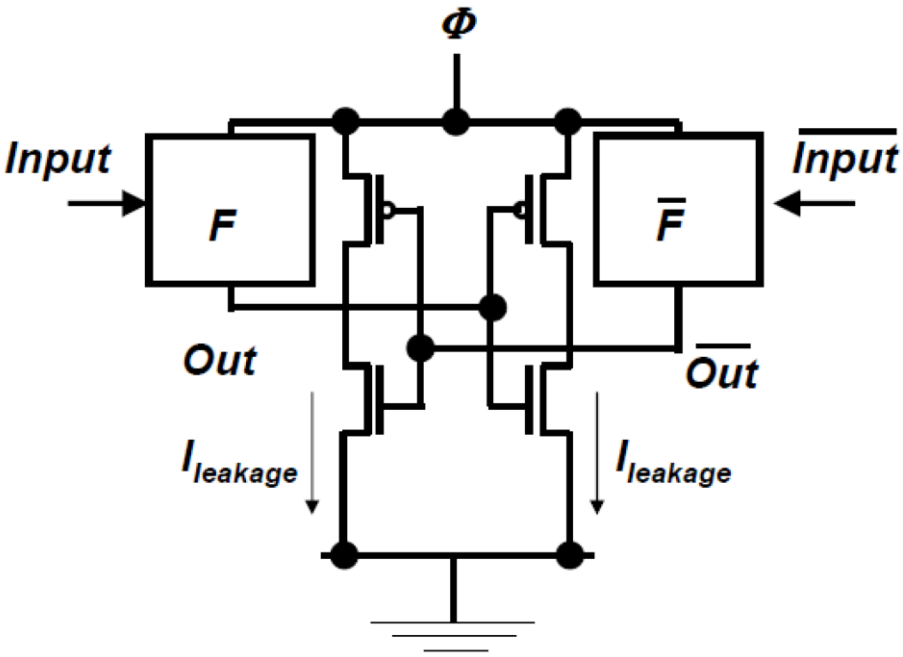
The general operation of Full adder Sum is as per the below table

A	B	Sum
0	0	0
0	1	1
1	0	1
1	1	0

The general operation of Full adder Carry is as per the below table

A	B	Sum
0	0	0
0	1	0
1	0	0
1	1	1

PFAL LOGIC

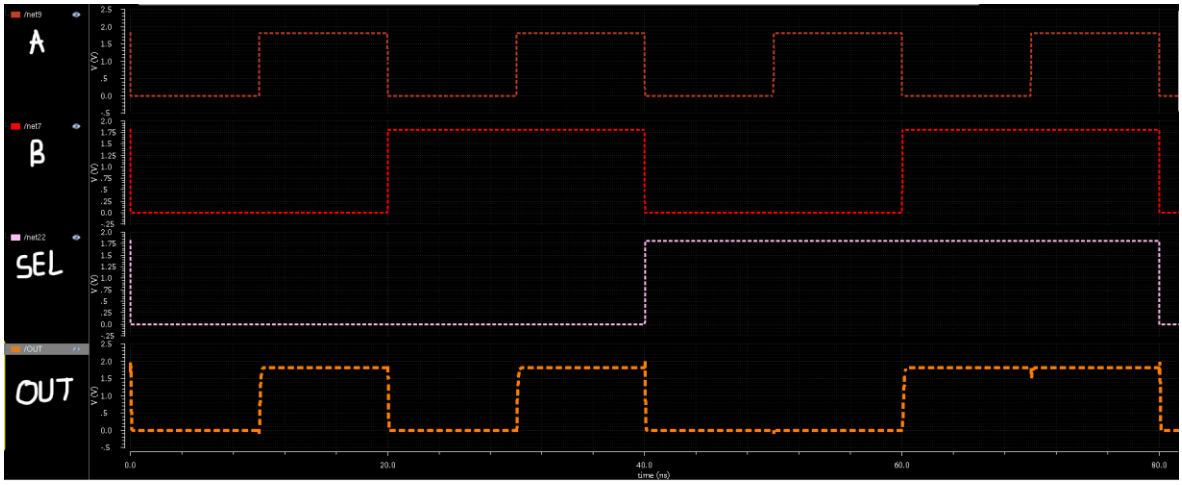


NMOS logic is used to implement the F and F blocks. The PMOS transistors are linked in parallel to the input NMOS network. There are no floating outputs in a PFAL gate, and all outputs have a complete logic swing. A four-phase clock is used. Evaluation, hold, recuperation, and wait are the four stages. During the assessment step, one of the outputs becomes logic '1', and the other becomes logic '0.' The outputs are steady during the hold period. During the recovery phase, the output with logic '1' serves as a source, causing the other outputs to be logic '1', but the source output is discharged to logic '0'. The output is steady during the waiting phase. Reversible logic is used to recycle energy.

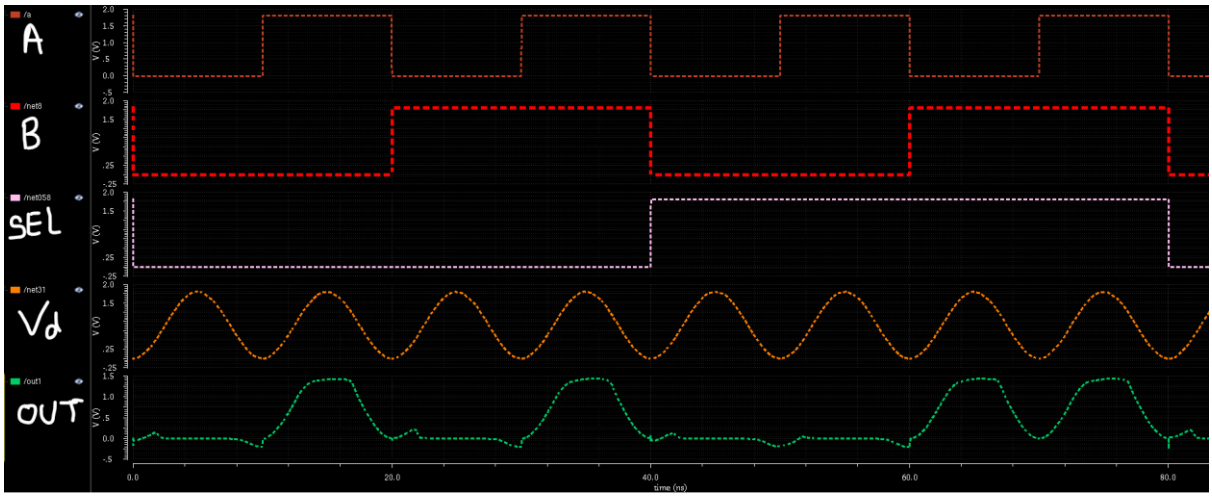
When selecting the clock's frequency, we must use extreme caution. It is worth noting that the clock frequency should be more than or equal to the inputs' maximum frequency. Otherwise, the results will be misinterpreted.

The output graphs of 2x1MUX circuits are presented for one Selection Line cycle. The output graphs in Full adder Sum circuits are presented for one complete cycle of A input. The output graphs of Full Adder Carry circuits are presented for one complete cycle of A input.

4. SIMULATION RESULTS

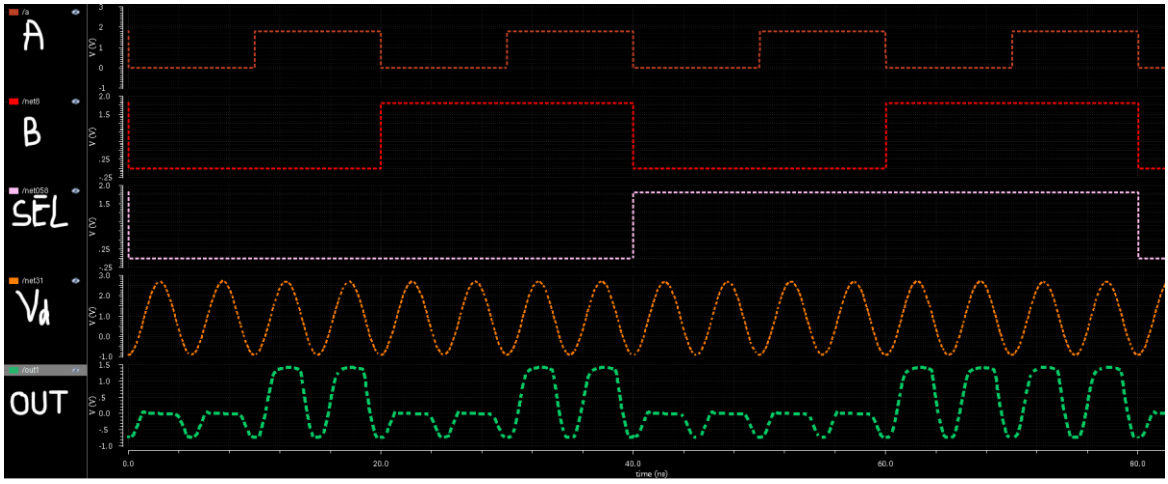


Simulation waveforms for 2x1 MUX using CMOS Logic (180 nm)



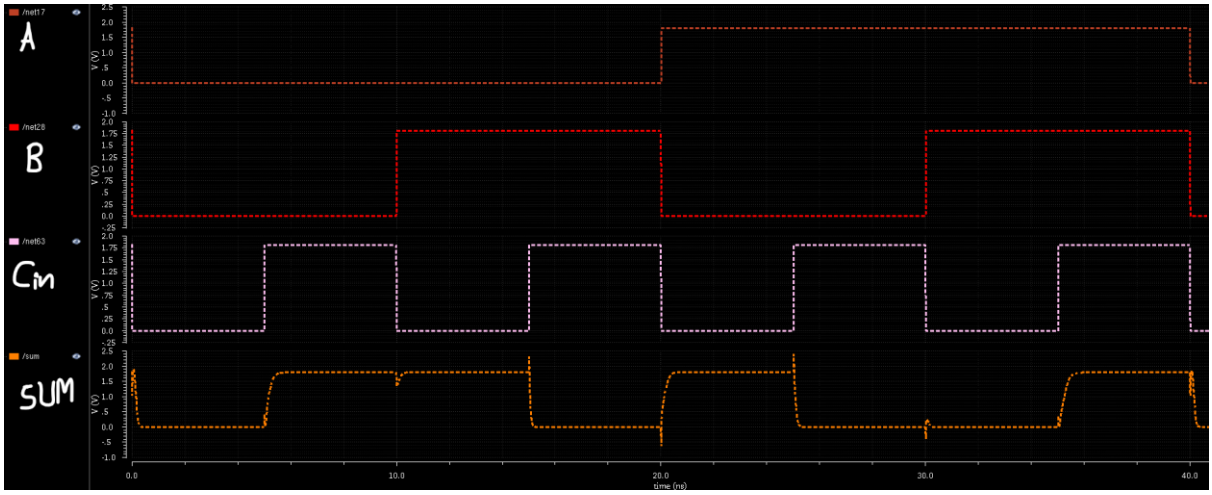
Simulation waveforms for 2x1 MUX using PFAL Logic (100 MHz)

(180 nm)



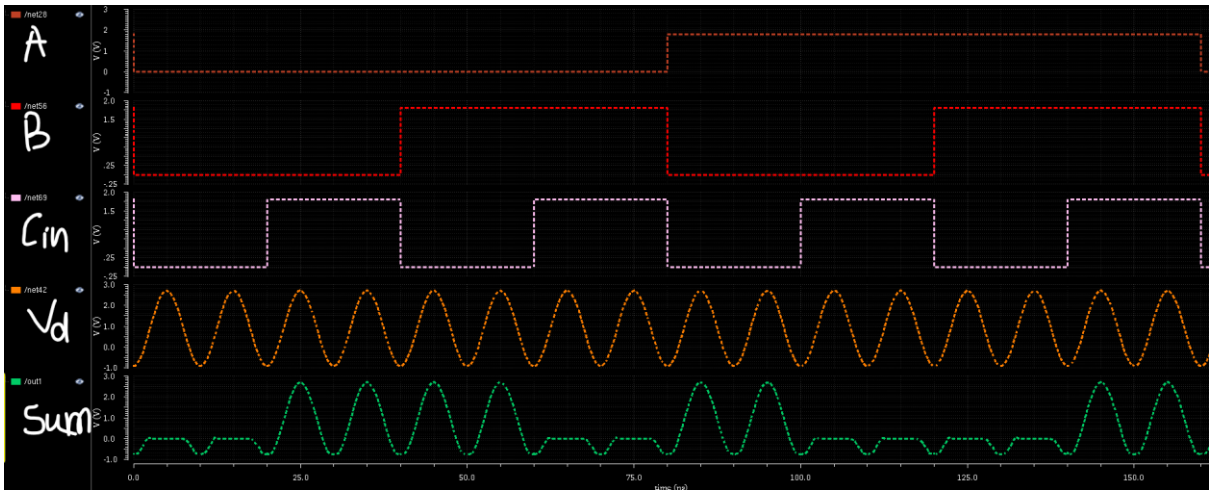
Simulation waveforms for 2x1 MUX using PFAL Logic (200 MHz)

(180 nm)



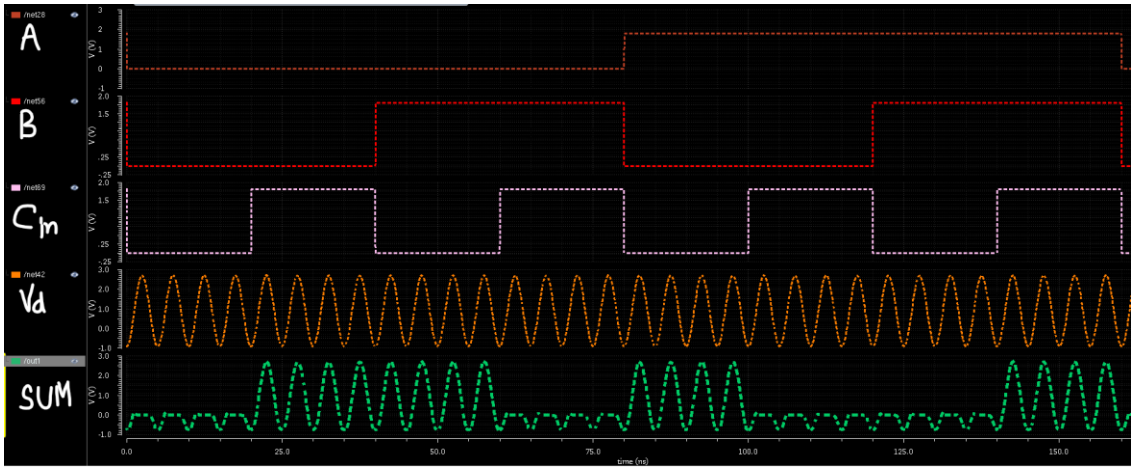
Simulation waveforms for Full adder Sum using CMOS logic

(180 nm)



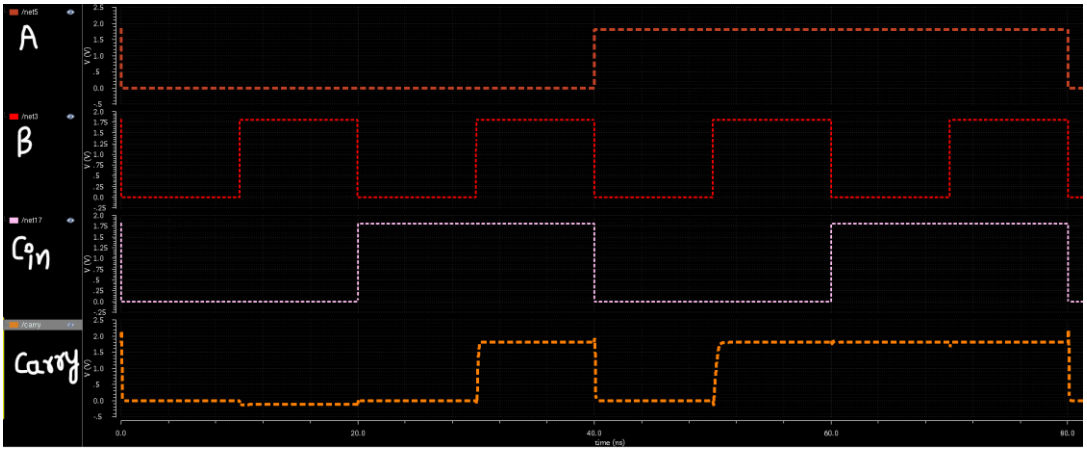
Simulation waveforms for Full adder Sum using PFAL logic (100 MHz)

(180 nm)



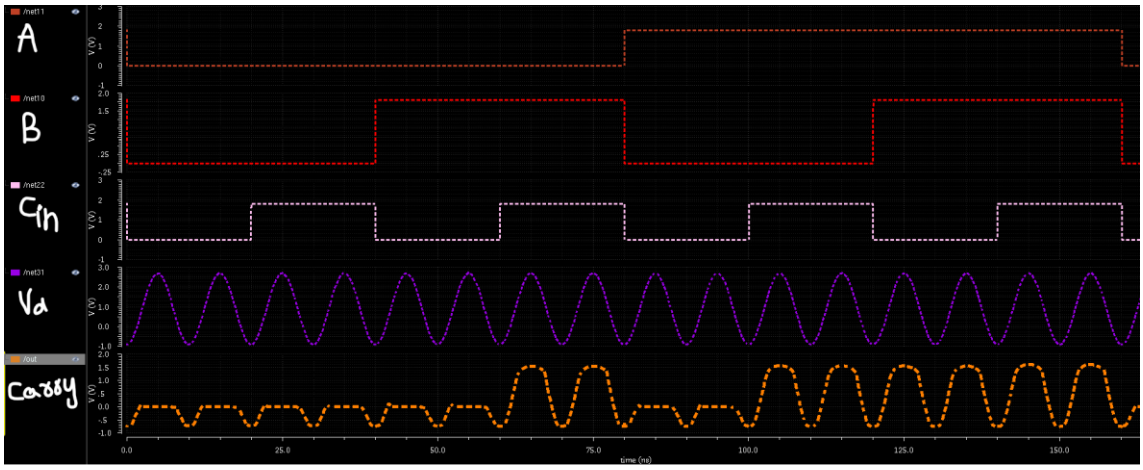
Simulation waveforms for Full adder Sum using PFAL logic (200 MHz)

(180 nm)



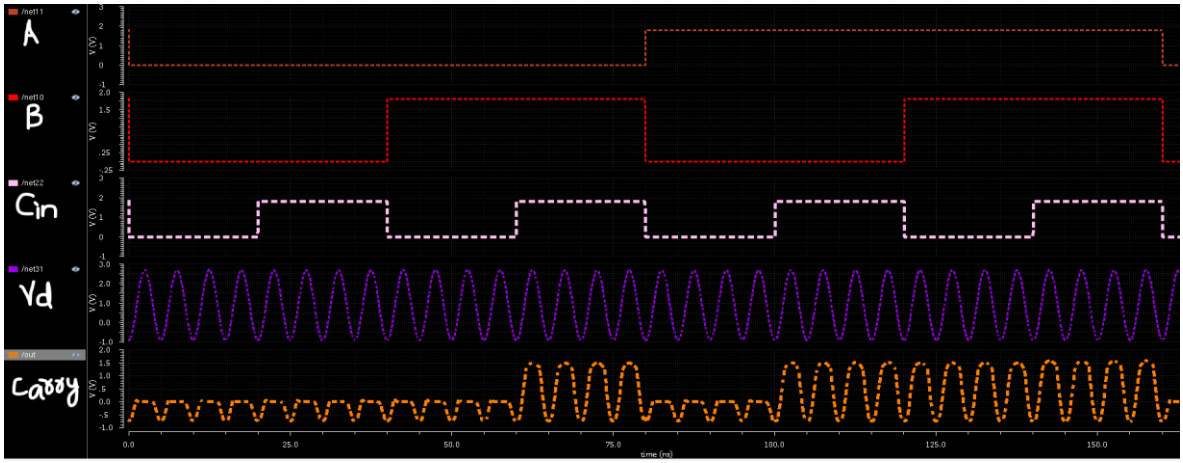
Simulation waveforms for Full adder carry using CMOS logic

(180nm)



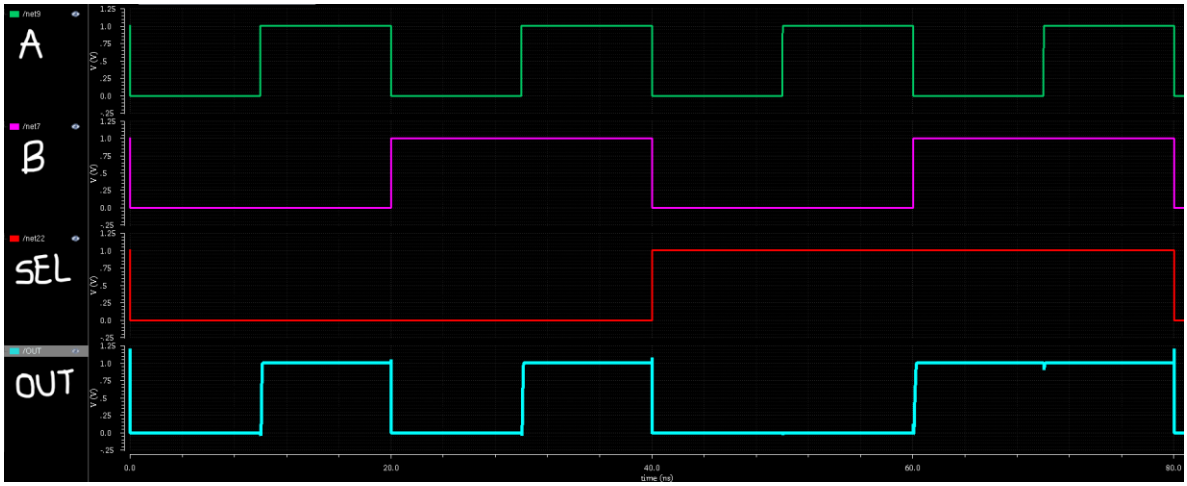
Simulation waveforms for Full adder carry using PFAL logic (100 MHz)

(180 nm)



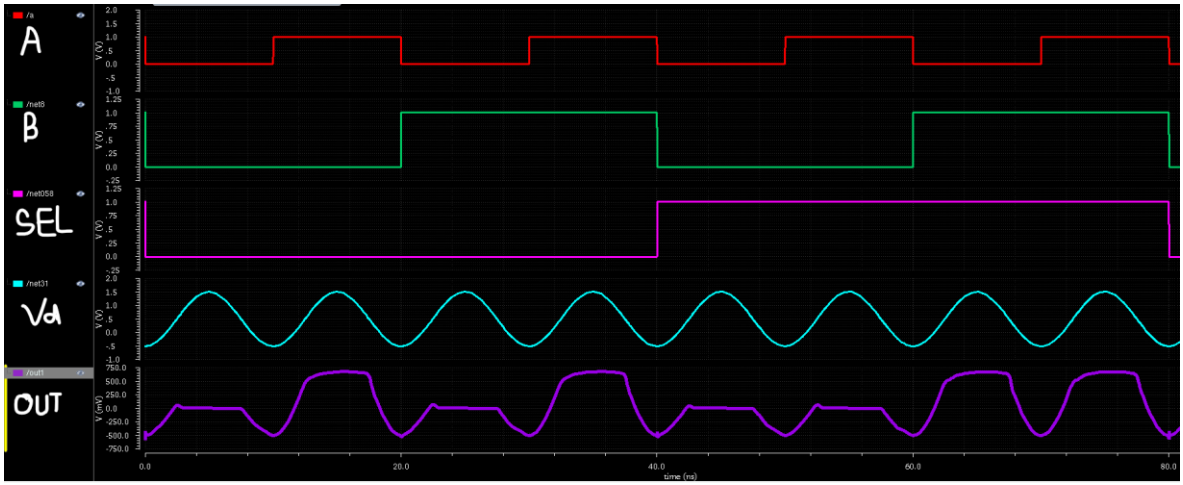
Simulation waveforms for Full adder carry using PFAL logic (200 MHz)

(180 nm)



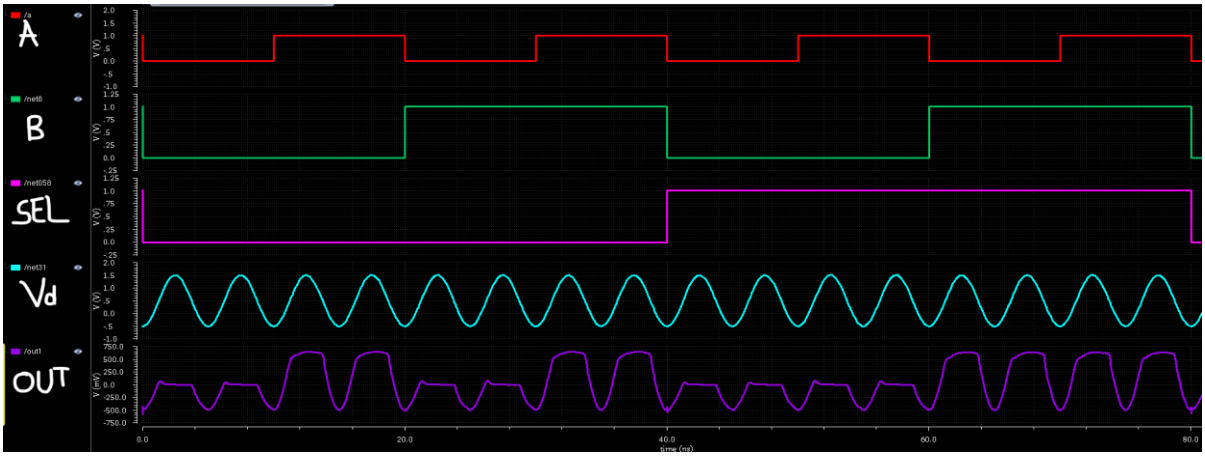
Simulation waveforms for 2x1 mux using CMOS

(45 nm)



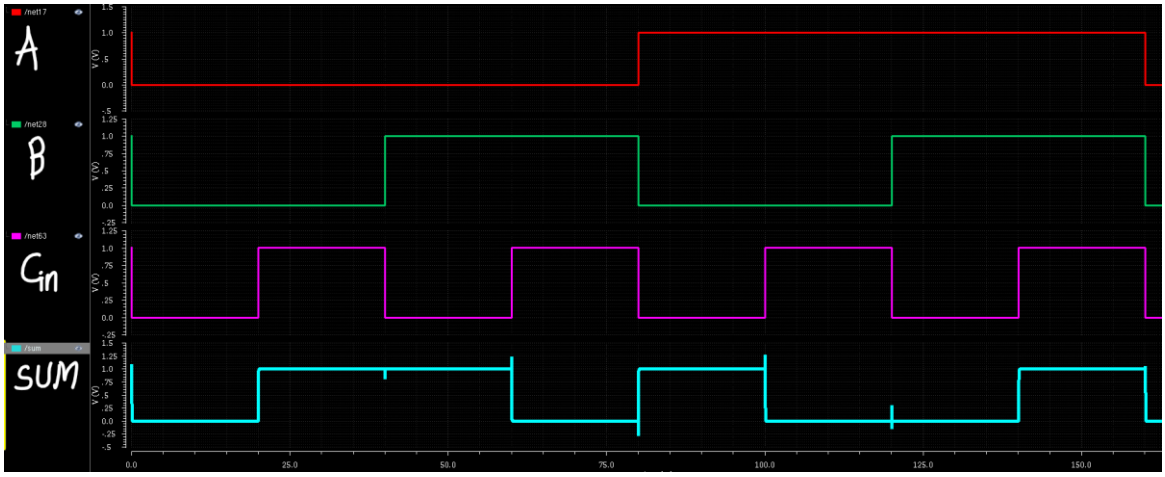
Simulation waveforms for 2x1 MUX using PFAL LOGIC (100 MHz)

(45 nm)



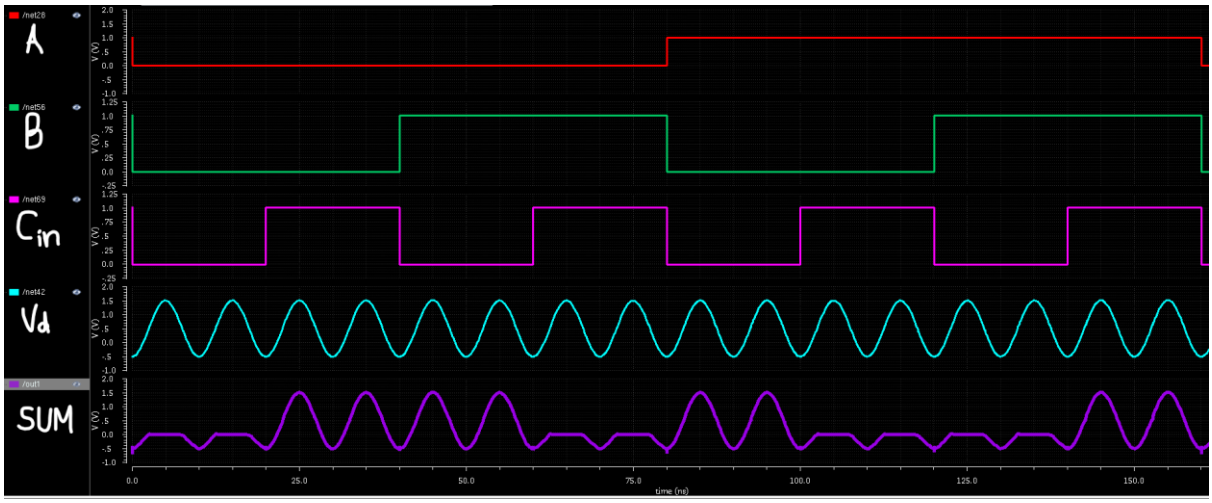
Simulation waveforms for 2x1 MUX using PFAL LOGIC (200 MHz)

(45 nm)



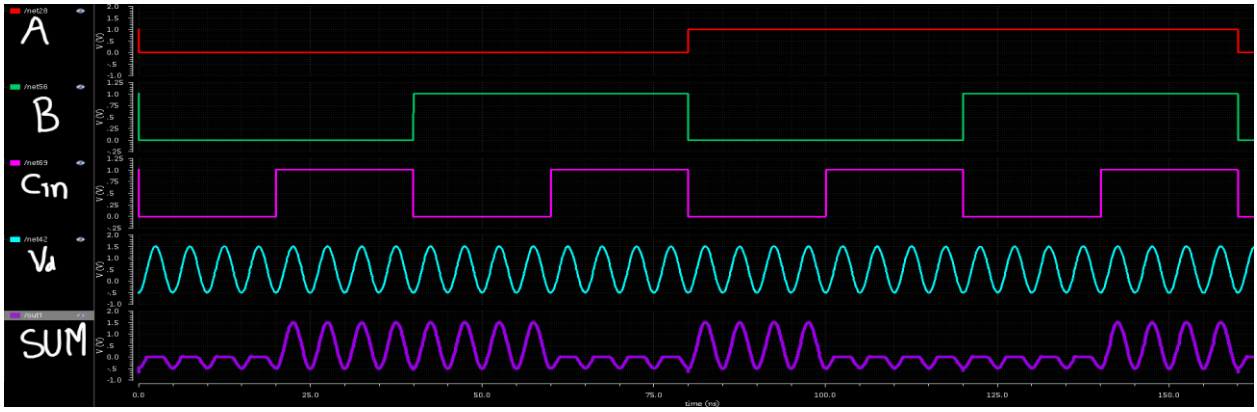
Simulation waveforms for Full adder sum using CMOS logic

(45 nm)



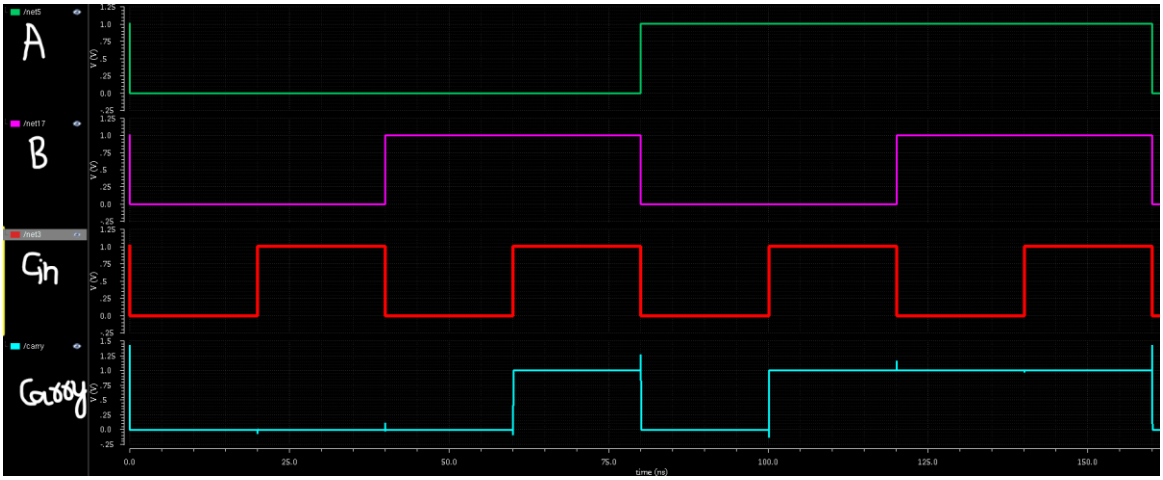
Simulation waveforms for Full adder Sum using PFAL Logic (100 MHz)

(45 nm)



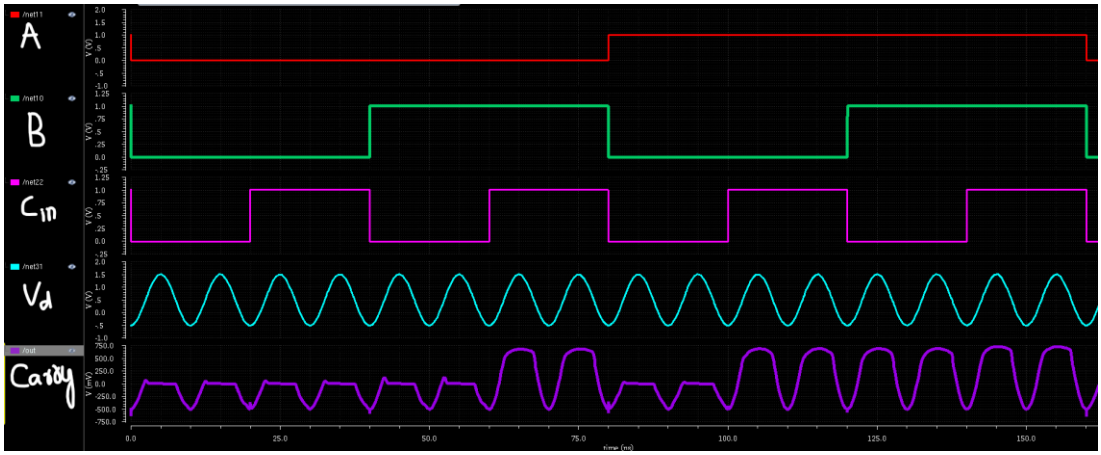
Simulation waveforms for Full adder Sum using PFAL Logic (200 MHz)

(45 nm)



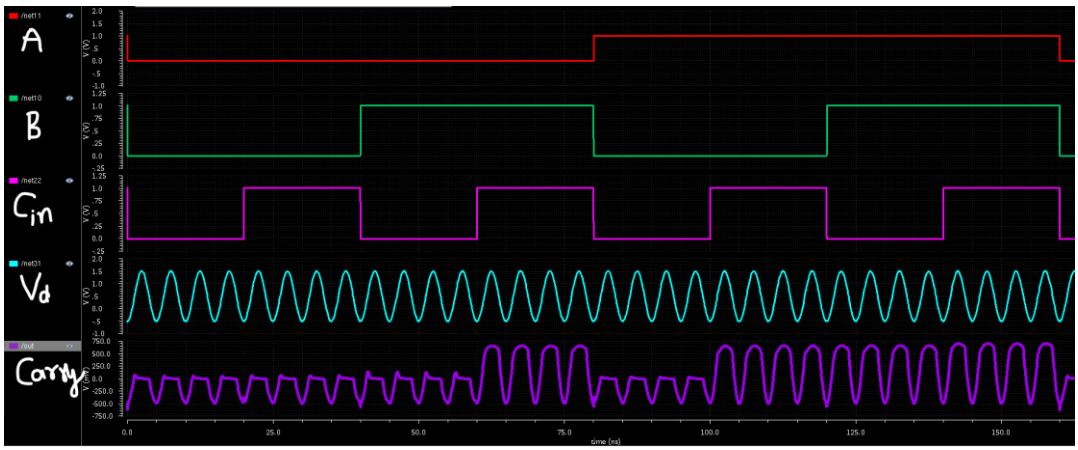
Simulation waveforms for Full adder carry using CMOS logic

(45 nm)



Simulation waveforms for Full adder carry using PFAL logic (100 MHz)

(45 nm)

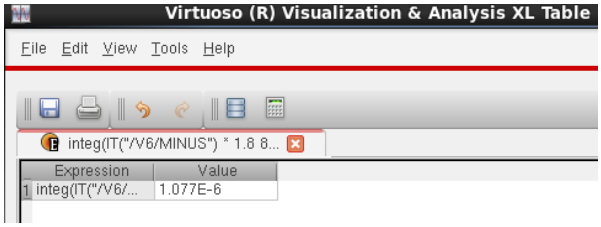


Simulation waveforms for Full adder carry using PFAL logic (200 MHz)

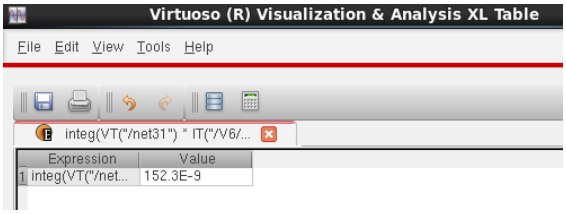
(45 nm)

5. CALCULATIONS AND OBSERVATIONS

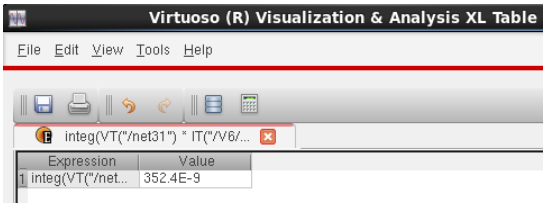
I. TECHNOLOGY NODE 180 nm



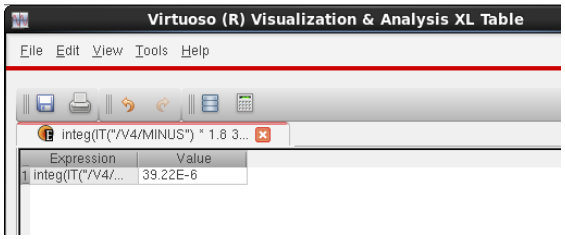
Average power for 2x1 MUX CMOS Logic



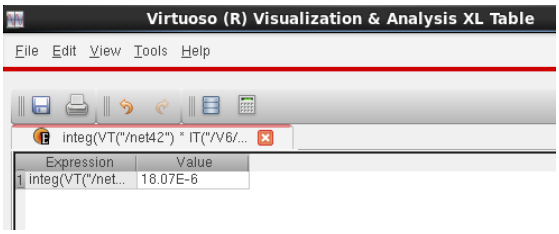
Average power for 2x1 MUX PFAL Logic (100MHz)



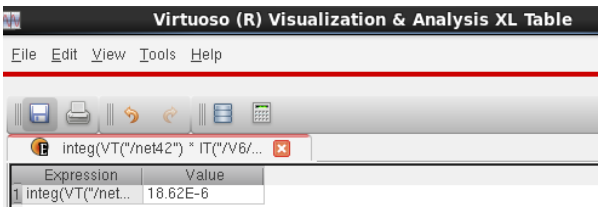
Average power for 2x1 MUX PFAL Logic (200MHz)



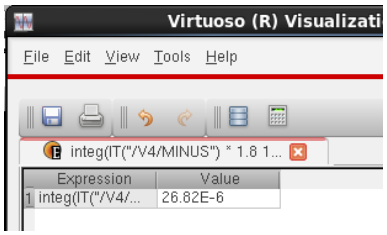
Average power for Full adder Sum CMOS Logic



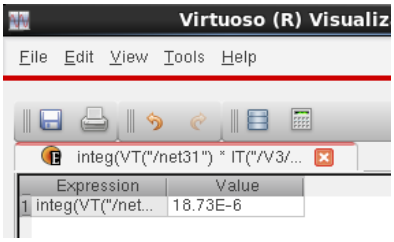
Average power for Sum PFAL Logic (100MHz)



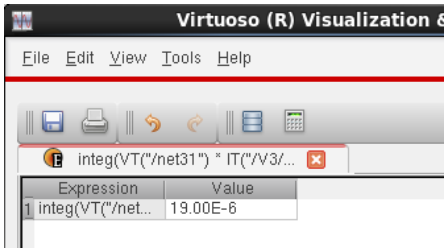
Average power for Full adder Sum PFAL Logic (200MHz)



Average power for Full adder Carry CMOS Logic



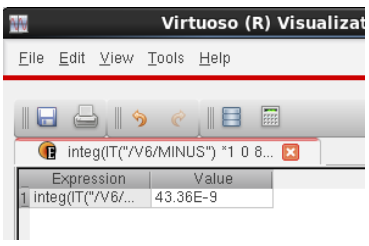
Average power for Carry PFAL Logic (100MHz)



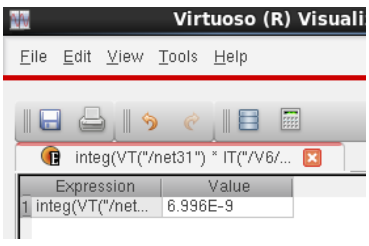
Average power for Full adder Carry PFAL Logic (200 MHz)

Circuit	CMOS LOGIC (180 nm)	PFAL LOGIC (180 nm) (Fd=100 MHz)	PFAL LOGIC (180 nm) (Fd=200 MHz)
	Average power	Average power	Average power
2x1 MUX	1.07 uW	0.1523 uW	0.352 uW
FULL ADDER SUM	39.22 uW	18.07 uW	18.62 uW
FULL ADDER CARRY	26.82 uW	18.73 uW	19 uW

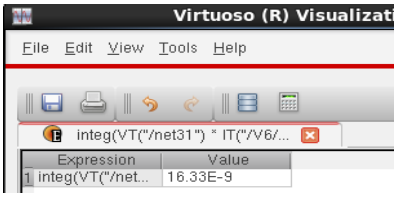
II. TECHNOLOGY NODE 45 nm



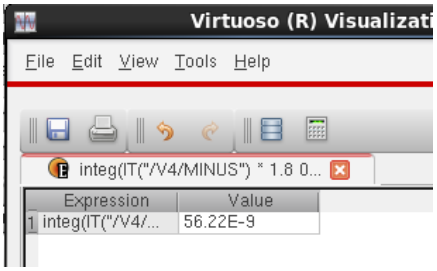
Average power for 2x1 MUX CMOS Logic



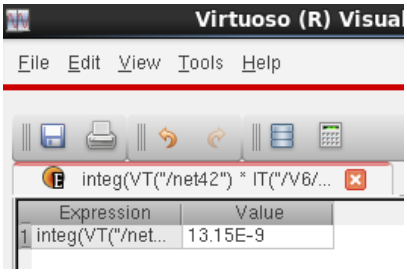
Average power for 2x1 MUX PFAL Logic (100MHz)



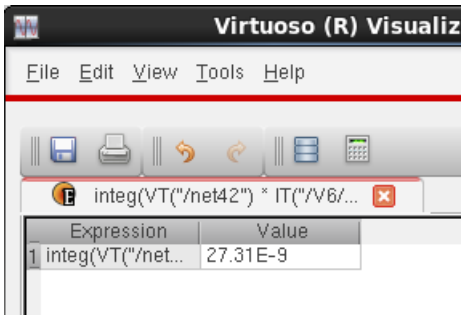
Average power for 2x1 MUX PFAL Logic (200MHz)



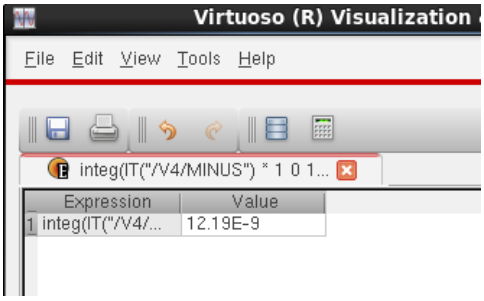
Average power for Full adder Sum CMOS Logic



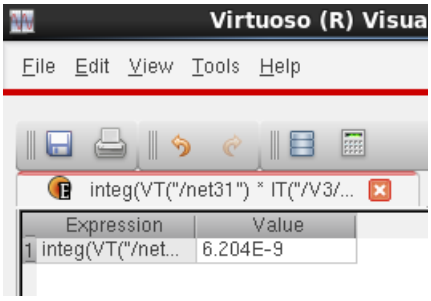
Average power for Sum PFAL Logic (100MHz)



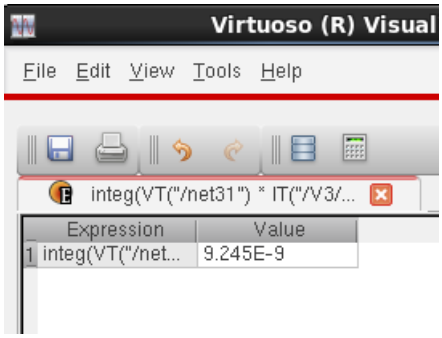
Average power for Full adder Sum PFAL Logic (200MHz)



Average power for Full adder Carry CMOS Logic



Average power for Carry PFAL Logic (100MHz)



Average power for Full adder Carry PFAL Logic (200 MHz)

Circuit	CMOS LOGIC (45 nm)	PFAL LOGIC (45 nm) (Fd=100 MHz)	PFAL LOGIC (45 nm) (Fd=200 MHz)
	Average power	**Average power**	**Average power**
2x1 MUX	43.36 nW	6.996 nW	16.33 nW
FULL ADDER SUM	56.22 nW	13.15 nW	27.31 nW
FULL ADDER CARRY	12.19 nW	6.204 nW	9.245 nW

6. CONCLUSIONS

- The circuit using CMOS logic uses more power than the circuit with PFAL logic, as seen in the tables above.
- According to the preceding statistics, power consumption increases with frequency in PFAL logic circuits. Therefore the PFAL logic circuit is significantly more effective in lower frequency circuits than higher frequency circuits.
- PFAL Logic is successful in different technology nodes, according to the simulated findings for two technology nodes.