DESIGN OF 7T SRAM CELL FOR LOW POWER APPLICATIONS

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Base paper Abstract:

Low power consumption is critical for VLSI system design as memory technology on Systems-on-Chip (SoC) shrinks and small devices and embedded systems emerge. More than 70% of the Soc is taken up by static random-access memory (SRAM). A standard 6T SRAM cell has two-bit lines for reading and writing operation; thus, it consumes more power. There are many techniques for power reduction like scaling of the supply voltage (Vo) and threshold voltage (Vt), multi- Vo, multi- Vt etc. The voltage scaling harms the SRAM cells' stability. A dual Vt 7T (seven transistors) SRAM cell is presented in this work and compared to a standard 6T SRAM cell based on reading delay, writing delay, leakage power consumption, and Static Noise Margin (SNM) (during the hold, read and write). Reading and writing activities are performed on a single bit line in this proposed cell. As a result, the cell's access time is improved. Leakage power consumption is decreased by 61.50 per cent. The write latency has been decreased by 66.67%. On 65nm technology, at 27 C, all simulation work is done with Mentor Graphics' Eldo SPICE tool.

Improvement of this project:

- Based on energy, space, and performance, design a security-oriented 7T SRAM in 45nm CMOS technology.
- To design a 7T SRAM 1-bit to 7T SRAM 8-bit security-focused SRAM.

Proposed Title:

CMOS Implementation of Low Power and High-Security Data Information using 7T SRAM Bit Cell

Proposed Abstract:

A current cryptographic application-based device with more sensitive data has the essential element of storing and retrieving the data. As a result, its impact on power analysis and side-channel analysis exploits the link between the instantaneous current used by power supply devices and information leakages. This paper will discuss a new security-oriented 7T SRAM cell design that uses two-phased write operations to decrease the correlation between the written and stored data in the memory and its power consumption. As a result, it offers a thorough examination of resilient memory. An extra transistor is included in this planned 7T cell.

Existing System:

Cryptographic devices that store sensitive data have increased in importance over the last several decades, becoming an essential component of many applications such as smart cards and mobile devices. Side-channel analysis (SCA) is a danger to these devices because it uses information about their physical behaviour to extract critical information. Because they need very minimal equipment and settings, PA assaults are regarded as one of the most effective forms of SCA techniques. To extract secret or sensitive information, PA attacks use the correlation between the instantaneous current utilized by the device's power supply and its processed and stored data.

Many VLSI system-on-chips (SoCs) include embedded memories, which are essential components of many cryptographic systems, such as smart cards and wireless networks that utilize cryptography methods, where they are used to store instruction data.

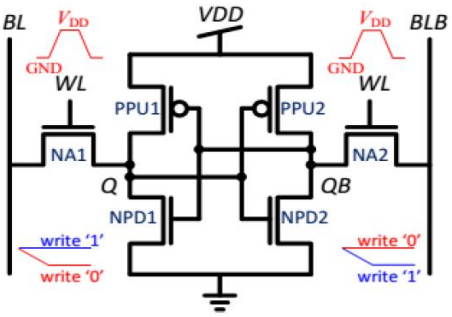

Figure 1: Schematic representation of 6T SRAM.

The signal waveforms of a typical 6T SRAM are displayed in Fig. 1 during a write operation. The word line (WL) is asserted, and the voltages on the bit-line pair (BL and BLB) are transferred to the internal storage nodes, Q and QB, respectively, to provide write access to the cell. The cell consumes dynamic energy to charge the internal cell capacitances when the written level differs from the value stored in the cell before the written event. Furthermore, the cell wastes short circuit power since the access transistors (NA1 and NA2) must overcome the cell's internal feedback (formed by NPD1, PPU1, NPD2, and PPU2) in order to modify the stored value. However, when the written value is comparable to the recorded data, the cell does not waste any dynamic energy, and the leakage currents dominate the overall power consumption.

The current consumption when writing '1' and '0' operations to a cell that previously held a '0' is depicted in Figure 5. Due to the altered state of the cell, which previously stored a '0,' the current waveforms show a considerable difference, with a peak current approximately four orders of magnitude lower during the write '0' (0.14 a) operation than the write '1' operation (100 a).

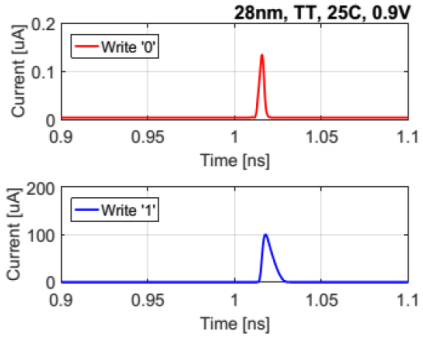

Figure 2: Current consumed during write ‘1’ and ‘0’ operations to a 6T SRAM.

In 28 nm CMOS technology, the energy distributions derived from a complete write cycle are presented in Fig. 3, recovered from 1000 Monte-Carlo (MC) simulations, incorporating device mismatch and process changes. As predicted, the write energy dissipated during a write '0' operation was nearly two orders of magnitude lower than that wasted during a write '1' operation. For writing '1' and '0,' the mean energy dissipations were 1.475 faja and 0.016 faja, respectively. The substantial variation in energy dissipations obtained from the various write operations to the cell reveals that the 6T SRAM's power consumption is significantly reliant on the written data to the cell, rendering it vulnerable to PA attacks.

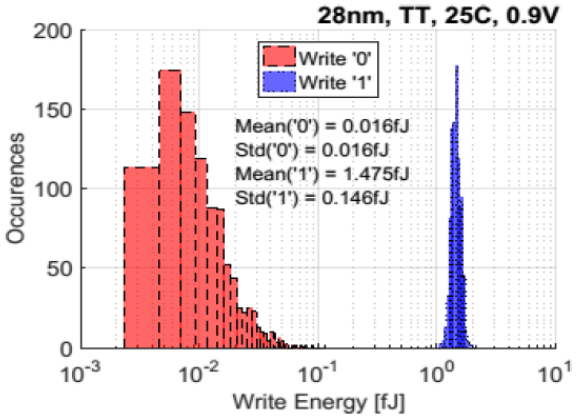

Figure 3: Write energy distribution of a 6T SRAM during write operations under process variations.

Disadvantages:

- The higher the area occupied, the longer the delay.
- The probability of a successful power analysis assault is very high.
- High dissipation of energy.

Proposed System:

The latest cryptographic application-based devices with more sensitive information play a critical role in data storage and retrieval. As a result, its impact on power analysis and side-channel analysis exploits the link between the instantaneous current used by power supply devices and information leakages. This paper will propose a unique security-oriented 7T SRAM cell design that uses two-phased write operations to minimize the correlation between the written and stored data in the memory and its power dissipation, resulting in a power analysis robust memory. This proposed 7T cell adds a transistor to the current 6T cell. Compared to the present 6T SRAM bit cell in terms of space, latency, and power leakage, this proposed study would develop a 7T SRAM bit cell in 45nm CMOS technology using TANNER EDA Software with single bit and 8-bit level operations.

Although an address accesses Random Access Memory, the latency of the access is unrelated to the address. The volatile memory is static random-access memory (SRAM), which maintains its data as long as the power supply is provided, whereas dynamic random-access memory (DRAM) must be updated regularly. A single bit of information in either '0' or '1' is stored in an SRAM cell. In cache memory, SRAM is employed. The size of CMOS devices has been reduced down for more than five decades to permit maximum memory on SoC. More memory allows for more data to be stored, which speeds up the machine. The system's low-power operation is achieved by decreasing the leakage current, which lowers leakage power consumption. Supply voltages and threshold voltages are decreased for this reason. However, this impacts SRAM cell stability, as the noise margin is reduced [1]. Technology's shrinking affects stability as well. The first portion of this paper covers the read and write operations of a typical 6T SRAM cell. The proposed dual-Vt 7T SRAM cell is addressed in the second part. The third part contains the parameters to be compared. The simulation is illustrated in the fourth section, followed by the conclusion. The single bit line is utilized in the proposed 7T SRAM cell, but the transistors are arranged to enable single-ended but the dual-port operation for reading and writing, i.e., separate bit lines are supplied for reading and writing. The dual-Vt (dual threshold voltage) approach is used to reduce leakage power, with essential pathways (those involved in the charging or discharging of the transistor) having a higher threshold voltage and non-critical channels having a lower threshold voltage.

High threshold provides the transistors with low leakage current; this contributes in.

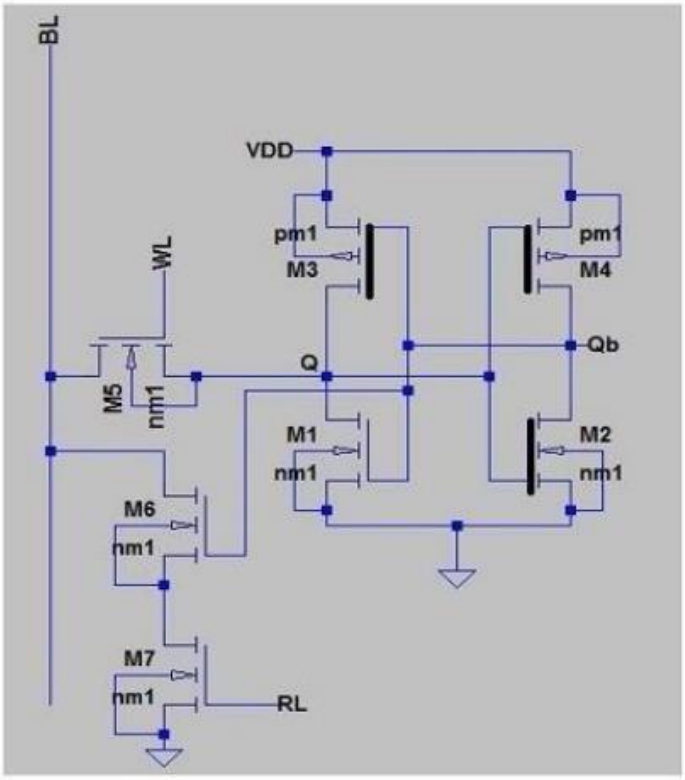

Figure 4 : Proposed dual 7T SRAM Cell

A. Read Operation Word line (WL) is deactivated. The bit line is recharged to VDD. When the Read Line (RL) goes high, it provides a path for the bit line to discharge. If the bit line discharges, it shows the content of the storage node is '0'; otherwise, it is '1'.

B. Write operation Read line is deactivated, and the WL goes to logic-high. The bit line is provided with the logic level that is to be written at the storage node. Access transistor M5 is made enough stronger to transfer the data from the bit line to the storage node.

A. Read delay - Time is taken by biting to go from one logic state to another, i.e., the time difference between 10% to 90% voltage swing of the biting. B. Write delay - The storage nodes take time to flip from one logic state to another, i.e., the time difference between 10% to 90% voltage swing of the storage nodes.
C. Leakage power - A tiny number of current flows through the transistors even in their OFF state; it is called leakage current. The multiplication of leakage current calculates leakage power with supply voltage.
D. Static Noise Margins (SNM) - It measures the stability of the SRAM cell. It gives the maximum avoidable noise voltage present at the input of the inverters without flipping the cell's content. It is measured using the butterfly curve method.

- Low Area.
- Low Energy Consumption.
- Reduction in power analysis attack.

Advantages:

Literature Survey:

• A 7T Security Oriented SRAM Bit cell Robert Gattermann, Onset Keren, and Alexander Fish 1549-7747 2018 IEEE. Power analysis (PA) attacks have become a severe threat to security systems by enabling secret data extraction by analyzing the current consumed by the system's power supply. Embedded memories, often implemented with six-transistor (6T) static random-access memory (SRAM) cells, serve as a critical component in many of these systems. However, conventional SRAM cells are prone to side-channel power analysis attacks due to the correlation between their current characteristics and written data. To provide resiliency to these types of attacks, we propose a security-oriented 7T SRAM cell, which incorporates an additional transistor to the original 6T SRAM implementation and a two-phase write operation, which significantly reduces the correlation between the stored data and the power consumption during write operations. The proposed 7T SRAM cell was implemented in a 28 nm technology and demonstrated over 1000× lower write energy standard deviation between writing '1' and '0' operations than a conventional 6T SRAM. In addition, the proposed cell has a 39%–53% write energy reduction and a 19%–38% reduced write delay compared to other power analysis resistant SRAM cells.

• Leakage Power Analysis Attacks: A Novel Class of Attacks to Nanometre Cryptographic Circuits Massimo Alioto, Senior Member, IEEE, Luca Giancana, Student Member, IEEE, Giuseppe Scotti, and Alessandro Trifiletti,1549-8328 2010 Giancana this paper, a novel class of power analysis attacks to cryptographic circuits is presented. These attacks aim at recovering the secret key of a cryptographic core from measurements of its static (leakage) power. These attacks exploit the dependence of the leakage current of CMOS integrated circuits on their inputs (including the secret key of the cryptographic algorithm that they implement), as opposed to traditional power analysis attacks focused on the dynamic power. For this reason, this novel class of attacks is named "Leakage Power Analysis" (LPA). Since the leakage power increases much faster than the dynamic power at each new technology generation, LPA attacks based on a solid theoretical background are presented. Advantages and measurement issues are also analyzed compared to traditional power analysis attacks based on dynamic power measurements. Examples are provided for various circuits, and an experimental attack to a register is performed first. An analytical model of the LPA attack result is also provided to understand the effectiveness of this technique better. The impact of technology scaling is explicitly addressed employing a simple analytical model and Monte Carlo simulations. Simulations on 65- and 90-nm technology and experimental results are presented to justify the assumptions and validate the adopted leakage power models.
• Effectiveness of Leakage Power Analysis Attacks on DPA-Resistant Logic Styles Under Process Variations Massimo Alioto, Simone Bongiovanni, Milena Djokovic, Giuseppe Scotti, and Alessandro Triflate 1549-8328 2013 Ileitis paper extends the analysis of the effectiveness of Leakage Power Analysis (LPA) attacks to cryptographic VLSI circuits on which circuit-level countermeasures against Differential Power Analysis (DPA) are adopted. Security metrics used for assessing the DPA-resistance of crypto core implementations, such as the minimum number to disclosure (MTD) and the asymptotic correlation coefficient, have been extended to the case of LPA. The LPA resistance has been evaluated in terms of MTD as a function of the on-chip noise. Noise variances up to 10000 times greater than the signal variance have been considered, and LPA attacks have been successfully executed for all the logic styles under analysis using less than 100000 measurements. Moreover, the role of process variations has been investigated

Through extensive Monte Carlo simulations to evaluate their impact on the leakage model for the logic styles under analysis. Results show that LPA attacks can be successfully carried out on the different anti-DPA logic styles, even in process variations. To the best of our knowledge, this work proves for the first time the effectiveness of LPA attacks in a real scenario where on-chip noise and process variations are taken into account.

• Leakage Power Attack-Resilient Symmetrical 8T SRAM Cell Robert Gattermann, Maoz Pienkowski, Isamar Levi, Yoav Weizmann, Onset Keren, and Alexander Fish 1063-8210 2018 IEEE. Power analysis attacks have become a severe threat to security systems by extracting confidential data using side-channel leakage information. Embedded memories, often implemented with 6T SRAM cells, serve as a critical component in many systems. However, conventional SRAM cells are prone to side-channel leakage power attacks. To provide resiliency to these attacks, we propose a symmetric 8T SRAM cell that incorporates two more transistors than the conventional 6T cell to significantly reduce the correlation between the stored data and the leakage currents. To demonstrate the improved security of the suggested memory array, both cells were implemented in 65-nm CMOS technology. Simulation results, including Monte Carlo analysis and signal-to-noise ratio comparison, illustrate the resiliency of the 8T cell to leakage power attacks.

• Design Solutions for Securing SRAM Cell Against Power Analysis Vladimir Razi˘ ca∗, Wim Deane† and Ingrid Debauched 978-1-4673-2340-6/12/$31.00 c 2012 IEEE. Side-channel attacks exploit physical imperfections of hardware to circumvent security features achieved by mathematically secure protocols and algorithms. This is achieved by monitoring physical quantities, usually power consumption or electromagnetic radiation, containing information about the secret data. As a countermeasure, several circuit styles have been proposed for designing side-channel resistant logic gates and flip-flops. However, little effort has been made to develop secure memory arrays. An SRAM cell with eight transistors has been proposed to obtain power analysis resistance using a dual-rail recharge principle, the same technique used in various secure logic styles. This paper looks into this cell's practical aspects, such as noise margins, layout strategy, and read current. In addition, we propose alternative solutions for power analysis resistant SRAM. We compare these solutions in terms of data stability, delay and side-channel resistance.

• SRAM Assist Techniques for Operation in a Wide Voltage Range in 28-nm CMOS Brian Zimmer, Student Member, IEEE, Seng Oona To, Member, IEEE, Huey Vo, Yun sup Lee, Student Member, IEEE, Olivier Thomas, Kriste Aganovic,' Senior Member, IEEE, and Borijove Nikolic,' Senior Member, IEEE 1549-7747 2013 IEEE. Reducing static random-access memory (SRAM) operational voltage (Vin) can significantly improve energy efficiency, yet SRAM Vin does not scale with technology due to increased process variability. Assist techniques have been shown to improve SRAM operation, but previous investigations of assist techniques at design time have either relied on static metrics that do not account for acute transient effects or make specific assumptions about failure distributions. This paper uses importance sampling of dynamic failure metrics to quantify and analyze the effect of different assist techniques, array organization, and timing on Vin at design time. This approach demonstrates that the most effective technique for reducing SRAM Vin is the negative bit line write assist, resulting in a Vin of 600 mV for a 28-nm LP process in the typical corner.

• Design and Iso-Area Vin Analysis of 9T Subthreshold SRAM With Bit-Interleaving Scheme in 65-nm CMOS Ming-Hung Chang, Student Member, IEEE, Yi-The Chiu, and Wei Hwang, Fellow, IEEE 1549-7747 2012 IEEE. This brief proposes a 9T bit cell to enhance writing ability by cutting off the positive feedback loop of a static random-access memory (SRAM) cross-coupled inverter pair. An access buffer isolates the storage node from the read path for better read robustness and leakage reduction in reading mode. The bit-interleaving scheme is allowed by incorporating the proposed 9T SRAM bit cell with additional write word lines (WWL/Wal) for soft-error tolerance. A 1-kb 9T 4-to-1 bit interleaved SRAM is implemented in 65-nm bulk CMOS

Technology. The experimental results demonstrate that the test chip minimum energy point occurs at 0.3-V supply voltage. It can achieve an operation frequency of 909 kHz with 3.51-μW active power consumption.

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