DESIGN OF PLL-BASED CLOCK AND DATA RECOVERY CIRCUITS

Submitted By:

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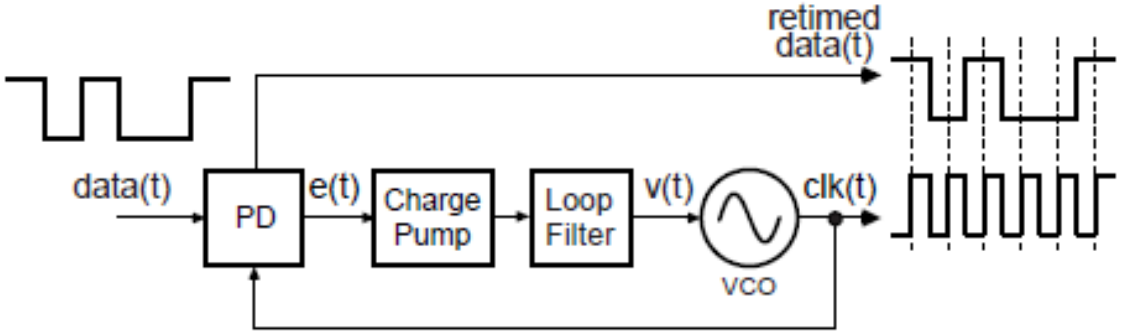
INTRODUCTION

In serial communication of digital data, clock recovery is the process of extracting timing information from a serial data stream to allow the receiving circuit to decode the transmitted symbols. Clock recovery from the data stream is expedited by modifying the transmitted data. Wherever a serial communication channel does not transmit the clock signal along with the data stream, the clock must be regenerated at the receiver, using the timing information from the data stream.

Block Diagram of PLL based CDR:

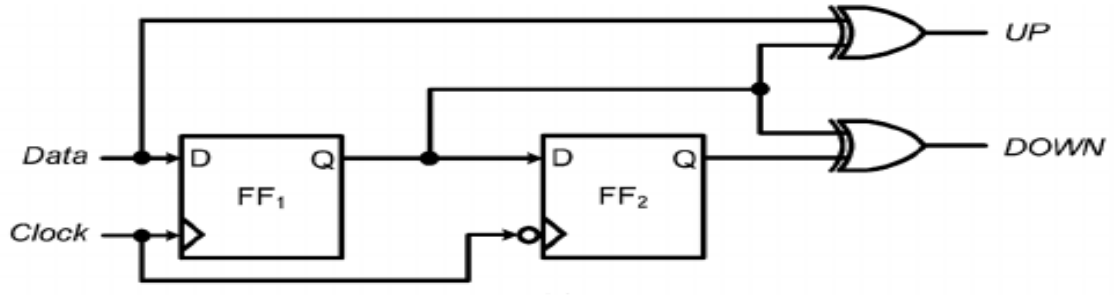


Phase detector :

The phase detector is the first component of the CDR. It takes the incoming bit stream and generated clock signal from the VCO as inputs and compares the phase difference between them. The output of the phase detector serves as the input of the second component, which is the charge pump. The phase detector converts the incoming phase difference into voltage. When the CDR is locked, the phase difference between the reference clock and feedback clock should remain a constant value. An ideal linear phase detector produces an output signal whose DC value is linearly proportional to the phase difference. There is also another type of phase detector called binary PD which produces an error signal whose value depends only on the sign of phase error.

We use a linear phase detector, which has wider frequency acquisition range and enables loop parameter calculation

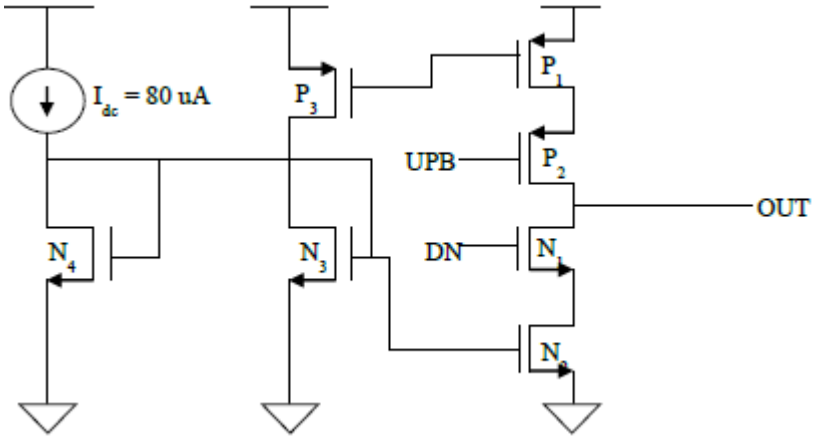
Hogge PD:



It consists of a positive edge triggered D flip-flop, a negative edge triggered D flip-flop and two XOR gates. Path UP produces proportional pulses in relation to phase difference while path DOWN produces half-clock-period-wide reference pulses. Under locked condition, UP and DOWN show pulses with equal width.

Charge Pump:

charge pump is the second stage of a CDR. A charge pump takes the output of the phase detector, a voltage signal, and transforms it into a current signal. Since the voltage-controlled oscillator needs a stable voltage signal to generate stable frequency signal, a large-valued capacitor is necessary.



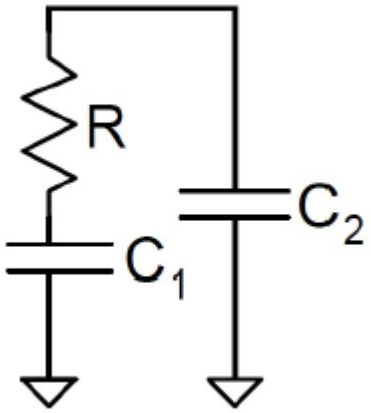
Charge pump primarily transfers both the PFD digital outputs to a single current signal. It helps in maintaining a steady control signal for maintaining the VCO frequency. Charge pump accumulates the charge in the loop filter capacitor. For the reduction of the error signal to a very small value an improved charge pump is used which is shown below . The charge pump is operated by the signals UPB

and DN. These signals are generated by the PFD. When P1 gets ON, UPB goes high. Similarly when N1 is ON, DN becomes low.

Low-pass Filter:

The output of the phase detector typically has a lot of high-frequency noise. Therefore, the LPF is to eliminate the high-frequency noise. Moreover, we need a charge storage device to maintain a stable input voltage signal to the voltage-controlled oscillator.

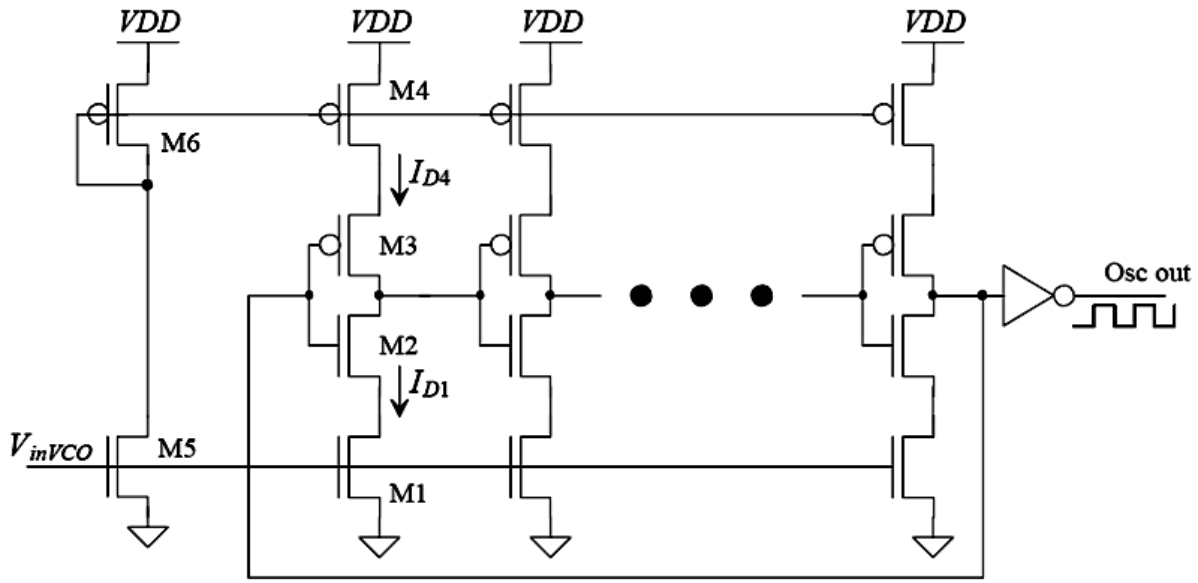
We will consider a passive loop filter in this case because it offers greater noise and power rejection performance and it is simpler to implement. It consists of a resister in series with a capacitor and they are in parallel with another capacitor



Voltage-Controlled Oscillator:

A voltage-controlled oscillator (VCO) is a device that can take in a control voltage and generate an output at a specific frequency. The output frequency ideally should be proportional to the input control voltage. There are two types of oscillators, ring oscillator and LC-tank oscillator. The ring oscillator is a digital circuit which has an odd number of inverters, with the last inverter output connected as the input to the first inverter. By utilizing the fact that the delay of each inverter depends on the amount of current it can sink in, the frequency of oscillation can be controlled.

Current Starved VCO :



This current starved VCO is designed using ring oscillator and its operation is also similar to that. From the schematic circuit shown in the Figure , it is observed that MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for the current. The MOSFETs M5 and M6 drain currents are the same and are set by input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage. The upper PMOS transistors are connected to the gate of M6 and source voltage is applied to the gates of
all lower NMOS transistors

VCO Design :

To determine the design equations for use with the current-starved VCO, the total capacitance on the drains of M2 and M3 is given by

$$C_{tot} = C_{out} + C_{in}$$

$$C_{tot} = C'_{ox}(W_p L_p + W_n L_n) + \frac{3}{2} C'_{ox}(W_p L_p + W_n L_n) \quad \ldots(1)$$

This is simply the output and input capacitances of the inverter. The equation can be written in more useful form as

$$C_{tot} = \frac{5}{2} C'_{ox}(W_p L_p + W_n L_n) \quad \ldots\ldots(2)$$

The time it takes to charge C_{tot} from zero to V_{SP} with the constant current I_{D4} is given by

$$t_1 = C_{tot} \cdot \frac{V_{SP}}{I_{D4}} \quad \ldots\ldots\ldots\ldots\ldots(3)$$

While the time it takes to discharge C_{tot} from VDD to V_{SP} is given by

$$t_2 = C_{tot} \cdot \frac{VDD - V_{SP}}{I_{D1}} \quad \ldots\ldots\ldots\ldots\ldots\ldots(4)$$

If $I_{D4} = I_{D1} = I_D$ (which is labelled as $I_{Dcenter}$ when V_{inVCO} = VDD/2), then the sum of t_1 and t_2 is simply

$$t_1 + t_2 = C_{tot} \cdot \frac{VDD}{I_D} \quad \ldots\ldots\ldots\ldots\ldots\ldots(5)$$

The oscillation frequency of the current starved VCO for N (an odd number >= 5) of stages is

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{1}{N \cdot C_{tot} \cdot VDD} \quad \ldots\ldots\ldots(6)$$

The centre frequency (f centre) of the VCO when $I_D = I_{Dcenter}$. The VCO stops oscillating, neglecting sub-threshold currents, when $V_{inVCO} < V_{THN}$. Therefore, $V_{min} = V_{THN}$ and $f_{min} = 0$.

The maximum VCO oscillation frequency, f_{max}, is determined by finding I_D when V_{inVCO} = VDD. At the maximum frequency, V_{max} = VDD.

Matlab calculations for Jitter :

NTF= Noise Transfer function

$NTFIN(s)=\Phi OUT(s)/\Phi IN(s)=LG(s)/1+LG(s)$ -Input jitter (5ps given)

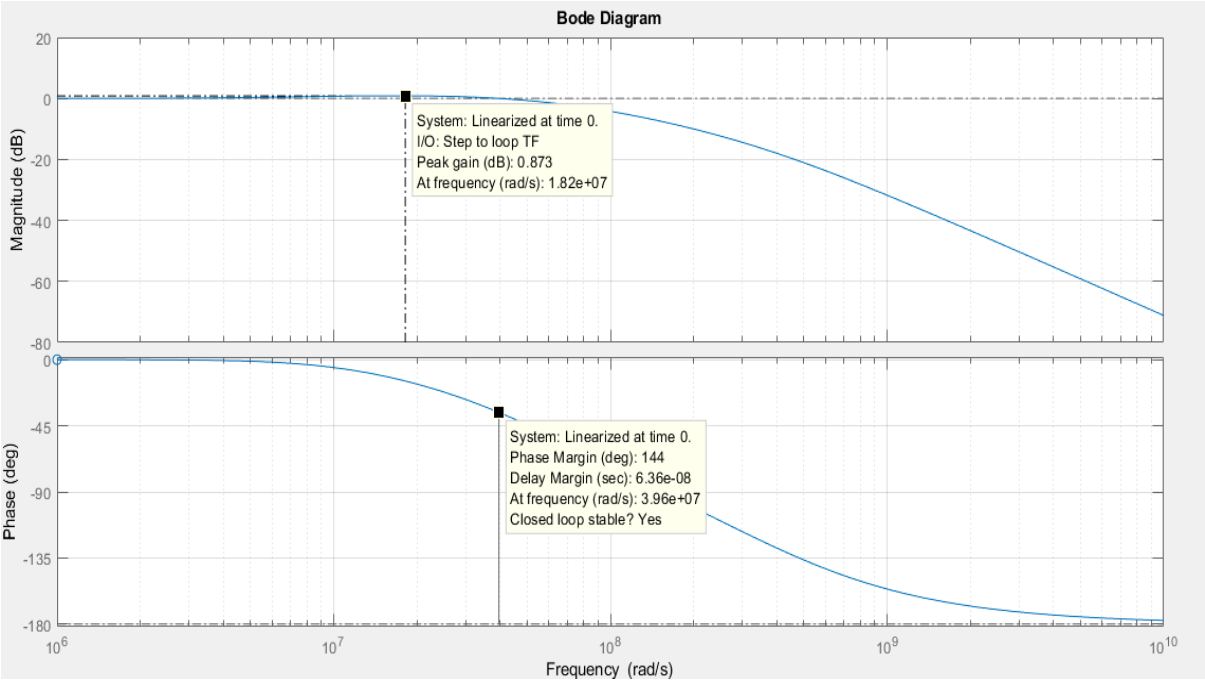
$NTFVCO(s)=\Phi OUT(s)/\Phi VCO(s)=1/1+LG(s)$ – VCO noise -100DBc/Hz

$S\Phi OUT/\Phi IN=P\Phi IN\cdot|NTFIN(s)|2$

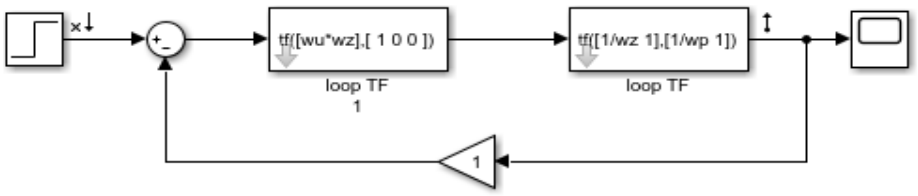
$S\Phi OUT/\Phi VCO$=P$\Phi VCO \cdot |NTFVCO(s)|2$

$S\Phi OUTTOTAL=S\Phi OUT/\Phi IN+ S\Phi OUT\ \Phi VCO$

Peak Gain of Closed loop Transfer function :



TF in Matlab :



Result :

parameters.m | systemparam.m

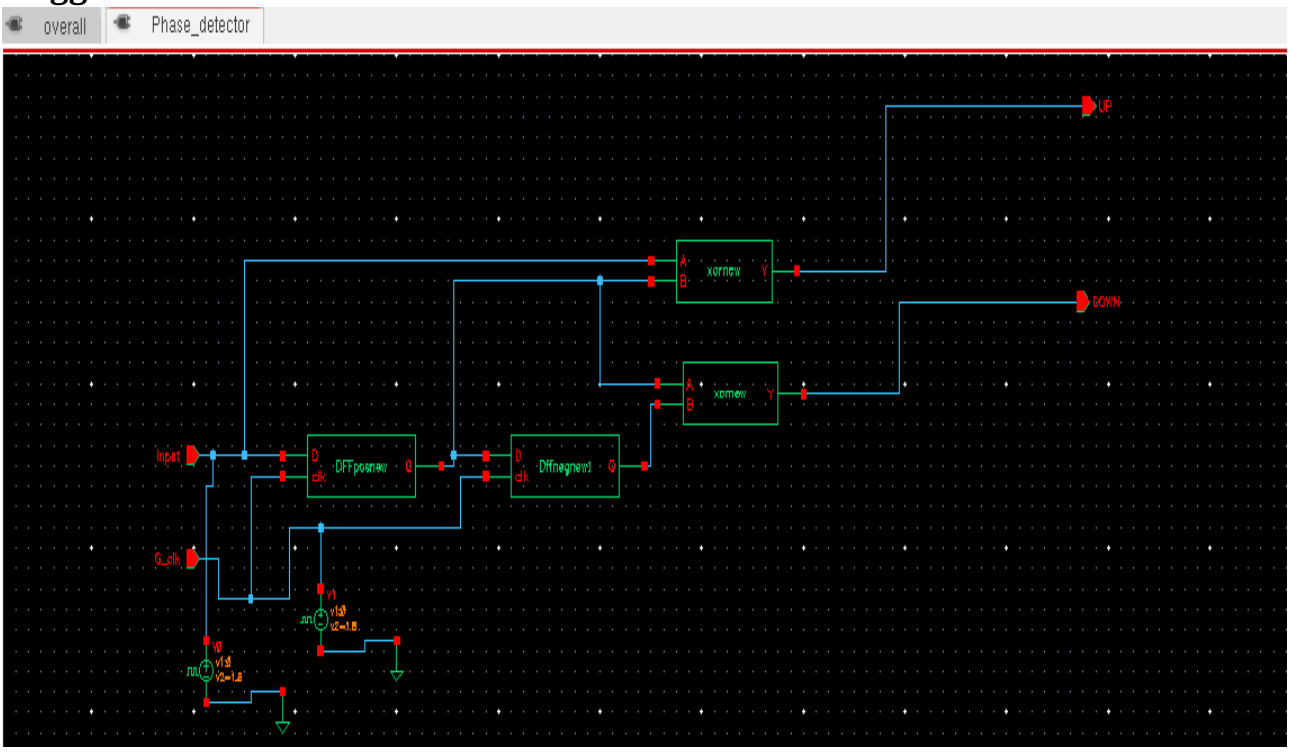
```
NTF_in=H_CLTF;
NTF_vco=1/1+H_LT;

fcn1= @(w) ((wu^2*wz^2*wp^2 + wu^2*wp^2*(w.^2))./((w.^6) + (w.^4)*wp^2 + wu^2*wz^2*wp^2 + wu^2*wp^2*(w.^2)));
fcn2= @(w) ((w.^6 + (w.^4)*wp^2)./((w.^6) + (w.^4)*wp^2 + wu^2*wz^2*wp^2 + wu^2*wp^2*(w.^2)));
```

Command Window

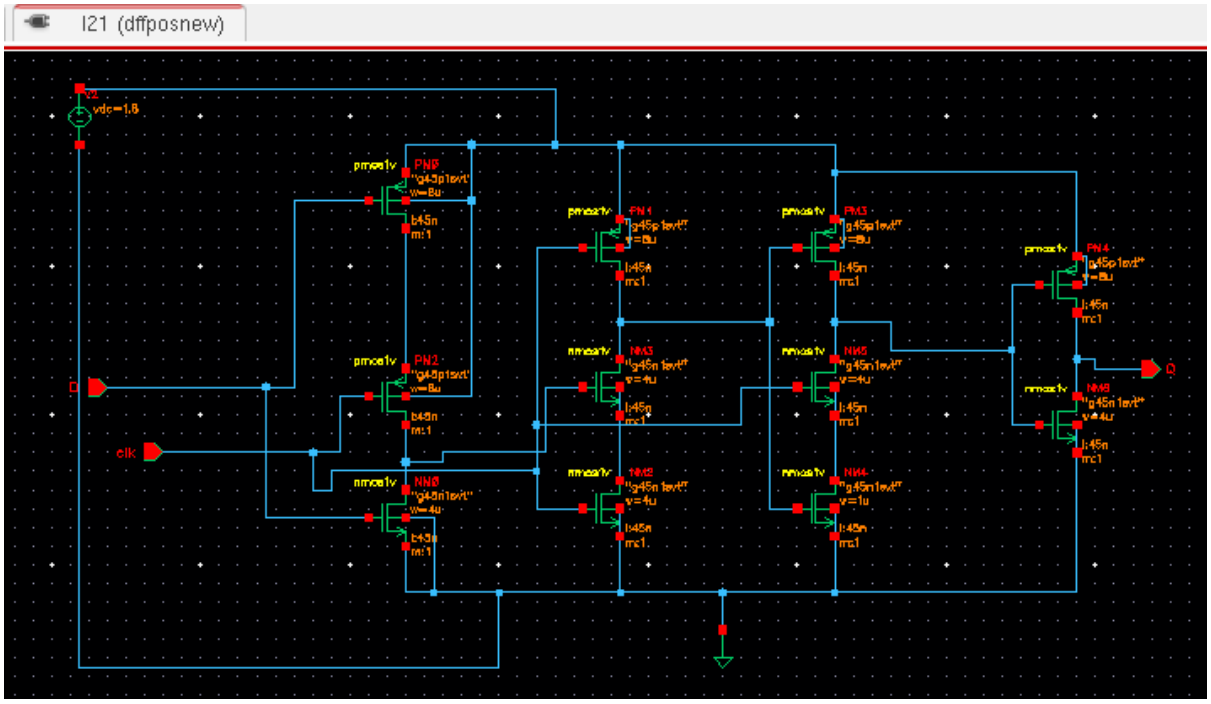
```
                2.226e30 s^4 + 9.992e38 s^3 + 8.79e45 s^2
  ------------------------------------------------------------------------
  8.057e13 s^6 + 7.087e22 s^5 + 1.781e31 s^4 + 9.992e38 s^3 + 8.79e45 s^2

Continuous-time transfer function.


pk_gain =

    0.8748


jitter =

   2.0953e-12
```

BLOCK LEVEL Circuits in Cadence :

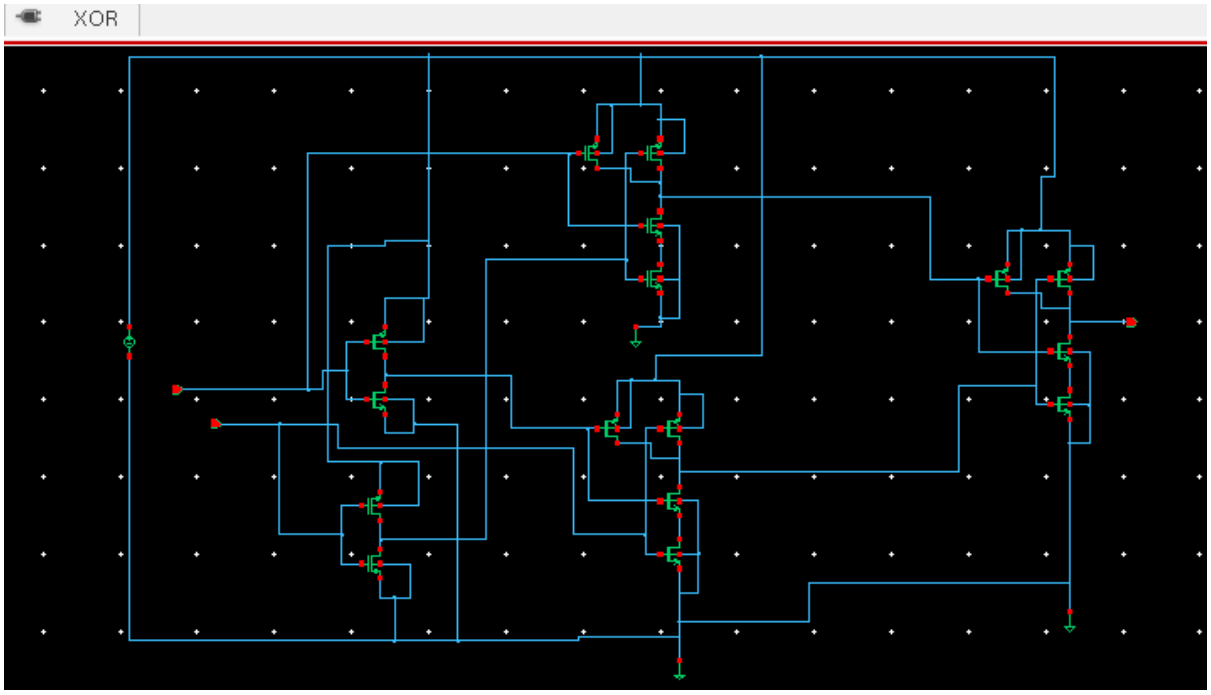
Hogge Phase Detector:



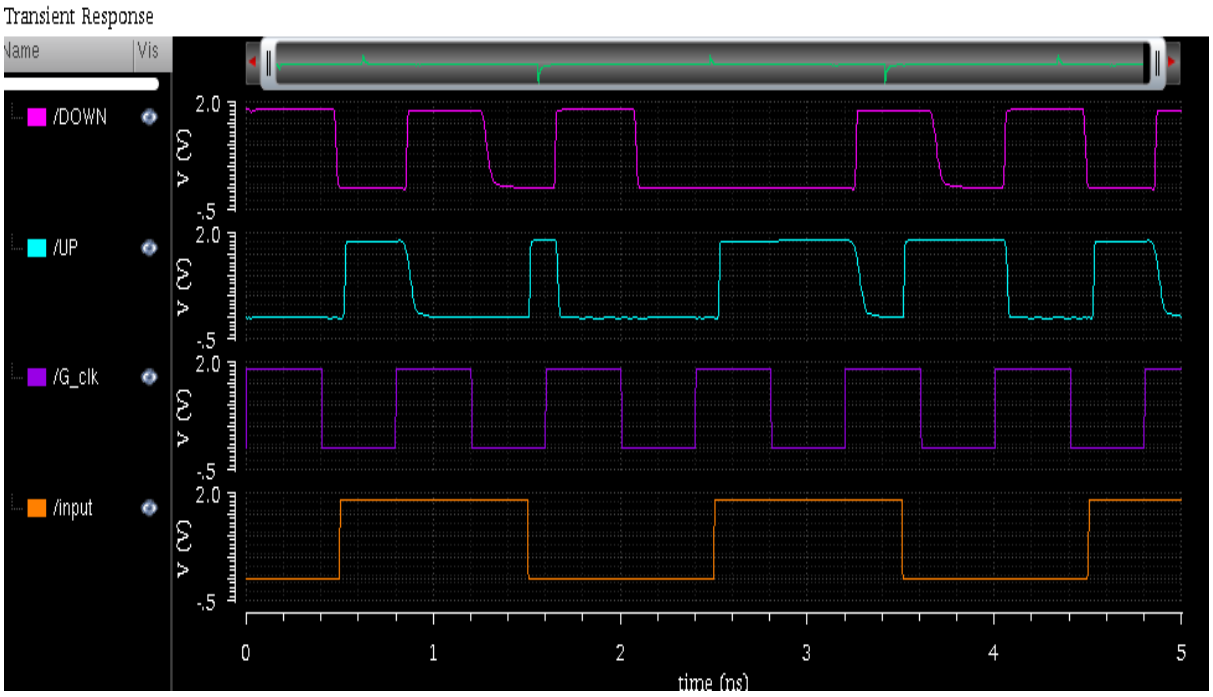
D-Flip Flop:



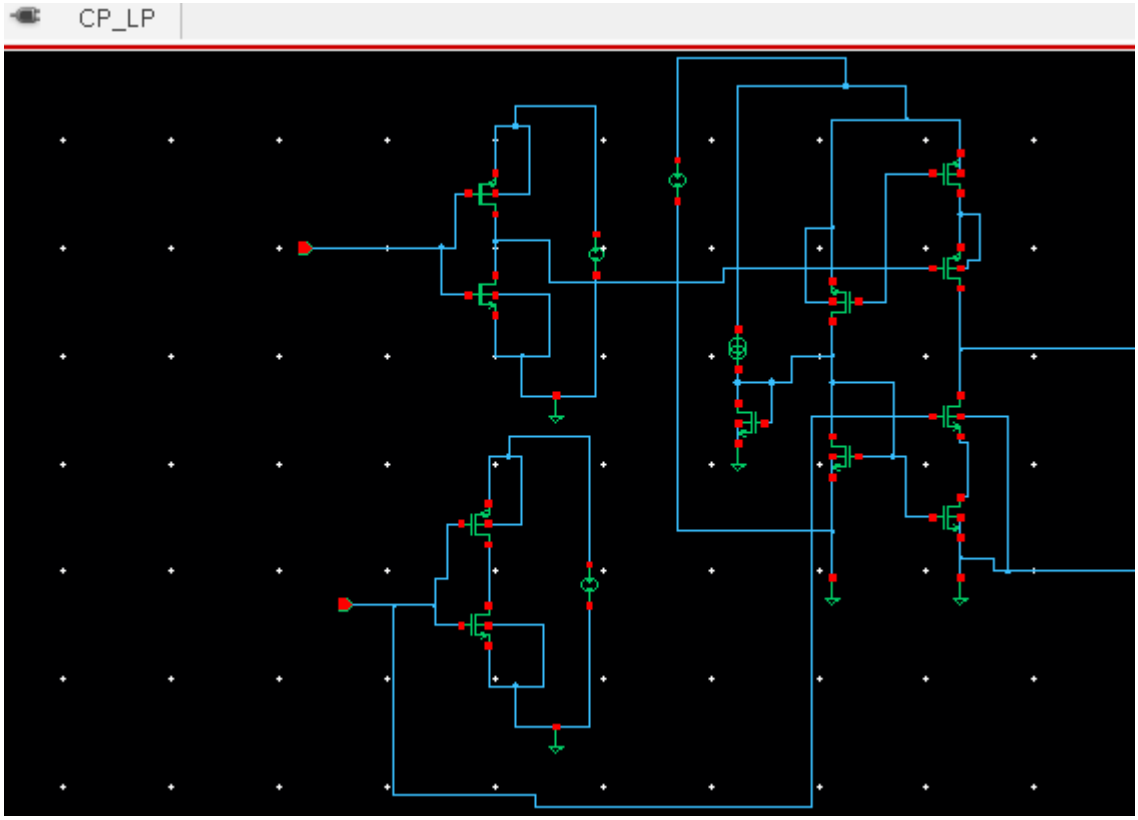
XOR gate:



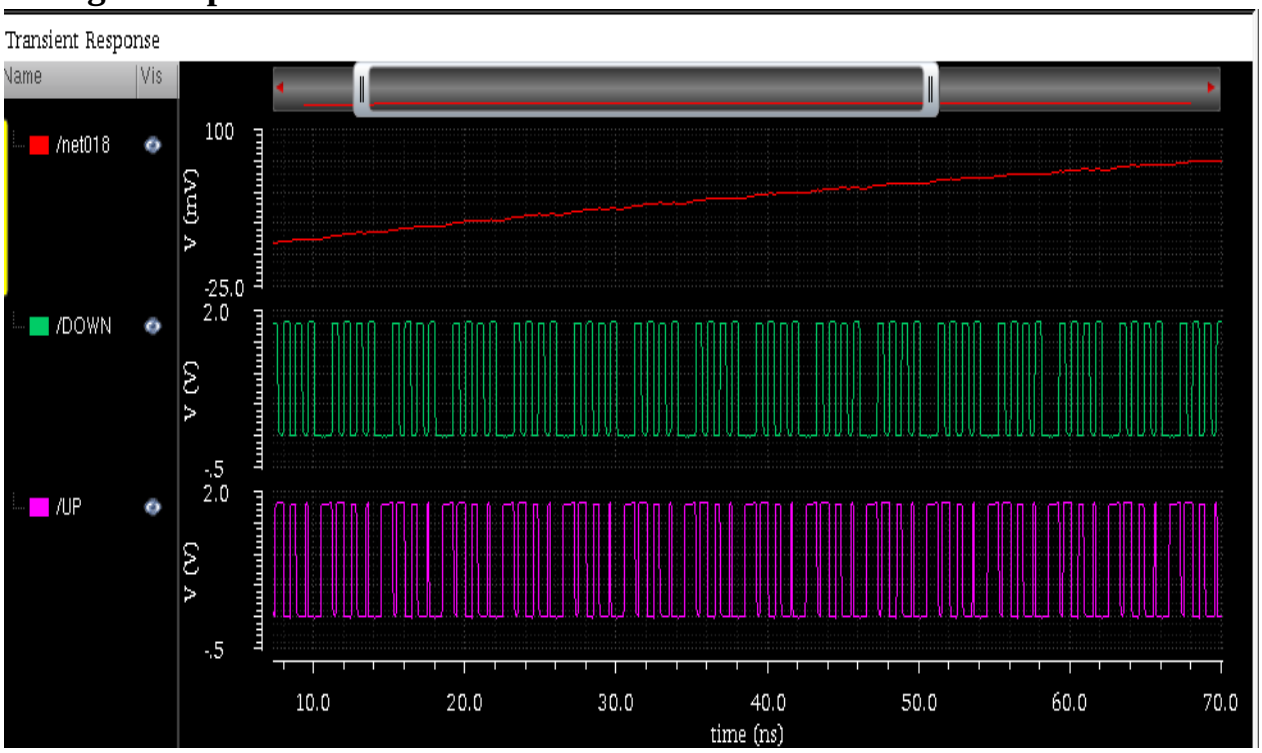
PFD Output Waveform :


Transient Response
Name
Vis
/DOWN
/UP
/G_clk
/input
2.0
-.5
0
1
2
3
4
5
time (ns)

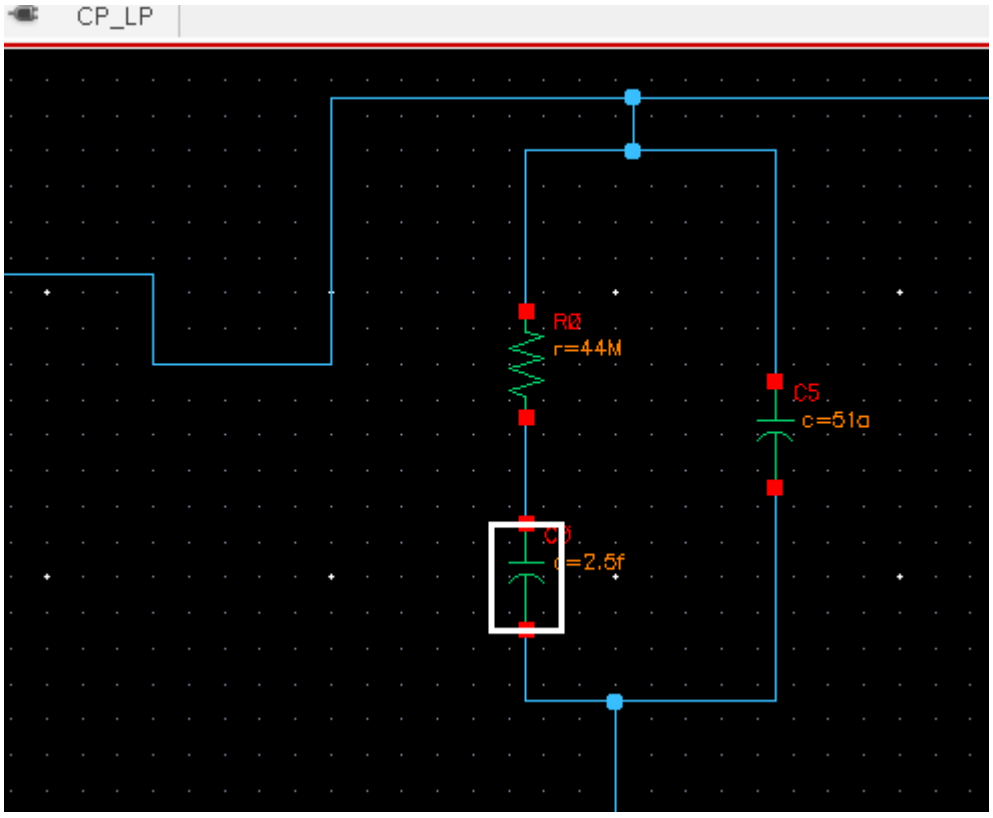
Charge Pump:


CP_LP

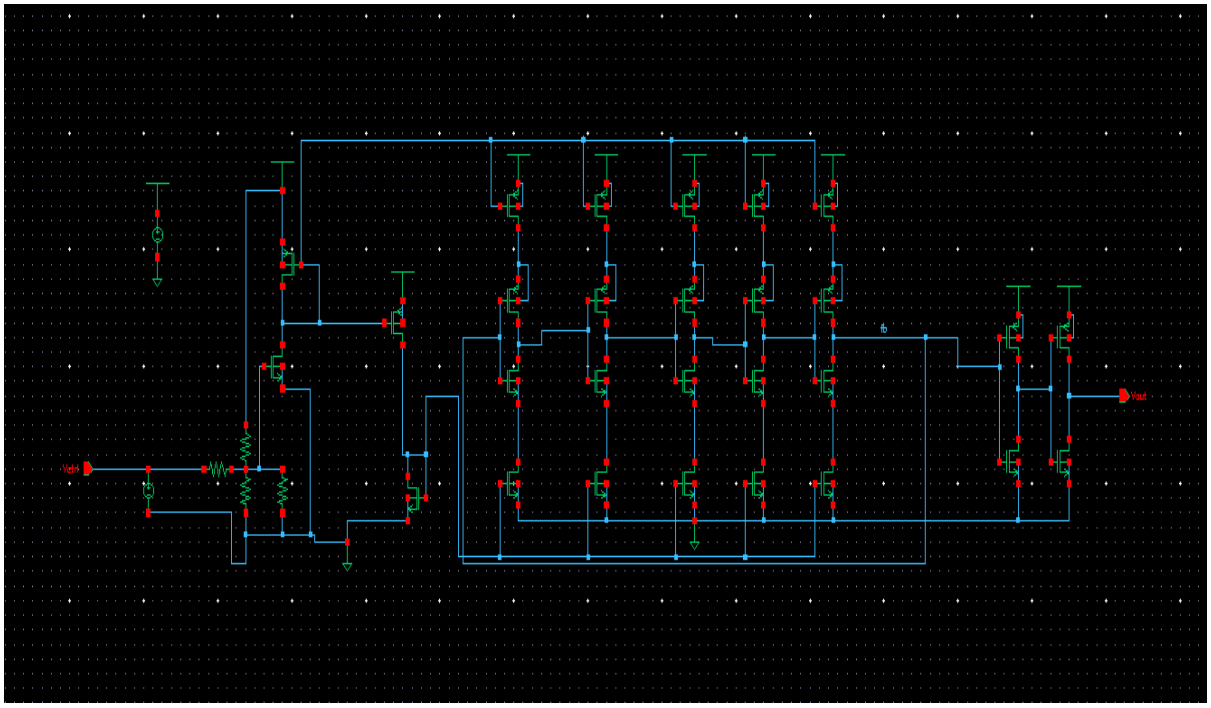
Charge Pump waveform :



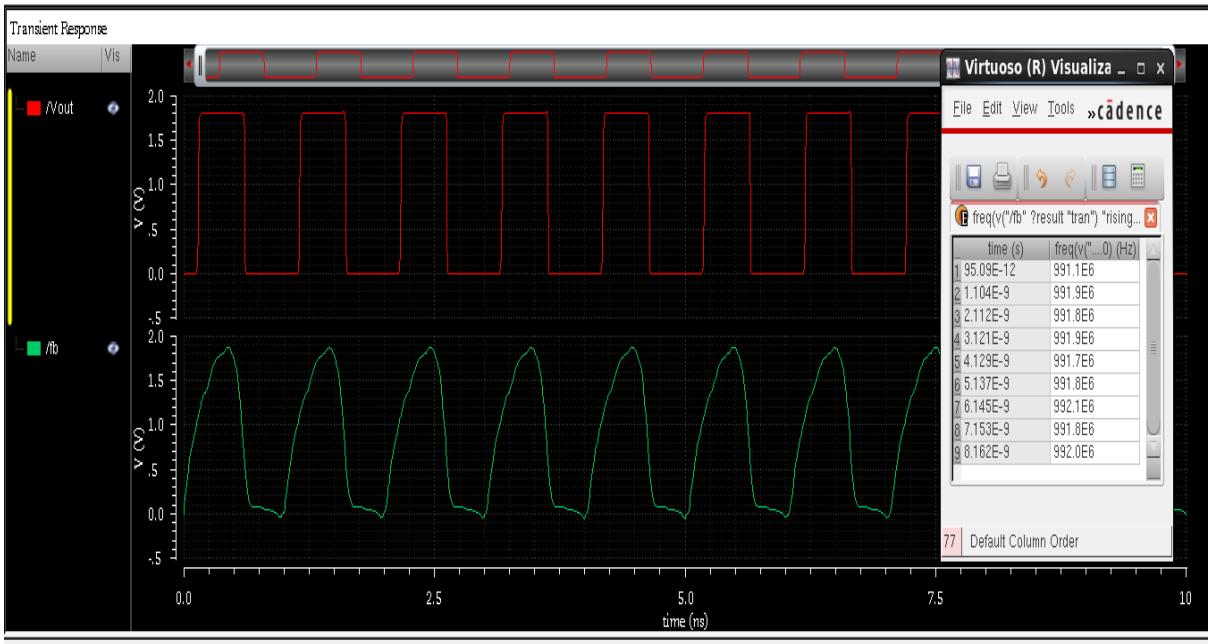
Loop Filter :



Voltage Controlled Oscillator :



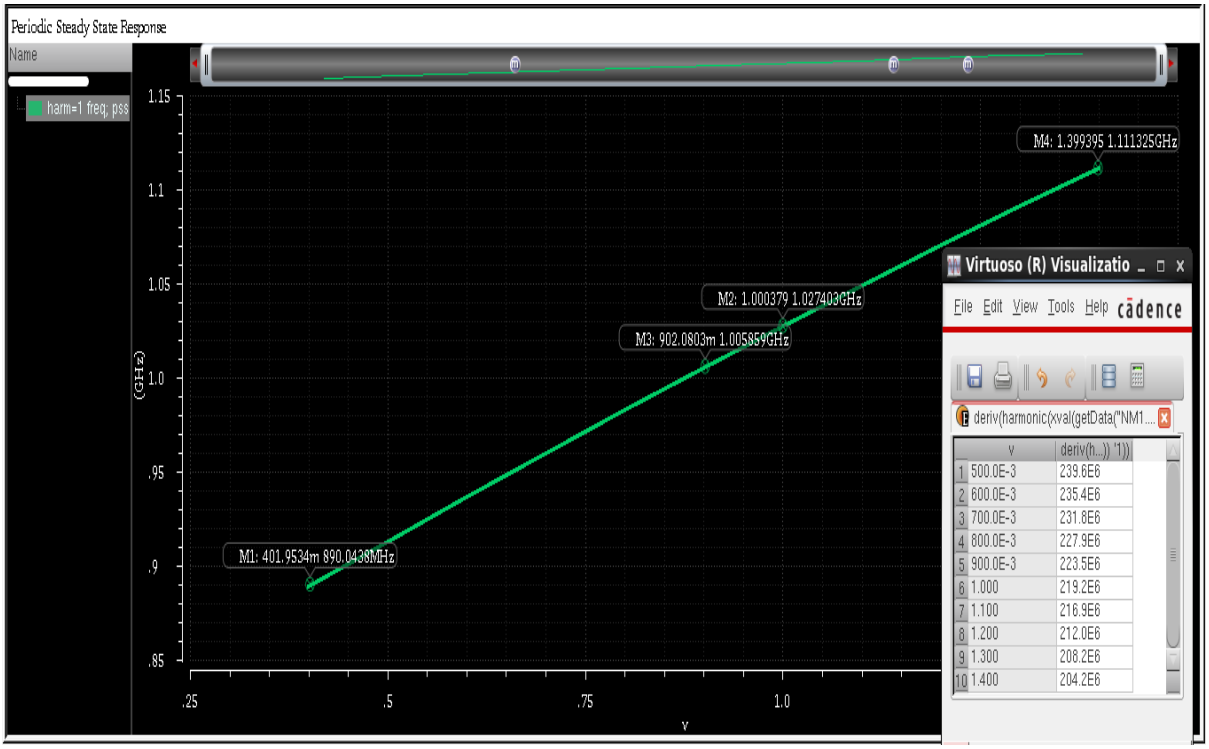
VCO output Waveform:



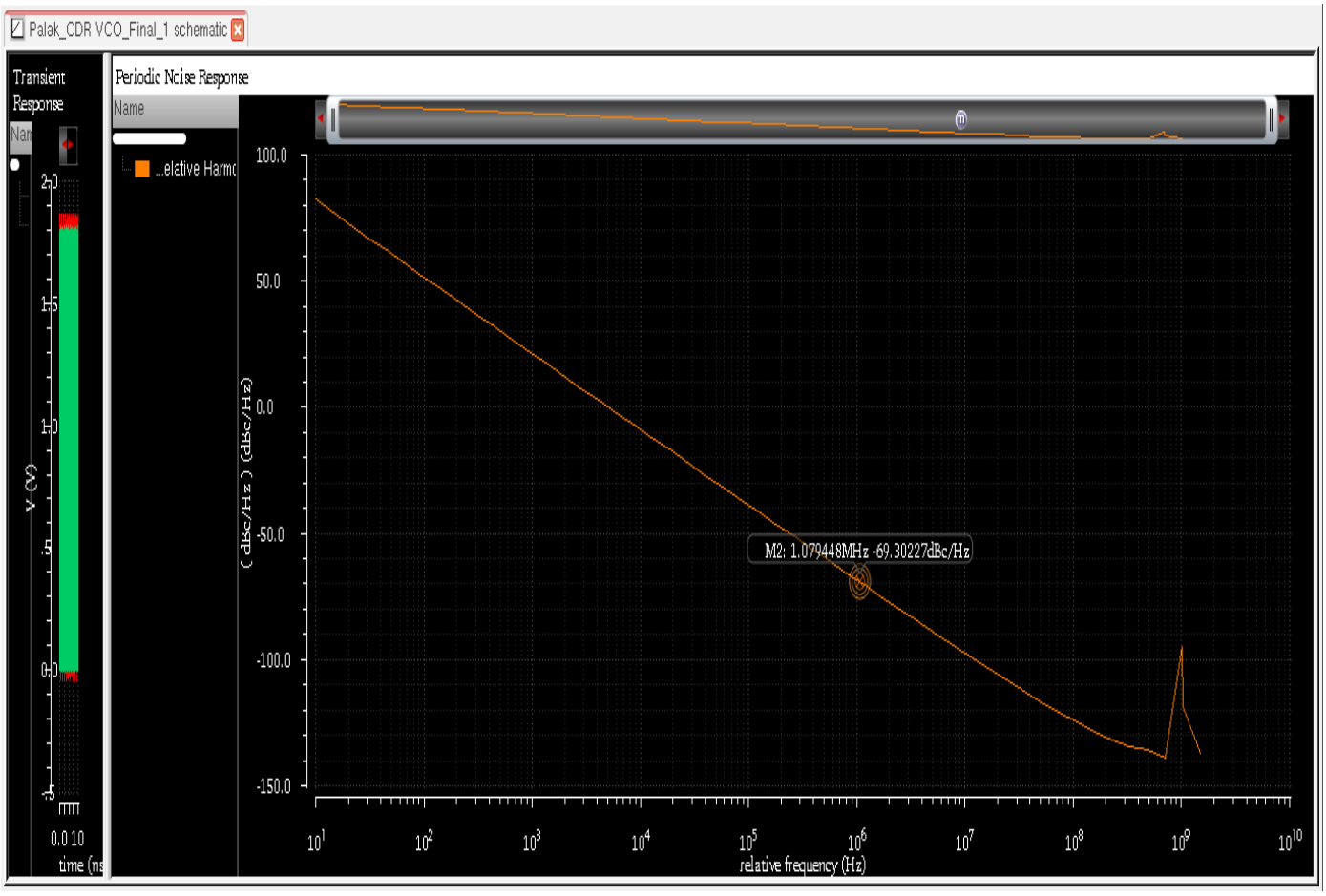
Results

Gain of VCO as a function of V control:

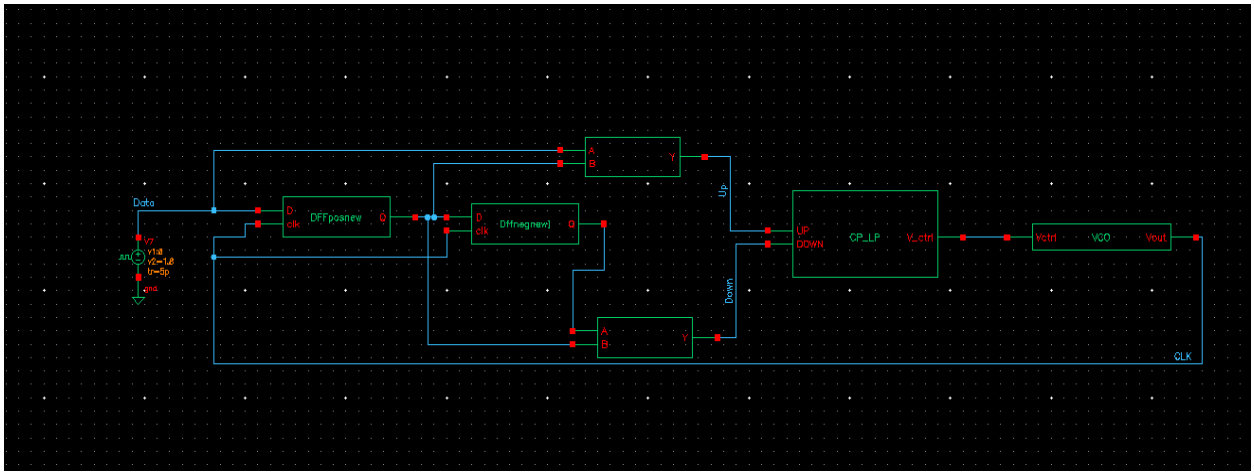
From the figure, Kv =220Mhz/V



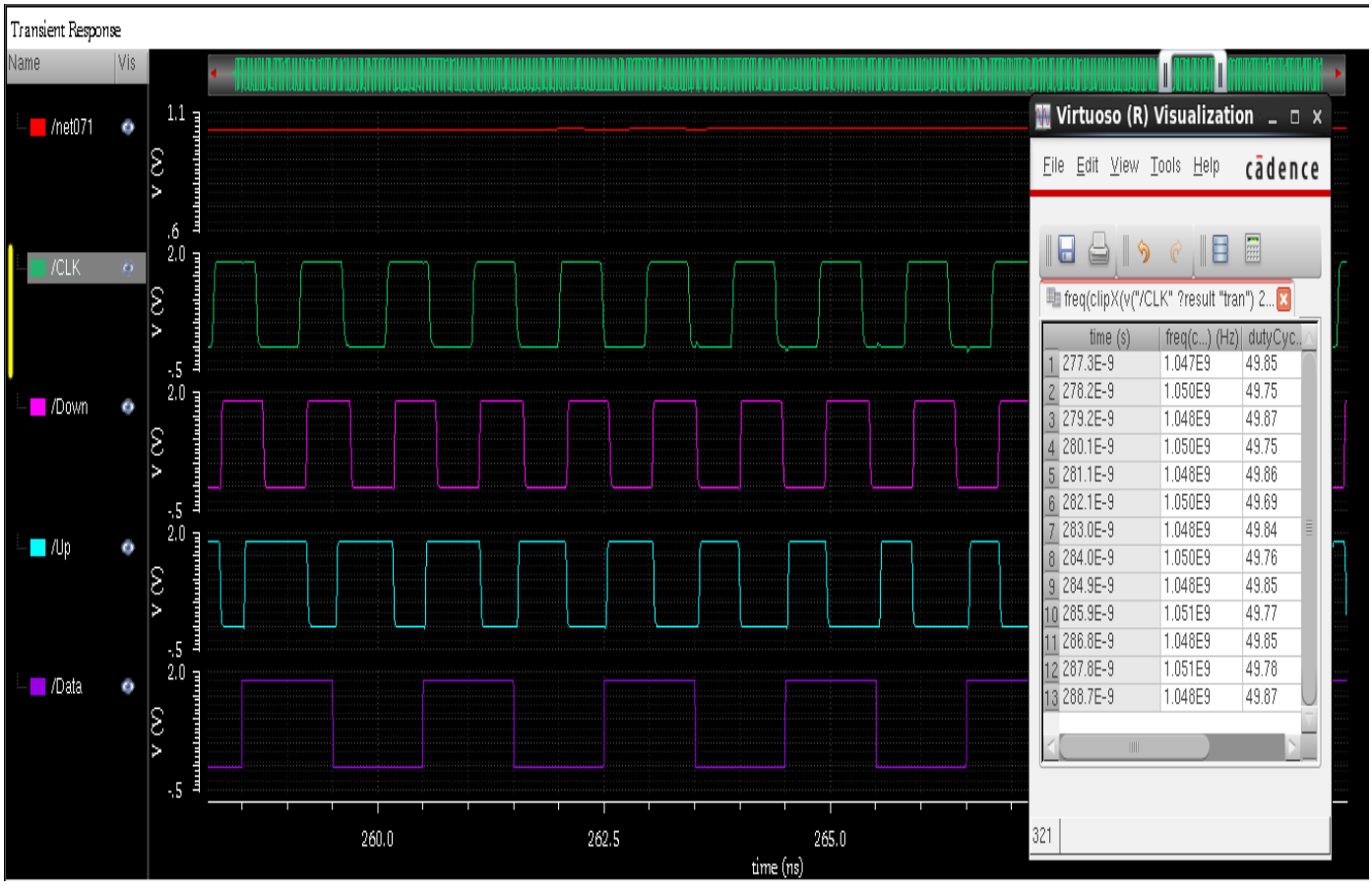
Phase noise Plot of VCO : -69Dbc/Hz @ 1Mhz Offset



Block Diagram of Overall System:

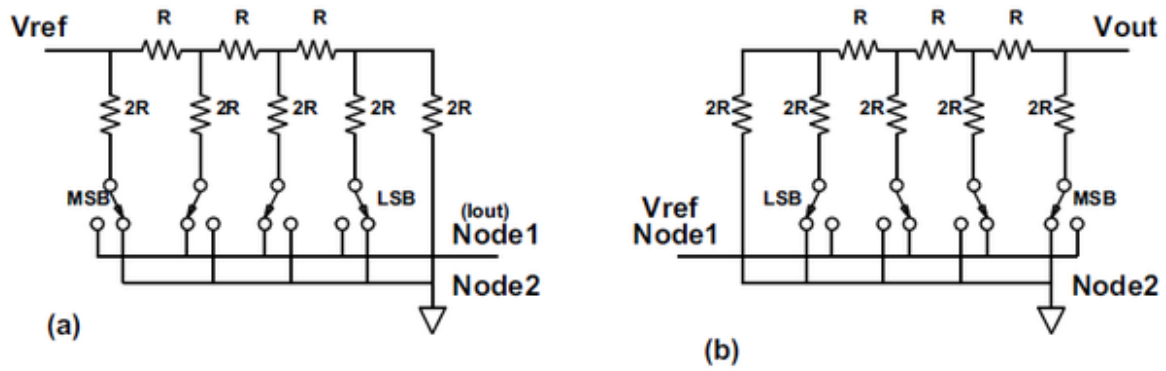


Locking of the Loop :

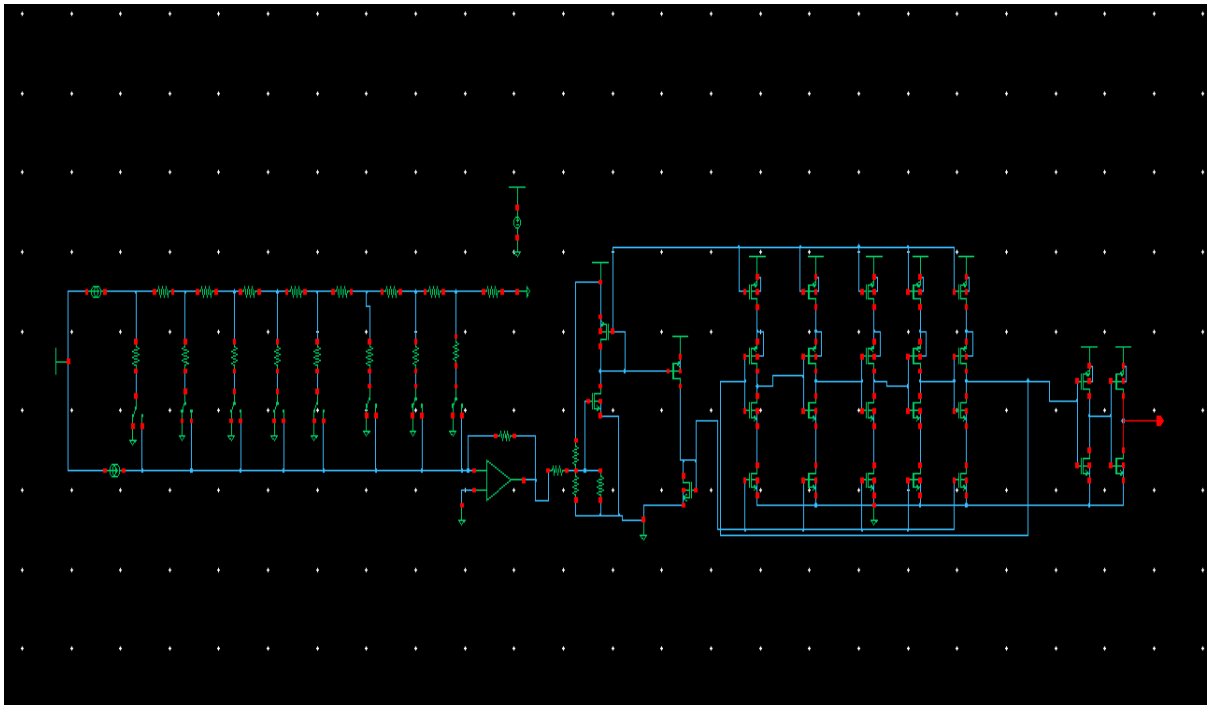


Digitally Controlled Oscillator :

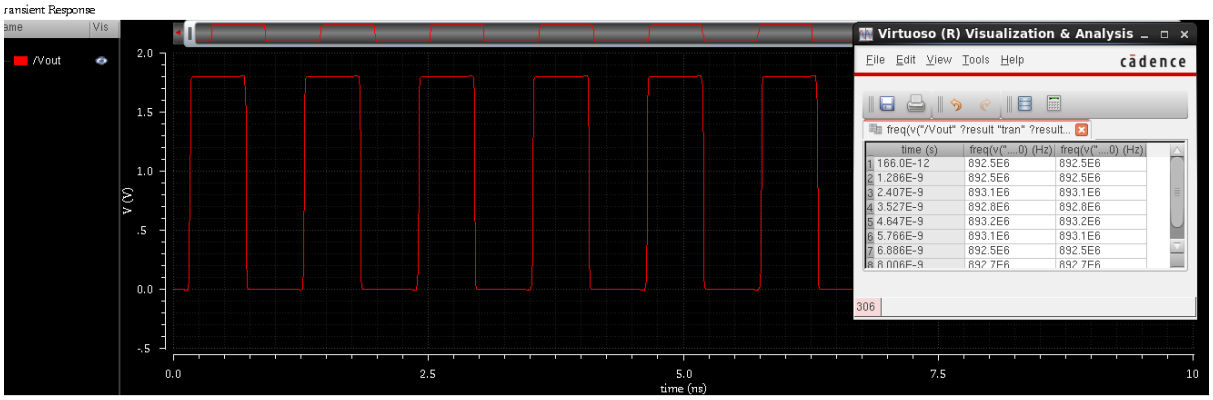
A DCO can be considered as a VCO that is synchronised to an external frequency reference. The reference in this case is the reset pulses. The counter acts as a frequency divider, counting pulses from a high frequency master clock (typically several MHz) and toggling the state of its output when the count reaches some predetermined value. The frequency of the counter's output can thus be defined by the number of pulses counted, and this generates a square wave at the required frequency. The leading edge of this square wave is used to derive a reset pulse to discharge the capacitor in the oscillator's ramp core. This ensures that the ramp waveform produced is of the same frequency as the counter output.



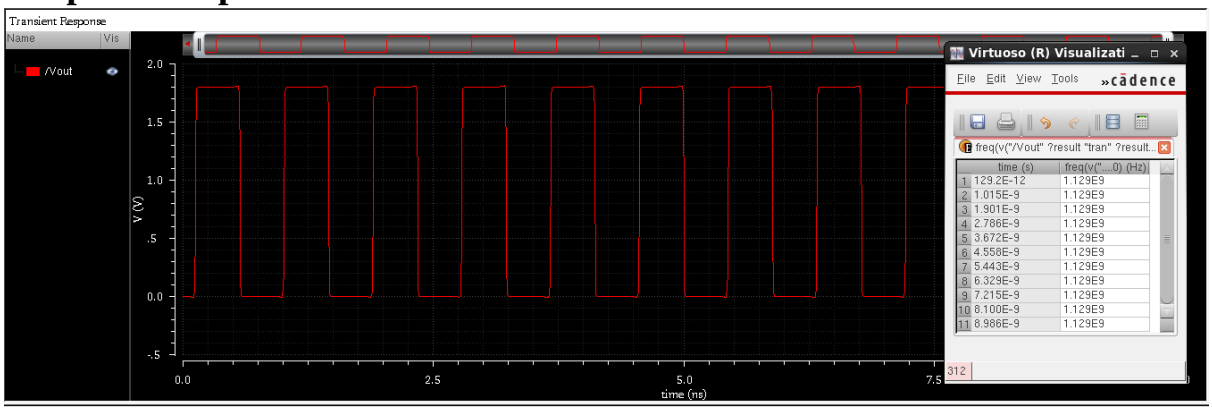
DCO implemented using Current switched DAC:



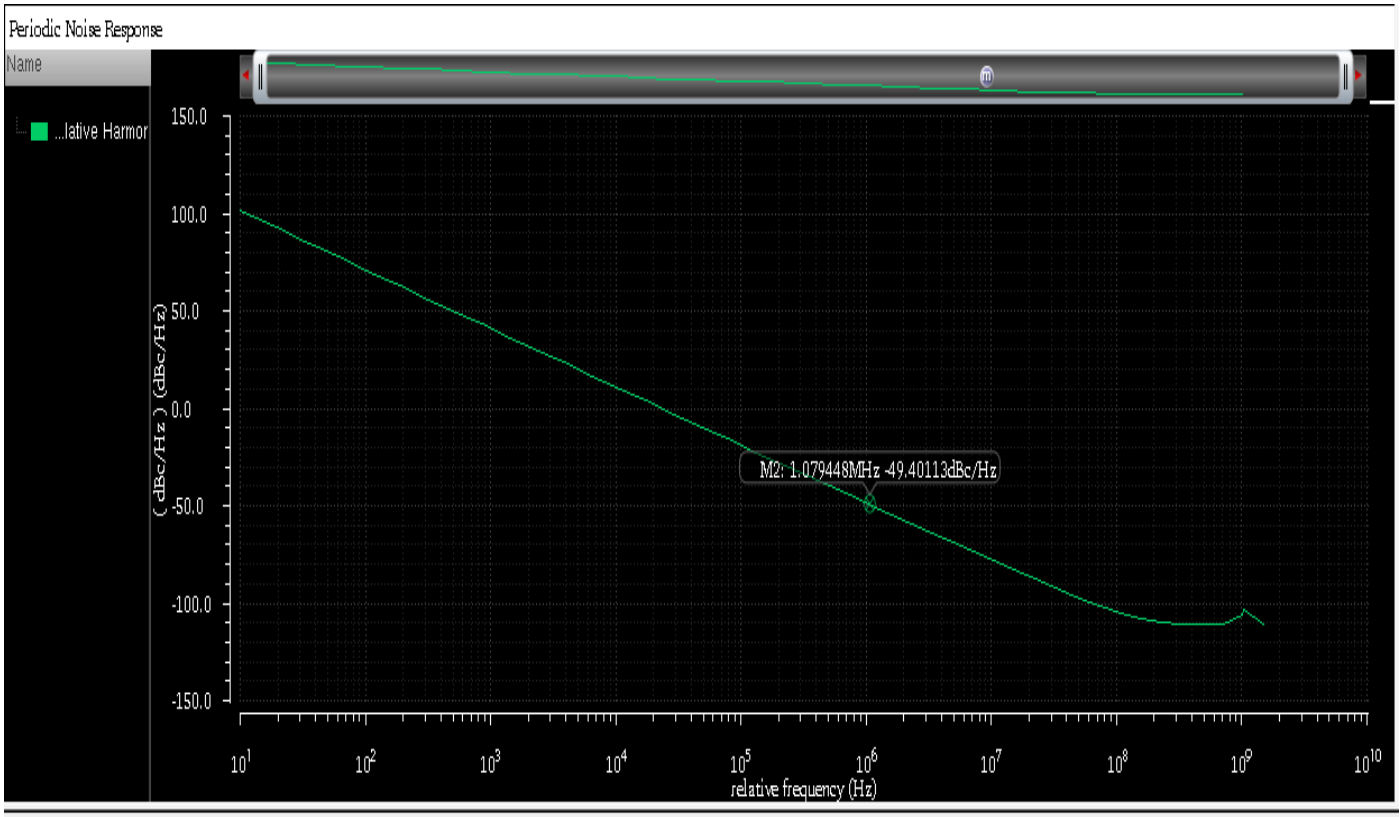
Output for input 00000000:



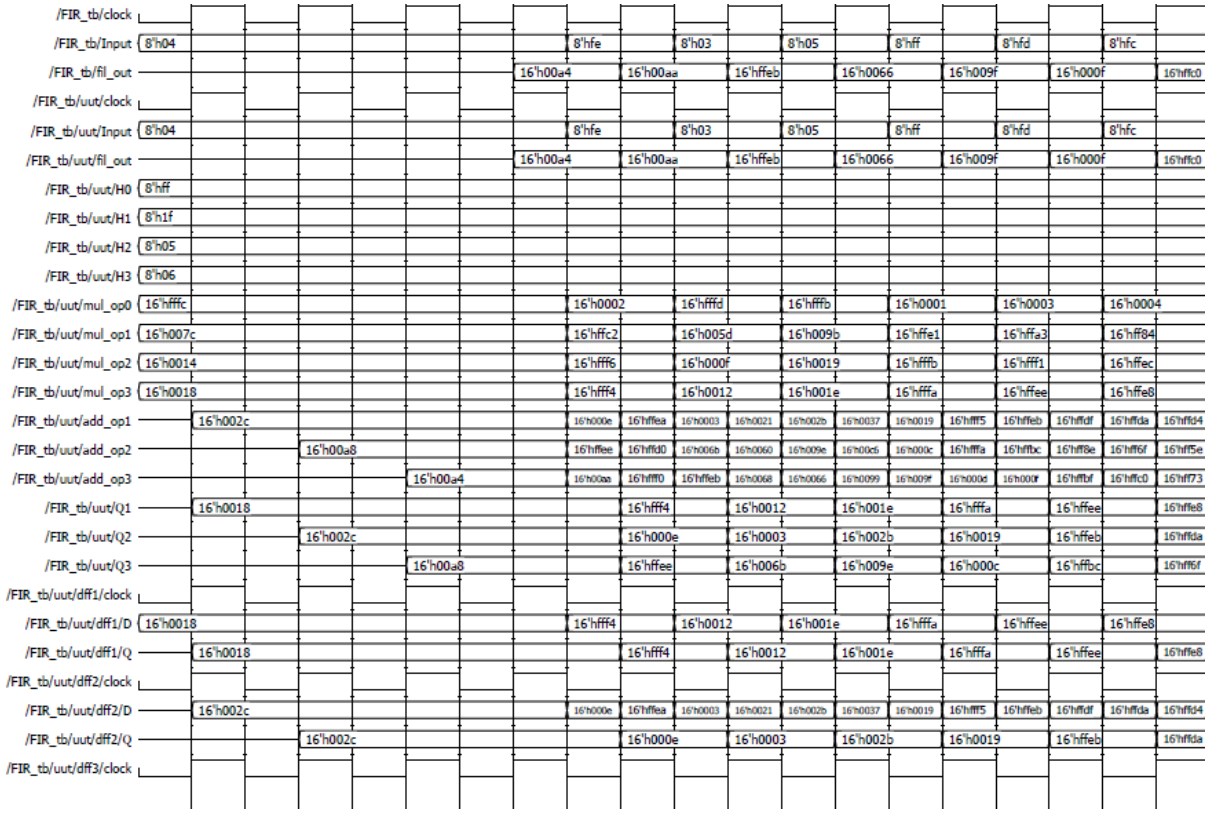
Output for input 11111111:



Phase noise Plot of DVCO : -49Dbc/Hz @ 1Mhz Offset :



4-Tap FIR FILTER Verilog Simulation:



Conclusion

The bandwidth of interconnects is becoming an increasingly important factor in modern computing systems and has led to a trend towards the use of serial interconnects. The integration of these interconnects into monolithic ICs provides benefits, especially in terms of system cost. The scaling of CMOS processes has enabled this integration, however the increasing variability associated with scaled processes means that robust design of integrated CDR circuits is becoming increasingly difficult.
Various CDR architectures were designed and implemented using Gpdk 45nm library. Various figures of merit used to characterize the performance of CDR circuits in both the frequency domain and the time domain were described.

References:

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