Integrating Drain Gating and Lector Techniques in Ultra Deep Submicron Technology to Reduce Leakage Power

Sukruth S

H20201400236

Abstract

In devices using extremely deep submicron technology, short channel effects are found due to scaling. Leakage current flows through the transistor as a result of the short channel effect, increasing the circuits' static power dissipation. Two prominent leakage reduction approaches, drain gating and lector techniques, are integrated in this study to minimise the leakage power of CMOS VLSI circuits. For various input vectors, this new combination approach is used to mimic various logic circuits. The performance of the inverter and NOR gate is evaluated in terms of dc power dissipation and propagation delay, and the results are compared to leakage reduction techniques already in use. The performance of the inverter and NOR gate is evaluated in terms of dc power dissipation and propagation delay, and the results are compared to leakage reduction techniques already in use. The combined impact of drain gating and lector methods results in a significant reduction in leakage power. For 45nm technology, the suggested method decreases the leakage power consumption of the Drain gating NOR gate by 44 percent and the Lector NOR gate by 22 percent.

Introduction

To extend battery life, potable electronic gadgets require very low power consumption. Power dissipation has been a major problem for CMOS VLSI circuits in recent years. To meet the needed performance standards, all sophisticated digital systems, such as mobile phones, laptops, and tablets, require very low power consumption. The power consumption in CMOS logic circuits is mostly made up of two components: static and dynamic power . For devices with a channel length of 180nm or less, dynamic power consumption was the most common . Because dynamic power consumption is quadratic in relation to supply voltage, dynamic power decreases dramatically when supply voltage is reduced. The reduction of static power dissipation is the primary issue of today's sophisticated technologies.

As the feature size shrinks, the constant filed scaling technique is used to scale down all voltage values. Due to non-ideal effects, lowering the threshold voltage produces an increase in leakage current. Gate oxide leakage power is also a substantial contributor to total leakage power. As the size of the feature shrinks, the constant filed scaling approach is used to scale down all voltage values. Non-ideal effects cause leakage current to rise when the threshold voltage is reduced . Overall leakage power is influenced by gate oxide leakage power as well.

As the feature size decreases, the constant filed scaling technique is used to scale down all voltage values. Because of non-ideal effects, lowering the threshold voltage produces a rise in leakage current . The leakage power of gate oxide also plays a significant role in overall leakage power. In this work we have focused on sub-threshold leakage power reduction.

The "Drain Gating Lector" is a novel circuit architecture suggested in this paper to reduce static power dissipation in CMOS technology. Drain gating and lector methods are two common approaches that are combined in the suggested technique. The benefits of both approaches have been combined in this study at the expense of area overhead.

Proposed work

To reduce leakage currents in CMOS circuits, a new hybrid design is suggested. Drain gating and lector methods are two common leakage reduction strategies that we have looked at here. To minimise static power usage, we combined these two approaches.

Figure 1 depicts the recommended circuit architecture. The leakage transistors LCT-P and LCT-N from LECTOR are shown here. DG-P and DG-N are two sleep transistors used in the drain gating method. As a result, the use of leakage transistors and sleep transistors aids in the stacking effect and raises the resistance between the supply voltage and ground terminal. The suggested logic is used to build an inverter circuit and a NOR gate, as shown in Figs. 2 and 3.

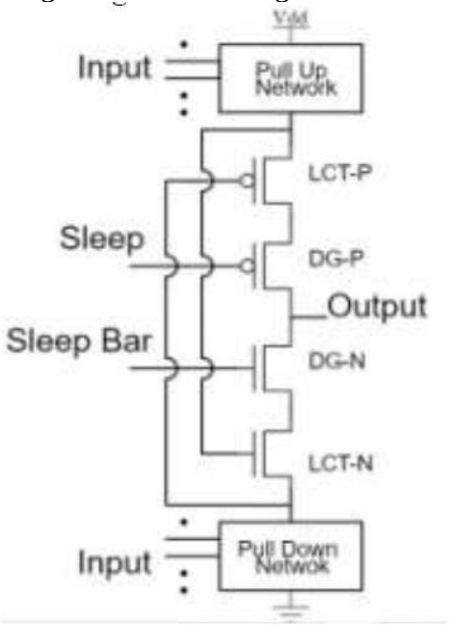

Fig. 1 General structure of the proposed technique

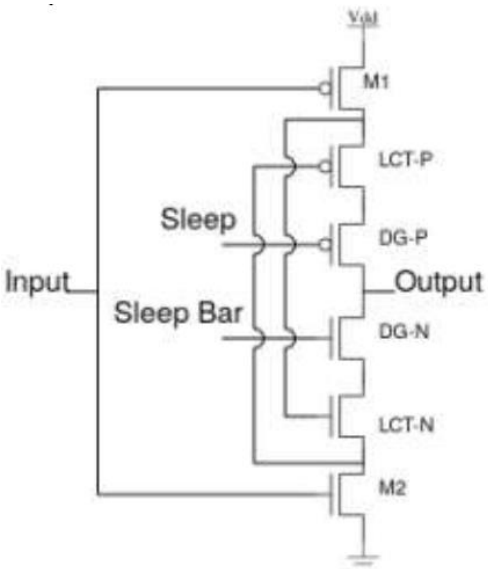

Fig. 2 Schematic of the inverter circuit

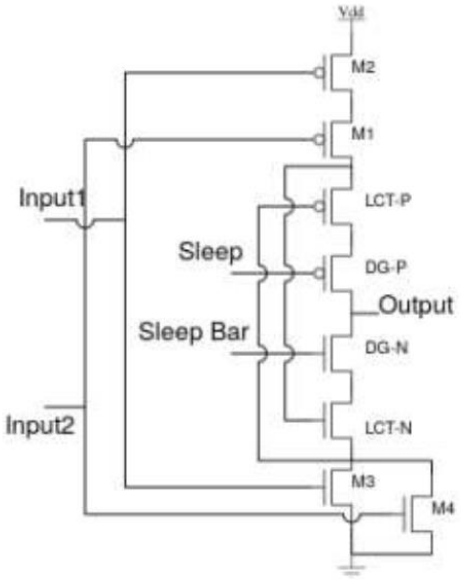

Fig. 3 The designed NOR gate using hybrid drain gating and lector technique

SIMULATION RESULTS AND DISCUSSIONS

Using 90nm and 45nm CMOS technologies, the suggested circuits are simulated in cadence. Figure 4 depicts the inverter circuit is simulated output. It is worth noting that the output waveform is an identical duplicate of the input waveform. For 90nm and 45nm technologies, the designed inverter uses static power of 0.39nW and 1.7nW, respectively.

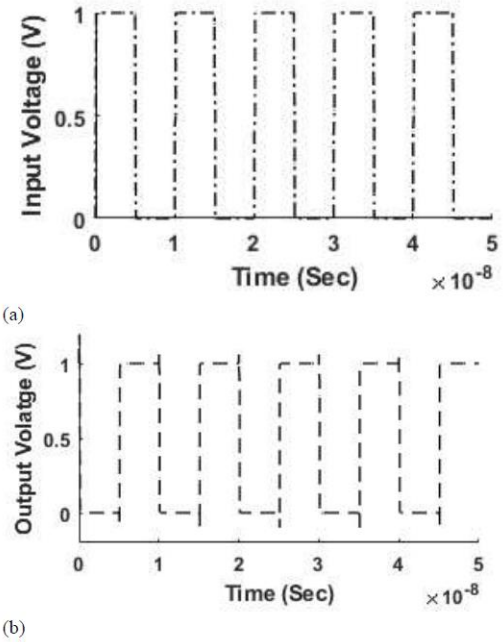

Fig. 4 simulation results of the designed inverter circuit showing (a) input and (b) output waveform

For 90nm technology, the average propagation delay is 34pS, while for 45nm technology, it is 46pS. Figure 5 shows the output voltage of the two-input NOR gate, as well as both inputs. It is worth noting that for each output, the complete signal swing is shown. The operation of the NOR gate for 45nm technology dissipates 4nW of power. The power consumption of 90nm is measured at 2.05nW.

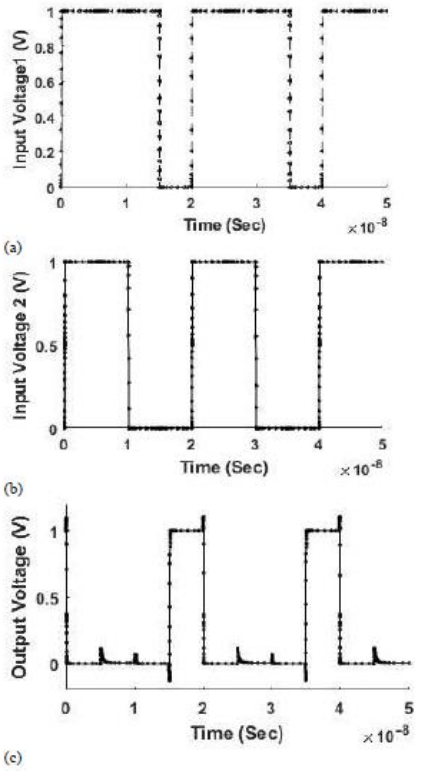

Fig. 5 simulated output of the implemented NOR gate, (a) input1 (b) input2 and (c) Output waveform

As a result, the power consumption nearly doubles from one technological node to the next. For 90nm and 45nm technologies, the average propagation delay is 63pS and 72pS, respectively. A comparison was made between the suggested approach and the current techniques, particularly the lector and drain gating techniques. In table I, a comparison of various approaches for an inverter circuit is shown. The suggested hybrid method is shown to produce the best results in terms of static power usage.

Table I: A comparison between leakage reduction techniques for inverter circuit

Leakage Reduction Technique	Static Power Consumption (nW)		Avg Propagation Delay (pS)	
	90nm	45nm	90nm	45nm
Drain Gating	1.05	2.6	35	47
Lector	1	2.3	60	93
Drain Gating Lector	0.39	1.7	37	50

In the 45nm technology node, the suggested inverter circuit provides a 35 percent and 26 percent improvement in leakage power consumption for drain gating and lector techniques, respectively. For both existing methods, the improvement in power consumption for 90nm technology is almost 60%. The suggested approach and the propagation delay drain gating technique provide almost identical results.

Table II: A comparison between leakage reduction techniques for NOR gate

Leakage Reduction Technique	Static Power Consumption (nW)		Avg Propagation Delay (pS)	
	90nm	45nm	90nm	45nm
Drain Gating	3.63	7.4	38	52
Lector	2.65	5.1	65	99
Drain Gating Lector	2.05	4	63	72

When using the 45nm technology node, the suggested inverter circuit reduces leakage power consumption by 35% and 26%, respectively, for drain gating and lector techniques. For both existing methods, the reduction in power consumption for 90nm technology is over 60%. Both the suggested method and the propagation delay drain gating technique yield almost identical results.

CONCLUSION

This study presents a new leakage reduction method. It is a hybrid of drain gating and lectoring. An inverter circuit and a NOR gate are designed using 45nm and 90nm CMOS technology to validate the suggested approach. For both of the circuits under examination, the simulation results indicate a rail to rail output signal swing. The static power consumption and average propagation latency are used to evaluate the performance of the constructed circuits.

The performance of the proposed circuit is clearly enhanced when compared to conventional techniques. The static power dissipation for the inverter circuit is 1.7nW, and the average propagation delay is 50pS.

In terms of static power consumption, the proposed inverter circuit improves by 35% and 26% for drain gating and lector techniques, respectively, while using 45nm technology. In the instance of the NOR gate, the drain gating and lector techniques are found to be 44 percent and 22 percent for drain gating and lector method, respectively. Although the suggested approach did not demonstrate any advantage in terms of propagation latency, it did not exhibit any substantial degradation when compared to existing strategies.