Design of low power SR-flip-flop with on/off (ONOFIC) implementation

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Abstract

Due to the superior scalability of the device structure, MOSFET-based ICs have constantly delivered cost reductions in semiconductor chips for data processing and memory. However, it is not without its shortcomings. In the nanoscale world, the most important ones are leakage power dissipation and propagation latency. Leakage power contributes more and more to total power dissipation. There are various techniques to reduce leakage in literature, each with its advantages and cons. One such implementation is the use of on-off logic, which includes two extra inserted transistors. In this study, the current ONOFIC methodology is upgraded and compared with pre-existing approaches. The improved ONOFIC methodology outperforms traditional, and leakage control NMOS transistor (LCNT) approaches in simulations. This report also highlights and compares various other leakage power reduction techniques with the modified proposed circuit concerning power, delay and other factors. Further, a comparison between the circuits based on technology node has also been explored.

Circuit schematics

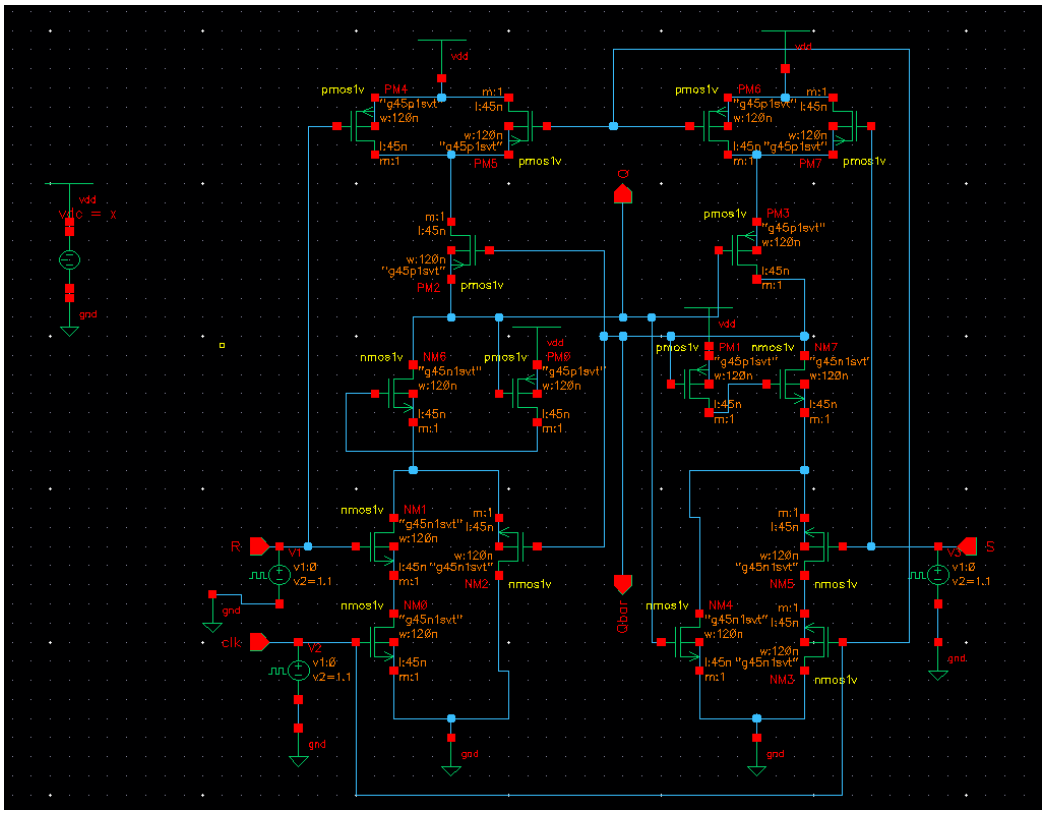


Figure 1. Onofic proposed in the paper.

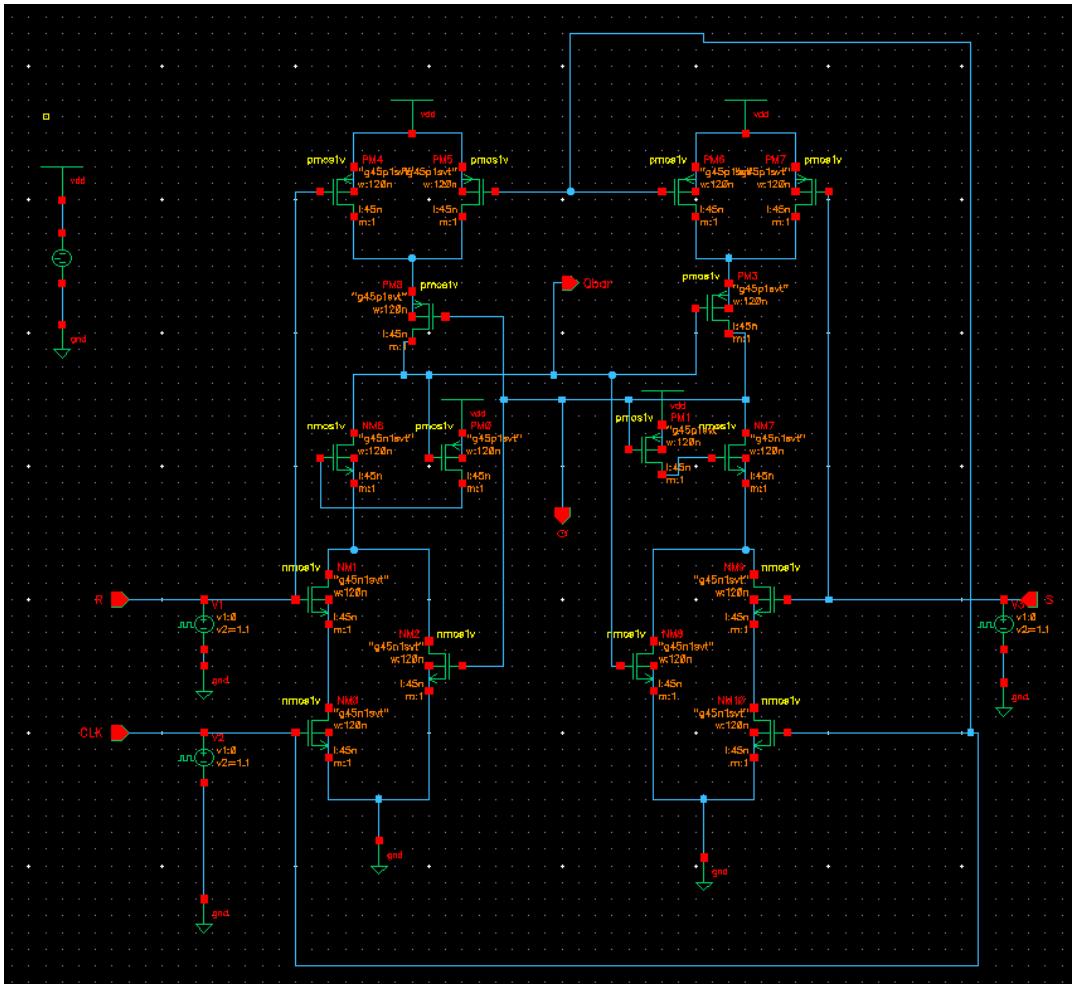


Figure 2. Onofic modified with complementary CMOS logic.

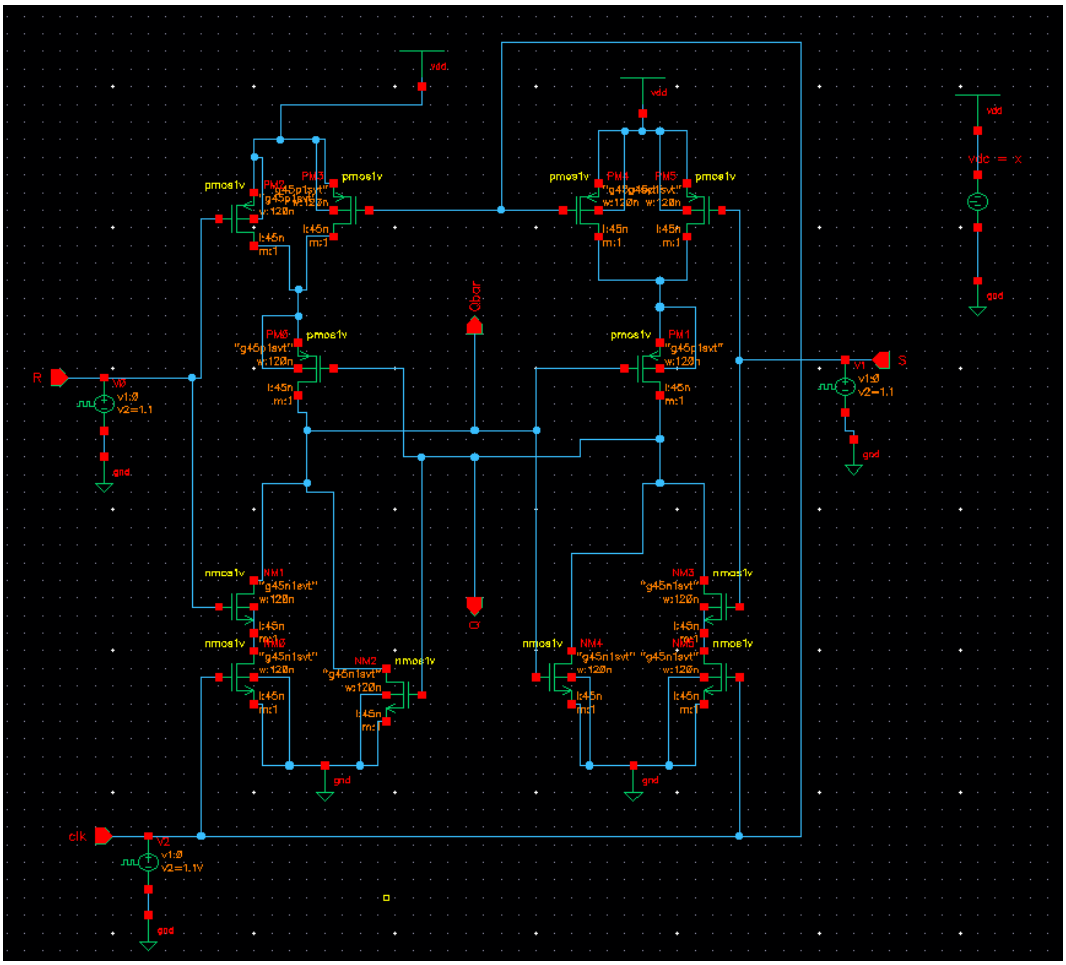


Figure 3. SR flip-flop modified with complementary CMOS logic.

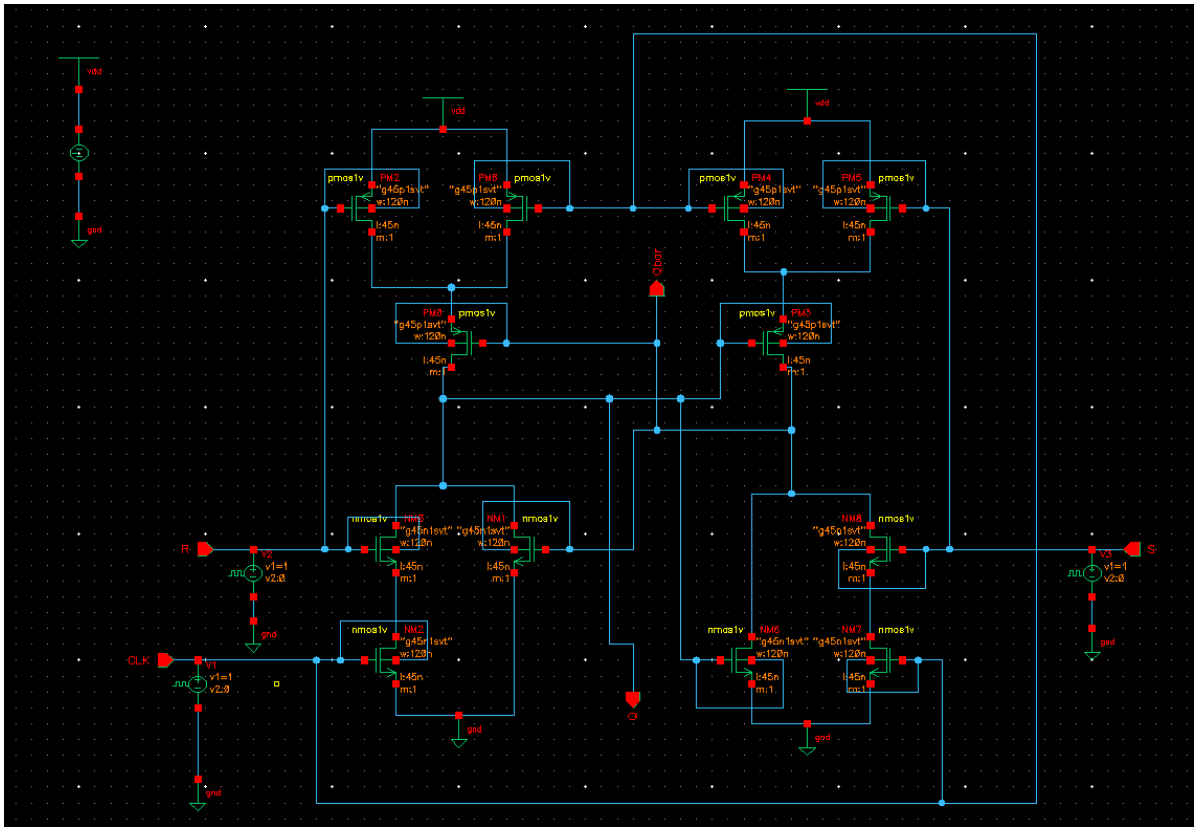


Figure 4. SR flip-flop with dynamic threshold MOS logic.

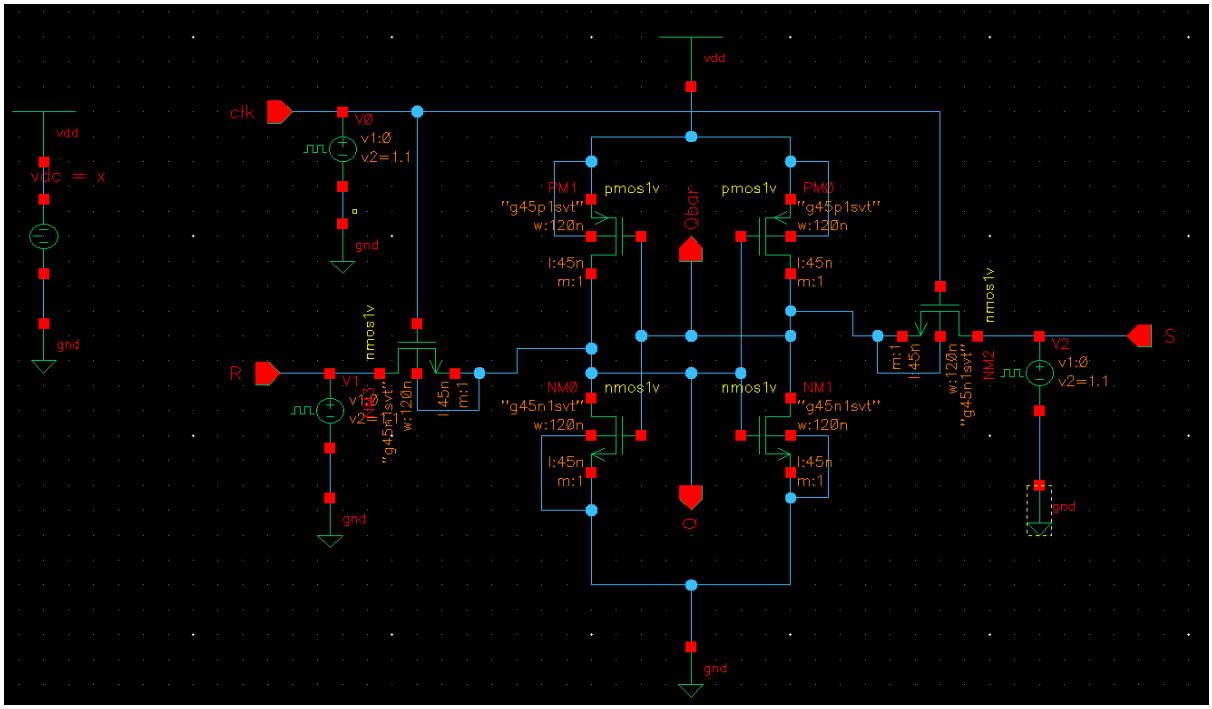


Figure 5. SR flip-flop using Transmission gate logic

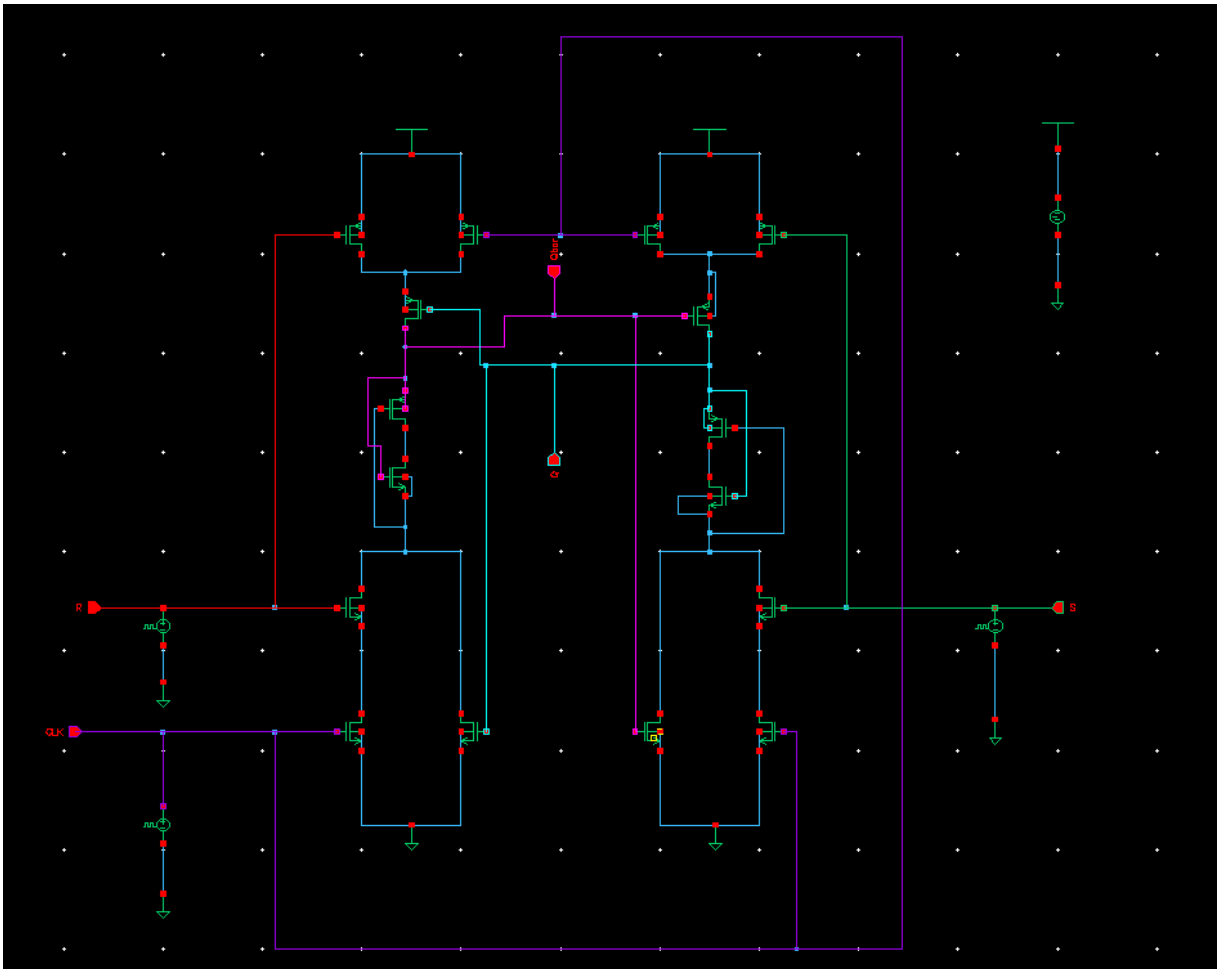


Figure 6. Lector implementation of SR flip-flop

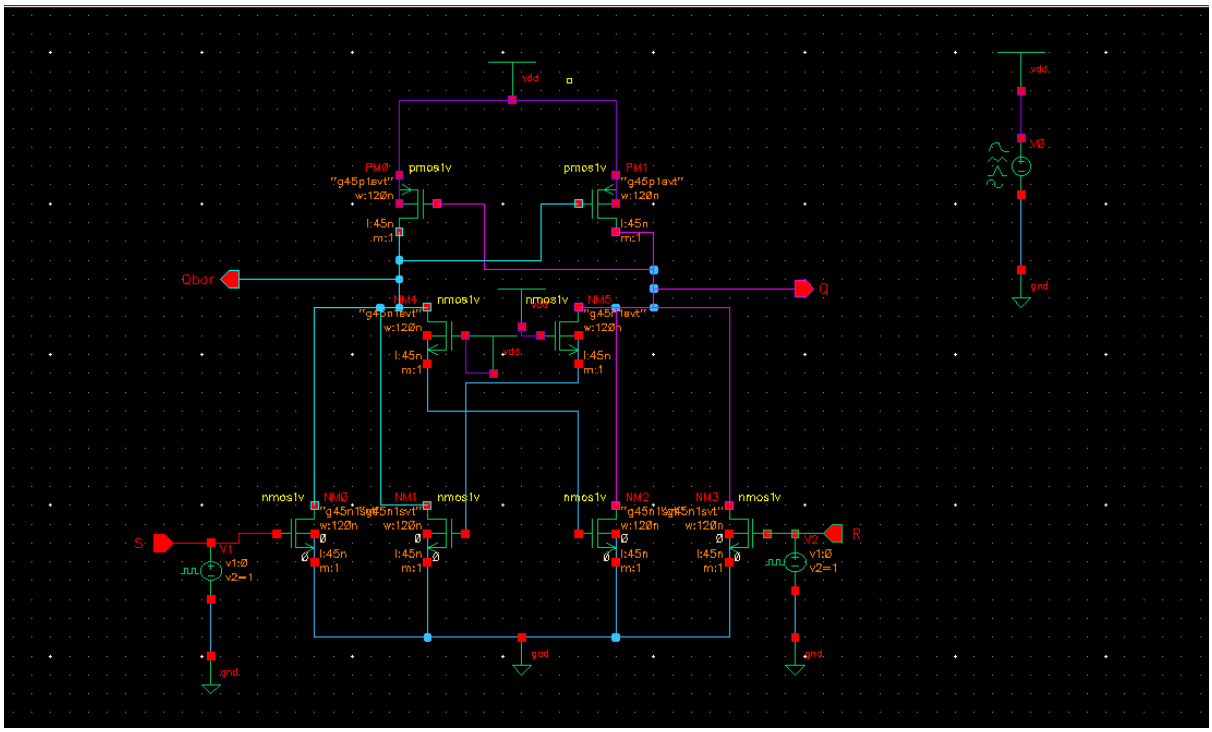


Figure 7. Adabiatic implementation of SR flip-flop

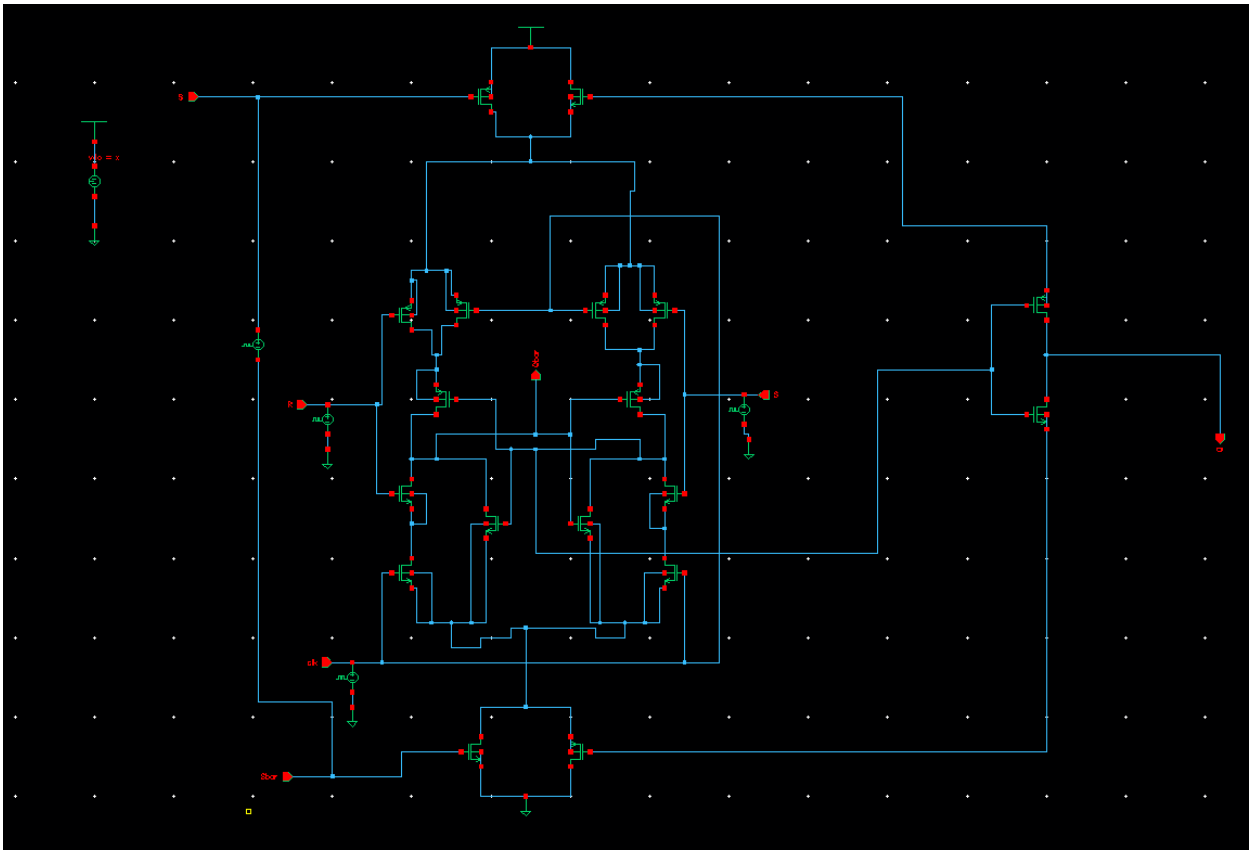


Figure 8. Leaky feedback approach implementation of SR flip-flop

Explanation of the circuit operation

The flip-flop SR is widely used. A set-reset flip-flop is another name for it. When inputs S = "1" and R = "1," Q and Q' can be either logical levels "1" or "0" outputs, depending on the state of the S or R input, given input. As a result, the condition S = R = "1" does not affect the state of output Q and Q'.

However, the input state S = "0" and R = "0" is undesirable or invalid and should be avoided. The condition S = R = "0" causes both output Q and Q' together to be high logic level "1" when reverse is usually Q. Q is losing the result of the check is that flip-flop Q and Q', And where the two inputs are now switched "high" after logical condition "1", the flip-flop becomes unstable and changes in a state of unknown data based on imbalance as shown in the pattern reduction Penalty.

S	R	Q	Q’
0	0	0	1
0	0	1	0
0	1	0	1
1	0	1	0
1	1	0	0

A logic block consisting of one PMOS and one NMOS is put between the pull-up and pull-down networks in the ONOFIC approach architecture. This logic block is an ON/OFF logic block, and we usually utilise PMOS as a pull-up and NMOS as a pull-down since NMOS allows us to go to zero and PMOS allows us to go to VDD most swing available in this circumstance. Specific output parameters must be sacrificed if the position of the pull-up and pull-down is changed.

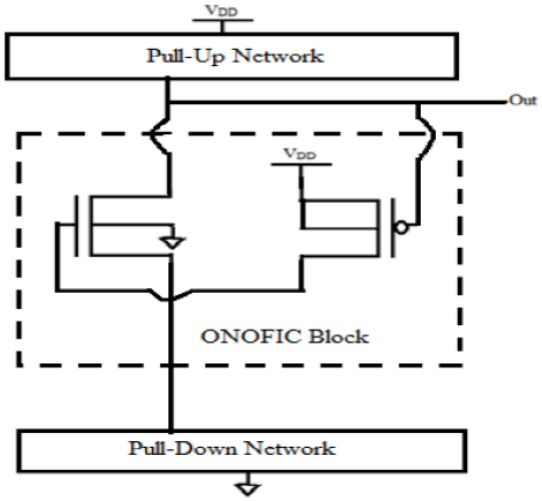


Figure 9. On-off implementation of SR flip-flop

This method is more straightforward since just one logic block is inserted between the pull-up and pull-down networks.

For any logic output, this PMOS and NMOS block should function in ON/OFF mode. This block operates on the force stacking principle, delivering the most significant resistance in the off state and minimal resistance in the on state, hence reducing leakage current. Depending on the output logic, these two transistors should be in a cut-off or linear condition. The ONOFIC methodology is depicted schematically in the figure below. This is how the ONOFIC transistors are linked. The NMOS gate is linked to the PMOS drain, the PMOS source is linked to VDD, and the PMOS gate is linked to the output. The right turning of the ONOFIC transistors helps us in low propagation delay.

Results

The results for 45nm designs are shown below.

Inputs

Parameters	DC voltage	AC Magnitude	Period	Pulse width
R	1	1	25n	12.5n
S	1	1	20n	10n
CLK	1	1	10n	5n

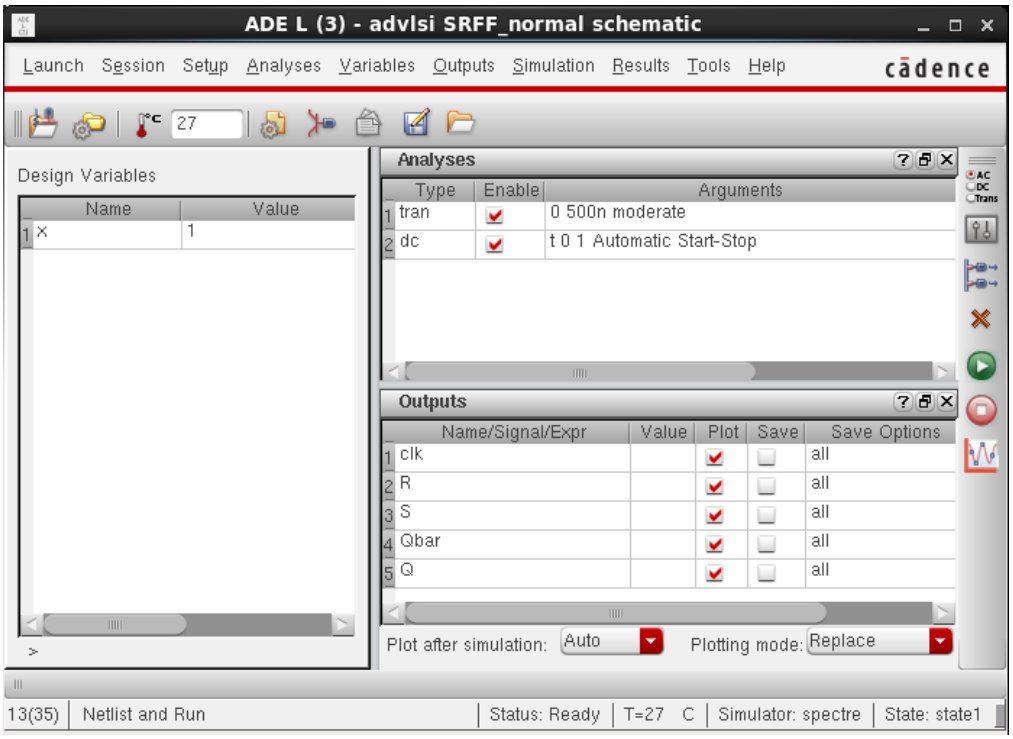


Figure 10. Analysis applied for all circuits.

Output

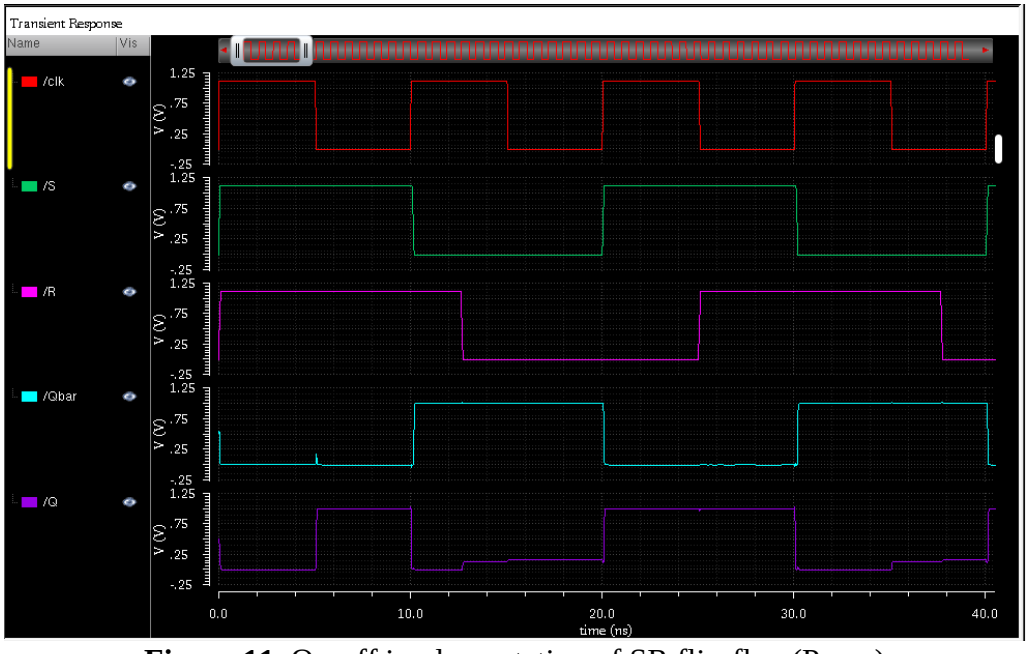


Figure 11. On-off implementation of SR flip-flop (Paper)

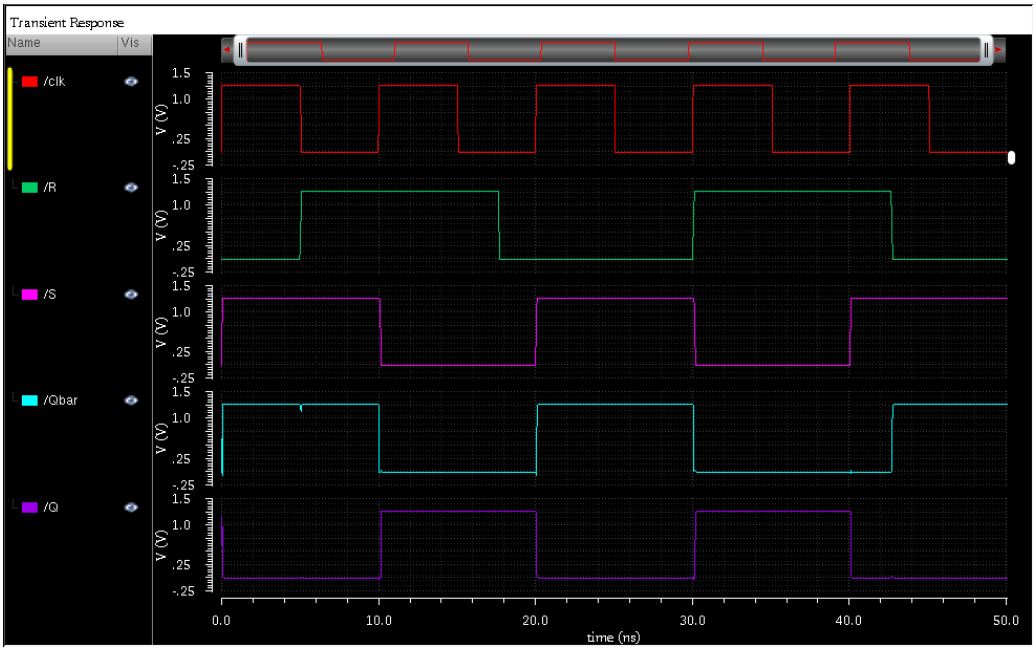


Figure 12. Modified SR flip-flop (proposed)

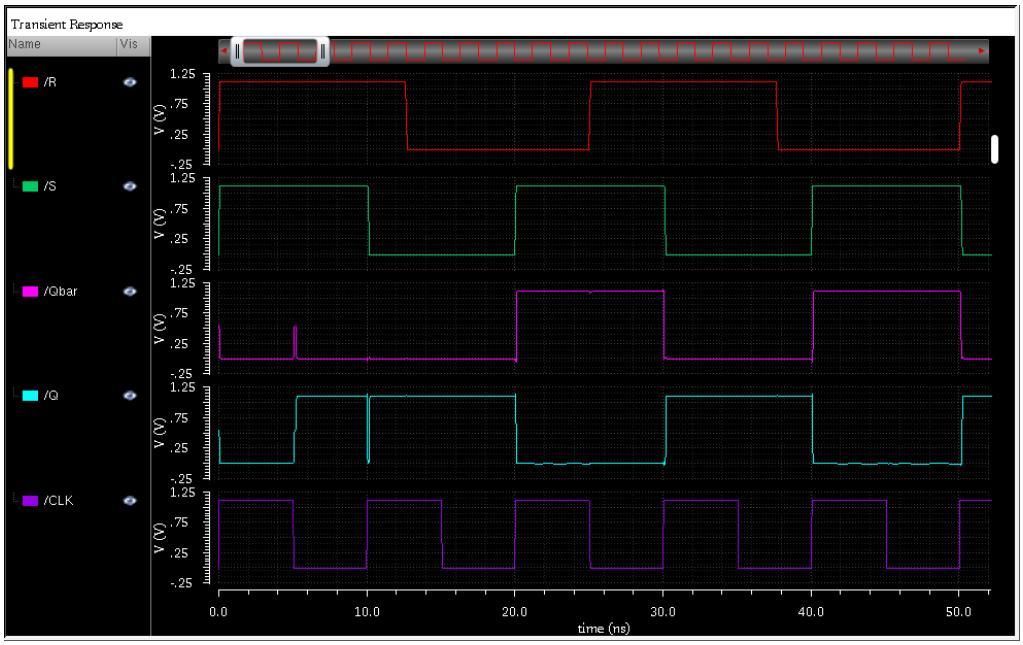


Figure 13. On-off implementation of modified SR flip-flop (proposed)

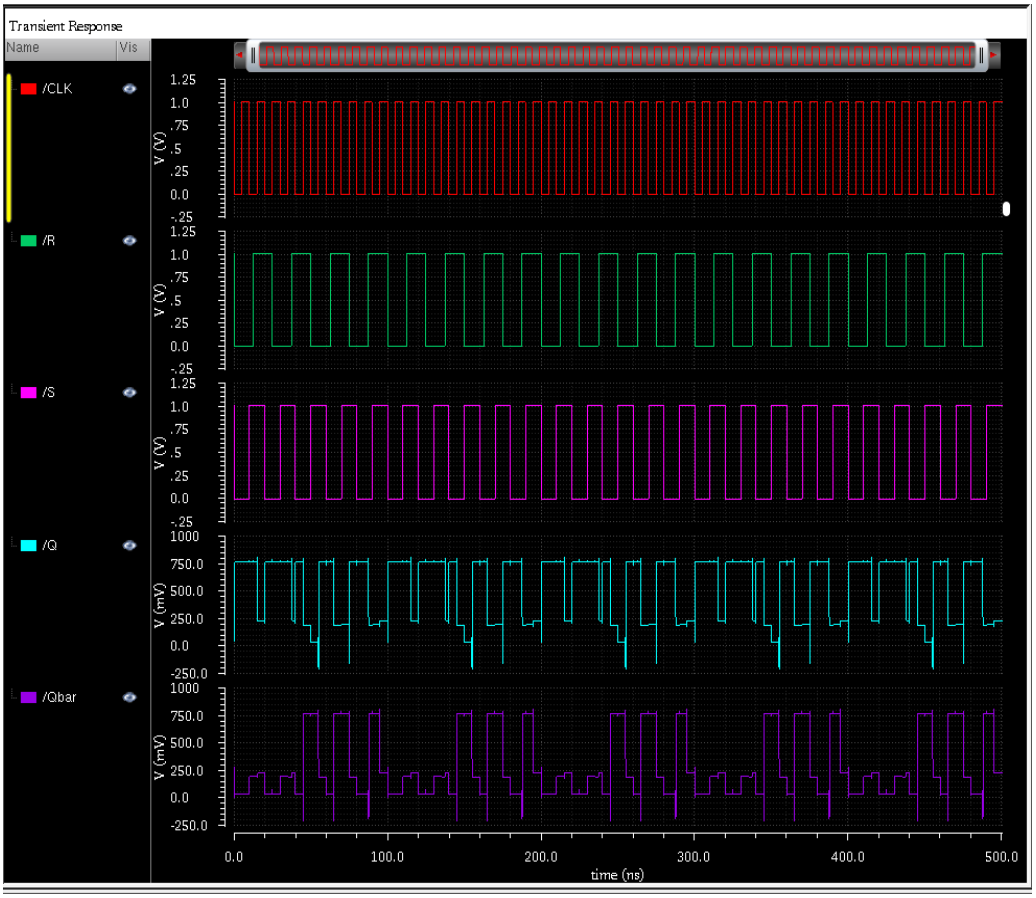


Figure 14. DTMOS SRFF

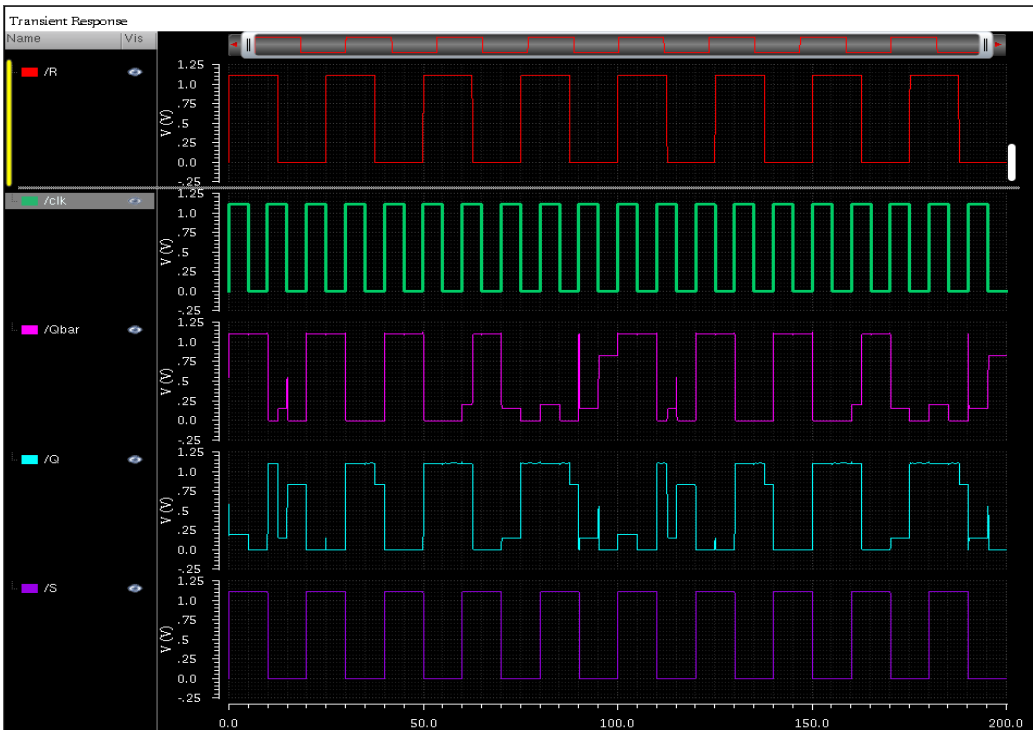


Figure 15. Lector implementation of SR flip flop

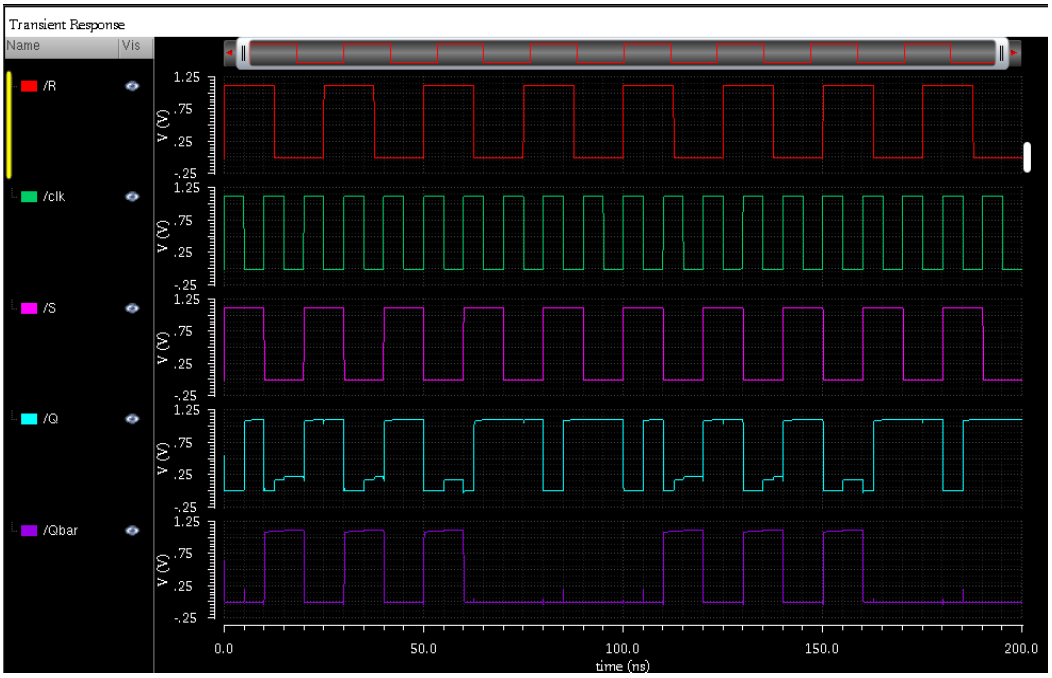


Figure 5. Transmission gate implementation of SR flip flop

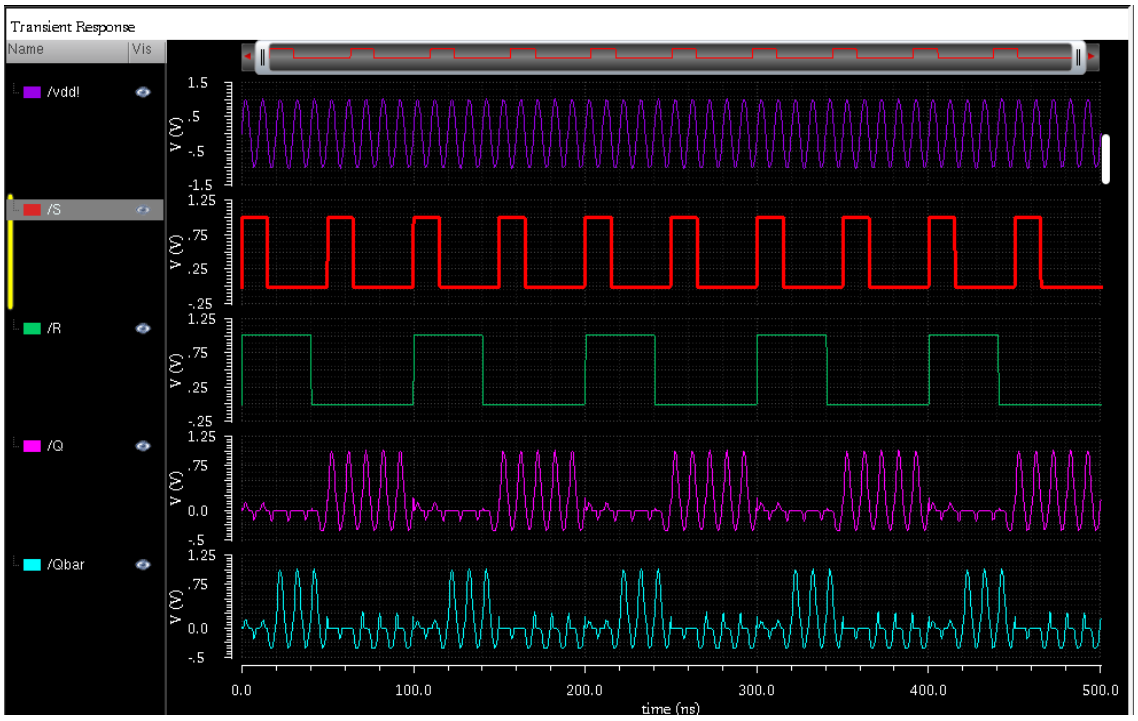


Figure 17. Adiabatic implementation of SR flip flop

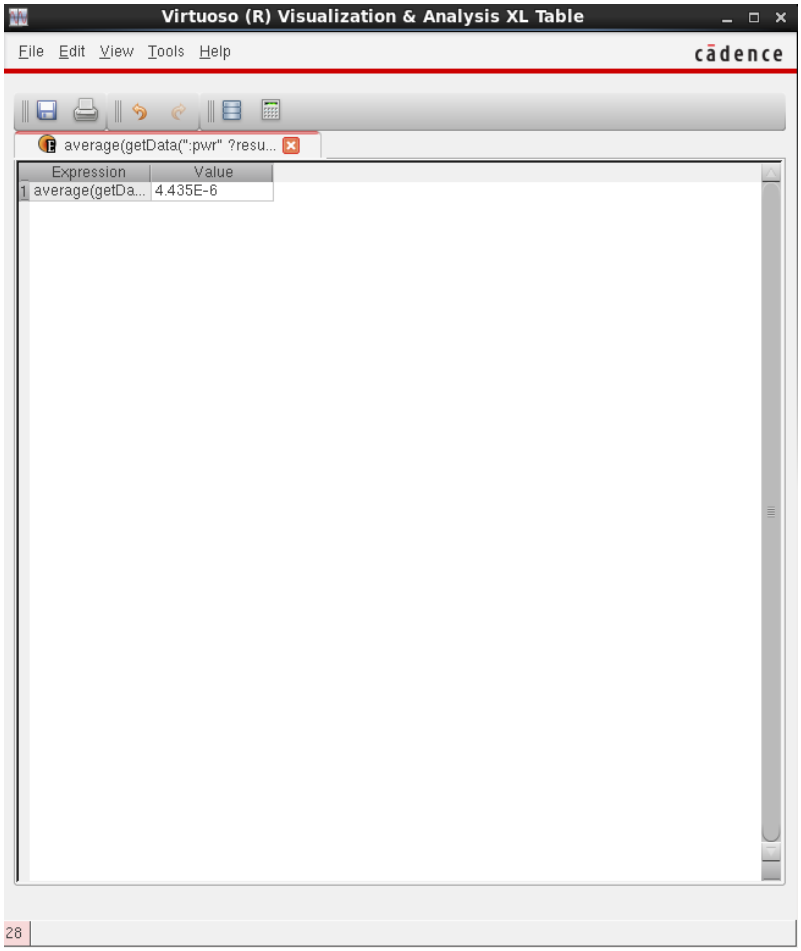


Figure 18. On-Off implementation(Paper) of SR flip flop transient average power

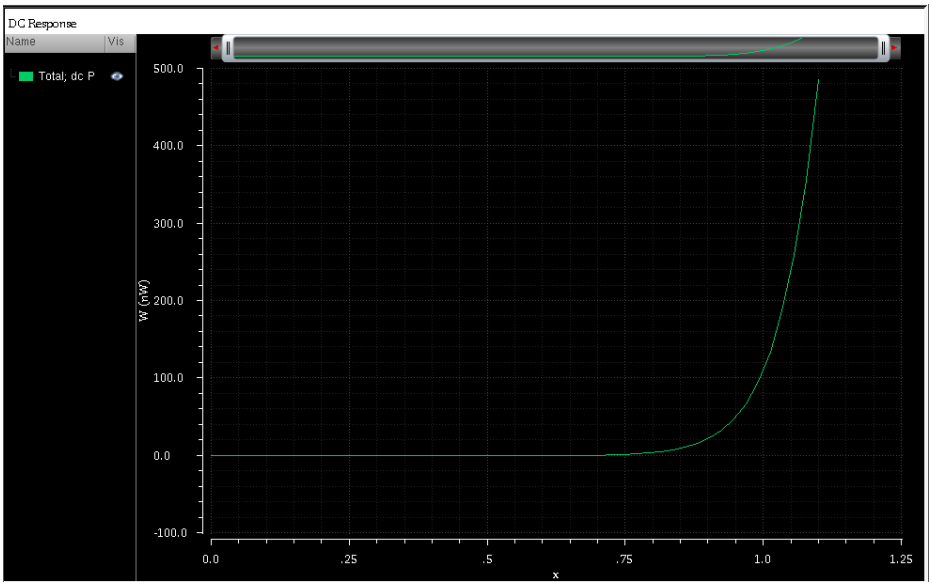


Figure 19. On-Off implementation(Paper) of SR flip flop DC power

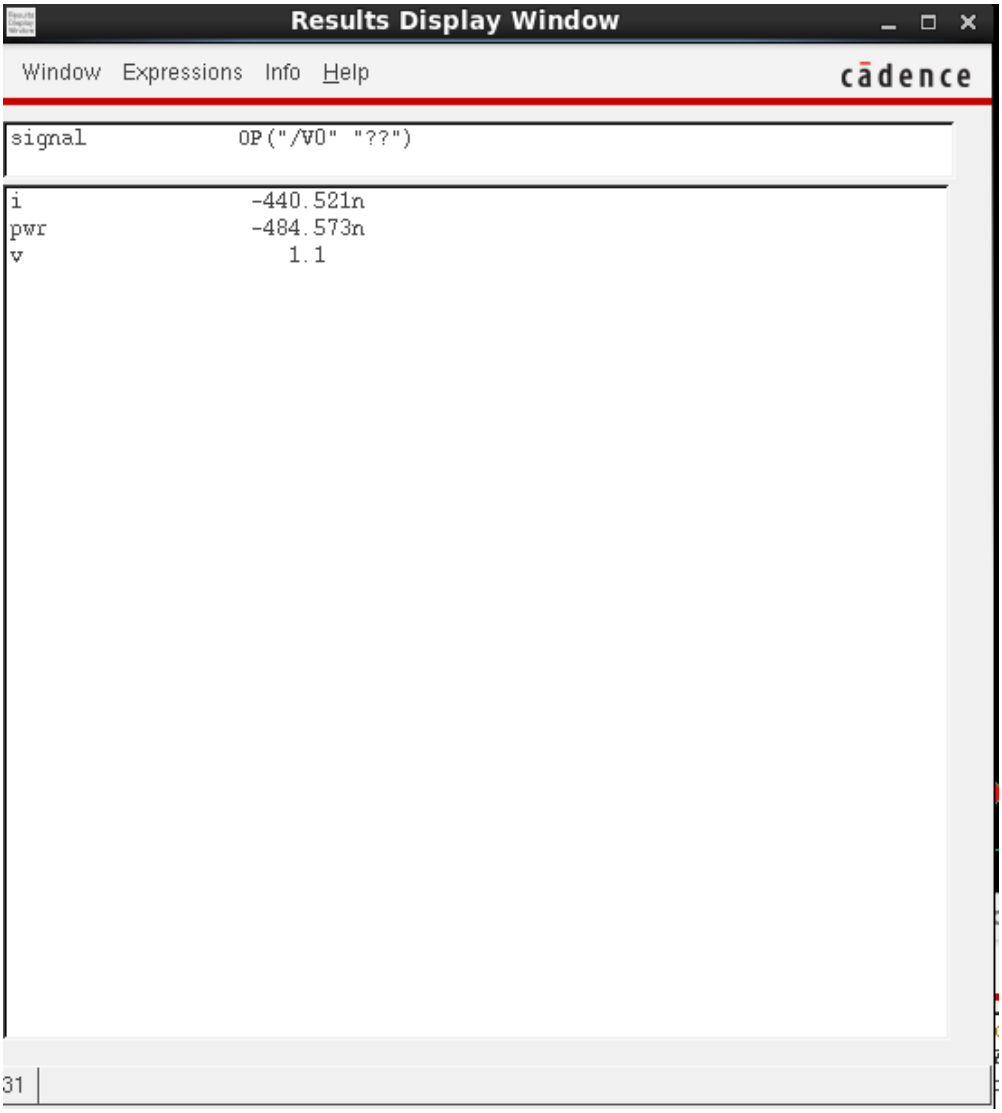


Figure 20. On-Off implementation(Paper) of SR flip flop power consumed in reference to dc source

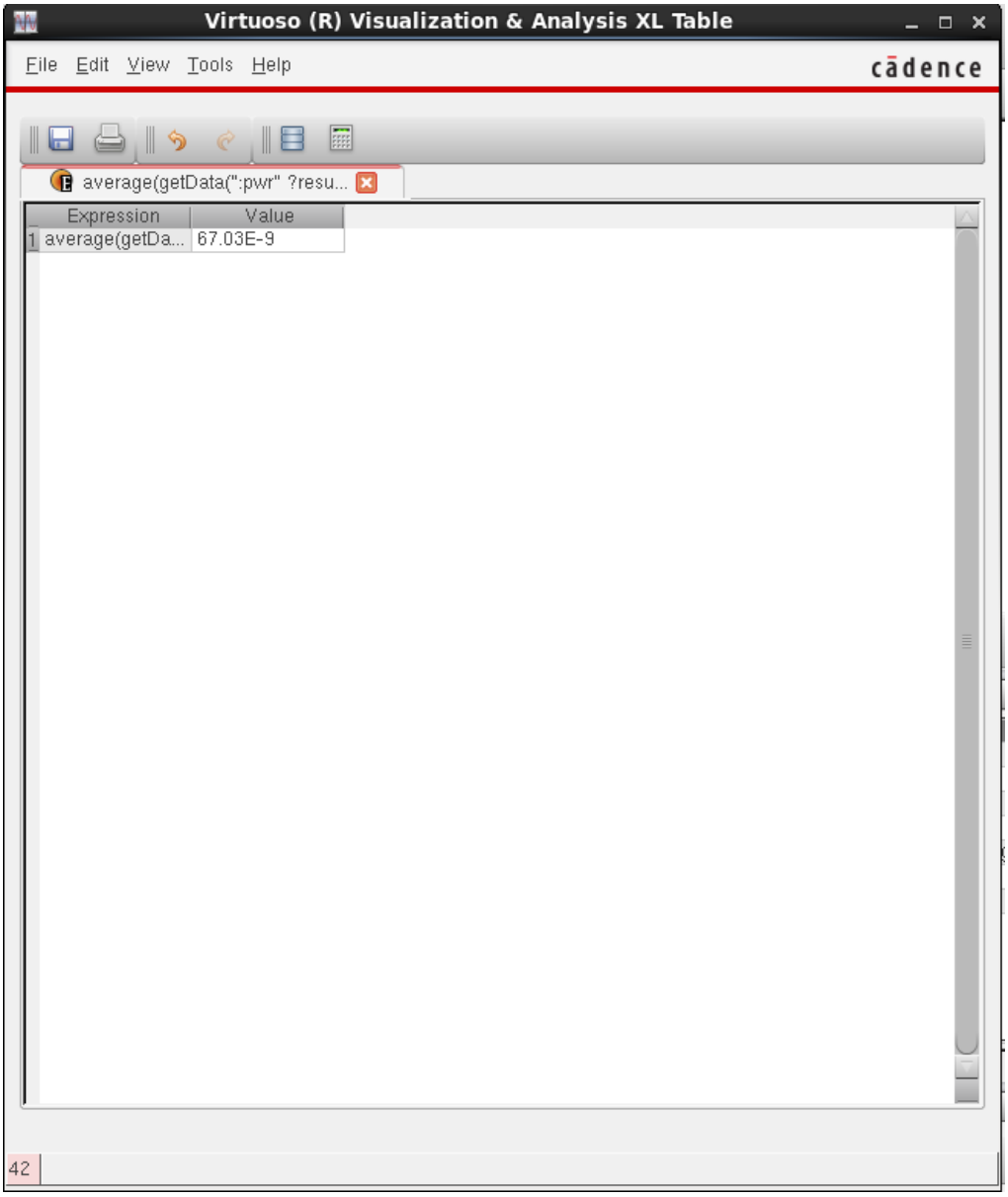


Figure 21. Implementation(proposed) of SR flip flop transient average power

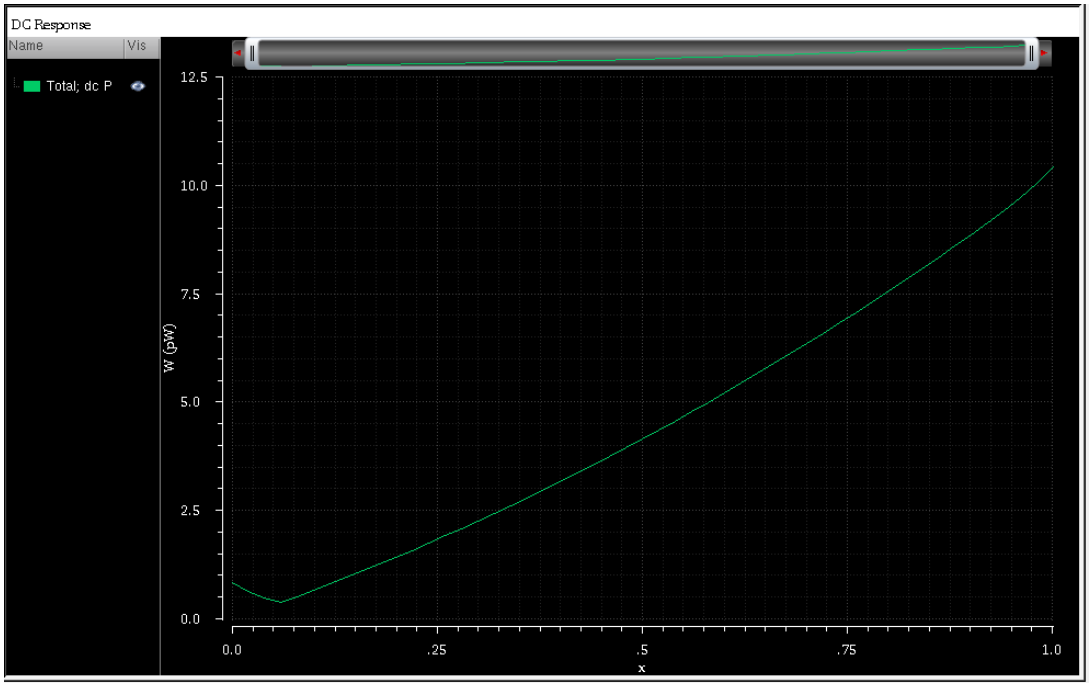


Figure 22. Implementation(proposed) of SR flip flop DC power

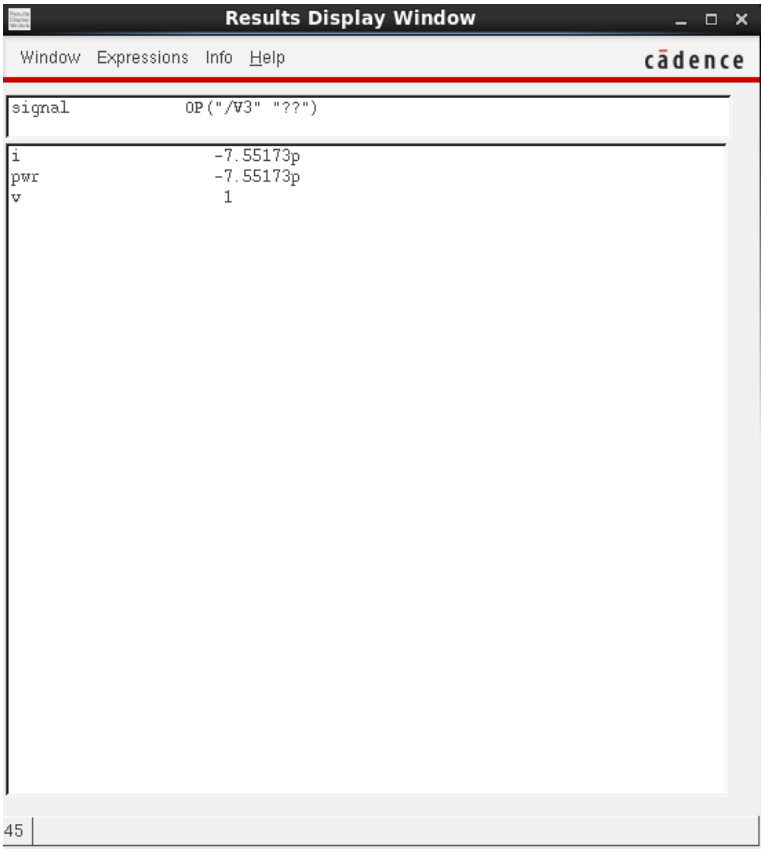


Figure 23. Implementation(proposed) of SR flip flop consumed power

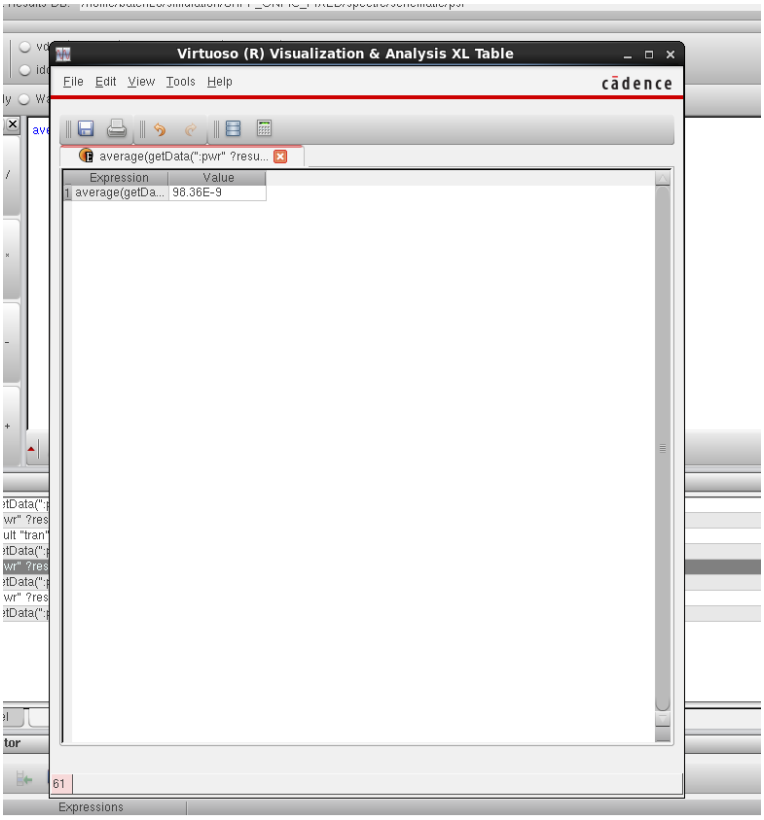


Figure 24. On-off Implementation(proposed) of SR flip flop transient average power

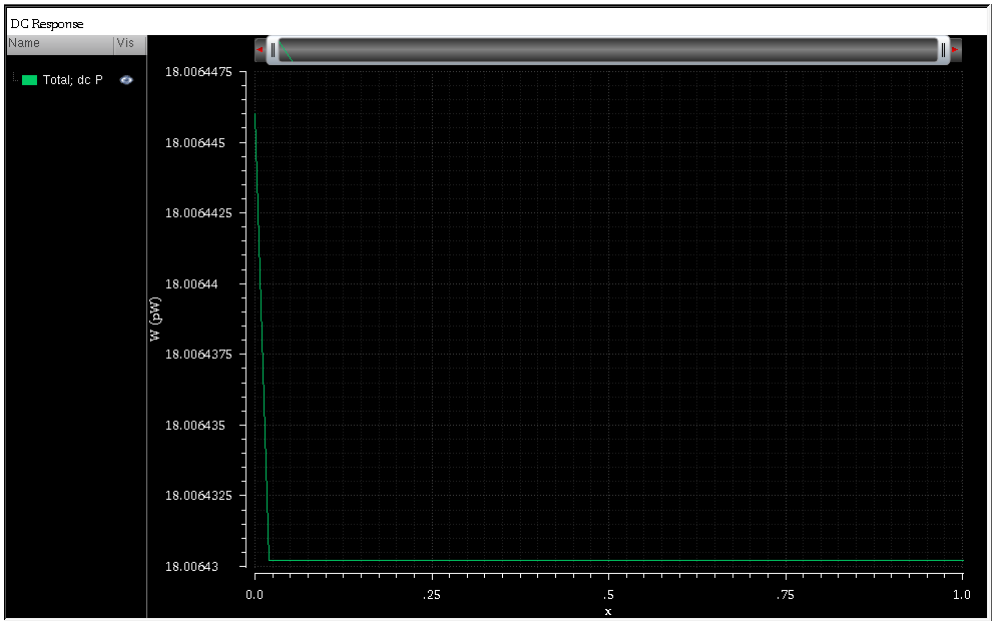


Figure 25. On-Off implementation(proposed) of SR flip flop DC power

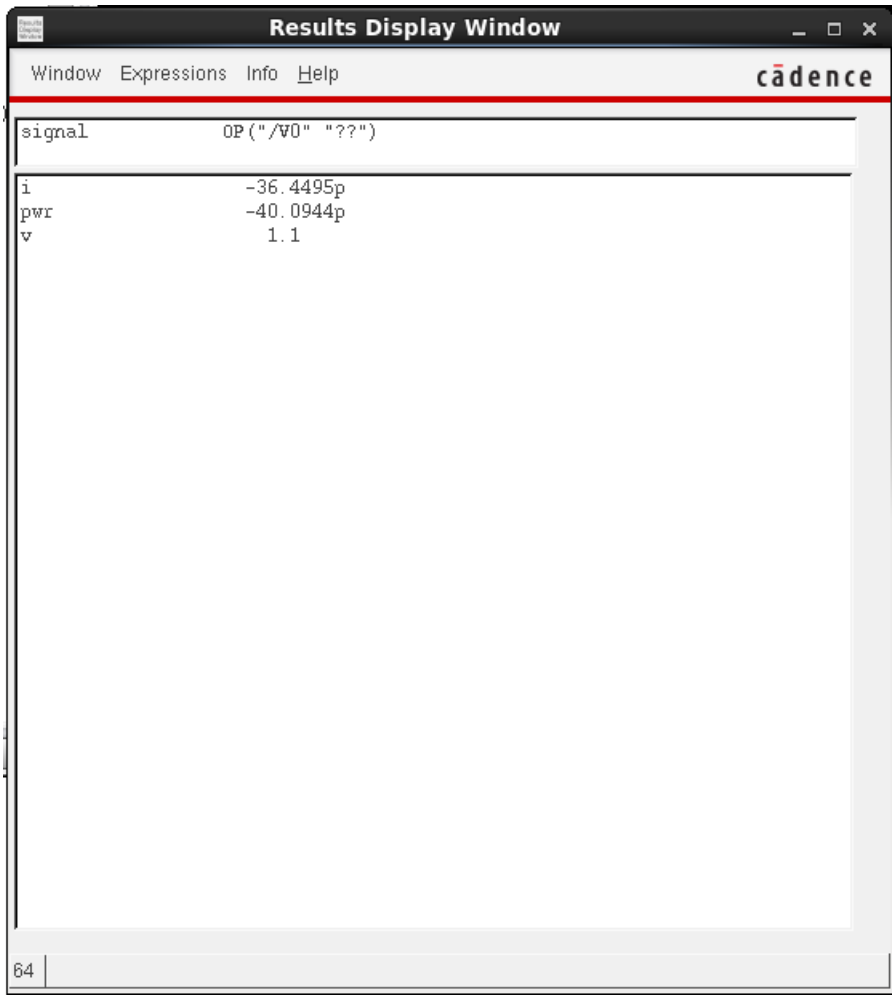
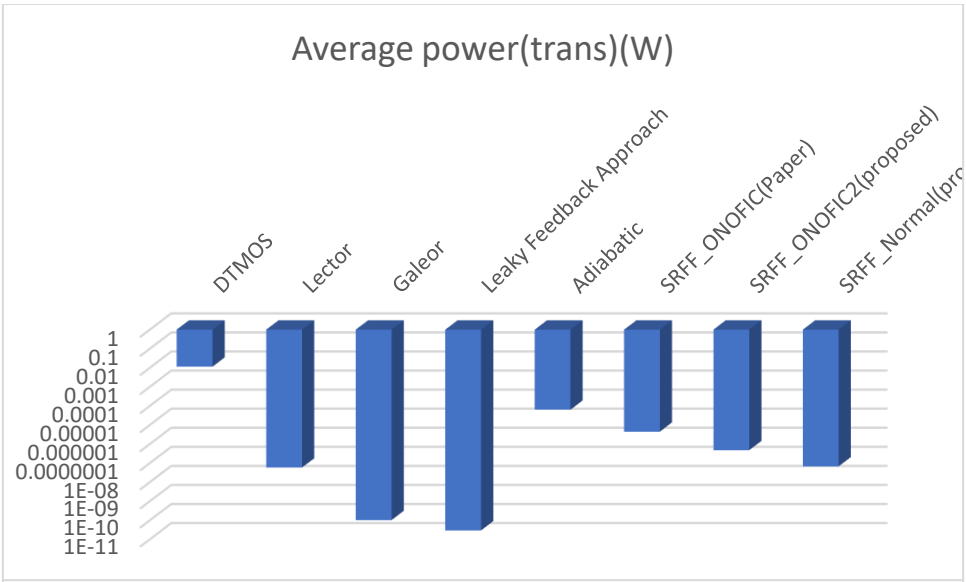
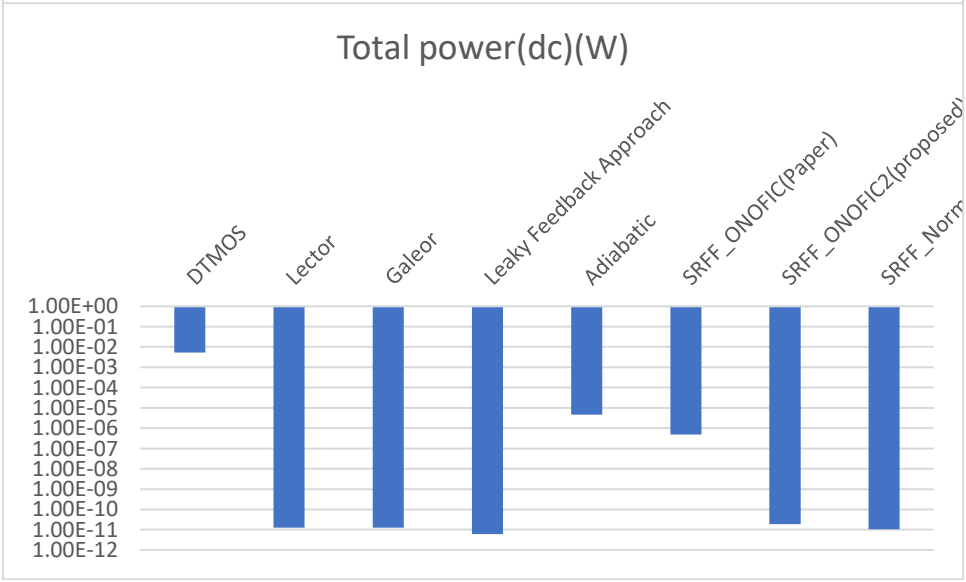


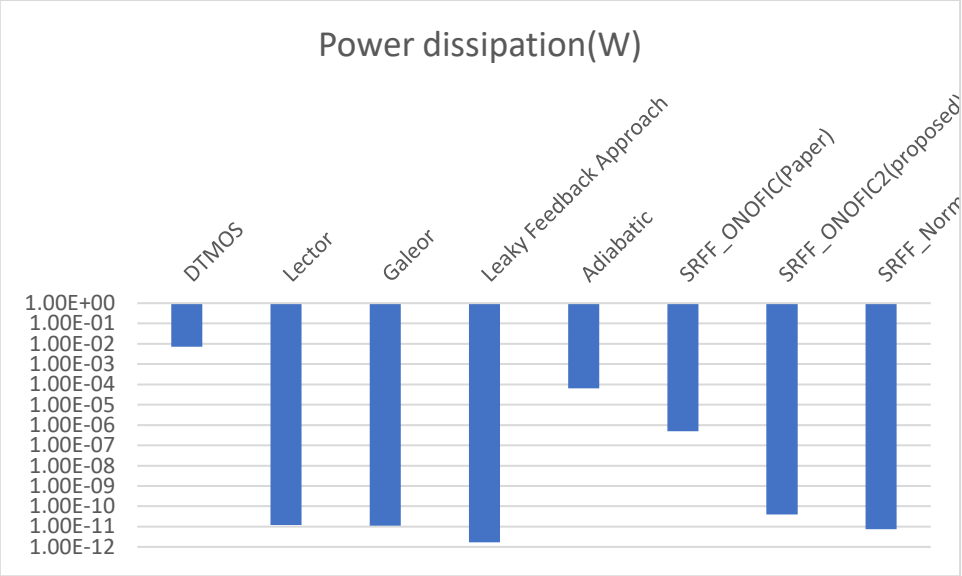
Figure 26. On-Off implementation(proposed) of SR flip flop consumed power with respect to dc source

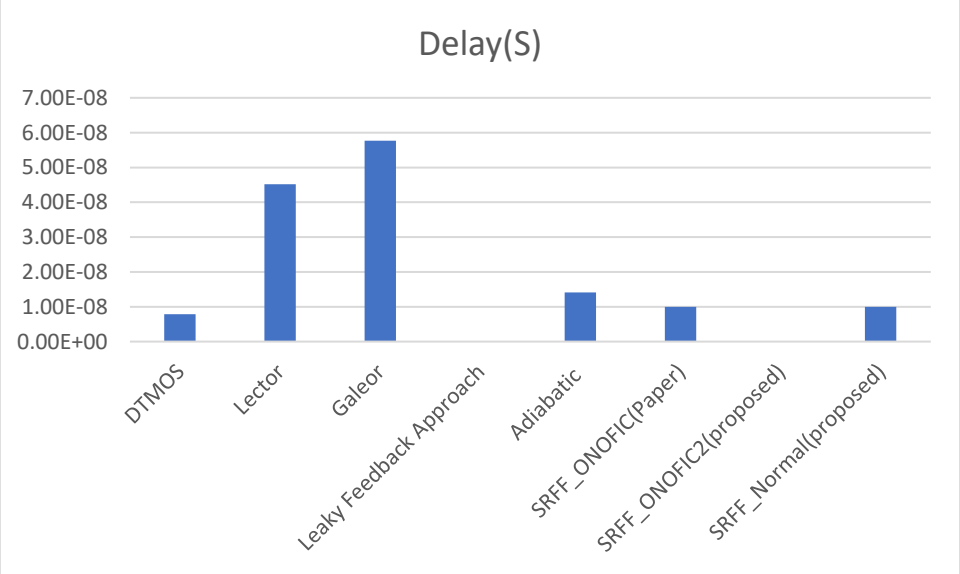
A comprehensive table containing the transient average power, total dc power, power dissipation and delay of various circuits implemented in this report is done.

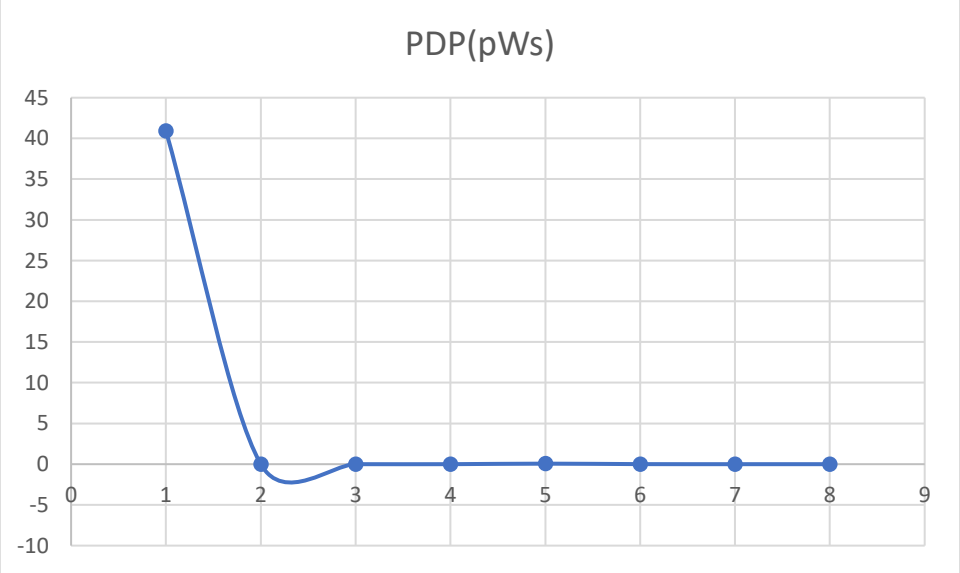
Type of circuit	Average power(trans)(W)	Total power(dc)(W)	Power dissipation(W)	Delay(S)	PDP(x10^-12)(Ws)
DTMOS	11.37m	5.23m	7.23m	7.823n	40.914
Lector	58.46n	12.86p	12.05p	45.22n	581.52n
Galeor	102.23p	12.8p	11.29p	57.73n	738.94n
Leaky Feedback Approach	29.33p	6.18p	1.66p	24.71p	152.70p
Adiabatic	63.192u	4.623u	63.303u	14.12n	65.27m
SRFF_ONOFIC(Paper)	4.436u	0.484u	0.494u	9.985n	4.832m
SRFF_ONOFIC2(proposed)	**98.36n**	**18.57p**	**40.094p**	**41.37p**	**768.24p**
SRFF_Normal(proposed)	**67.03n**	**10.38p**	**7.55p**	**9.97n**	**103.48n**

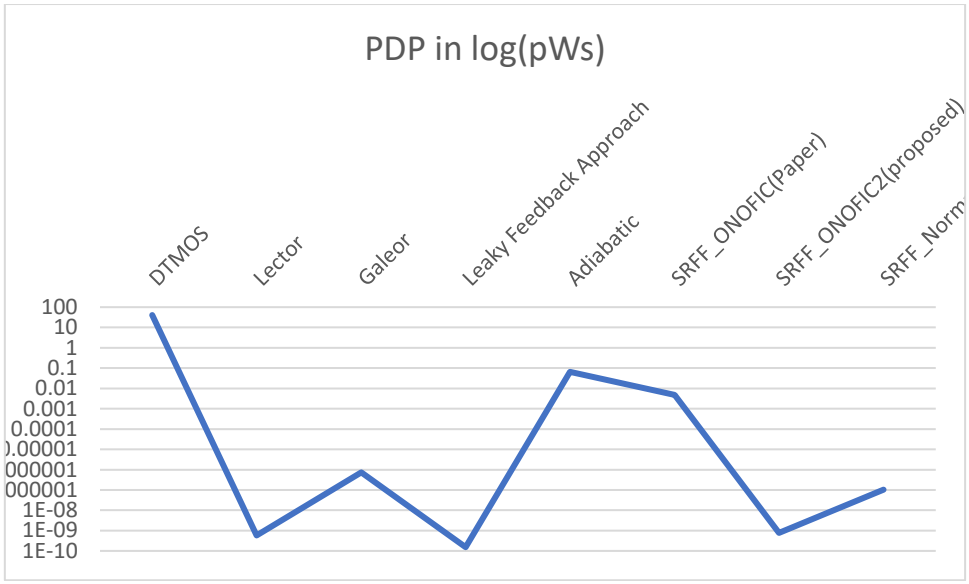





Power dissipation(W)
DTMOS
Lector
Galeor
Leaky Feedback Approach
Adiabatic
SRFF_ONOFIC(Paper)
SRFF_ONOFIC2(proposed)
1.00E+00
1.00E-01
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
1.00E-12


Delay(S)
7.00E-08
6.00E-08
5.00E-08
4.00E-08
3.00E-08
2.00E-08
1.00E-08
0.00E+00
DTMOS
Lector
Galeor
Leaky Feedback Approach
Adiabatic
SRFF_ONOFIC(Paper)
SRFF_ONOFIC2(proposed)
SRFF_Normal(proposed)


PDP(pWs)
45
40
35
30
25
20
15
10
5
0
-5
-10
0
1
2
3
4
5
6
7
8
9


PDP in log(pWs)
DTMOS
Lector
Galeor
Leaky Feedback Approach
Adiabatic
SRFF_ONOFIC(Paper)
SRFF_ONOFIC2(proposed)
SRFF_Norm
100
10
1
0.1
0.01
0.001
0.0001
.00001
000001
000001
1E-08
1E-09
1E-10

Results at the other technology nodes

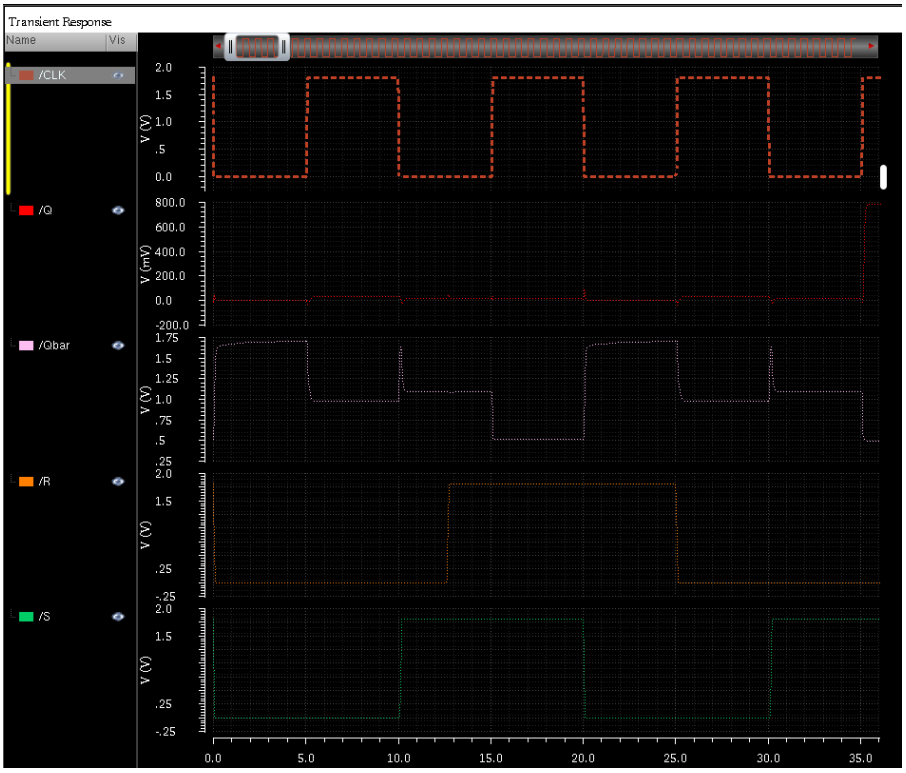


Figure 27. On-off implementation of SR flip flop(180nm)

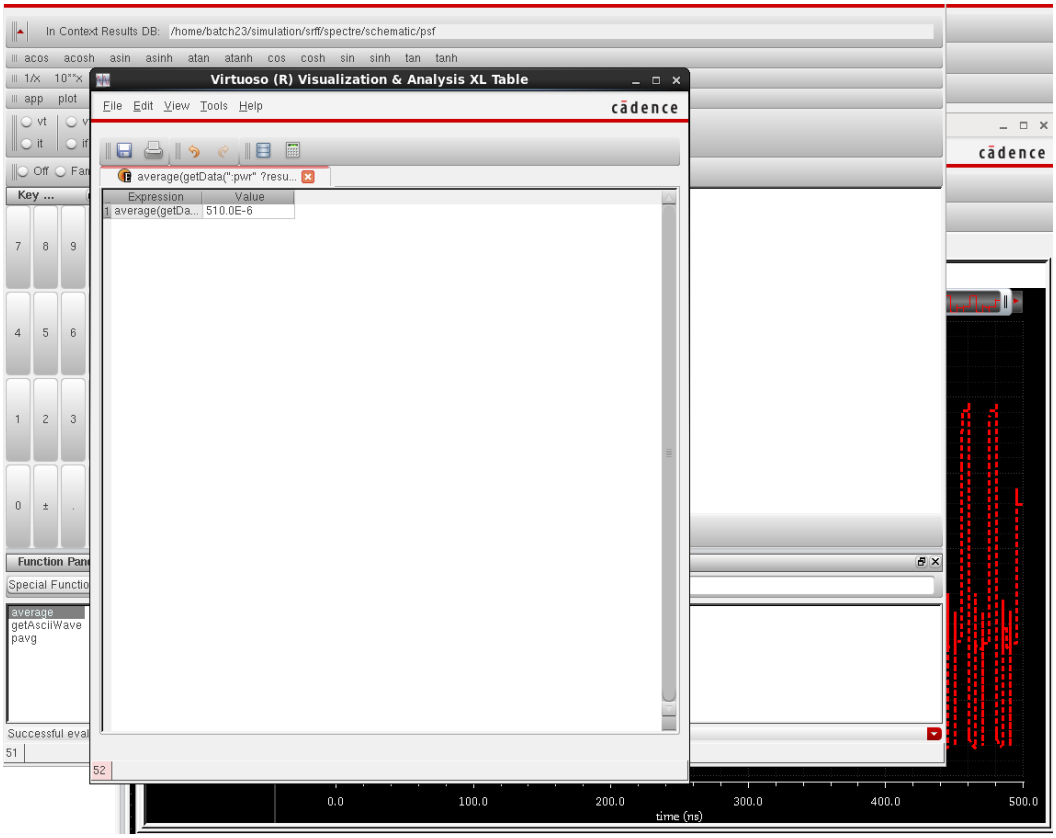


Figure 28. Transient power average of On-off implementation of SR flip flop(180nm)

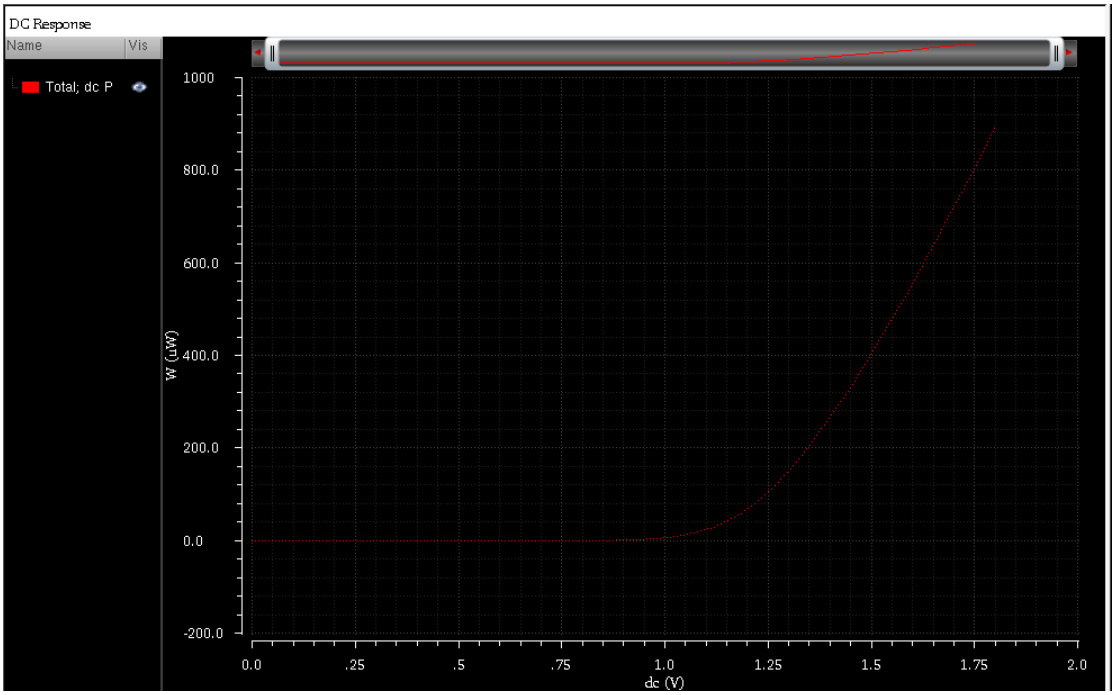


Figure 29. Total Dc power of On-off implementation of SR flip flop(180nm)

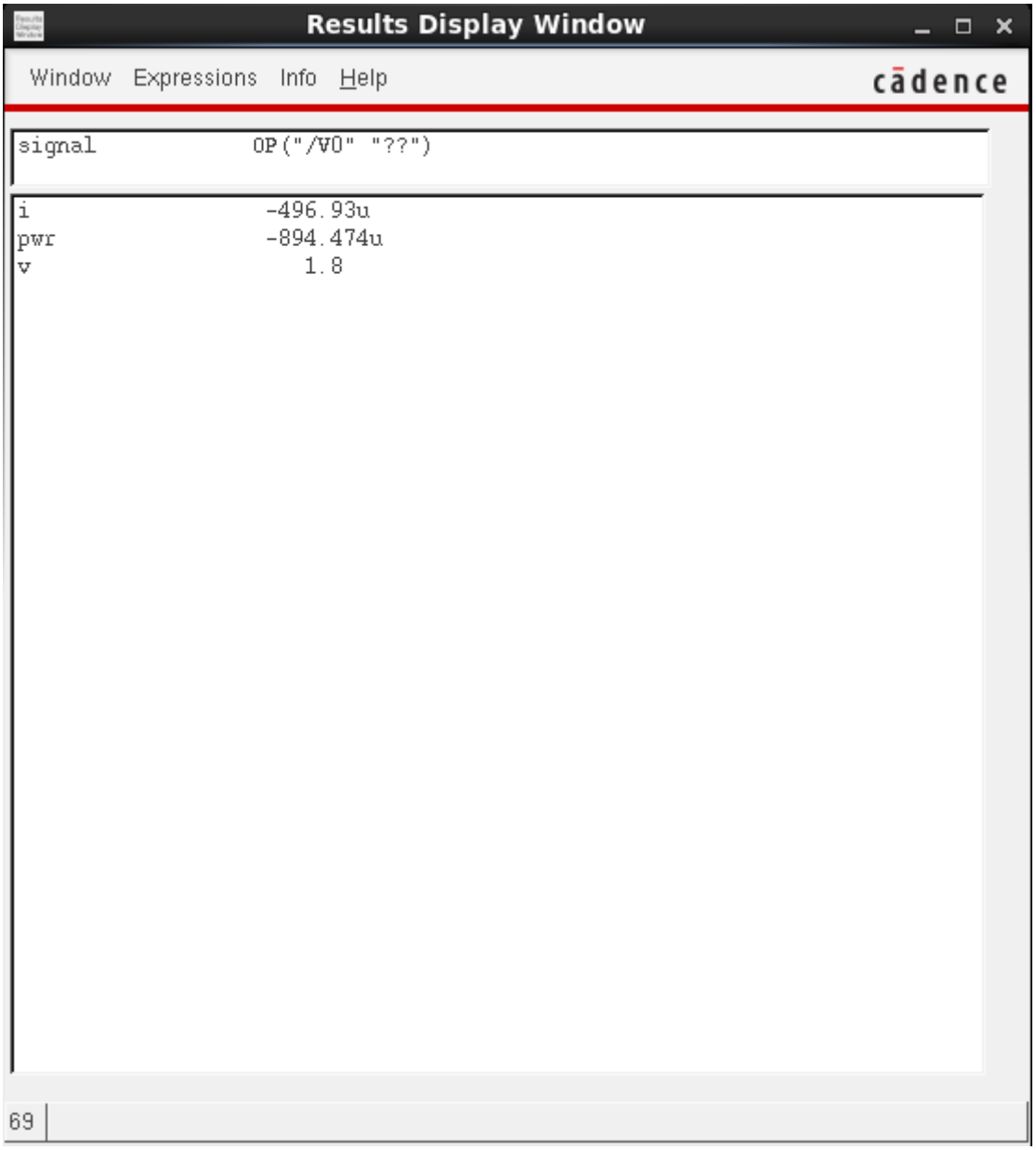


Figure 31. Power consumed of On-off implementation of SR flip flop(180nm)

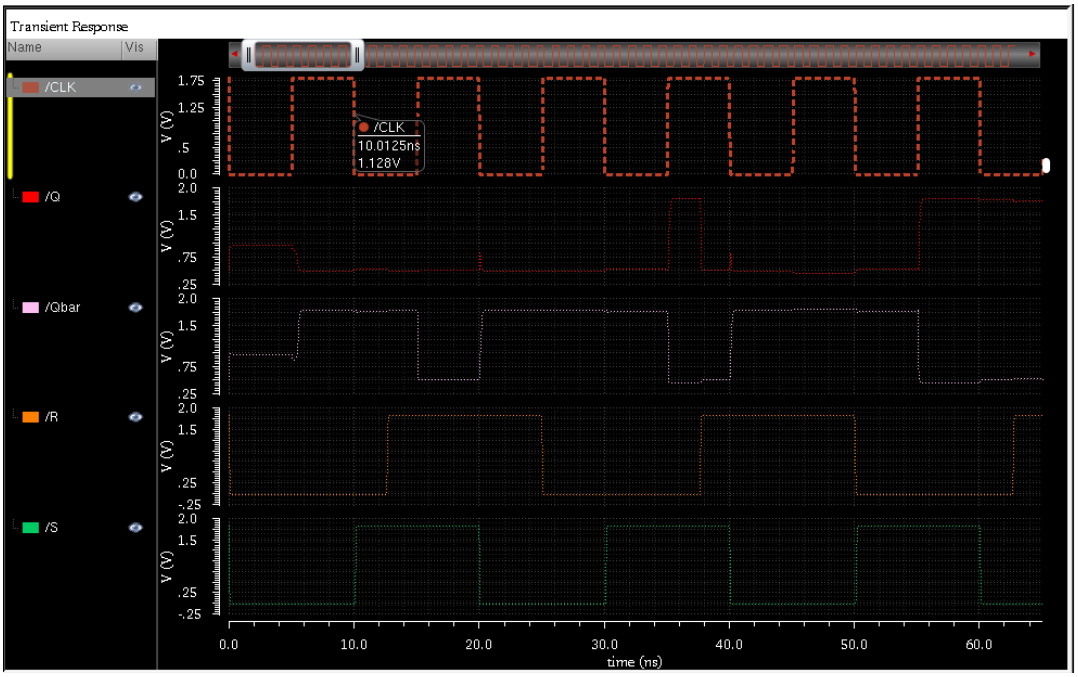


Figure 32. Implementation of proposed SR flip flop(180nm)

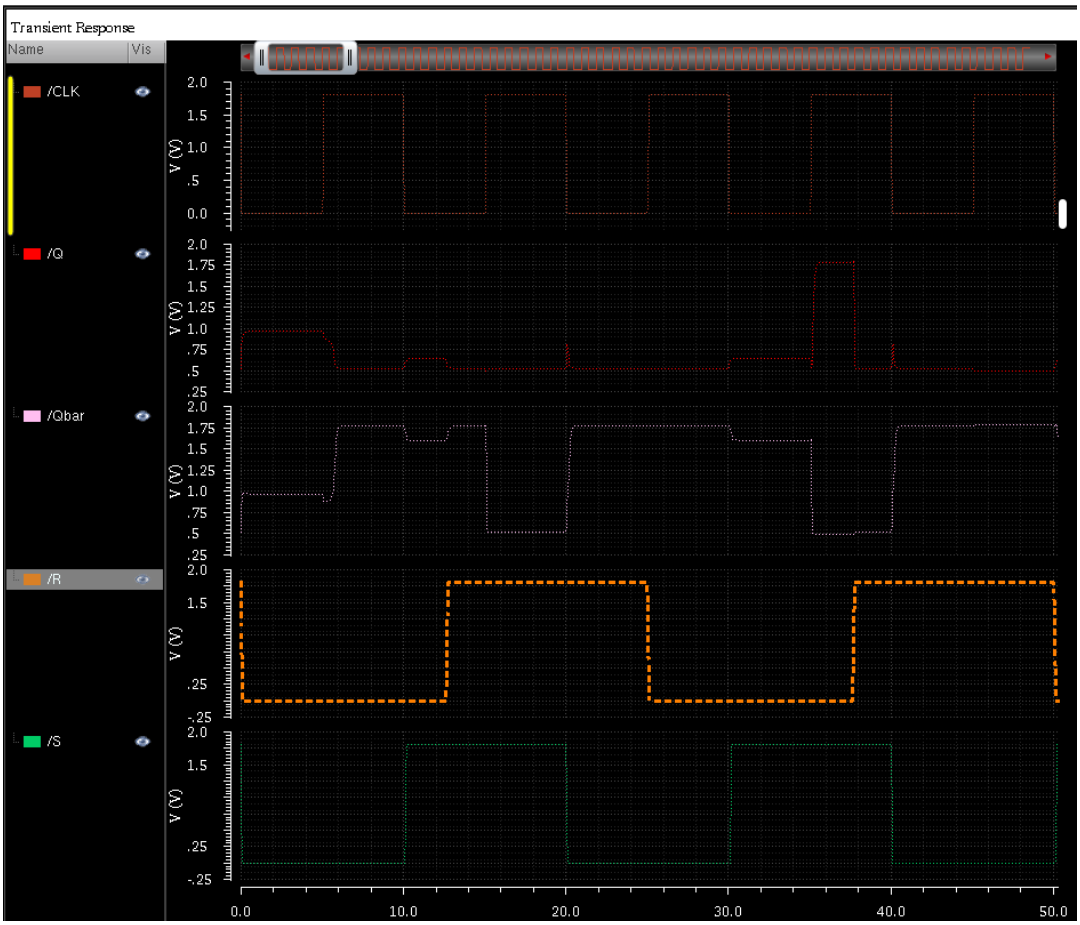
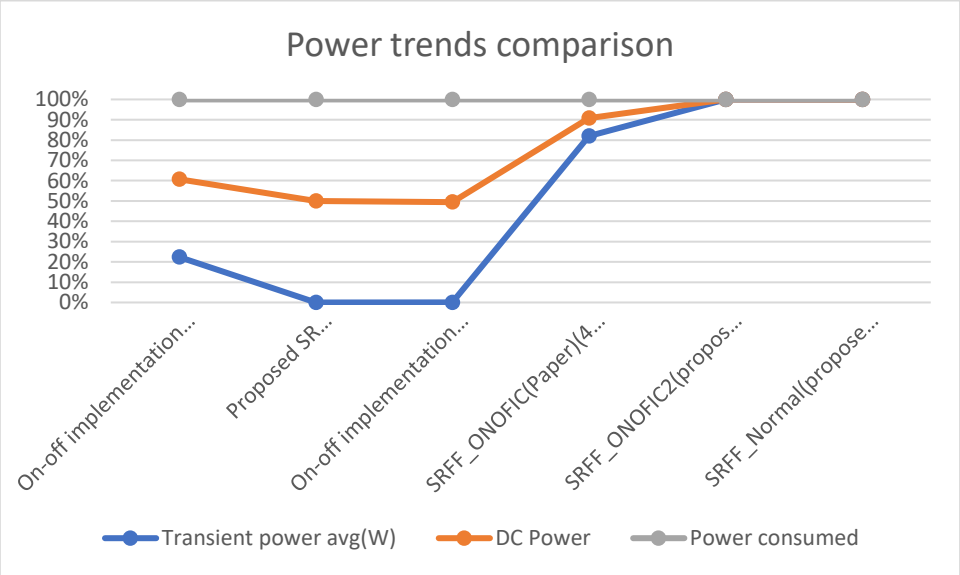
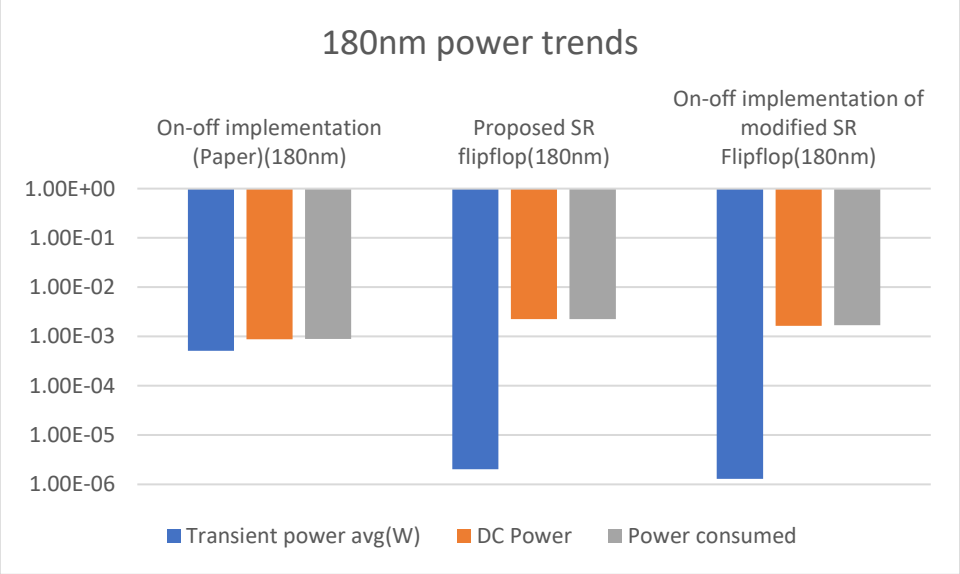
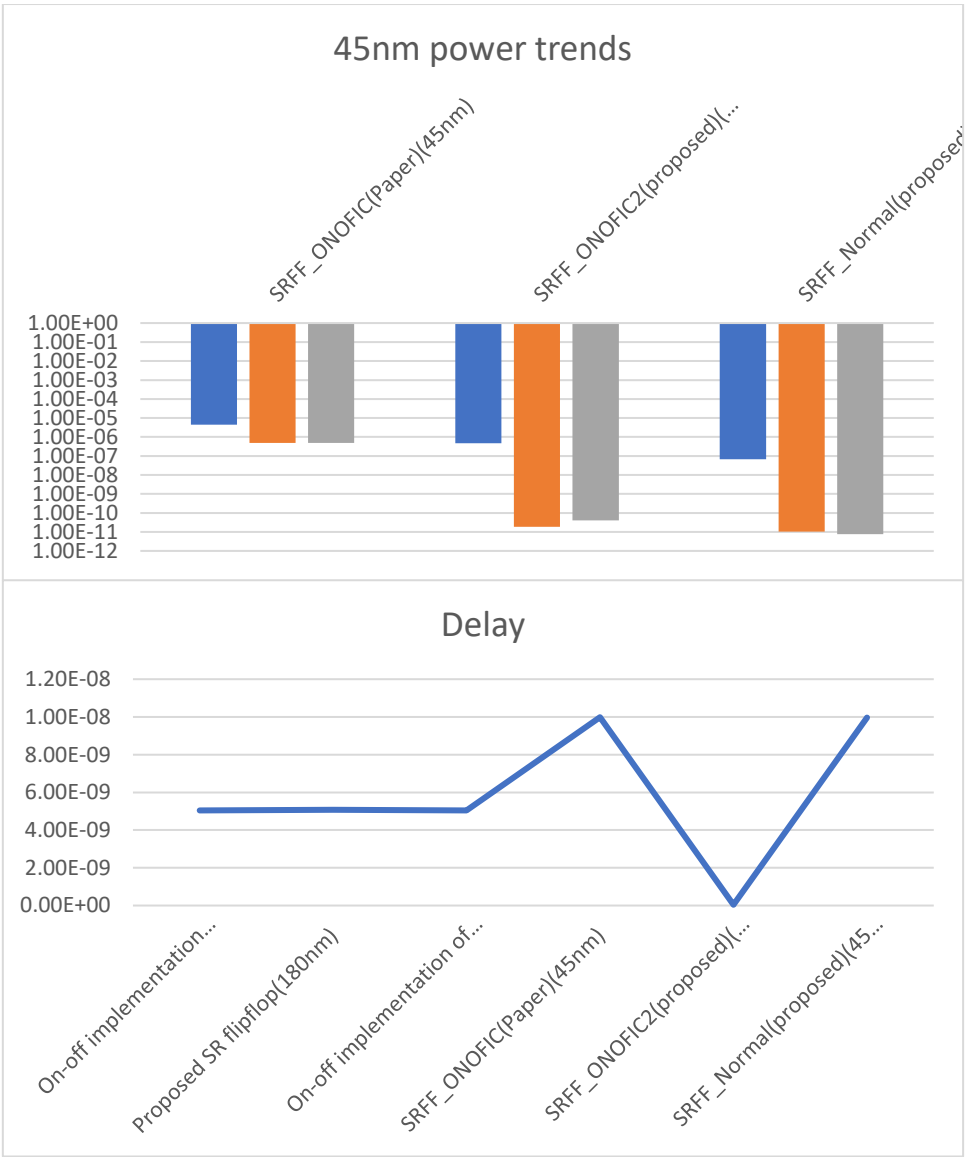


Figure 33. On-Off implementation of proposed SR flip flop(180nm)

Parameter	On-off implementation (Paper)	Proposed SR flip-flop	On-off implementation of modified SR Flipflop
Transient power avg(W)	510u	2.023u	1.29u
DC Power	0.874m	2.27m	1.65m
Power consumed	0.894m	2.27m	1.69m
Delay	5.04n	5.08n	5.046n
Product of power and delay(pWs)	4.404	11.53	8.32



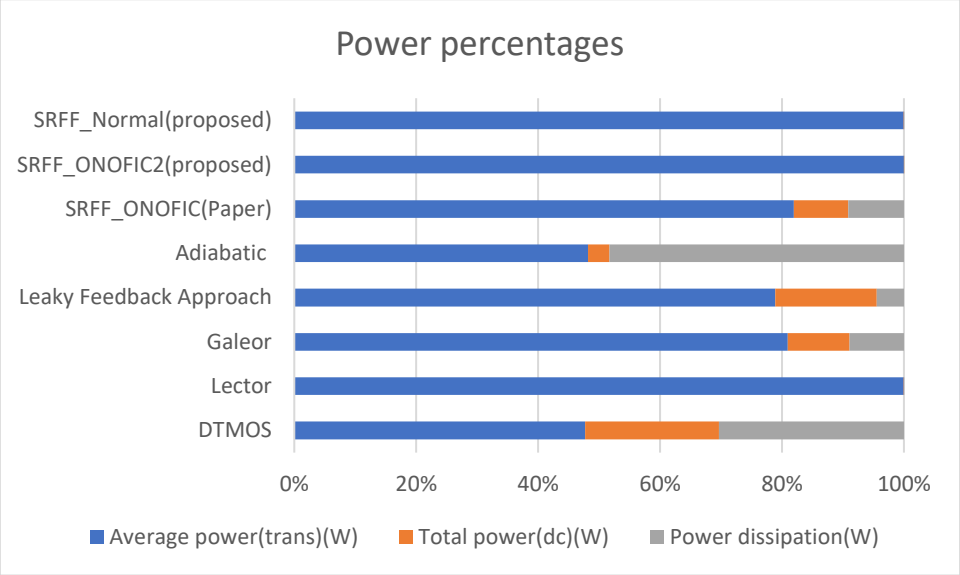


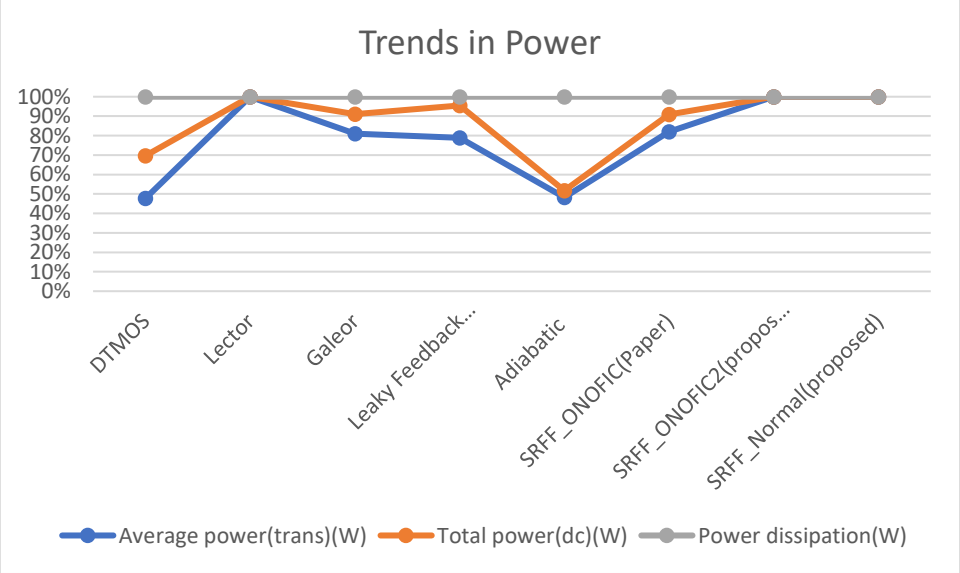

45nm power trends
SRFF_ONOFIC(Paper)(45nm)
SRFF_ONOFIC2(proposed)(...
SRFF_Normal(proposed
1.00E+00
1.00E-01
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
1.00E-12
Delay
1.20E-08
1.00E-08
8.00E-09
6.00E-09
4.00E-09
2.00E-09
0.00E+00
On-off implementation...
Proposed SR flipflop(180nm)
On-off implementation of...
SRFF_ONOFIC(Paper)(45nm)
SRFF_ONOFIC2(proposed)(...
SRFF_Normal(proposed)(45...

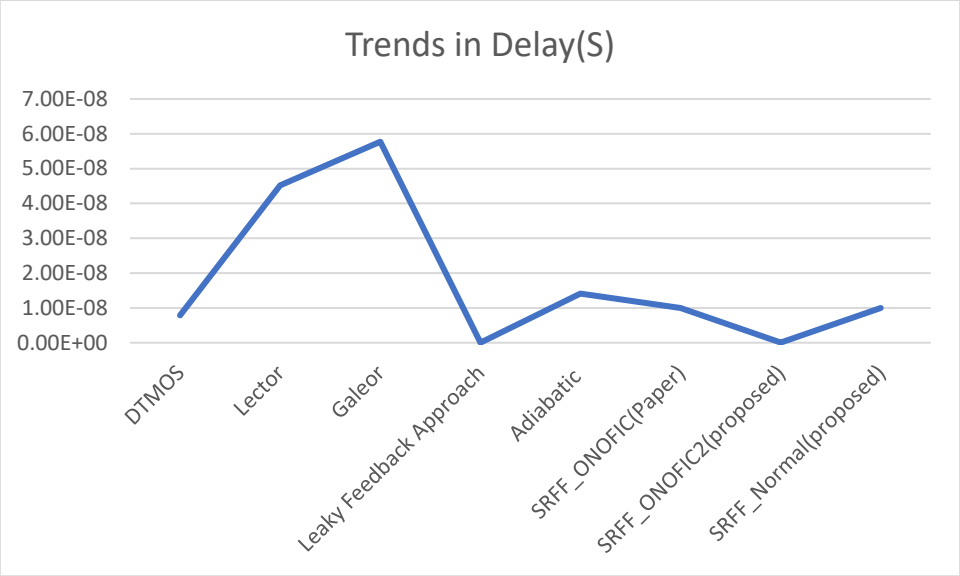
Conclusion

In this work, we looked at a variety of leakage currents and their impact on low-power devices. In VLSI technology, IC designers are primarily concerned with low power consumption. Therefore, the previously described ON/OFF (ONOFIC) method was used to create an SR flip-flop. The ONOFIC technique is straightforward, relying on only one threshold voltage to decrease leakage current. The main advantage of this technique is that it provides better ON/OFF functionality.

The proposed implementation of the sr flip-flop using On-off implementation maintains a lower power rating while keeping a delay identical to the sr flip-flop described in the paper, as evidenced by the data. Furthermore, compared to the circuit proposed in the flip flop, the power delay product is lower. Below are graphs depicting power percentages. ONOFIC reduces leakage power and increases digital circuit performance, both of which are important at this time. In addition, this technique uses very little energy. The future potential of this technique is that it will assist in lowering the propagation latency of logic circuits if this logic block is turned on and off in a more efficient manner.






Trends in Delay(S)
7.00E-08
6.00E-08
5.00E-08
4.00E-08
3.00E-08
2.00E-08
1.00E-08
0.00E+00
DTMOS
Lector
Galeor
Leaky Feedback Approach
Adiabatic
SRFF_ONOFIC(Paper)
SRFF_ONOFIC2(proposed)
SRFF_Normal(proposed)