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**B.Sc. (Engineering) in Computer Science and Engineering**
**Semester Final Examination (Online) 2019 (July-December)**
**Level: 2 Semester: II, Credit: 3.0**
**Course Code: CSE 259, Course Title: Computer Architecture and Organization (Theoretical)**

**Time: 1 hour and 30 minutes**                                             **Full Marks: 90**

*[**N.B.** The figure in the right margin indicates the marks for respective question, answer any **3 (Three)** questions from each section, and split answer to any question is unacceptable.]*

## Section-A

1.  a)  Explain the basic performance equation of a processor with proper example.                                          6

    b)  The sharing of a processor by a user program and OS routines – illustrates it. An output device and disk storage must be included in the discussion.          9

2.  a)  An $n$-bit integer needs to store in $m$-bit location (here $m > n$). Using the twos complement representation, mathematically validate its range extension procedure.          6

    b)  Explain the multiplication procedure of $7 \times (-3)$ by using the Booth's algorithm.          9

3.  a)  Data hazard can be handled by the software – justify your answer.                                          6

    b)  Define structural hazard and explain it with proper example.                                          9

4.  a)  Apply all 6 kinds of shift and rotate operations (3-bits) on the input stream `10100010`.          6

    b)  Compare between one address and three address instructions that could be used to compute the equation: $Y = (P + Q/R)/(S - T)$.          9

## Section-B

5.  a)  Point out the difference between the CISC and RISC architecture.                                          6

    b)  Explain indirect addressing mode and displacement addressing mode.                                          9

6.  a)  Mention the control sequence for the instruction **Add R1,R2,R3** for the three-bus organization.          6

    b)  Explain the *register transfer* operation with the aid of suitable example and appropriate figure (here, the processor's datapath has the facility of single-bus organization).          9

7.  a)  Design a static RAM cell by using the inverter circuits and introduce its basic operation.          6

    b)  Explain the internal organization of a $1K \times 1$ semiconductor RAM memory chip and calculate number of external connections also.          9

8.  a)  If a system enters in infinite loop during the execution of multiple interrupts, then what are the techniques to overcome from such situation?          6

    b)  Design a multiple-priority scheme for interrupts, where each device has a separate interrupt-request and interrupt-acknowledge line. Briefly explain it also.          9