Bi-Directional Amplifier Architecture for Sub-6 GHz 5G

PICO Design Contest Submission

Abstract

This document summarizes the bi-directional amplifier design submission in PICO 21 SSCS design contest

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Table of Contents

Bi-Directional Amplifier Architecture for Sub-6 GHz 5G

PICO Design Contest Submission

1 Introduction

- TDD (Time division duplexing) RF front ends operate in such a manner that
  - During Transmission, Receiver side is isolated using and switch and power amplifier is driving the transmission antenna, as shown in Figure 1
  - During Reception, transmitter chain is isolated and the received signal from the antenna is fed to a low noise amplifier, as shown in Figure2

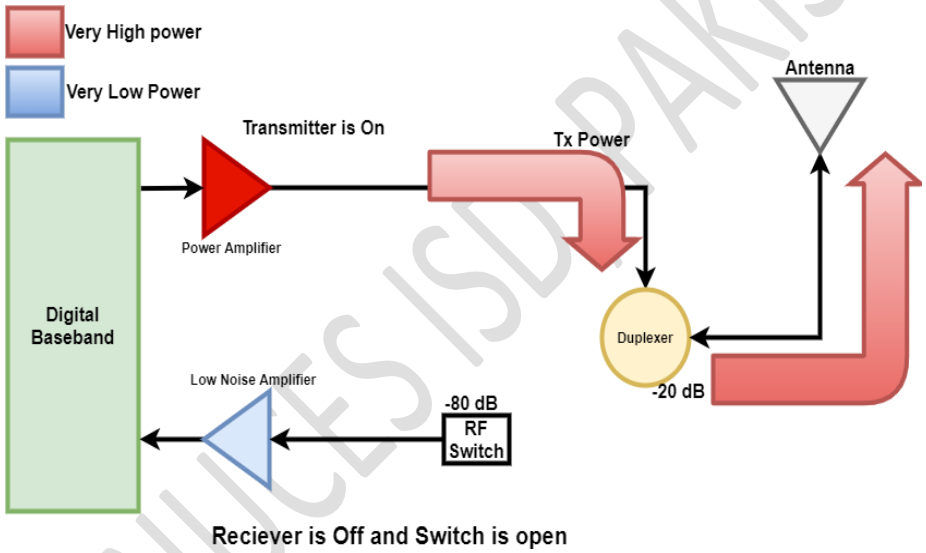


Figure 1 Transmitter on

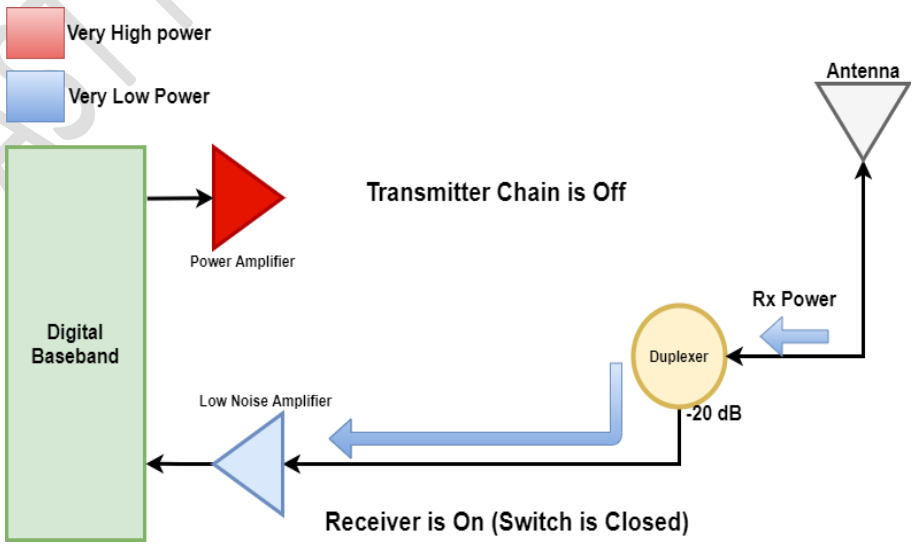


Figure 2 Receiver on

2 Bi-Directional Amplification Architecture

- The Bi-Directional Amplifier architecture aims to exploit the inherent TDD nature of the classical architecture.
- At a given time, either the power amplifier (Transmission) or the low noise amplifier (LNA) is working.
- Both LNA and PA occupy silicon space and have power consumption.
- Bi-Directional architecture makes use of a single circuit that acts as both the power amplifier (during transmission) and the low noise amplifier (during reception).
- This way we can conserve area and power, thereby, reduce cost.

Figure 3 shows the proposed architecture of bi-directional amplification using same amplifier and a set of switches.

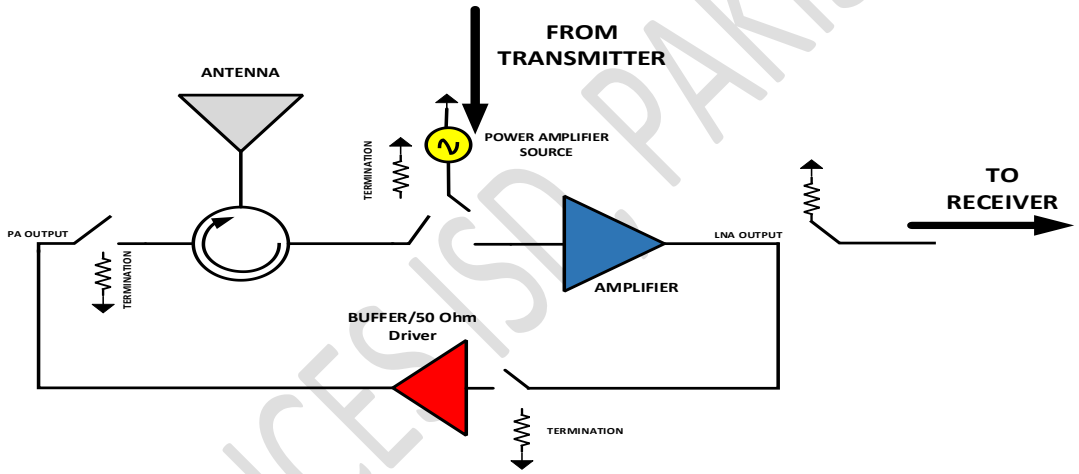


Figure 3 Bi-Directional Amplifier Architecture using Switches

2.1 State of Switches During Reception

Figure 4 shows the state of switches during the reception mode. In this mode the amplifier acts as a low noise amplifier. The power received from antenna is fed to the amplifier and the amplified signal is then sent to receiver path.

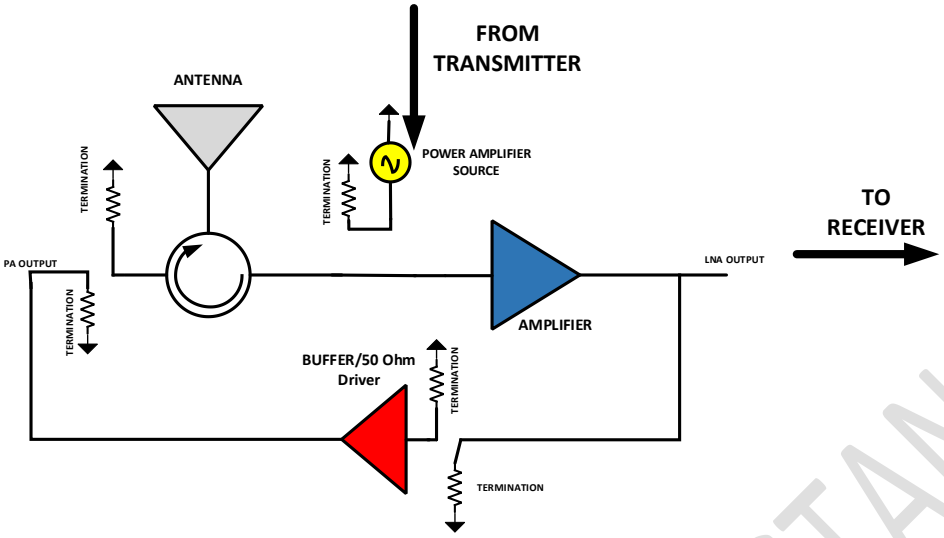


Figure 4 Amplification During Reception

2.2 State of Switches During Transmission

Figure 5 shows the state of switches during transmission. In this case the signal from transmitter is power amplified and fed to a 50Ω antenna.

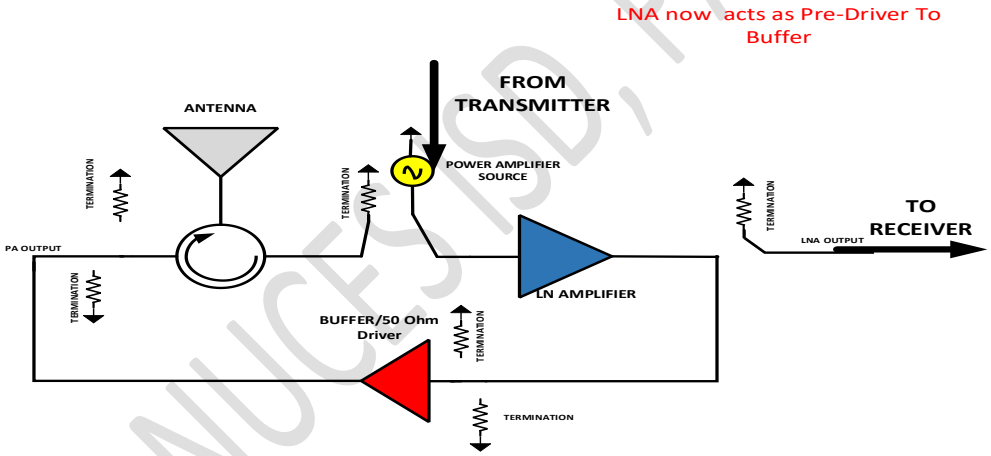


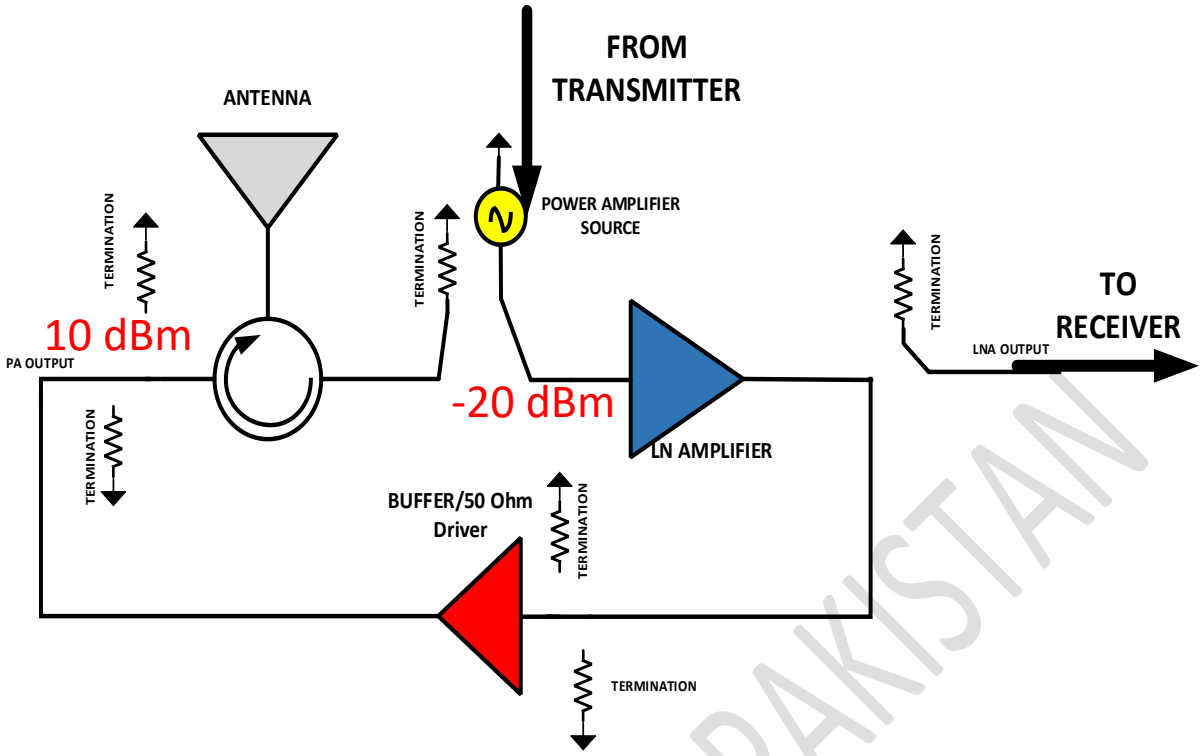
Figure 5 Amplifier during Transmission

3 Budget Analysis

A simple power budget analysis was done to get the design specifications for the circuit.

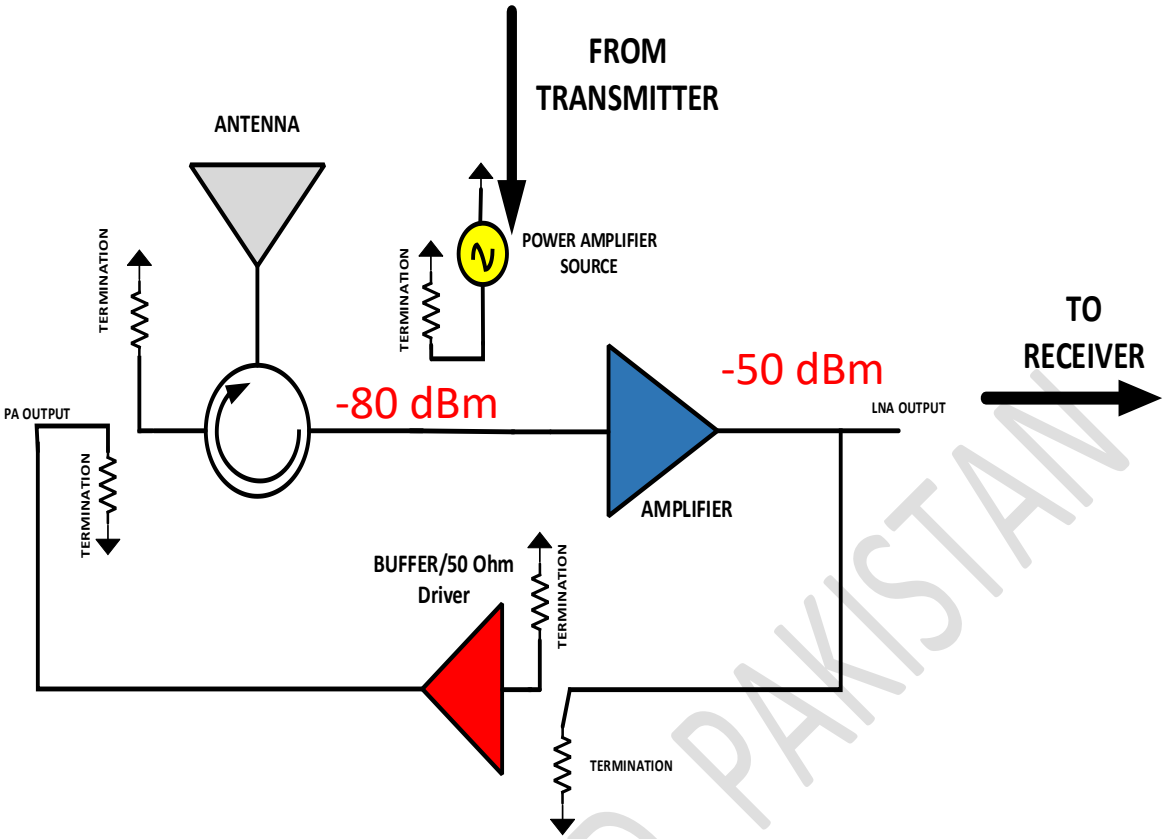
3.1 Transmission Budget Analysis

- Output Power at Antenna $\geq$ 10dBm (WLAN standard)
- Gain of Pre-Driver Circuit= 30 dB
- Minimum input power level required from Power Source= -20 dBm (10dBm – 30dB)
- The 50 Ohm buffer should have P1dB (out) > 10 dBm



3.2 Reception Budget Analysis

- Minimum power at the antenna≥ -80 dBm (WLAN standard)
- Gain of LNA=30 dB
- Power of signal after LNA=-50 dBm (-80 dBm+30dB)
- Further amplification is usually done in the IF/Baseband domain
- The LNA should have noise Figure $\leq 4dB$



4 Circuit Specifications

- Since the amplifier in the loop is now acting as both the power amplifier and the low noise amplifier, it must have following characteristics

Specification	Value
Gain	>20 dB
Area	As low as possible
Noise Figure	~ 3dB
Power	~30 mW
Linearity	~-20 dBm (input referred)
Output Power	~10 dBm (WLAN Applications)
Input Matching	<-10 dB in the band

5 Schematic

Figure 6 shows the 2-stage amplifier that is used to provide voltage gain in the circuit. In the first stage Transistors M0 and M1 provide transconductance. Transistor M1 also reduces current through

M2 and increases the value of Resistor and drain of M2. Due to this cascode and current re-use technique we obtain a large voltage gain. Transistor M4 is used to provide voltage to current feedback from output to input such that the input impedance is governed transistor M4. Transistor M5 establishes bias voltage for the gate of M0. The second stage combines the differential output from stage 1 in such a way that the noise contribution of transistor M4 is cancelled.

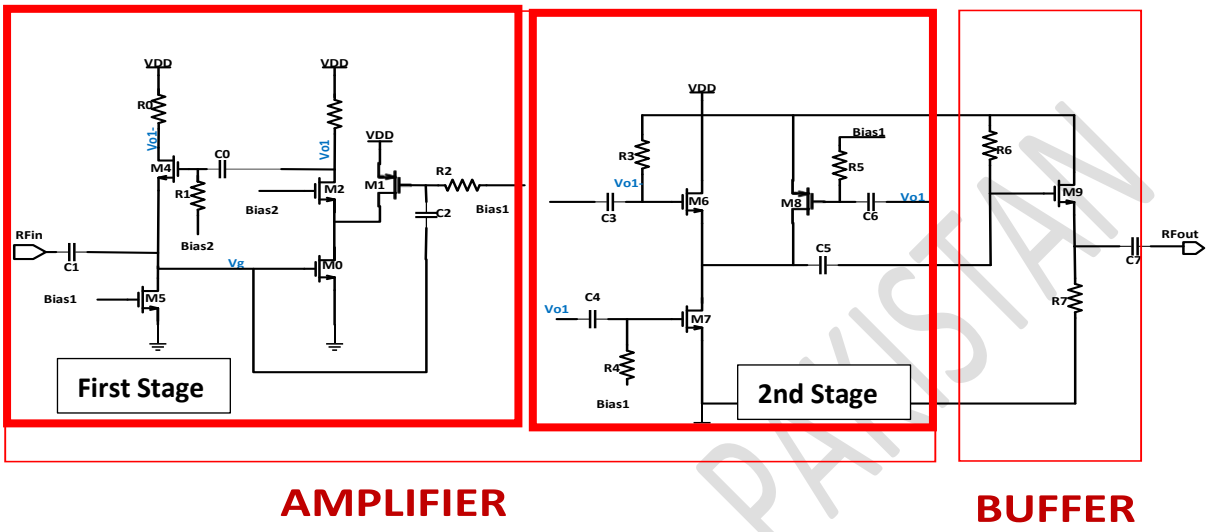


Figure 6 2-Stage Low Noise Amplifier With 50 Ohm Buffer

The equations describing the above circuits are

$$A_{v1} = \frac{(g_{m0} + g_{m1})}{(g_{ds0} + g_{ds1} + g_{m2})}(g_{m2} * R) \qquad Gain\ of\ First\ Stage$$

$$Z_{in} = \frac{1}{g_{m4}(1 + A_{v1})} \qquad Input\ Impedance\ seen\ by\ RFIN$$

$$g_{m6} = g_{m7} * \frac{A_{v1} * Rs}{R_0} \qquad Noise\ Cancel\ Condition\ for\ M4\ at\ second\ Stage$$

5.1 Design Process

- Optimum Size for good Noise Figure at selected bias conditions
- Selection of feedback transistor size for input matching
- Selection of proper size at stage two for noise cancellation
- Output buffer to match 1/gm=50 Ohms

Figure 7 shows the schematic setup to simulate small signal noise figure in Xschem and Ngspice. The noise response at selected size and bias is shown in Figure 8.

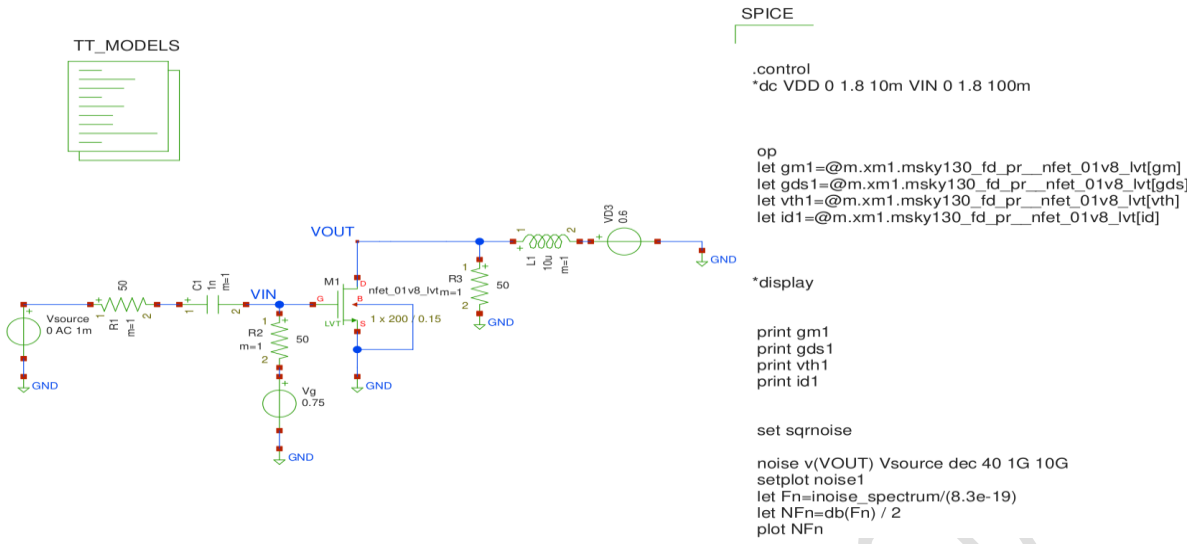


Figure 7 Schematic setup to simulate small signal noise figure

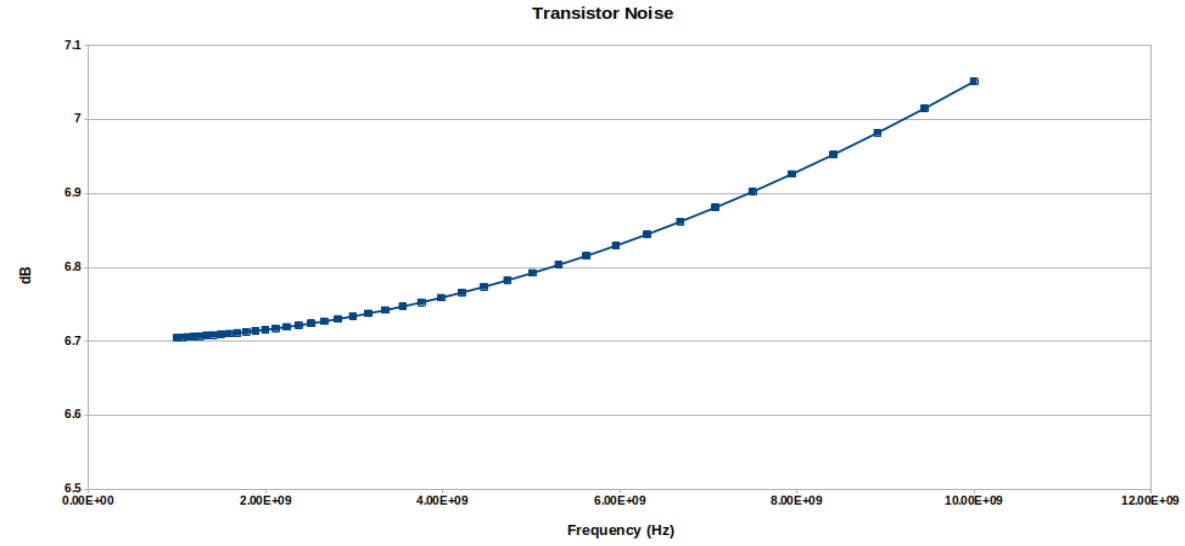


Figure 8 Noise Figure Response @200u/0.15u

Since by design this noise figure will be reduced by 3~4 dB at first stage this size was chosen.

5.2 DC Bias Point Simulations

To calculate bias points an Xschem Schematic was mad with all transistors at their bias points as shown in Figure 8.

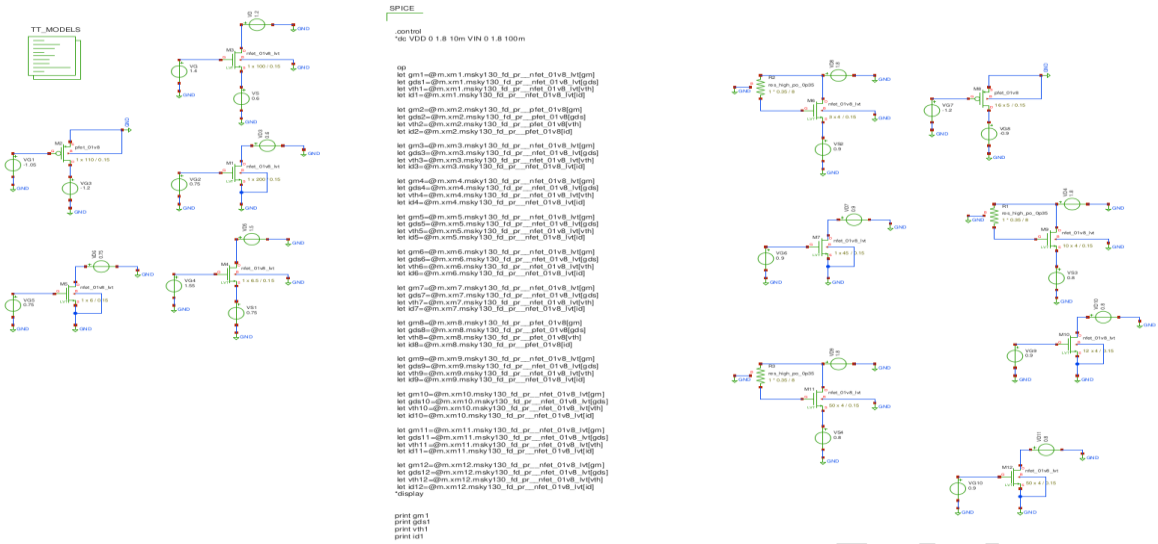


Figure 9 DC Bias Point Simulation for all transistors

5.3 Two Stage Low Noise Amplifier

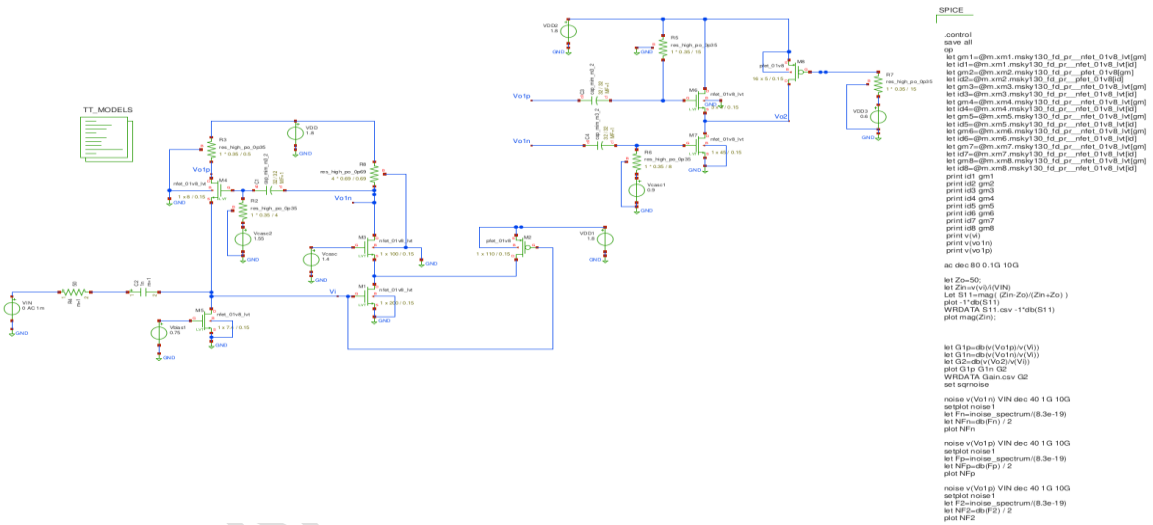


Figure 10 Xschem Schematic for two stage amplifier shown in Figure 6

5.3.1 Gain

Figure 11 shows the gain vs frequency graph of 2 Stage LNA. The voltage gain is 32 dB with the band width of 6.5 GHz.

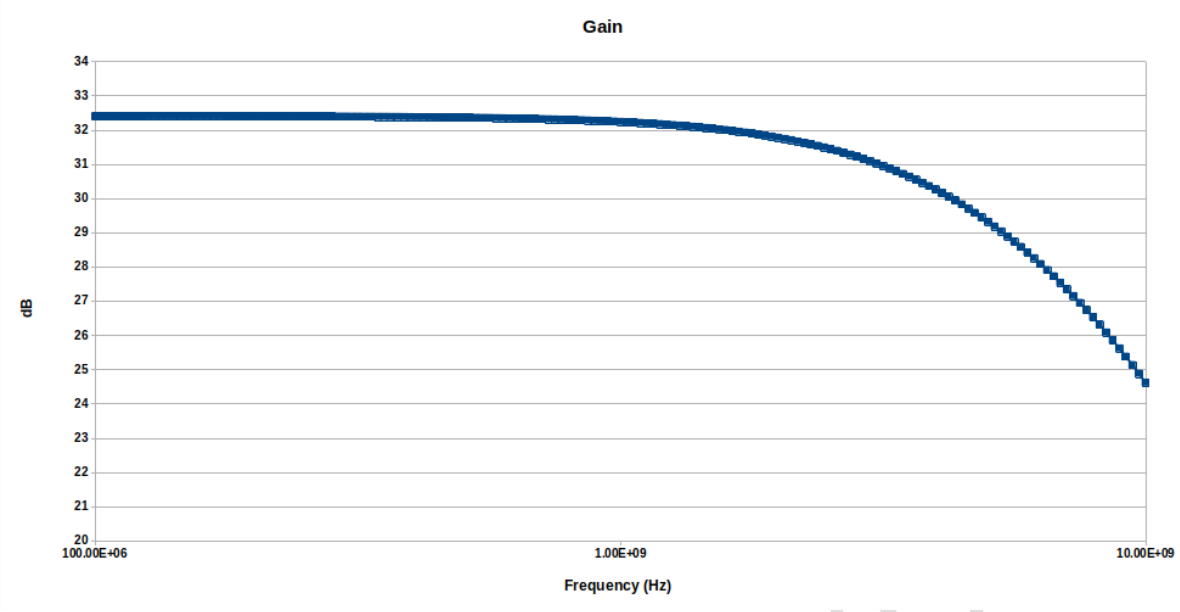


Figure 11 Gain vs Frequency graph of 2 stage LNA

5.3.2 Input Matching

Figure 12 shows the input matching characteristic of the LNA in the form of S11. The S11<-10 dB in the band of interest.

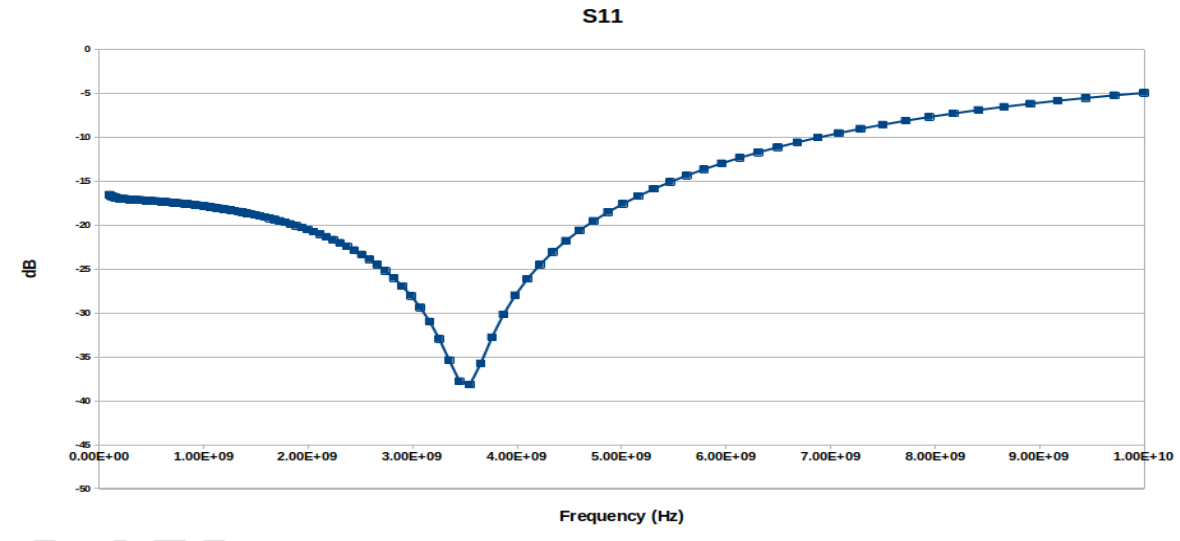


Figure 12 S11 of 2-Stage LNA

5.3.3 Noise Figure

Figure 13 shows the small signal noise figure graph of the 2-stage LNA. The noise figure is estimated from ac analysis using

$$S_{11} = 20\log\left(\left|\frac{Z_{in} - 50}{Z_{in} + 50}\right|\right)$$

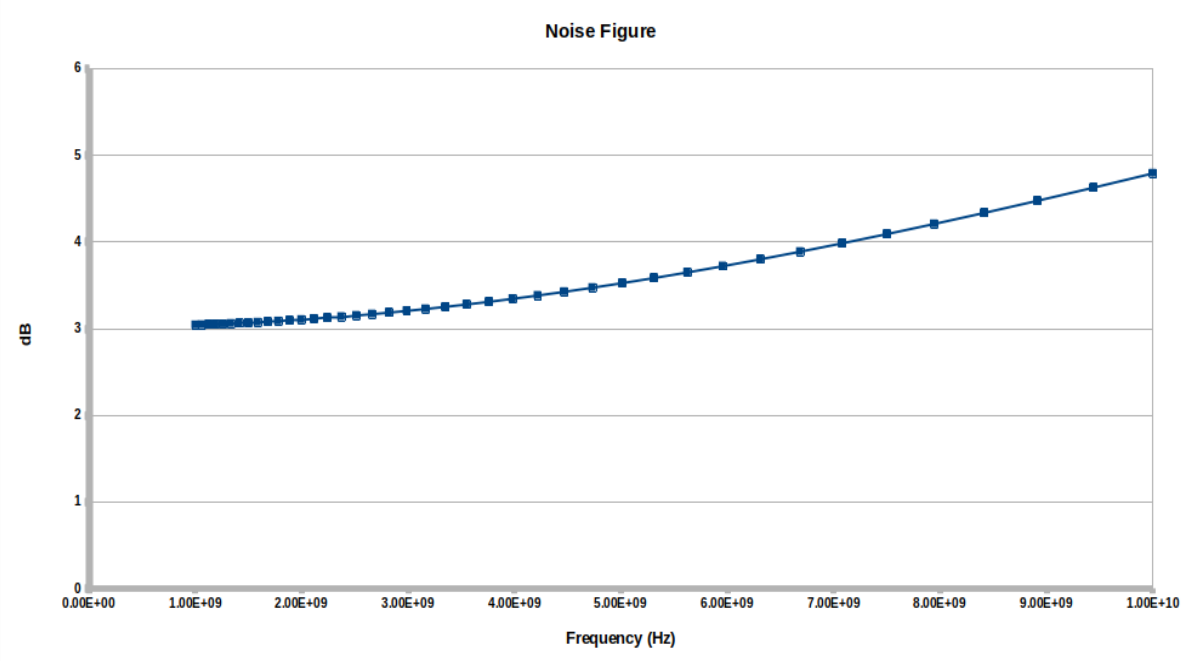


Figure 13 Noise Figure of 2-Stage LNA

5.4 Complete Schematic

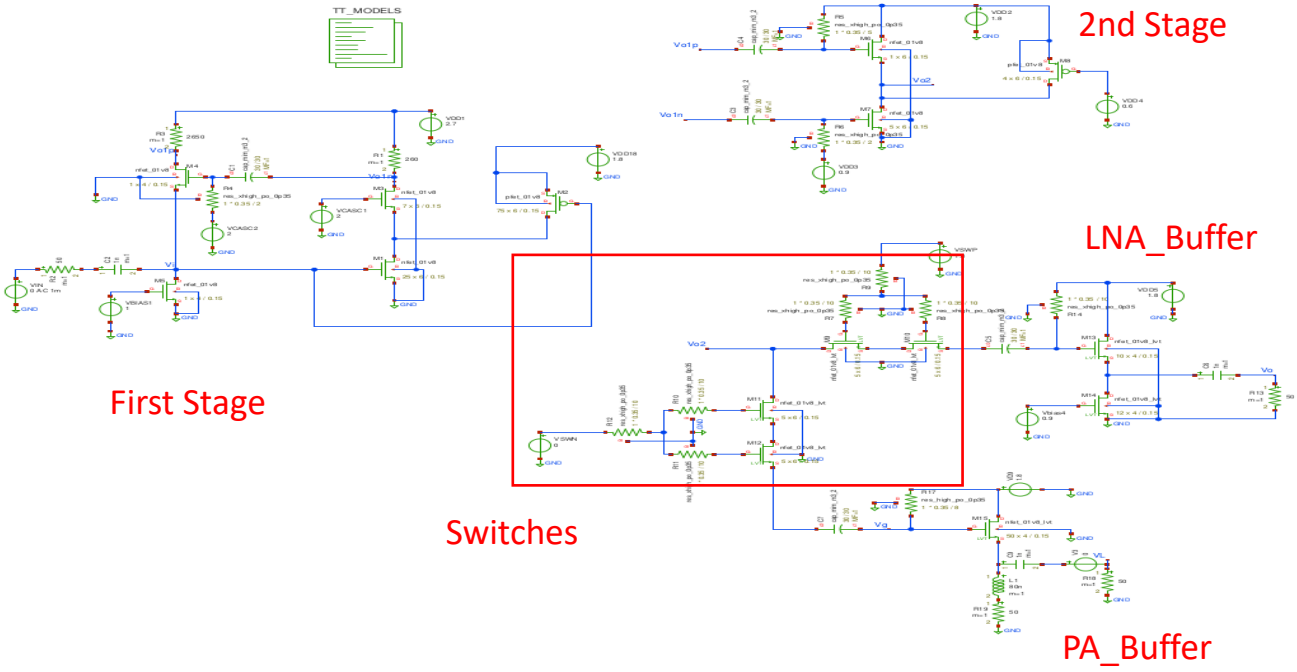


Figure 14 Complete Schematic of Bi- Directional Amplifier Architecture

6 Layout

After schematic simulations, the layout was done in Magic VLSI. Individual modules were laid out separately with clean DRC and LVS and then were combined together. The layouts are shown in Following Figures.

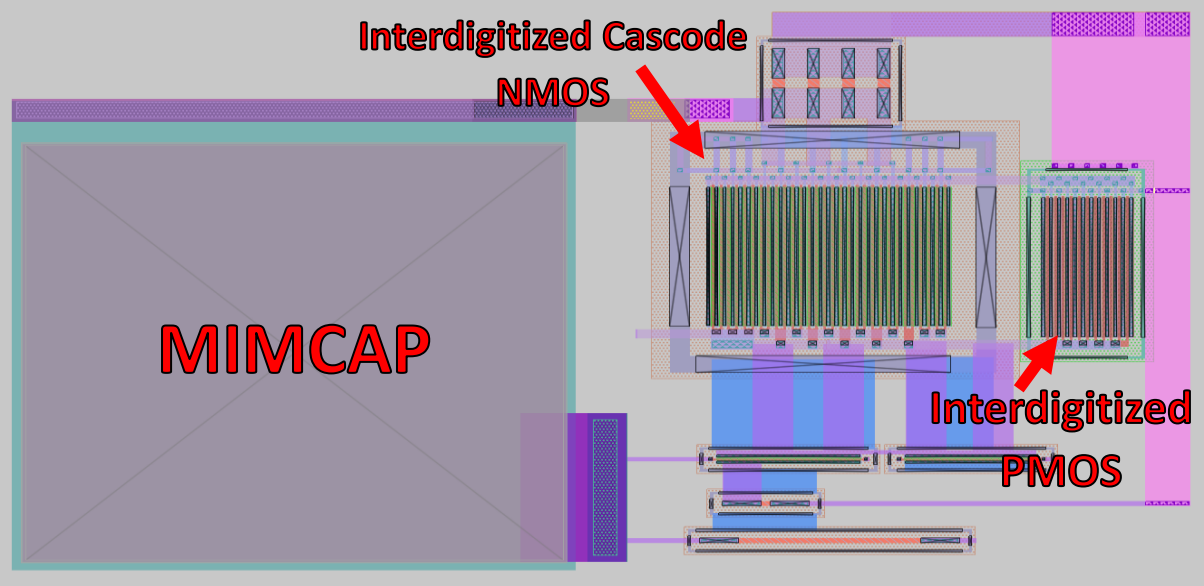


Figure 15 Layout of First stage of LNA

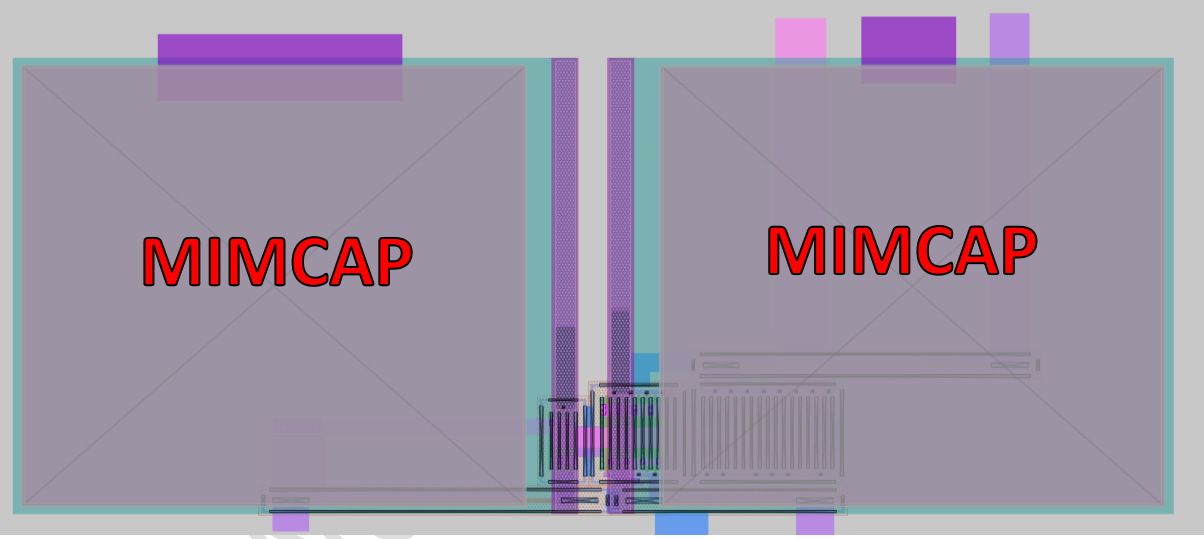


Figure 16 Layout of Second Stage of Amplifier

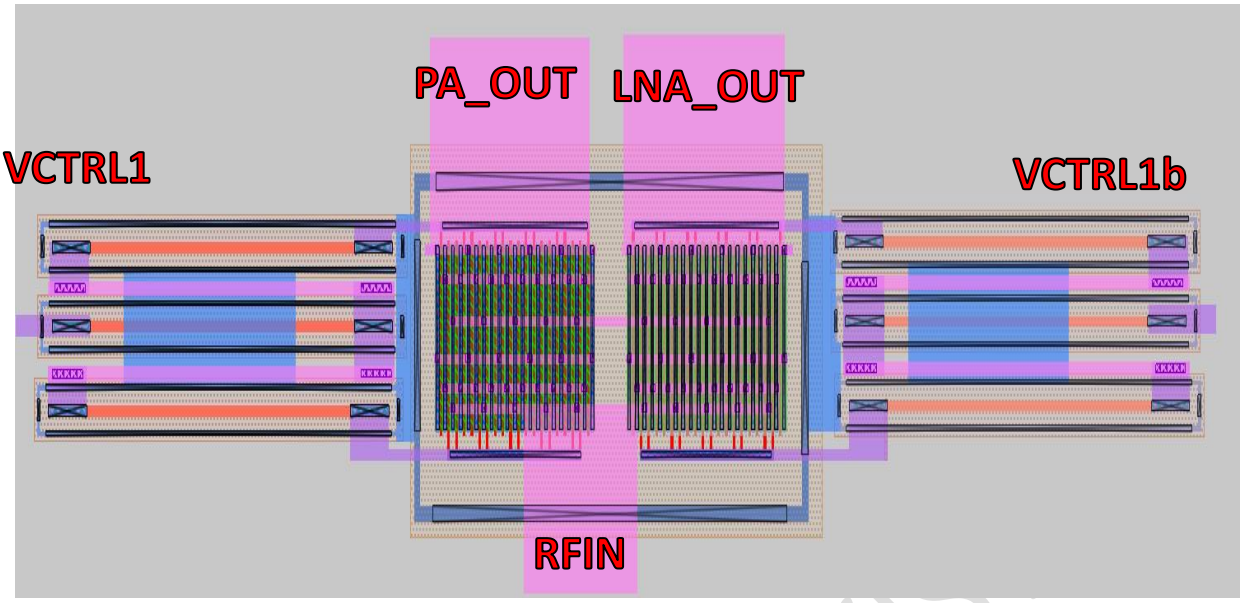


Figure 17 Layout of Switches

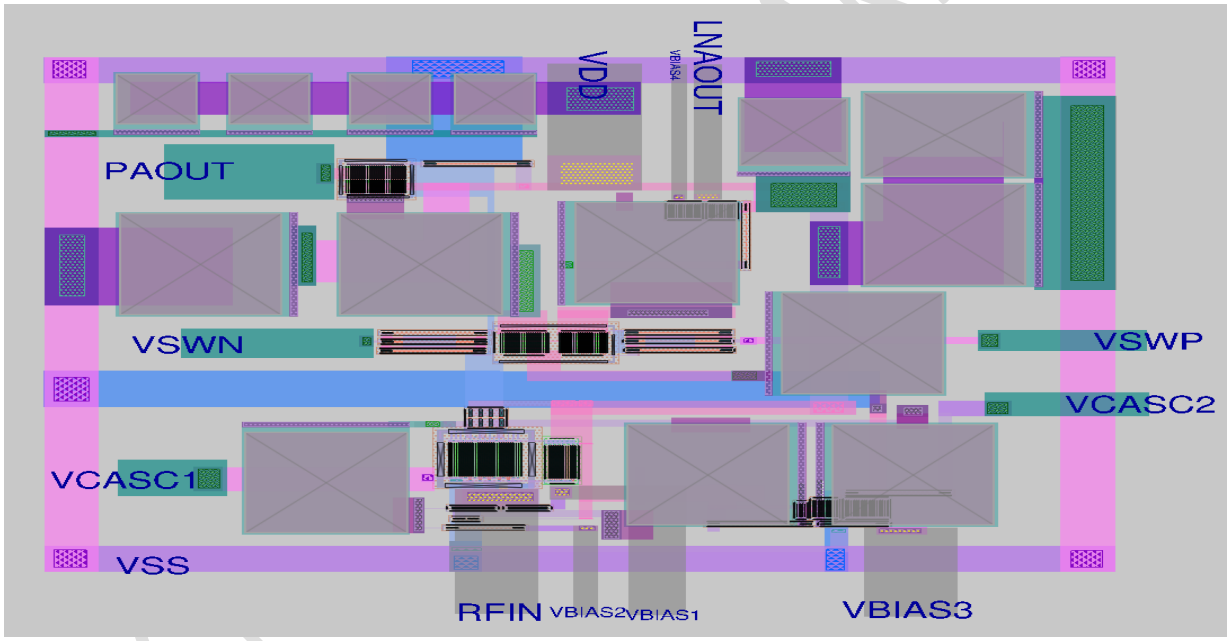


Figure 18 Complete DRC, Antenna, LVS clean layout of Bidirectional Amplifier

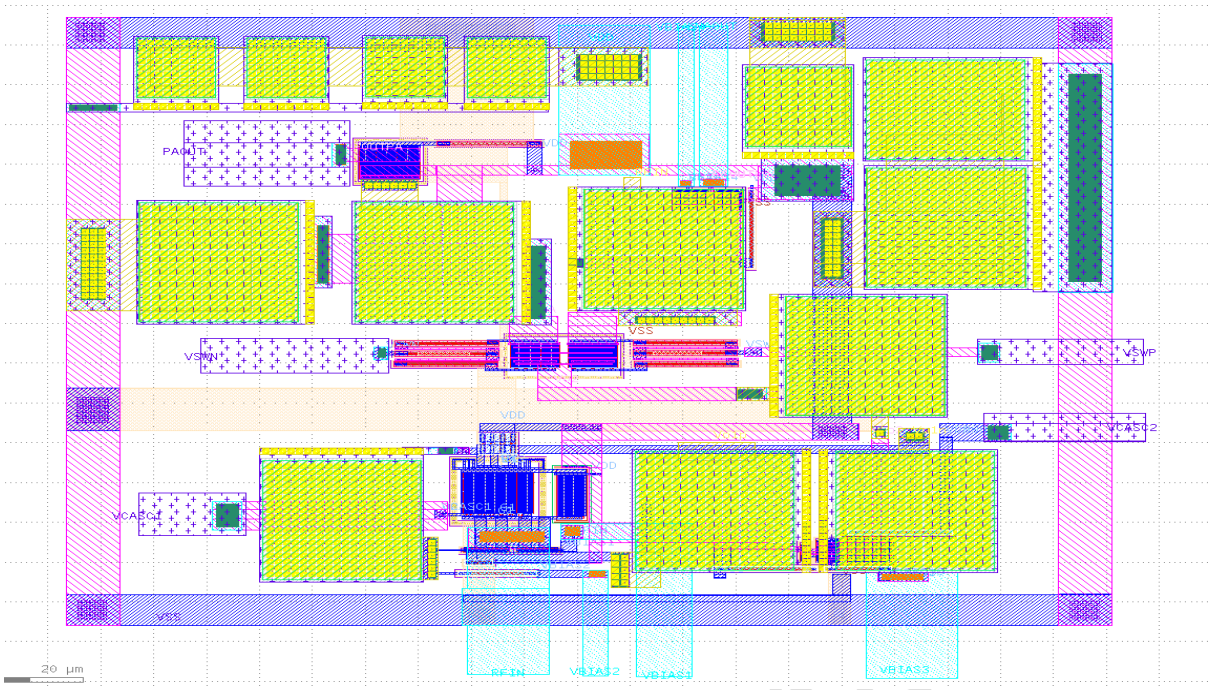


Figure 19 GDS view of complete layout in KLayout tool

7 Post layout Simulation

Netlists extracted from the magic were simulated again in xschem to verify circuit functionality post layout. The schematic symbol is shown in Figure 20.

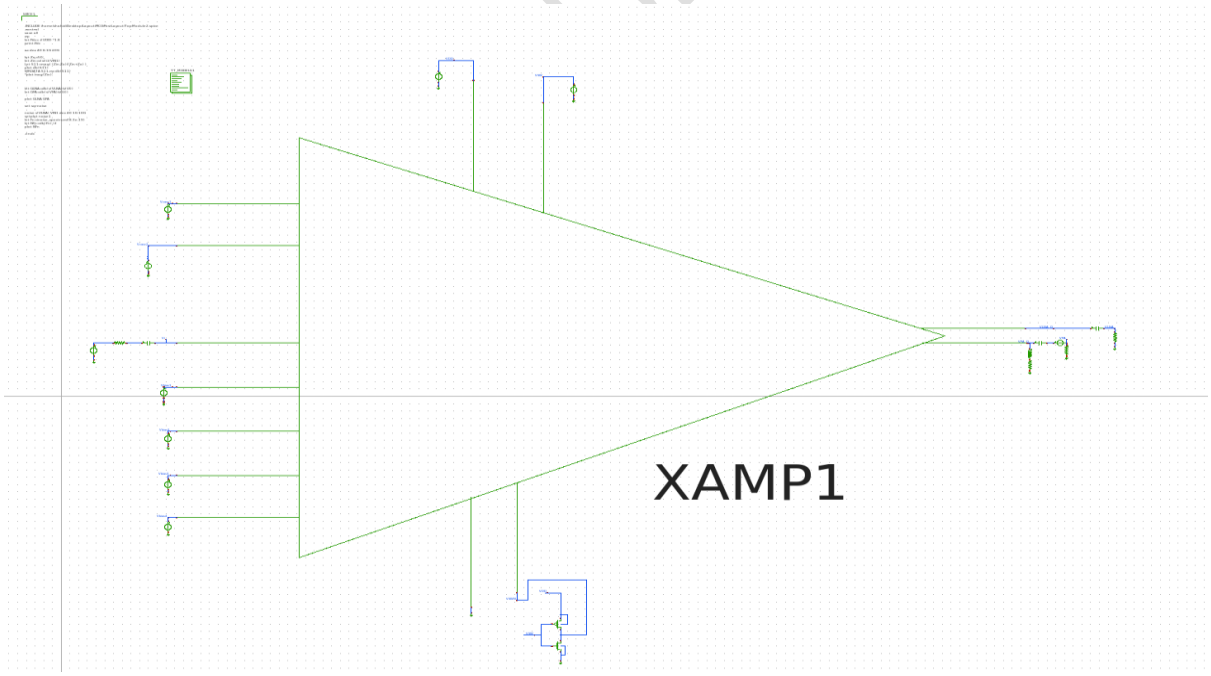


Figure 20 Post Layout Simulation Setup in Xschem against magic extracted netlists

7.1 Noise Figure

The noise figure response is shown in Figure 21. Surprisingly the noise figure has improved. This is probably due to the fact that no parasitic resistances were calculated at the RFIN net since we were

not able to extract resistance in magic (some issue to do with **extresist** command not working in hierarchical designs).

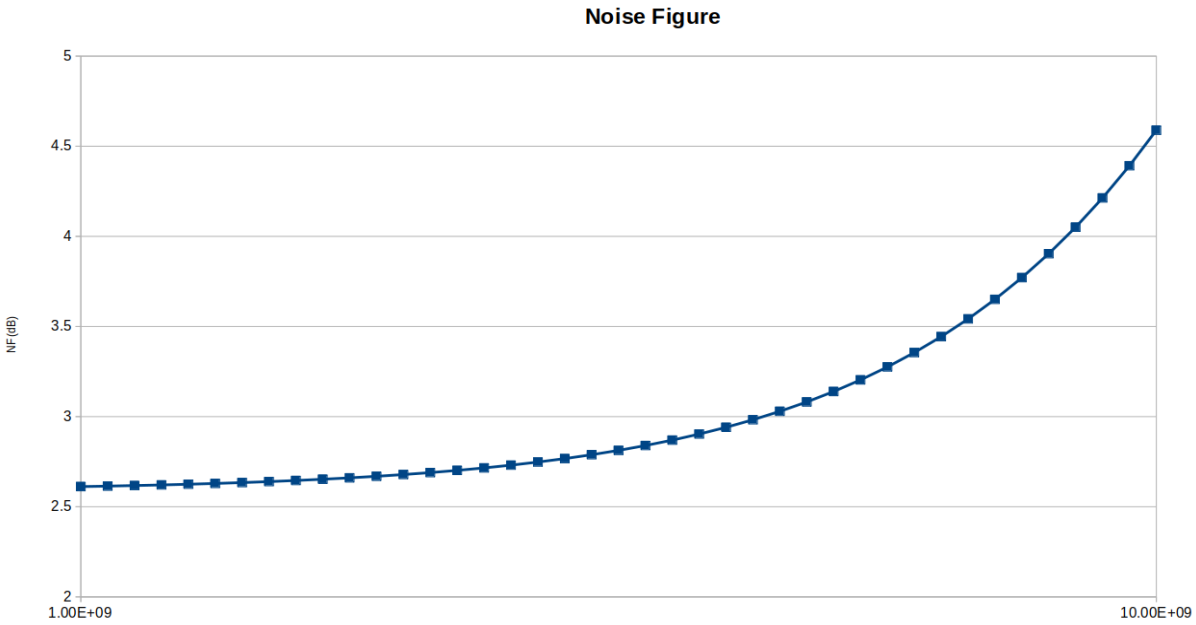


Figure 21 Post layout Noise Figure Response

7.2 Input Matching

Figure 22 shows the matching at input in the form of S11.

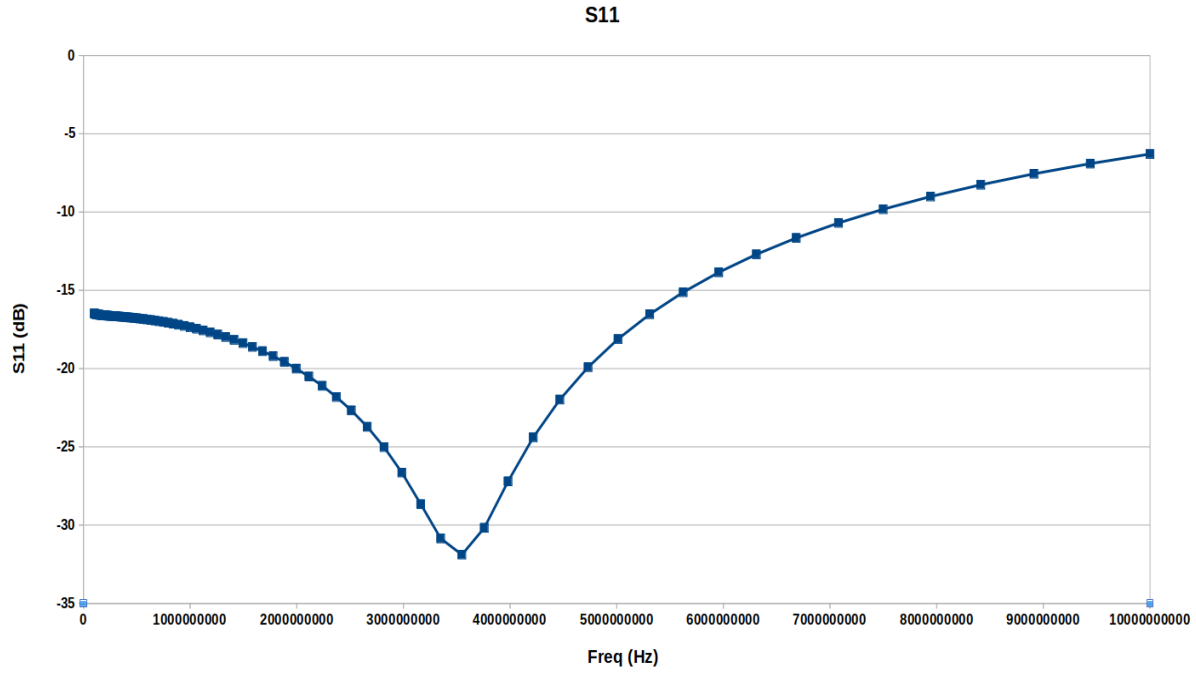


Figure 22 Post Layout S11 graph

7.3 Voltage Gain

Figure 23 shows the voltage gain of the amplifier when the switches for receiver path (LNA) are on. We can see that the gain is 25 dB as compared to original 32dB. The 7dB loss is due to the buffer at

the output to drive 50Ω test equipment. Also the LNA to PA isolations is about 35 dB. The bandwidth is 4.5 GHz.

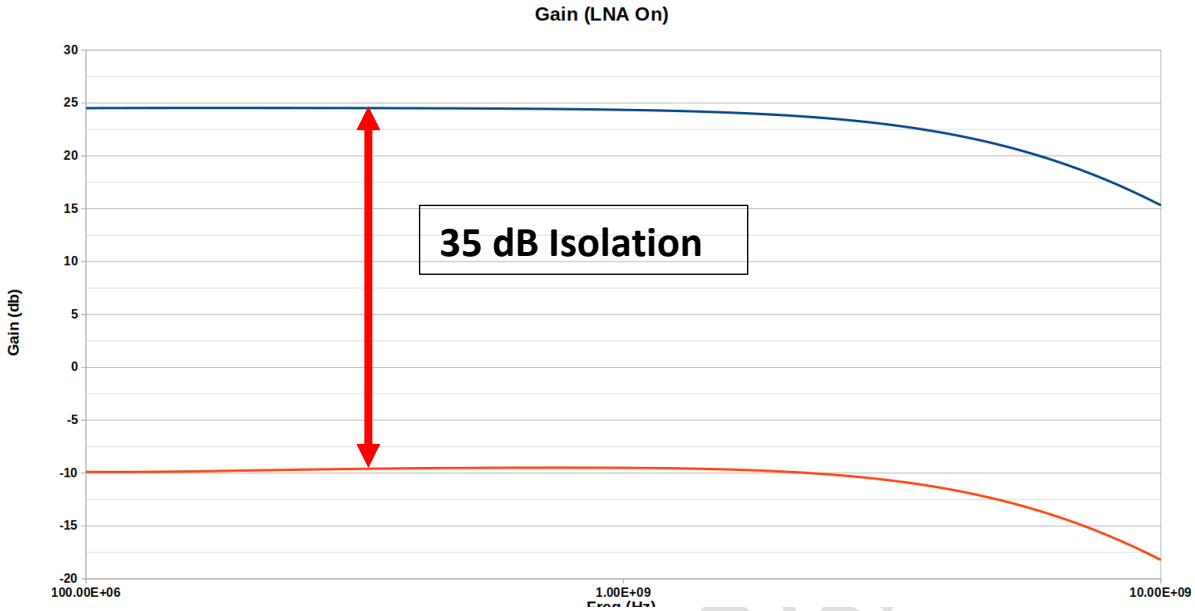


Figure 23 Post Layout Voltage Gain of LNA

Figure 24 shows the voltage gain when switches for Transmitter (PA) are on. We can see that the voltage gain is about 27dB. The isolation between LNA and PA is still greater than 35 dB.

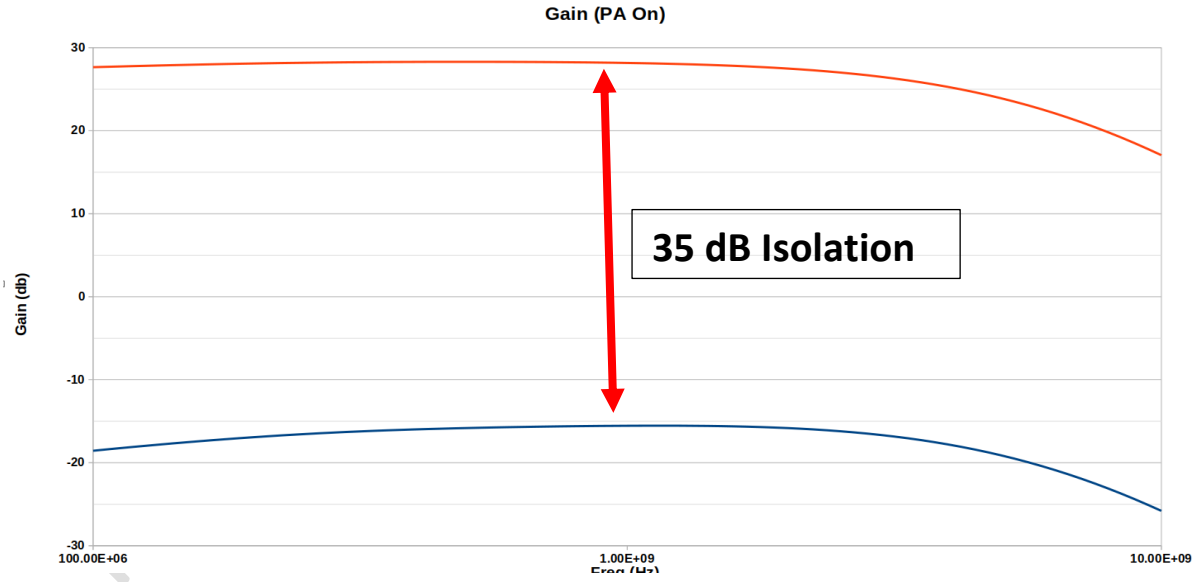


Figure 24 Post Layout small signal PA Gain

However, this is really a small signal voltage gain and does not include compression and non-linear effects of large signal saturation. Since Ngspice does not have a PSS/Harmonic balance simulator we were not able to do large signal analysis. However, we did plot output vs input power using transient analysis. The 1-dB compression graph is shown in Figure 25.

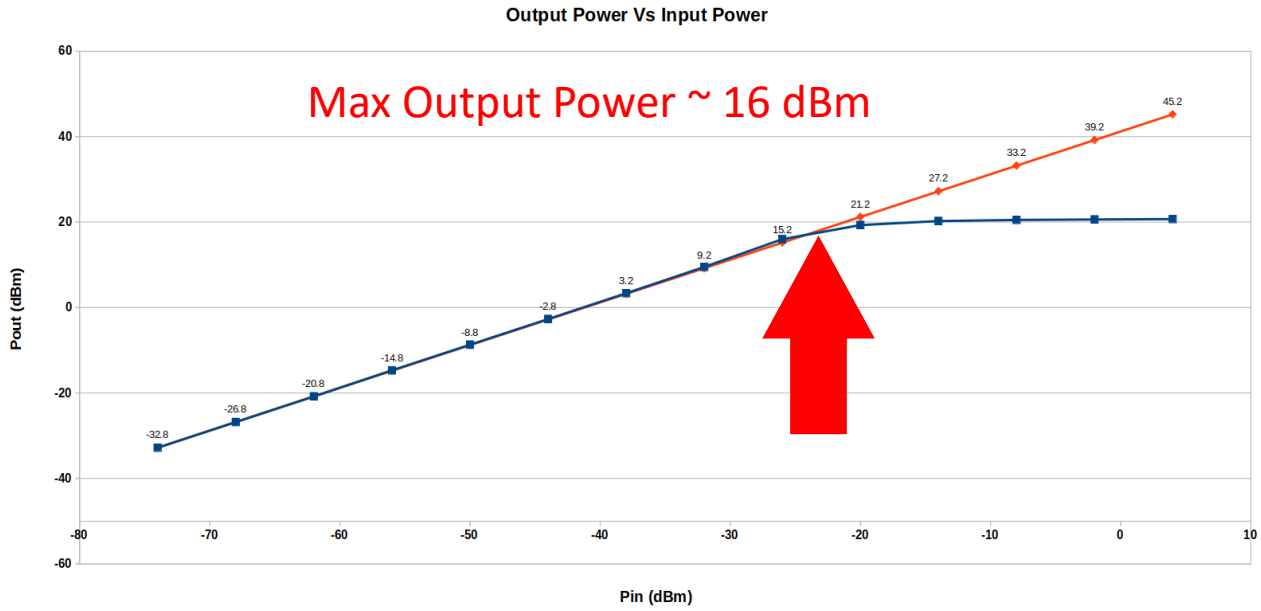


Figure 25 Post layout Input Vs Output Power

8 Post layout Results Summary

Specification	Designed Value	Post Layout Value
Gain	>20 dB	25 dB (32 dB without buffer)
BandWidth	6 GHz	4.5 GHz
Area	As low as possible	0.033880 sq mm (0.204x 0.166)
Power	<30mW	27 mW
Noise Figure	~ 3dB	3 dB
Linearity	~-20 dBm (input referred)	~-22 dB
Output Power	~10 dBm (WLAN Applications)	16 dBm
Input Matching	<-10 dB in the band	<-10 dB in the band
LNA-PA Isolation	>30 dB	35-45 dB isolation

9 Conclusion

The design is ready to be integrated in caravel chip