Project Report

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Section:03

Course:CSE 332

I have made a 18 bit datapath design

ISA instruction:

00881:It is an OR operation where destination register is 00001,one source register is 00100,another source register is 00010 and opcode is 000

08881:It is a NOR operation where destination register is 00001,one source register is 00100,another source register is 00010 and opcode is 001

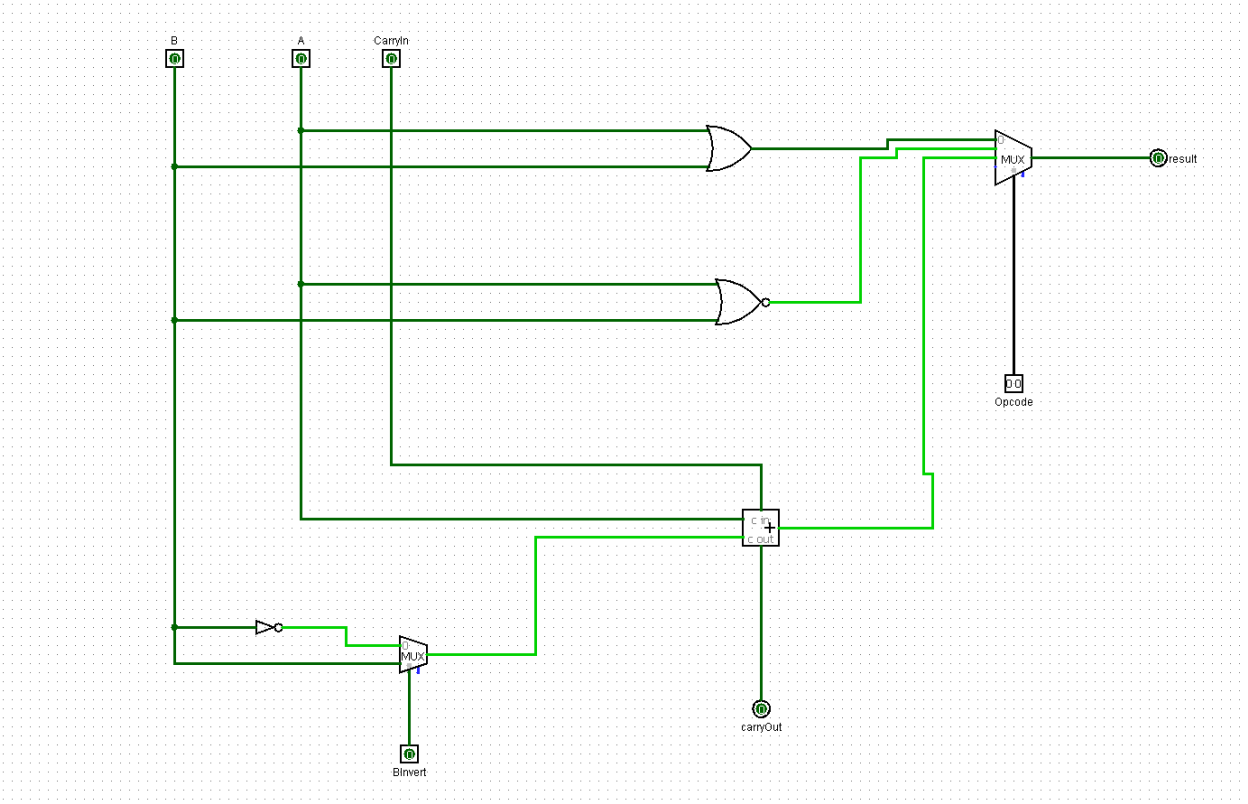
10881:It is an add or subtract operation where destination register is 00001,one source register is 00100,another source register is 00010 and opcode is 010.If we put 0 in B invert, it will perform add operation and if we put 1 in B invert,it will perform subtract operation

For immediate value,I have put load,store,select and clear in the ROM.Whenever we want to load or store a value,I will use the accessed primary memory.We can use an immediate value usimg it also

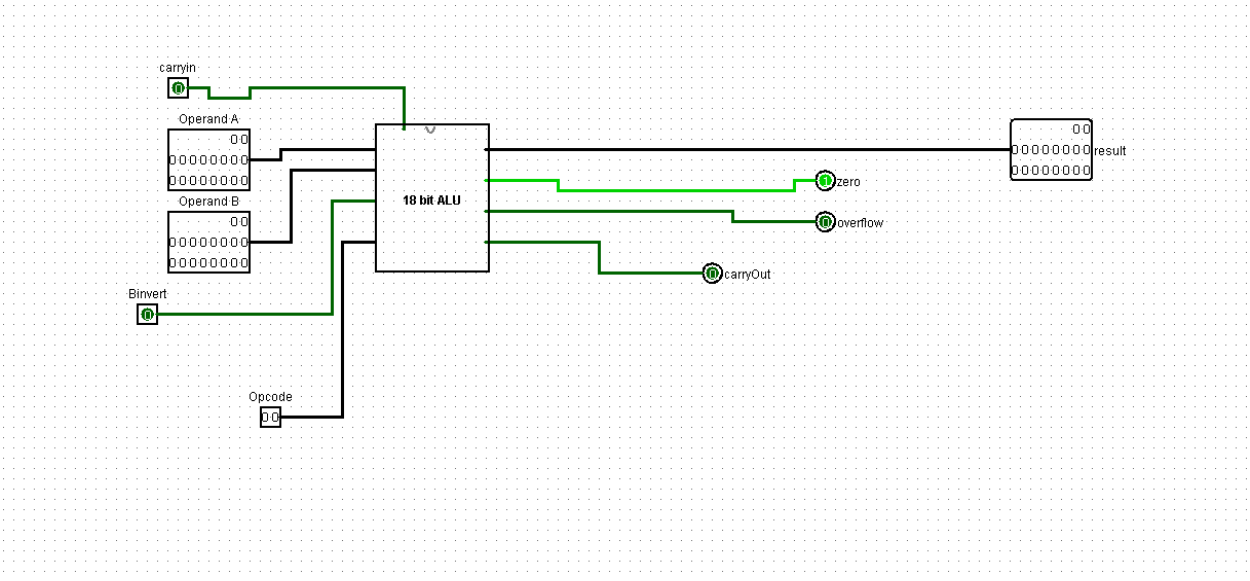
Screenshot:

Sub circuits:

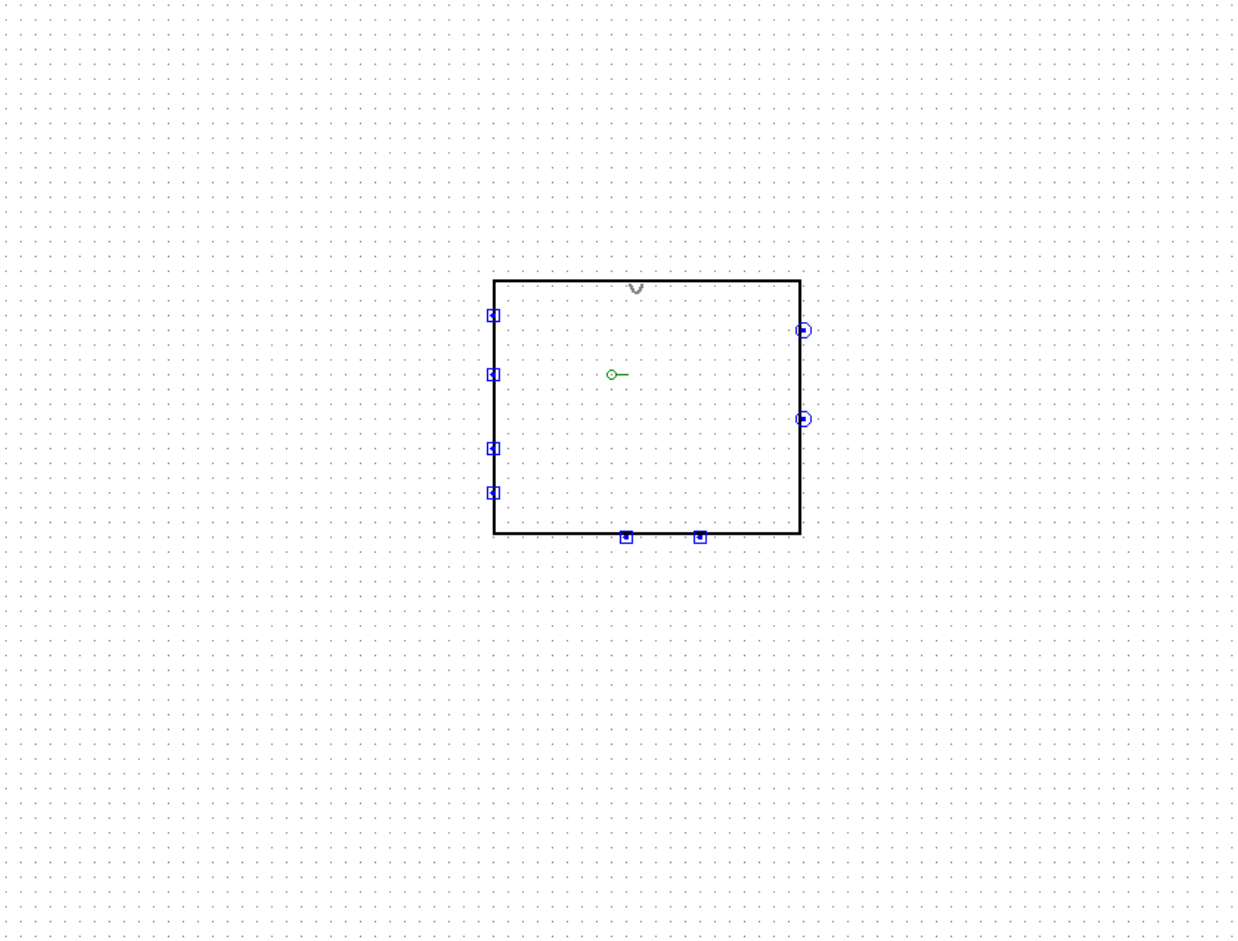
1 bit alu


B
A
CarryIn
MUX
result
Opcode
C_in
C_out
MUX
carryOut
BInvert

18 bit ALU

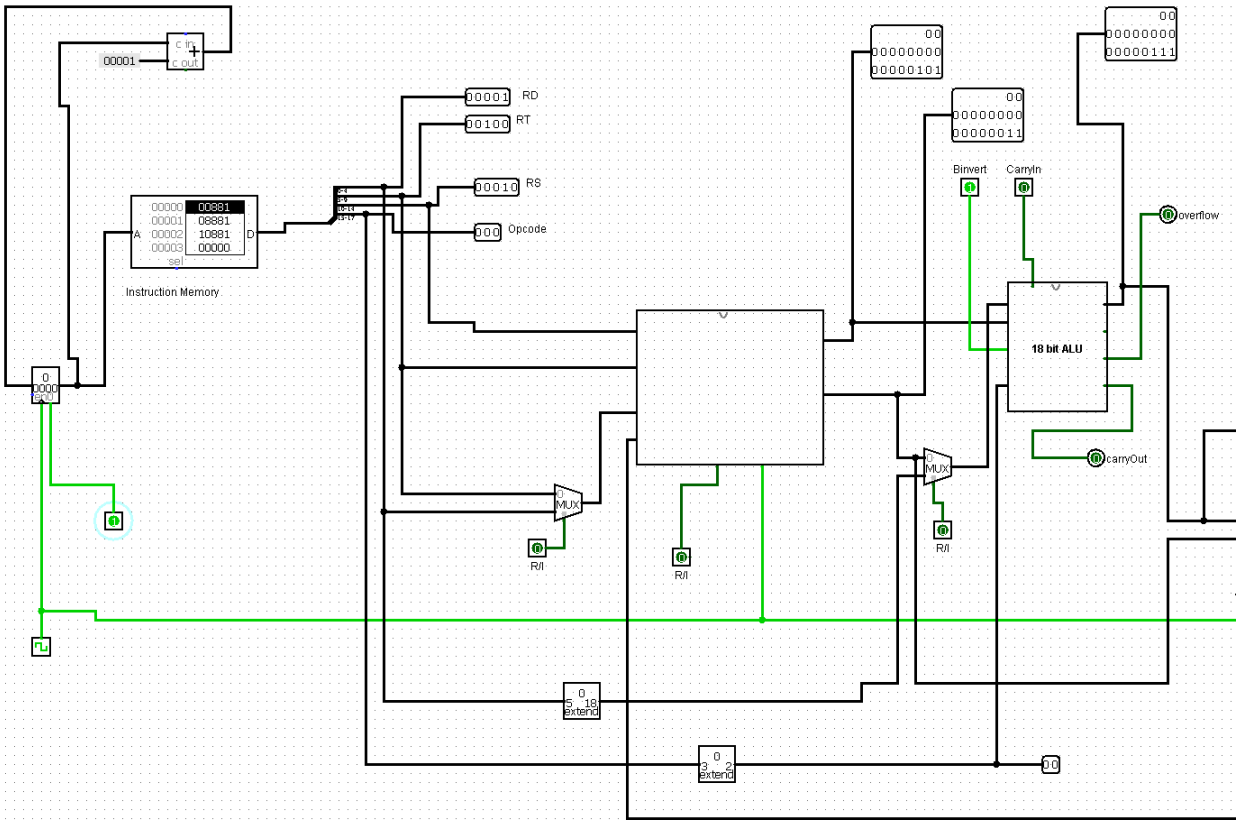

carryin
Operand A
Operand B
18 bit ALU
result
zero
overflow
carryOut
Binvert
Opcode

18 bit register file

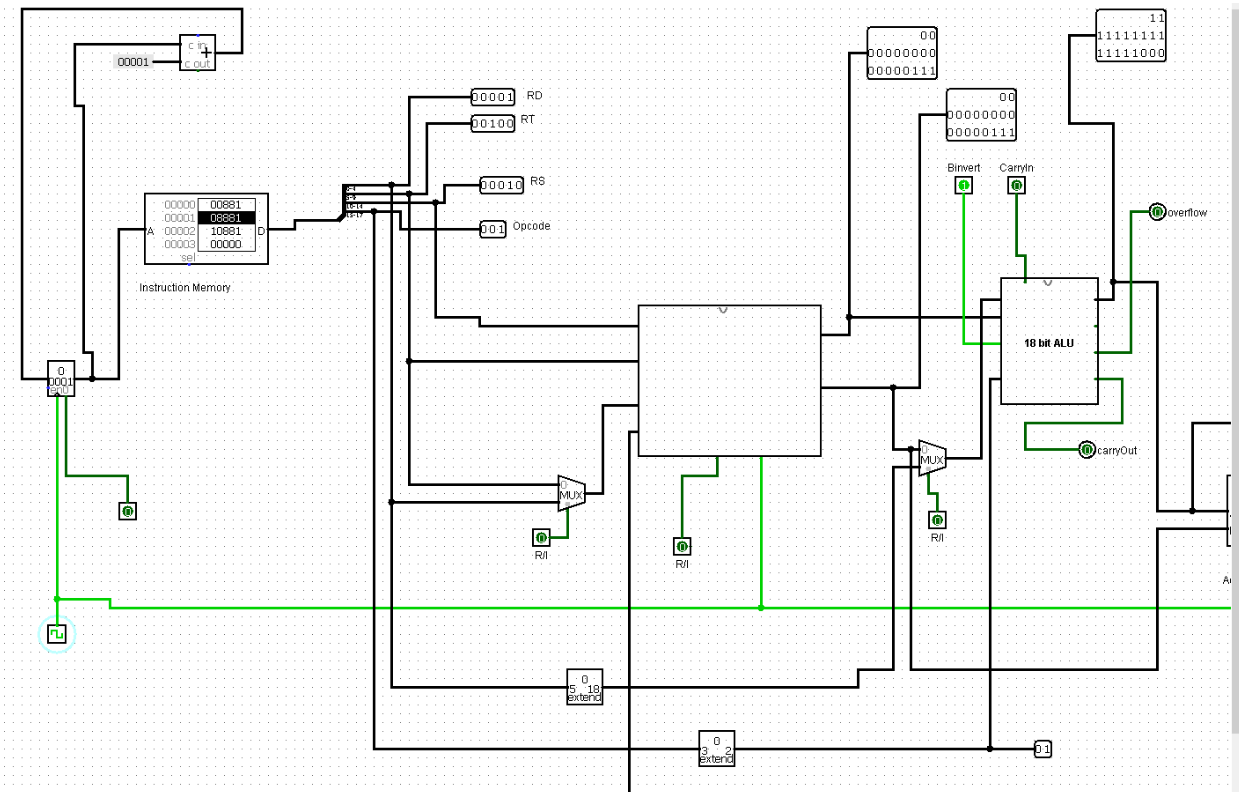


Main circuit:

For or

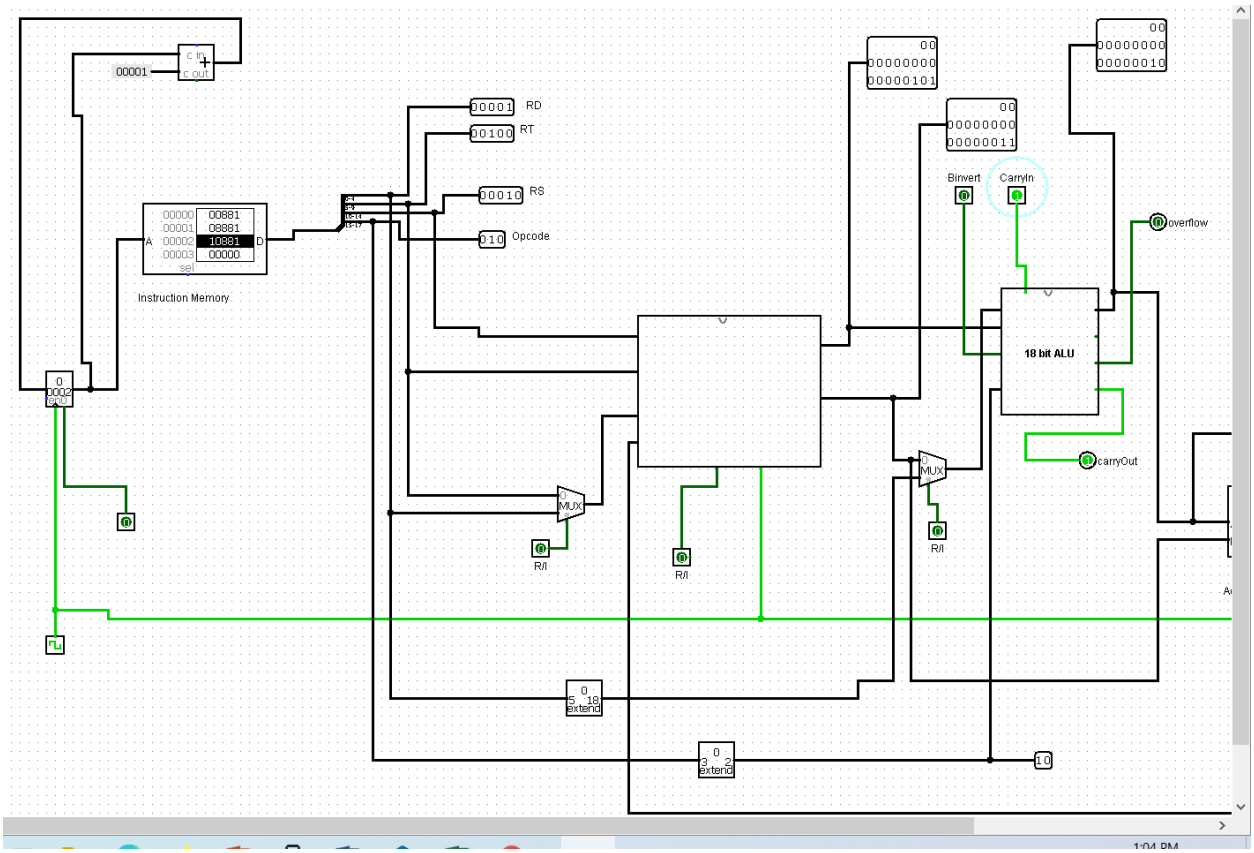

00001
c in
c out
00001
RD
00100
RT
00010
RS
000
Opcode
00000 00881
00001 08881
A 00002 10881
00003 00000
D
sel
Instruction Memory
00000101
00000011
00000111
Binvert
CarryIn
overflow
18 bit ALU
carryOut
MUX
R/I
5 18
extend
3 2
extend

For NOR

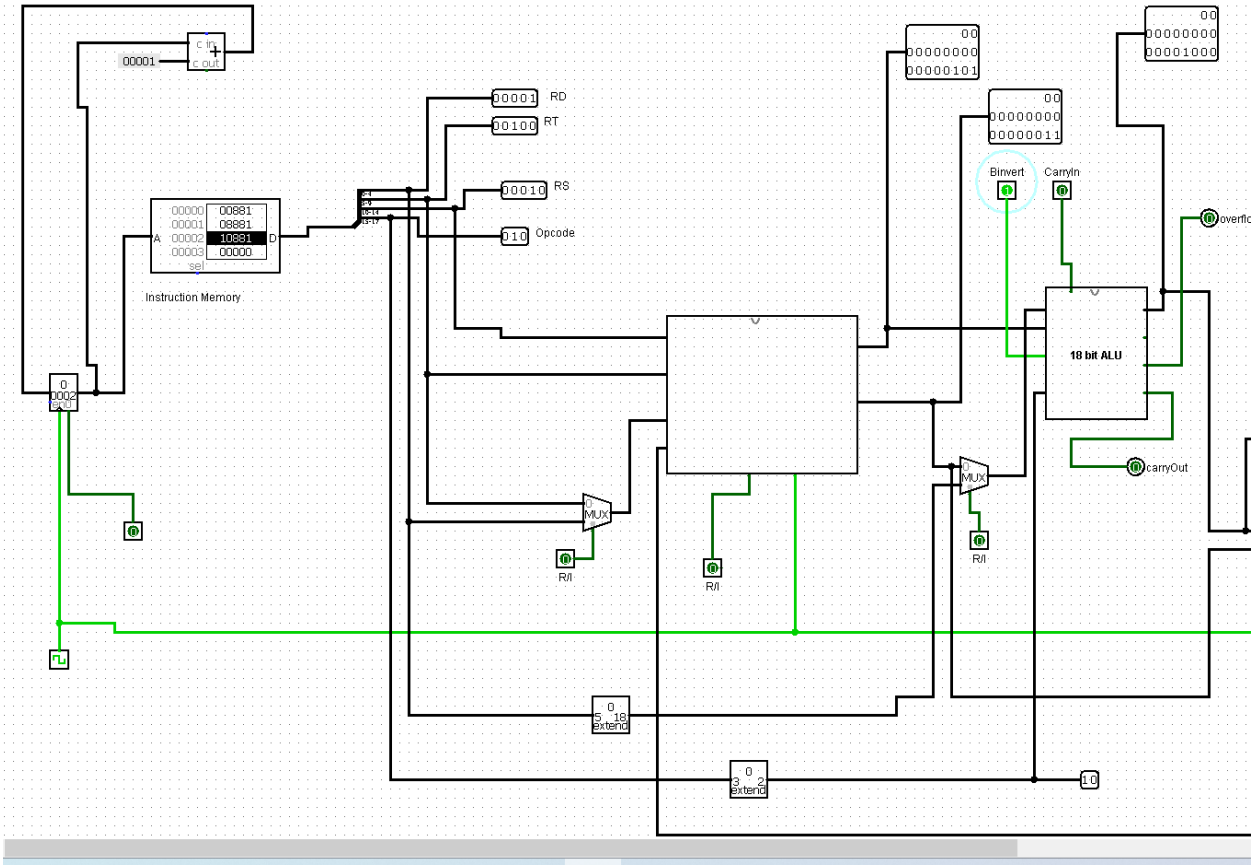


00001
Instruction Memory
RD
RT
RS
Opcode
R/I
R/I
R/I
Binvert
CarryIn
overflow
18 bit ALU
carryOut
extend
extend

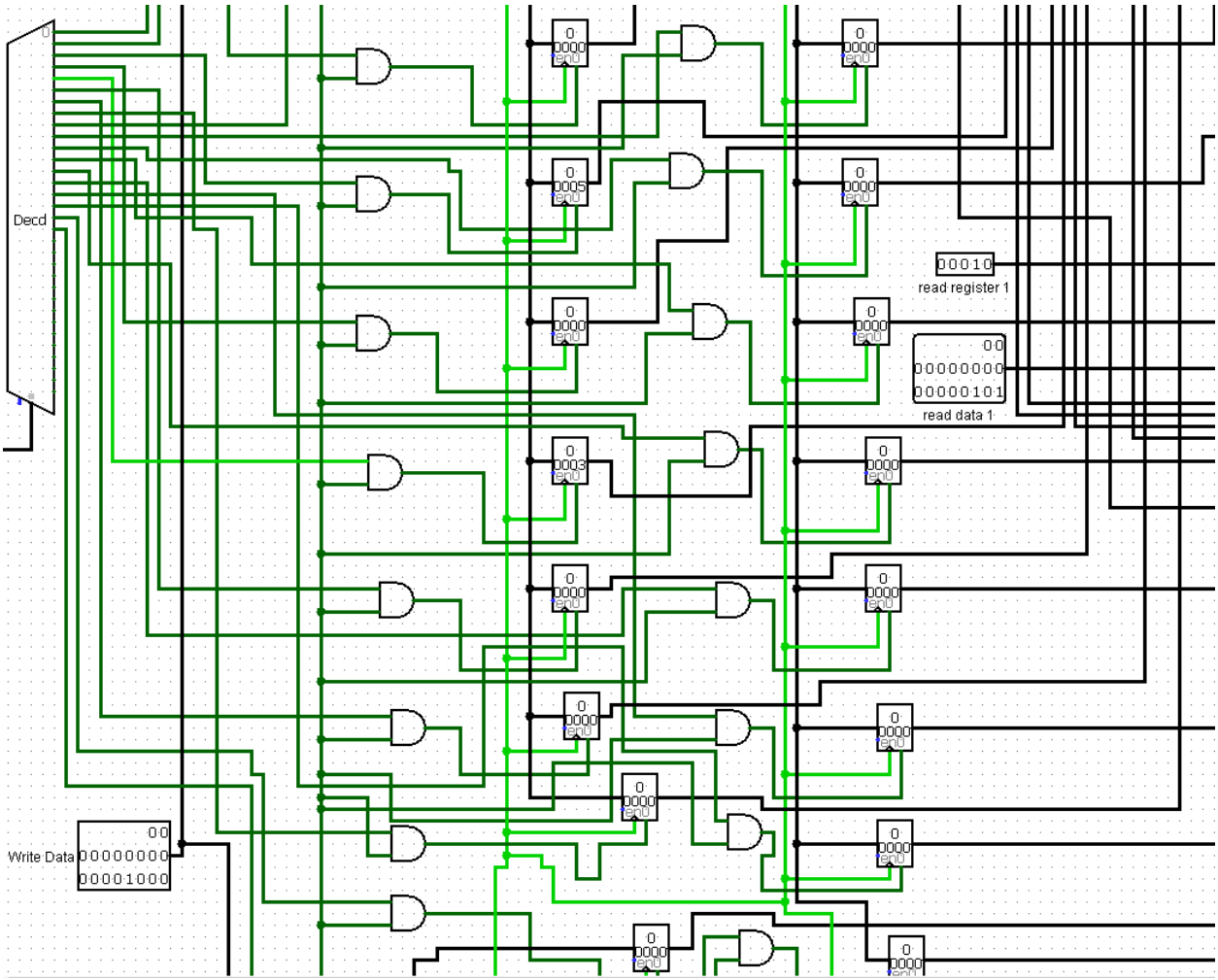
For sub:


00001
C in
C out
00001 RD
00100 RT
00010 RS
010 Opcode
Instruction Memory
00881
08881
10881
00000
18 bit ALU
Binvert
CarryIn
overflow
carryOut
MUX
R/I
5 18
extend
3 2
extend

For add:



To write that add result in the register


Decd
00
00000000
00001000
Write Data
00010
read register 1
00
00000000
00000101
read data 1