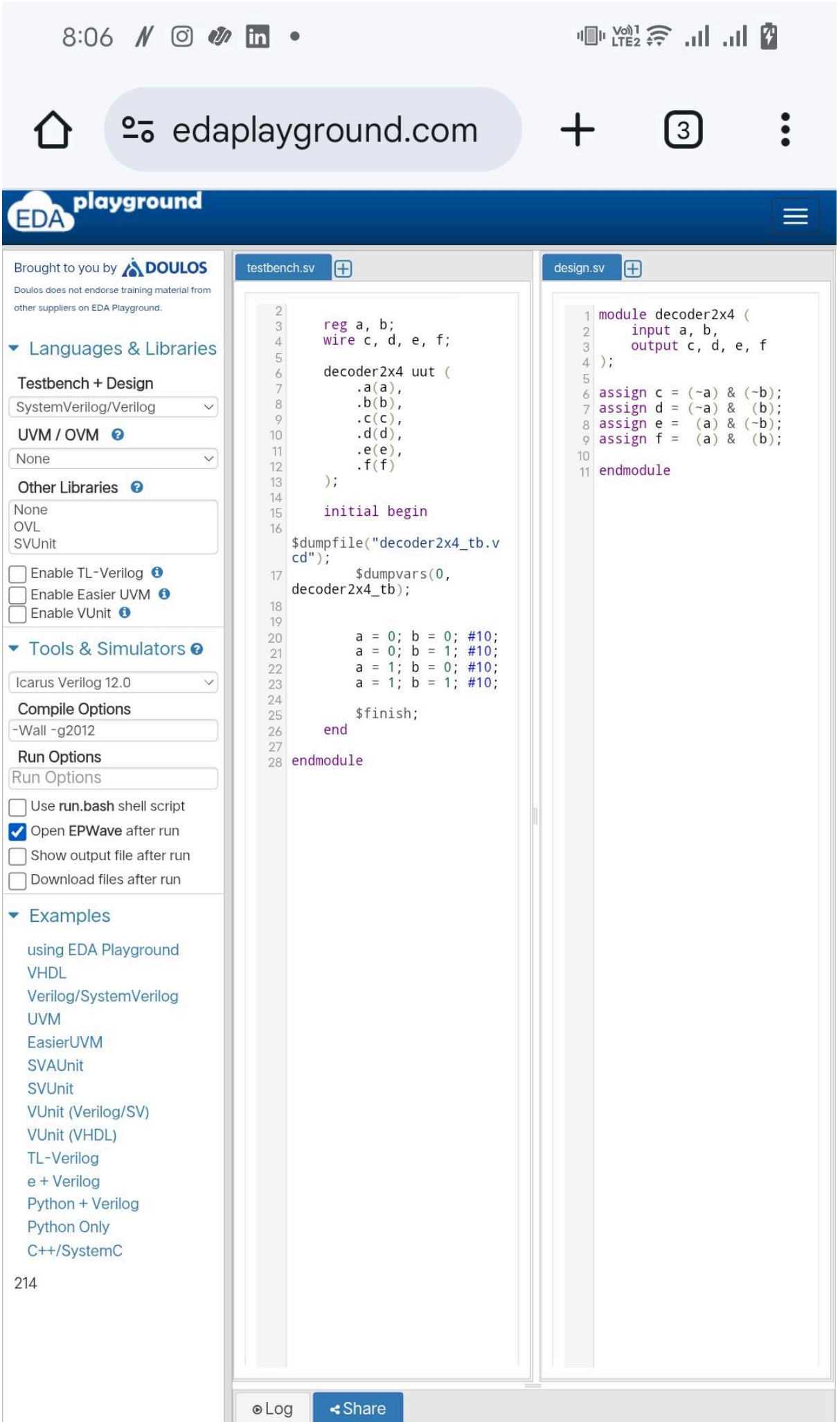
2: 4 decoder


8:06
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UVM / OVM
None
Other Libraries
None
OVL
SVUnit
Enable TL-Verilog
Enable Easier UVM
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Tools & Simulators
Icarus Verilog 12.0
Compile Options
-Wall -g2012
Run Options
Run Options
Use run.bash shell script
Open EPWave after run
Show output file after run
Download files after run
Examples
using EDA Playground
VHDL
Verilog/SystemVerilog
UVM
EasierUVM
SVAUnit
SVUnit
VUnit (Verilog/SV)
VUnit (VHDL)
TL-Verilog
e + Verilog
Python + Verilog
Python Only
C++/SystemC
214
testbench.sv
design.sv
reg a, b;
wire c, d, e, f;
decoder2x4 uut (
.a(a),
.b(b),
.c(c),
.d(d),
.e(e),
.f(f)
);
initial begin
$dumpfile("decoder2x4_tb.vcd");
$dumpvars(0, decoder2x4_tb);
a = 0; b = 0; #10;
a = 0; b = 1; #10;
a = 1; b = 0; #10;
a = 1; b = 1; #10;
$finish;
end
endmodule
module decoder2x4 (
input a, b,
output c, d, e, f
);
assign c = (~a) & (~b);
assign d = (~a) & (b);
assign e = (a) & (~b);
assign f = (a) & (b);
endmodule
Log
Share

8:07

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EDA playground

EPWave

From:

0s

To:

40s

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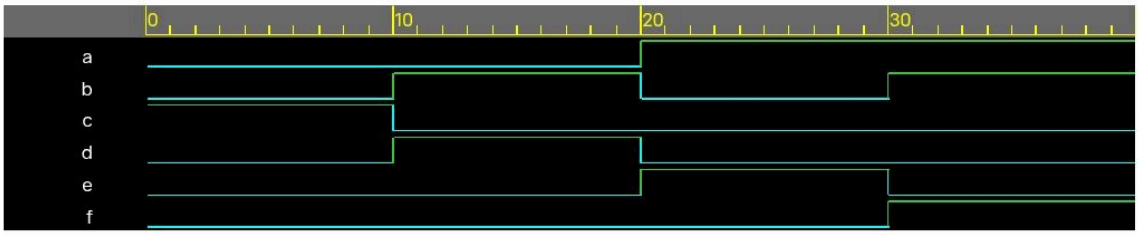

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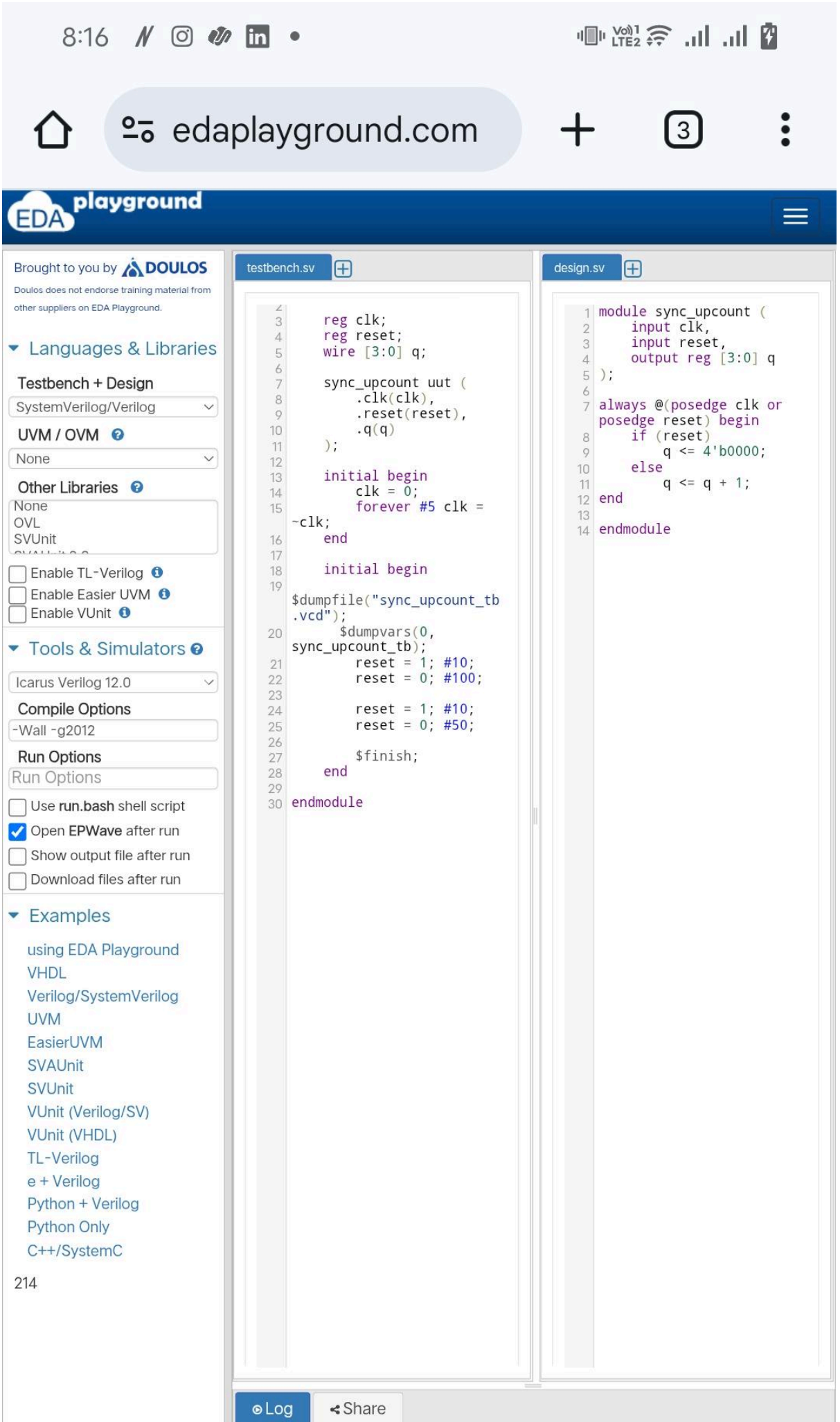
4 bit synchronous up counter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214
testbench.sv
reg clk;
reg reset;
wire [3:0] q;
sync_upcount uut (
.clk(clk),
.reset(reset),
.q(q)
);
initial begin
clk = 0;
forever #5 clk = ~clk;
end
initial begin
$dumpfile("sync_upcount_tb.vcd");
$dumpvars(0, sync_upcount_tb);
reset = 1; #10;
reset = 0; #100;
reset = 1; #10;
reset = 0; #50;
$finish;
end
endmodule
design.sv
module sync_upcount (
input clk,
input reset,
output reg [3:0] q
);
always @(posedge clk or posedge reset) begin
if (reset)
q <= 4'b0000;
else
q <= q + 1;
end
endmodule
Log
Share

8:16

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EDA playground

EPWave

From:

0s

To:

170s

Instructions: x

Click on an edge to display a cursor. CTRL-click on another edge to display a second cursor.
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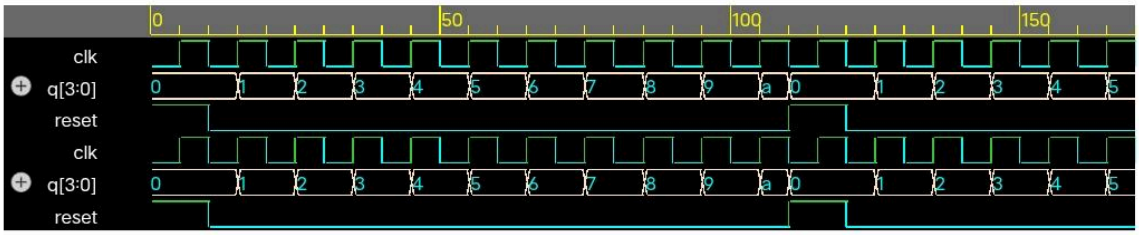

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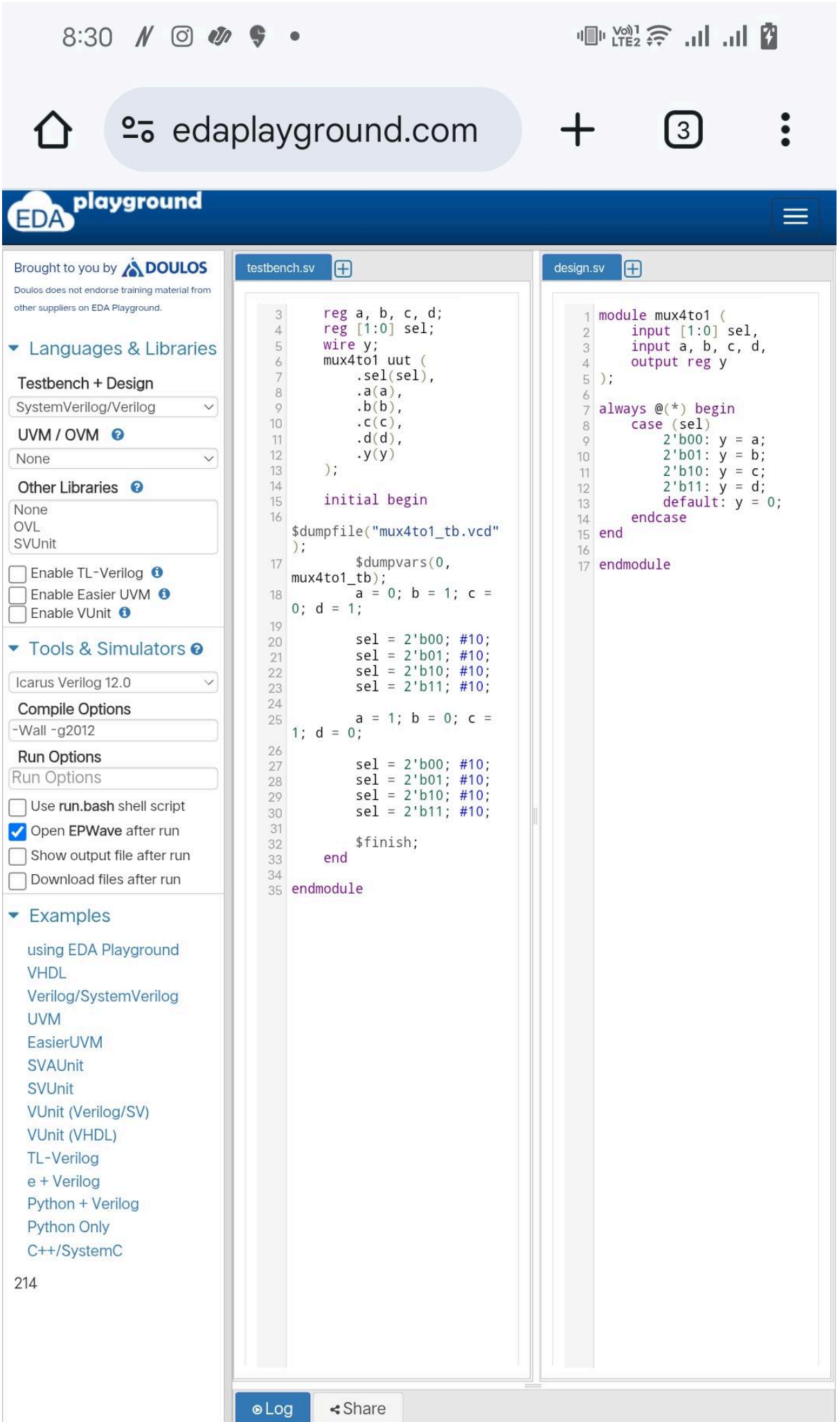
4:1 mux behavioural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Python + Verilog
Python Only
C++/SystemC
214
testbench.sv
reg a, b, c, d;
reg [1:0] sel;
wire y;
mux4to1 uut (
.sel(sel),
.a(a),
.b(b),
.c(c),
.d(d),
.y(y)
);
initial begin
$dumpfile("mux4to1_tb.vcd");
$dumpvars(0, mux4to1_tb);
a = 0; b = 1; c = 0; d = 1;
sel = 2'b00; #10;
sel = 2'b01; #10;
sel = 2'b10; #10;
sel = 2'b11; #10;
a = 1; b = 0; c = 1; d = 0;
sel = 2'b00; #10;
sel = 2'b01; #10;
sel = 2'b10; #10;
sel = 2'b11; #10;
$finish;
end
endmodule
design.sv
module mux4to1 (
input [1:0] sel,
input a, b, c, d,
output reg y
);
always @(*) begin
case (sel)
2'b00: y = a;
2'b01: y = b;
2'b10: y = c;
2'b11: y = d;
default: y = 0;
endcase
end
endmodule
Log
Share

8:29

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EDA playground

EPWave

From:

0s

To:

80s

Instructions: x

Click on an edge to display a cursor. CTRL-click on another edge to display a second cursor.
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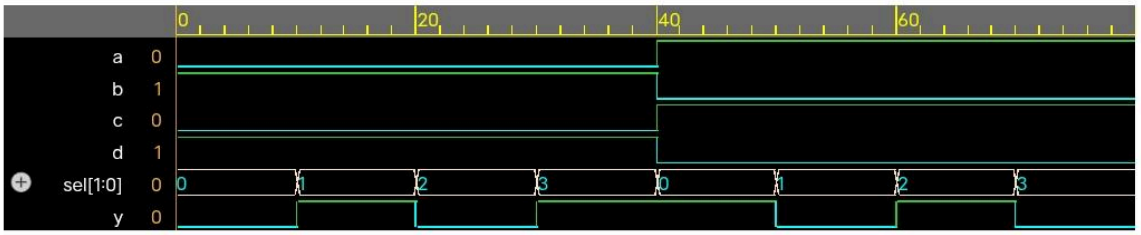

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