

3 to 8 decoder



playground

Brought to you by **DOULOS**
Doulos does not endorse training material from other suppliers on EDA Playground.

Languages & Libraries

Testbench + Design: SystemVerilog/Verilog

UVM / OVM: None

Other Libraries: None, OVL, SVUnit

Enable TL-Verilog

Enable Easier UVM

Enable VUnit

Tools & Simulators

Icarus Verilog 12.0

Compile Options: -Wall -g2012

Run Options: Run Options

Use run.bash shell script

Open EPWave after run

Show output file after run

Download files after run

Examples

using EDA Playground
VHDL
Verilog/SystemVerilog
UVM
EasierUVM
SVAUnit
SVUnit
VUnit (Verilog/SV)
VUnit (VHDL)
TL-Verilog
e + Verilog
Python + Verilog
Python Only
C++/SystemC

testbench.sv

```
1 module
2   decoder3to8_df_tb();
3   reg a, b, c;
4   wire d0, d1, d2, d3, d4,
5       d5, d6, d7;
6   decoder3to8_df dut(a, b,
7       c, d0, d1, d2, d3, d4, d5,
8       d6, d7);
9   initial begin
10    $dumpfile("decoder3to8_df.
11    vcd");
12    $dumpvars(0,
13      decoder3to8_df_tb);
14    $monitor("t=%0t
15    abc=%b%b%b
16    | d0..d7=%b%b%b%b%b%b%b",
17    time, a, b,
18    c, d0, d1, d2, d3, d4, d5,
19    d6, d7);
20    {a,b,c}=3'b000; #10;
21    {a,b,c}=3'b001; #10;
22    {a,b,c}=3'b010; #10;
23    {a,b,c}=3'b011; #10;
24    {a,b,c}=3'b100; #10;
25    {a,b,c}=3'b101; #10;
26    {a,b,c}=3'b110; #10;
27    {a,b,c}=3'b111; #10;
28
29    $finish;
30  end
31
32 endmodule
```

design.sv

```
1 module decoder3to8_df(
2   input a, b, c,
3   output d0, d1, d2,
4   d3, d4, d5, d6, d7
5 );
6 assign d0 = ~a & ~b & ~c;
7 assign d1 = ~a & ~b & c;
8 assign d2 = ~a & b & ~c;
9 assign d3 = ~a & b & c;
10 assign d4 = a & ~b & ~c;
11 assign d5 = a & ~b & c;
12 assign d6 = a & b & ~c;
13 assign d7 = a & b & c;
14
15 endmodule
```

Log

Share

8:14



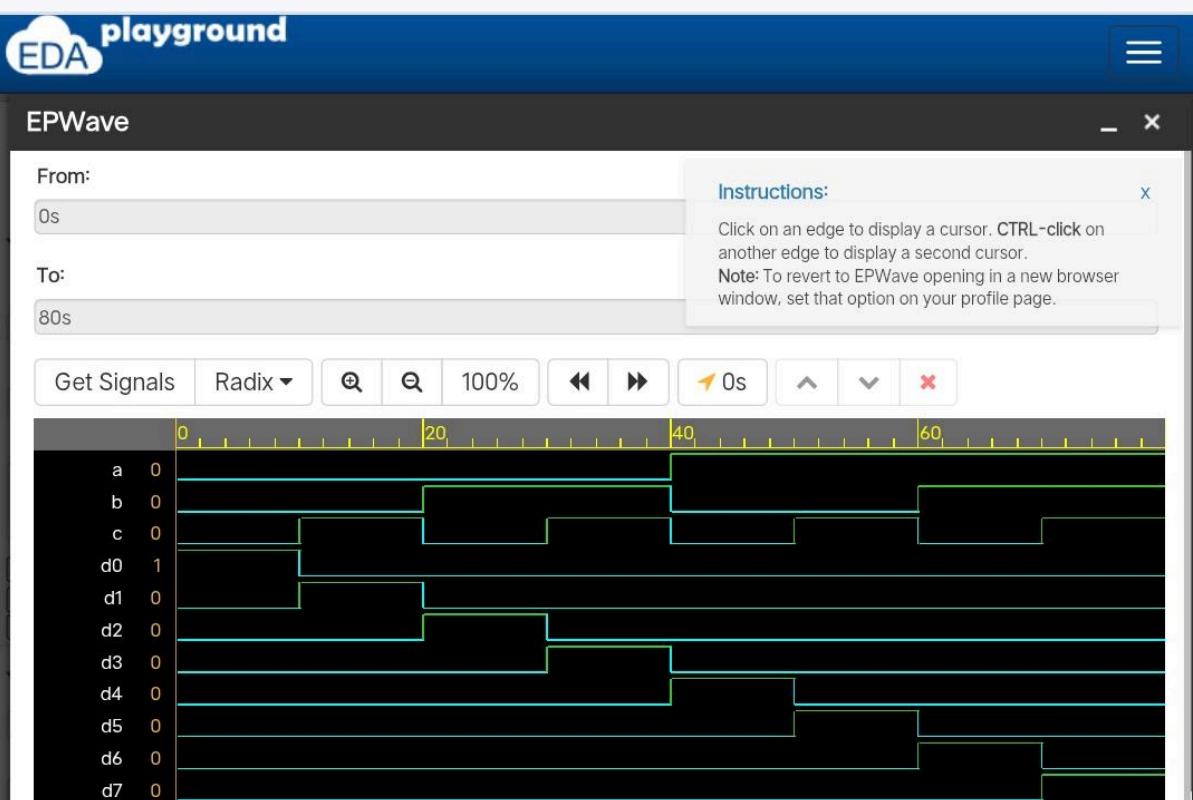
VoIP1 LTE2



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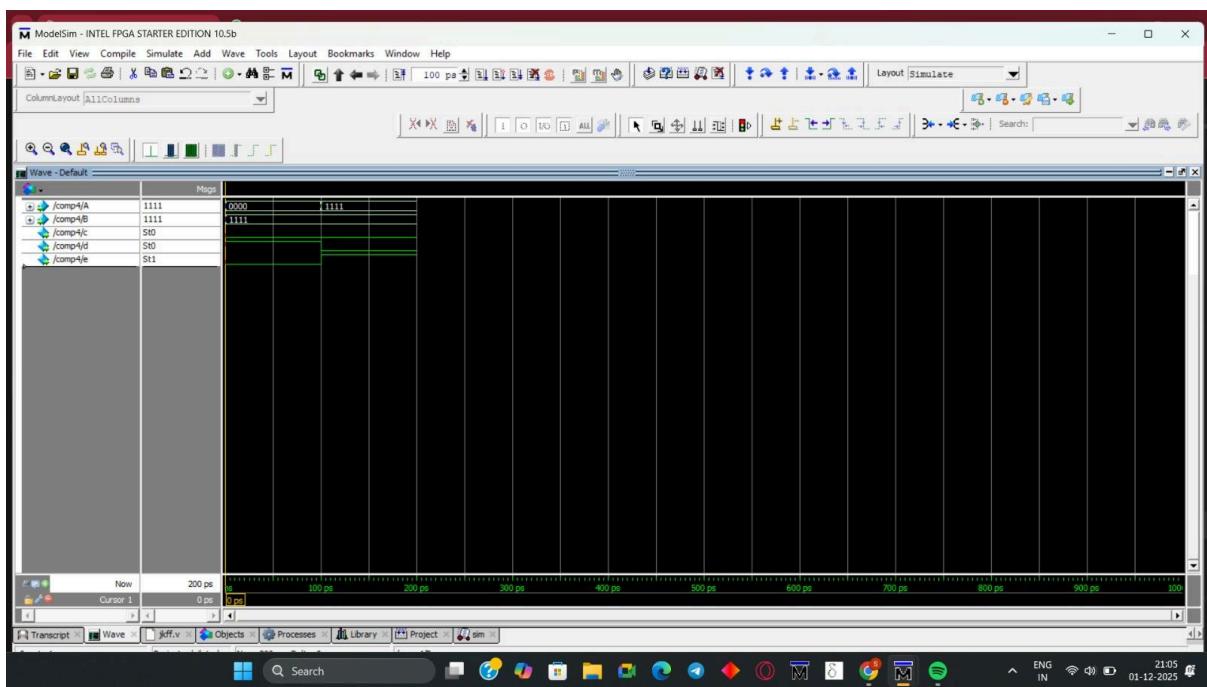
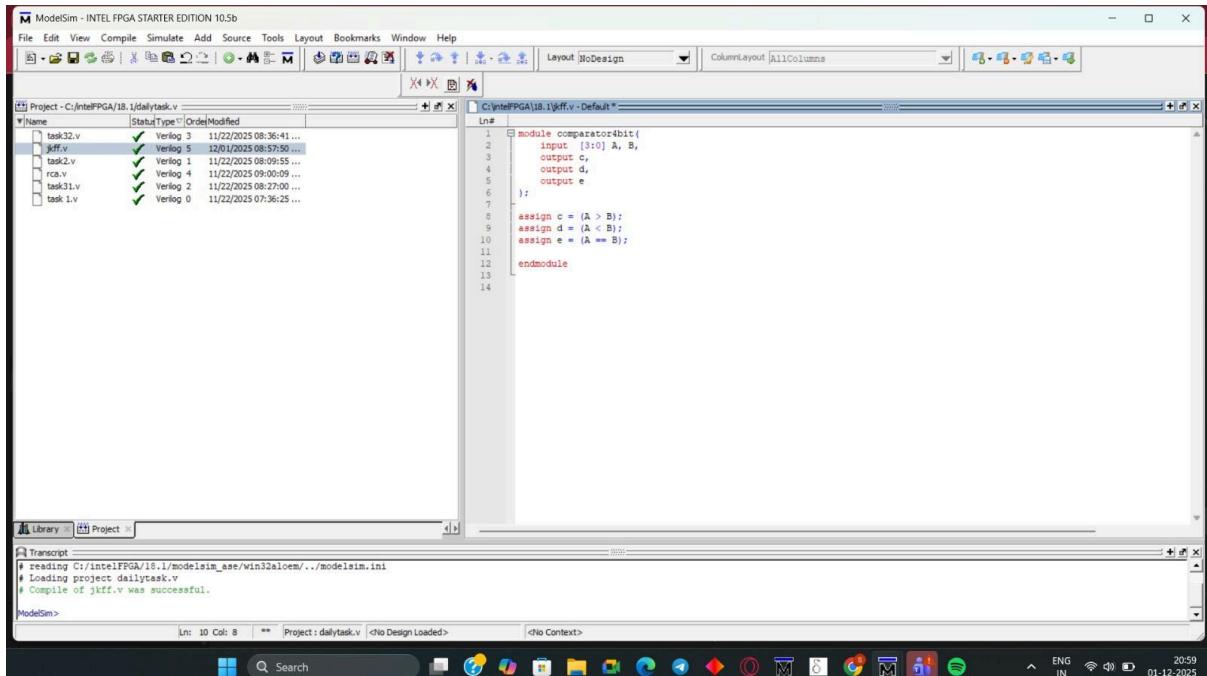


5



Note: To revert to EPWave opening in a new browser window, set that option on your profile page.

4 bit comparator



Jk ff

ModelSim - INTEL FPGA STARTER EDITION 10.5b

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

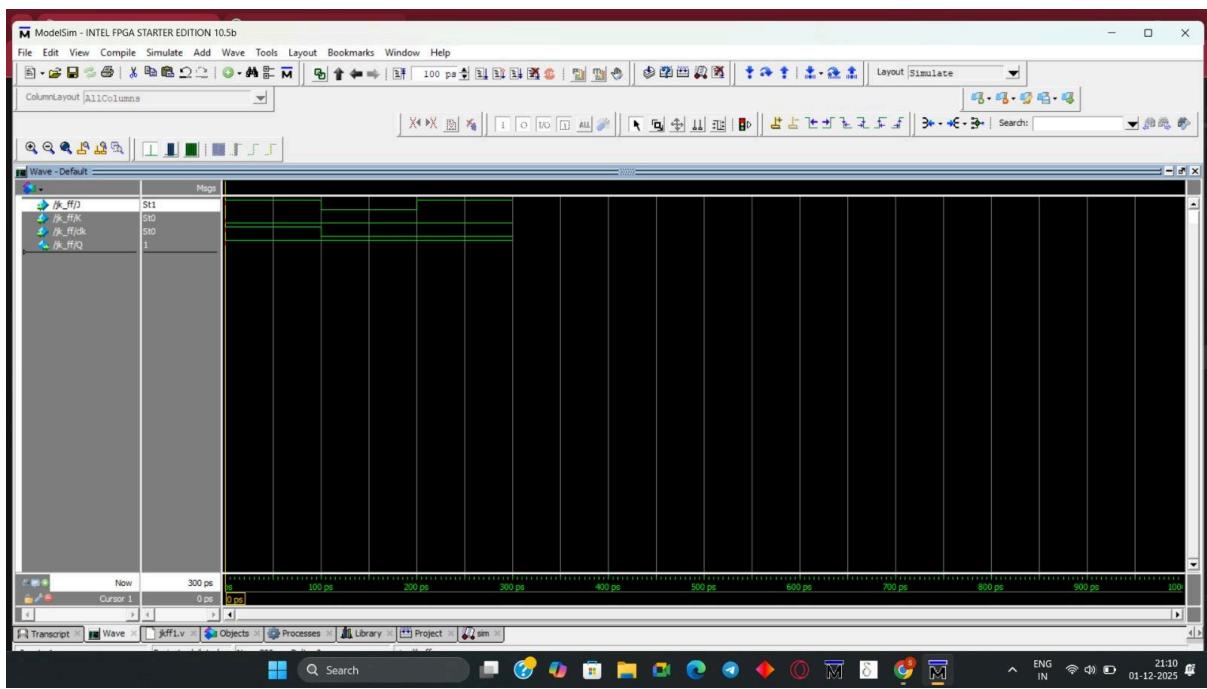
ColumnLayout [AllColumns]

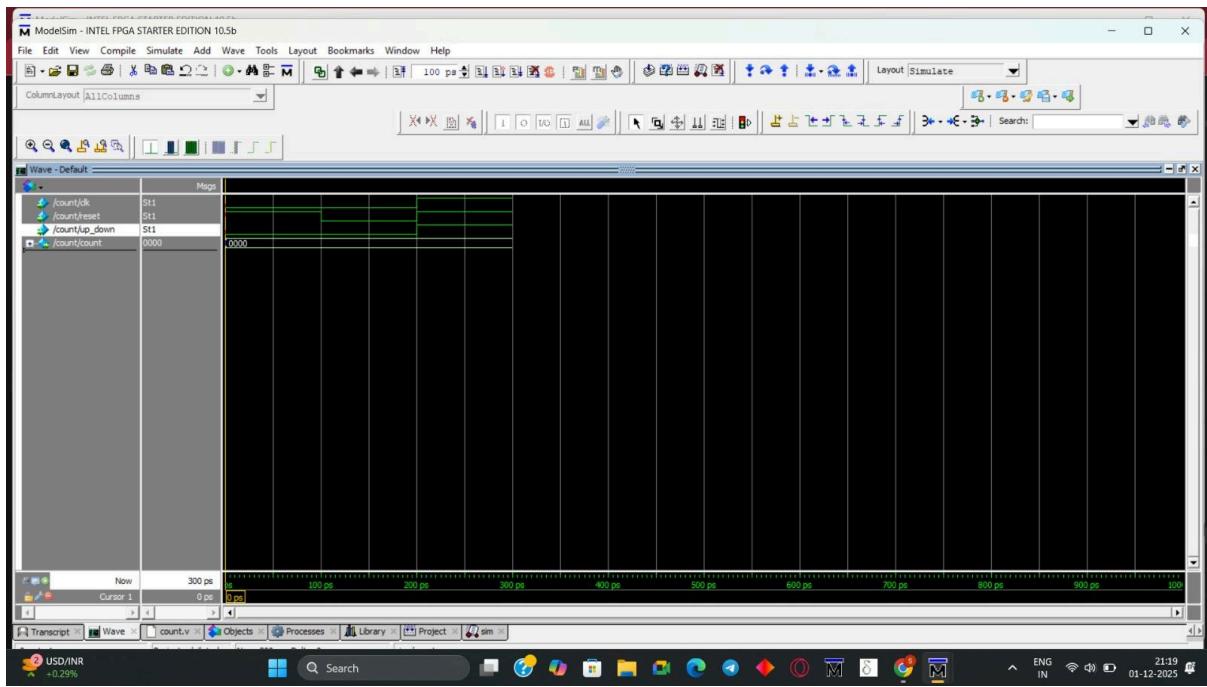
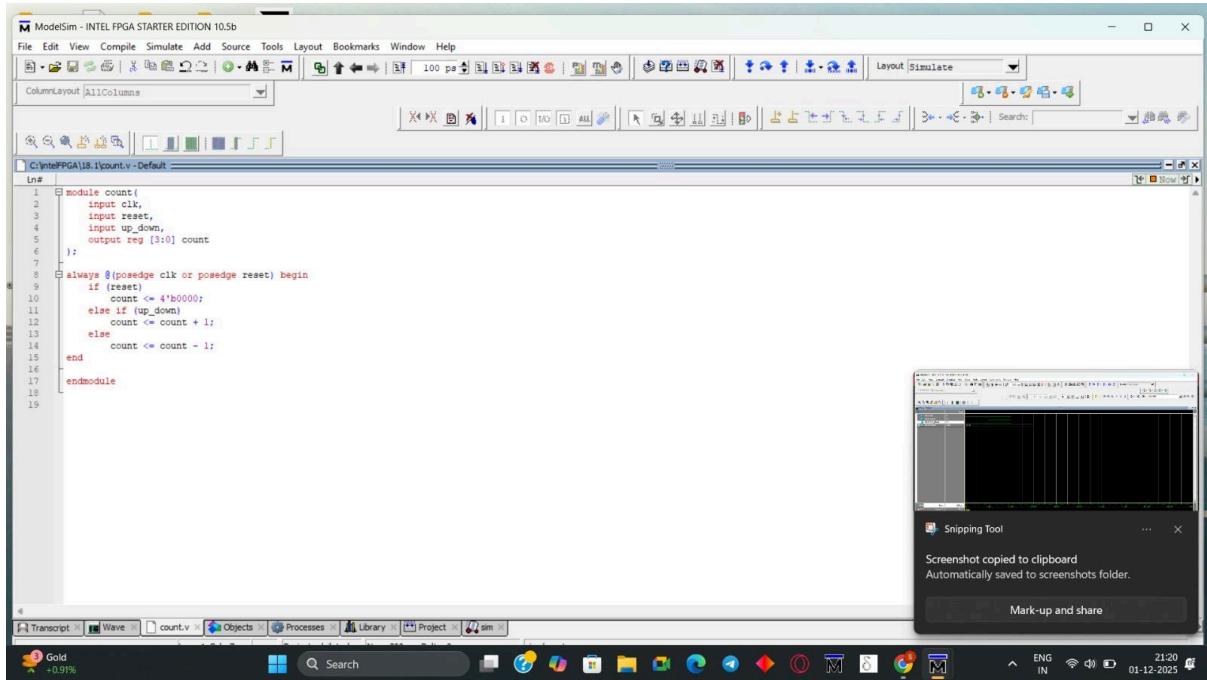
C:\IntelFPGA\18.1\jkff1.v (jk_ff) - Default

```
Ln# 1 module jk_ff();
2   input J, K, clk;
3   output reg Q;
4 endmodule
5
6 always @ (posedge clk) begin
7   case ({J,K})
8     2'b00: Q <= Q;
9     2'b01: Q <= 0;
10    2'b10: Q <= 1;
11    2'b11: Q <= ~Q;
12  endcase
13 end
14
15 endmodule
16
```

Transcript Wave Objects Processes Library Project sim

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Led code

```
int LED = 13;
int delay_value = 500;

void setup() {
    pinMode(LED, OUTPUT);
}

void loop() {
    digitalWrite(LED, HIGH);
```

```
delay(delay_value);

digitalWrite(LED, LOW);
delay(delay_value);
}
```