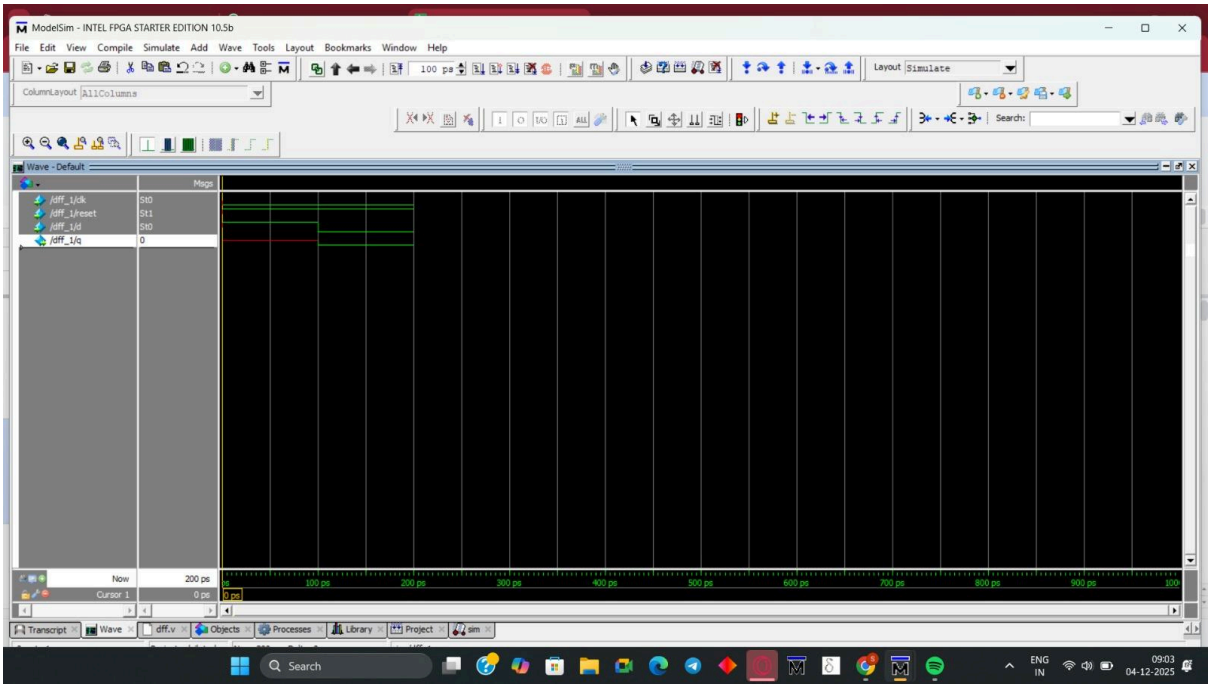
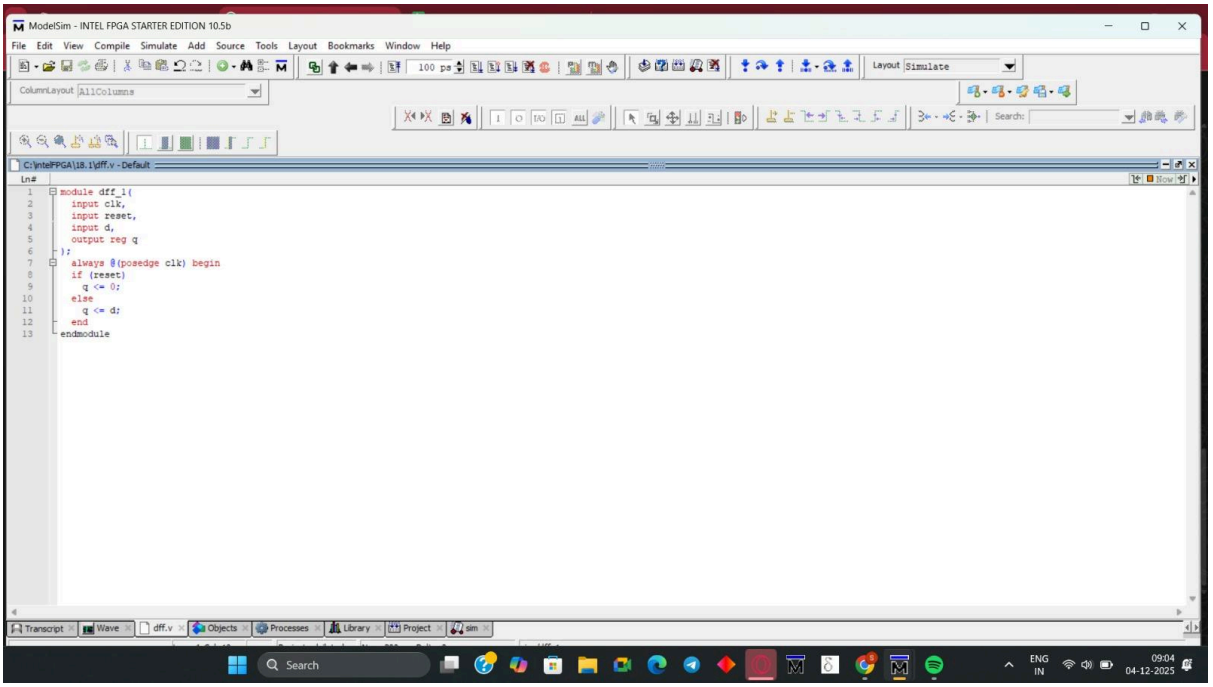
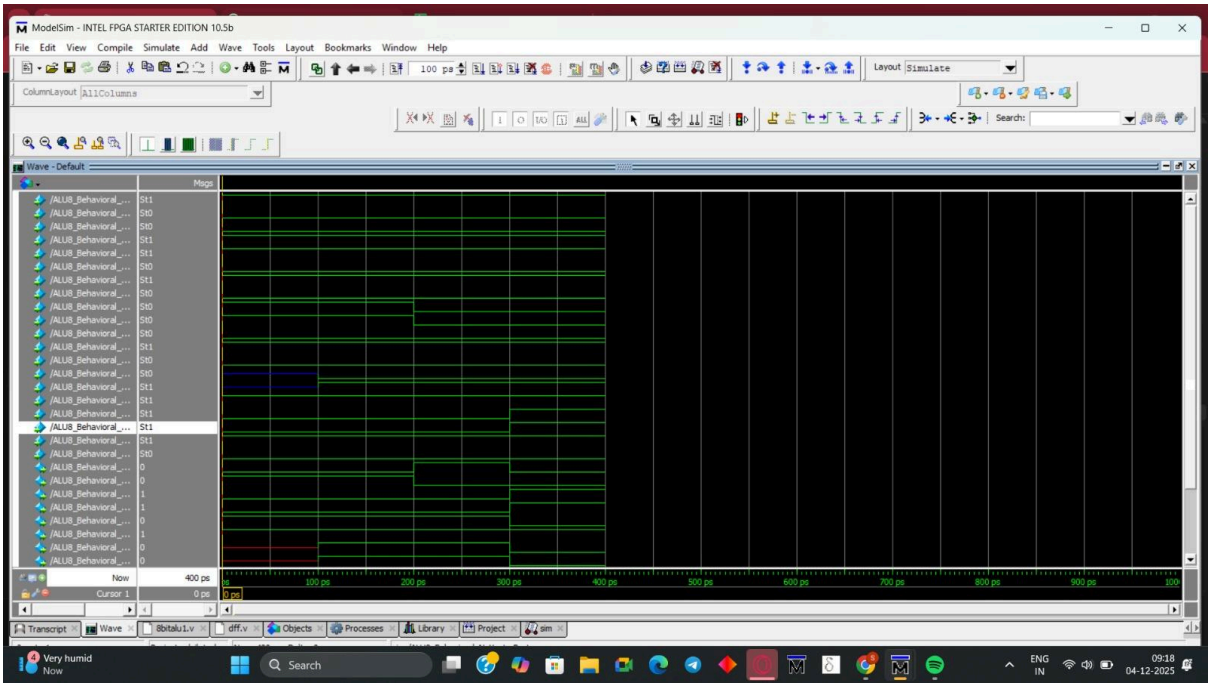
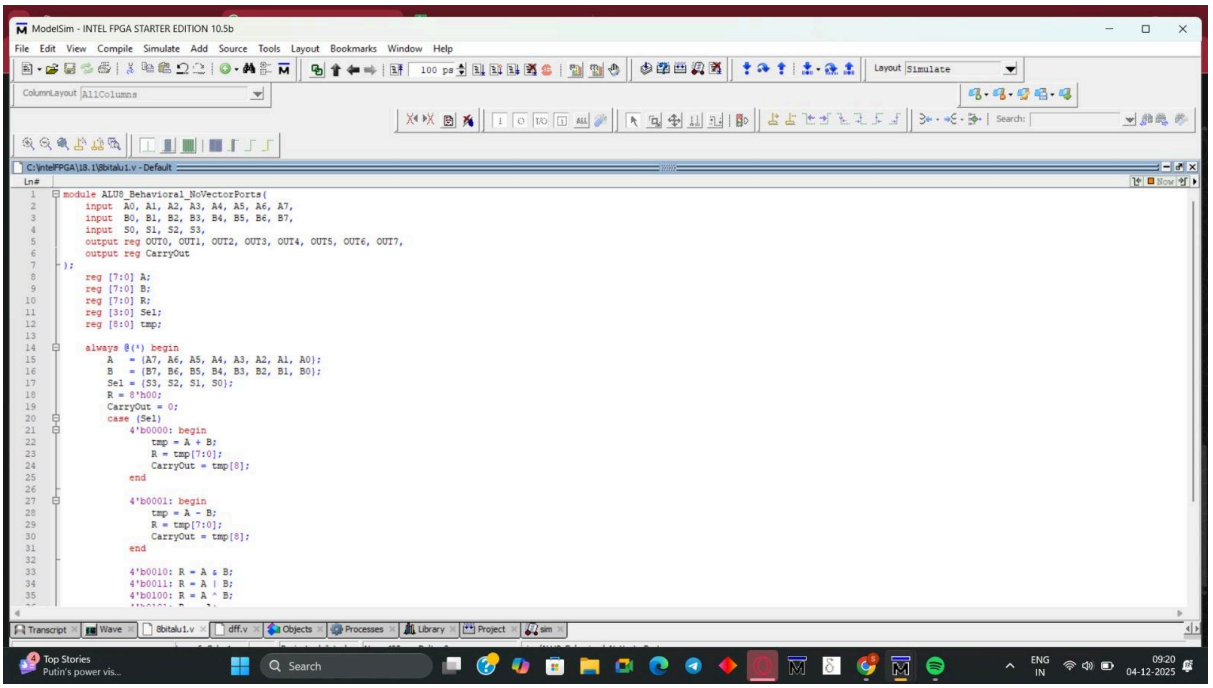
Dff


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
/dff_1/clk
/dff_1/reset
/dff_1/d
/dff_1/q
Now
Cursor 1
Transcript
Wave
dff.v
Objects
Processes
Library
Project
sim
Search
ENG
IN
09:03
04-12-2025

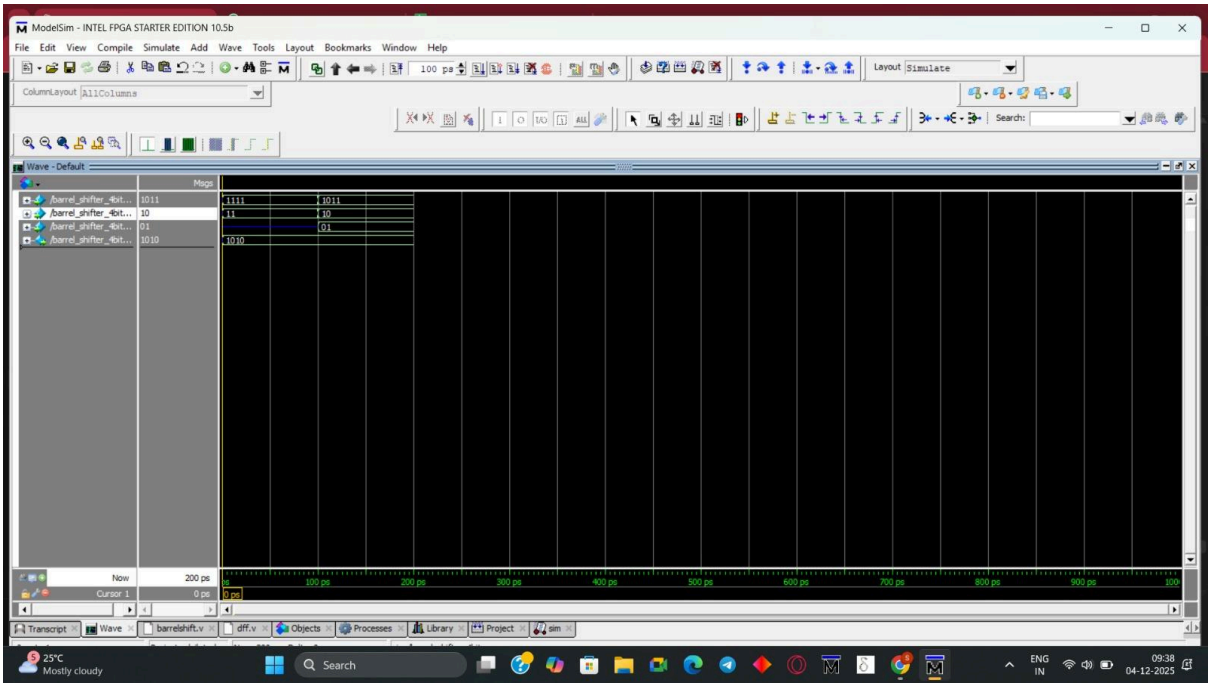

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
C:\intelFPGA\18.1\dff.v - Default
module dff_1(
input clk,
input reset,
input d,
output reg q
);
always @(posedge clk) begin
if (reset)
q <= 0;
else
q <= d;
end
endmodule
Transcript
Wave
dff.v
Objects
Processes
Library
Project
sim
Search
ENG
IN
09:04
04-12-2025

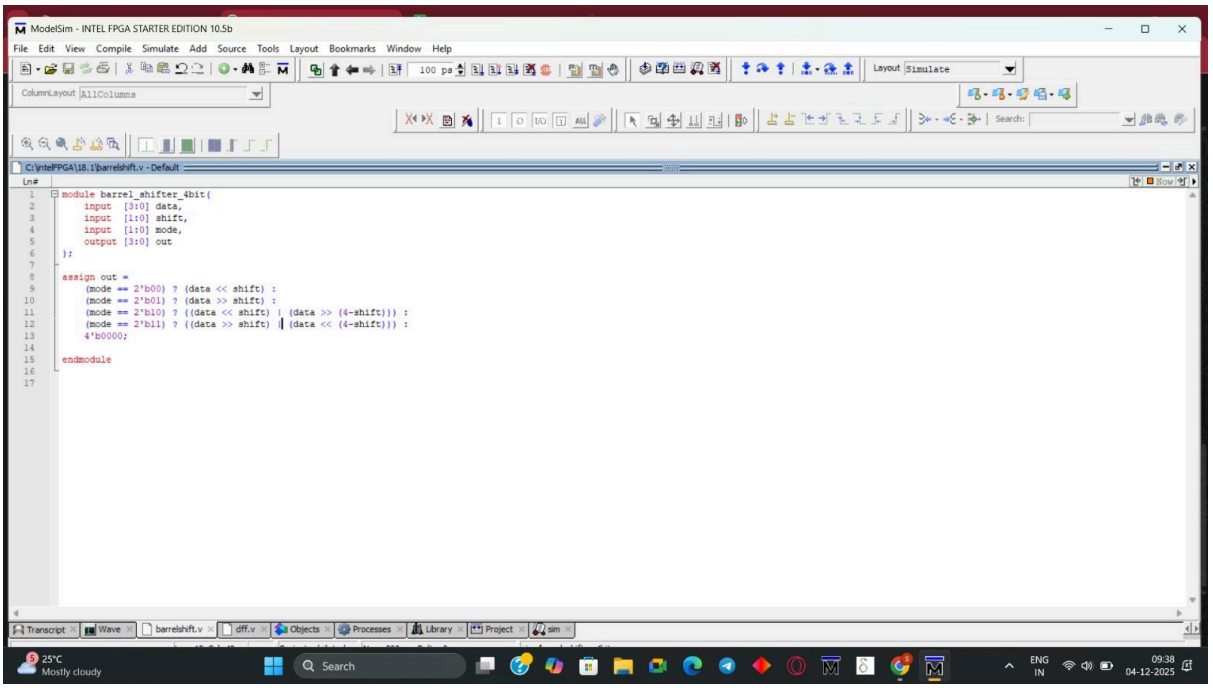
8 bit alu



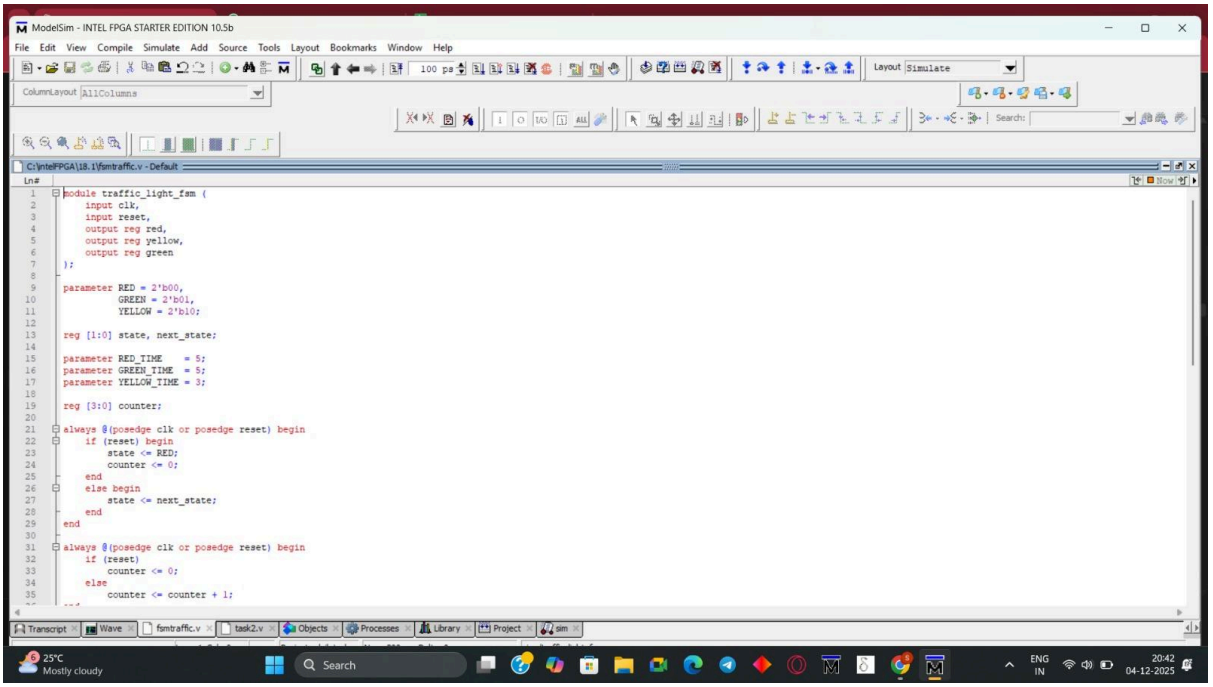


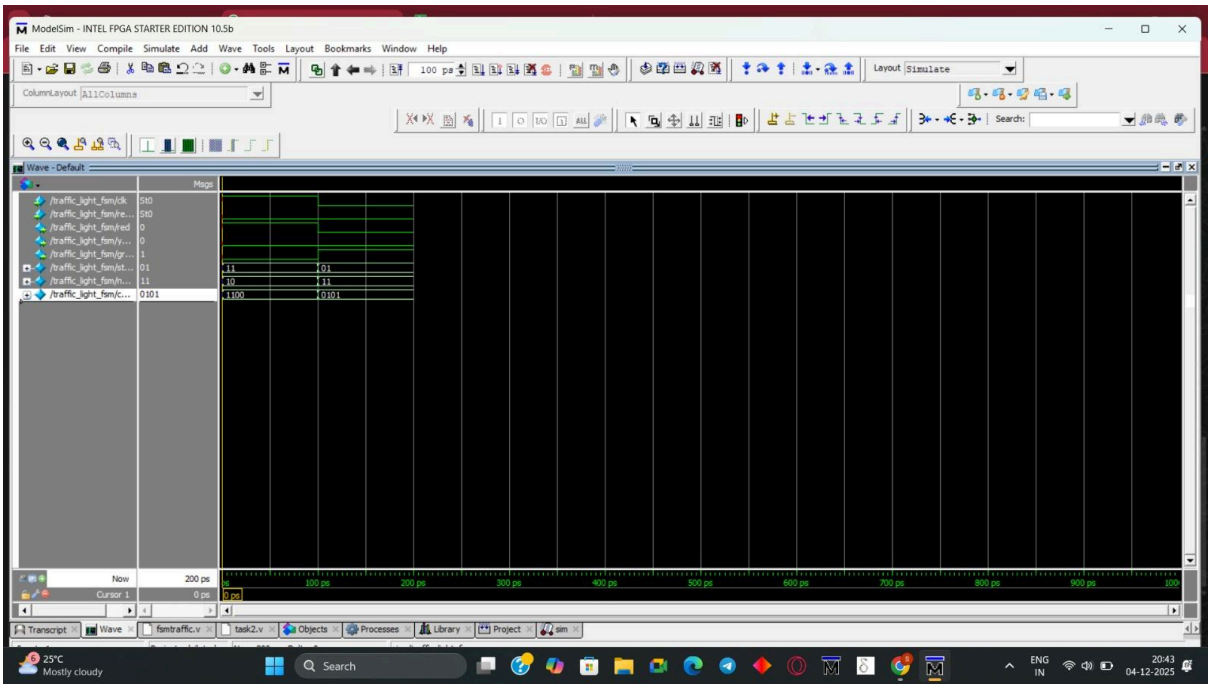
Barrel shift



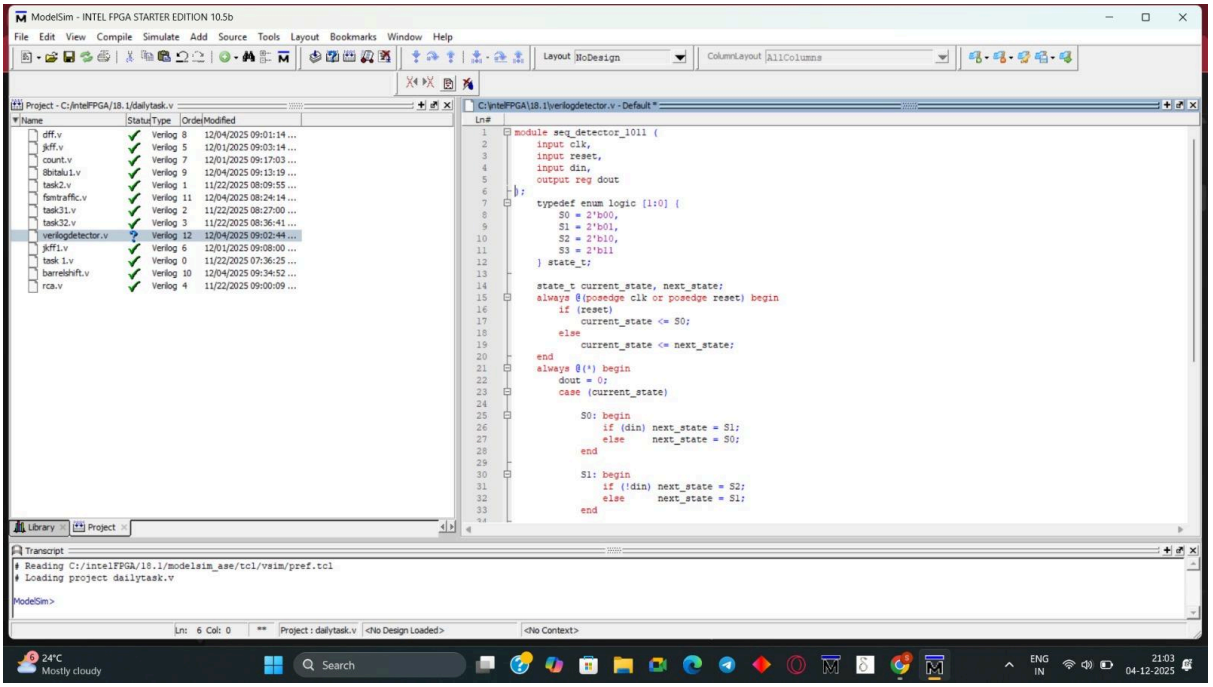


Traffic light fsm





Verilog sequence detector


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Project - C:/intelFPGA/18.1/dailytask.v
Name Status Type Order Modified
dff.v Verilog 8 12/04/2025 09:01:14 ...
jkff.v Verilog 5 12/01/2025 09:03:14 ...
count.v Verilog 7 12/01/2025 09:17:03 ...
8bitalu1.v Verilog 9 12/04/2025 09:13:19 ...
task2.v Verilog 1 11/22/2025 08:09:55 ...
fsmtraffic.v Verilog 11 12/04/2025 08:24:14 ...
task31.v Verilog 2 11/22/2025 08:27:00 ...
task32.v Verilog 3 11/22/2025 08:36:41 ...
verilogdetector.v Verilog 12 12/04/2025 09:02:44 ...
jkff1.v Verilog 6 12/01/2025 09:08:00 ...
task 1.v Verilog 0 11/22/2025 07:36:25 ...
barrelshift.v Verilog 10 12/04/2025 09:34:52 ...
rca.v Verilog 4 11/22/2025 09:00:09 ...
Library
Project
C:\intelFPGA\18.1\verilogdetector.v - Default *
Ln#
1 module seq_detector_1011 (
2 input clk,
3 input reset,
4 input din,
5 output reg dout
6);
7 typedef enum logic [1:0] {
8 S0 = 2'b00,
9 S1 = 2'b01,
10 S2 = 2'b10,
11 S3 = 2'b11
12 } state_t;
13
14 state_t current_state, next_state;
15 always @(posedge clk or posedge reset) begin
16 if (reset)
17 current_state <= S0;
18 else
19 current_state <= next_state;
20 end
21 always @(*) begin
22 dout = 0;
23 case (current_state)
24
25 S0: begin
26 if (din) next_state = S1;
27 else next_state = S0;
28 end
29
30 S1: begin
31 if (!din) next_state = S2;
32 else next_state = S1;
33 end
Transcript
Reading C:/intelFPGA/18.1/modelsim_ase/tcl/vsim/pref.tcl
Loading project dailytask.v
ModelSim>
Ln: 6 Col: 0
Project : dailytask.v
<No Design Loaded>
<No Context>
24°C
Mostly cloudy
Search
ENG
IN
21:03
04-12-2025