# Lab Report: 04

# Course Code: CSE 430

# Topic: Control Logic

***Submitted By:***



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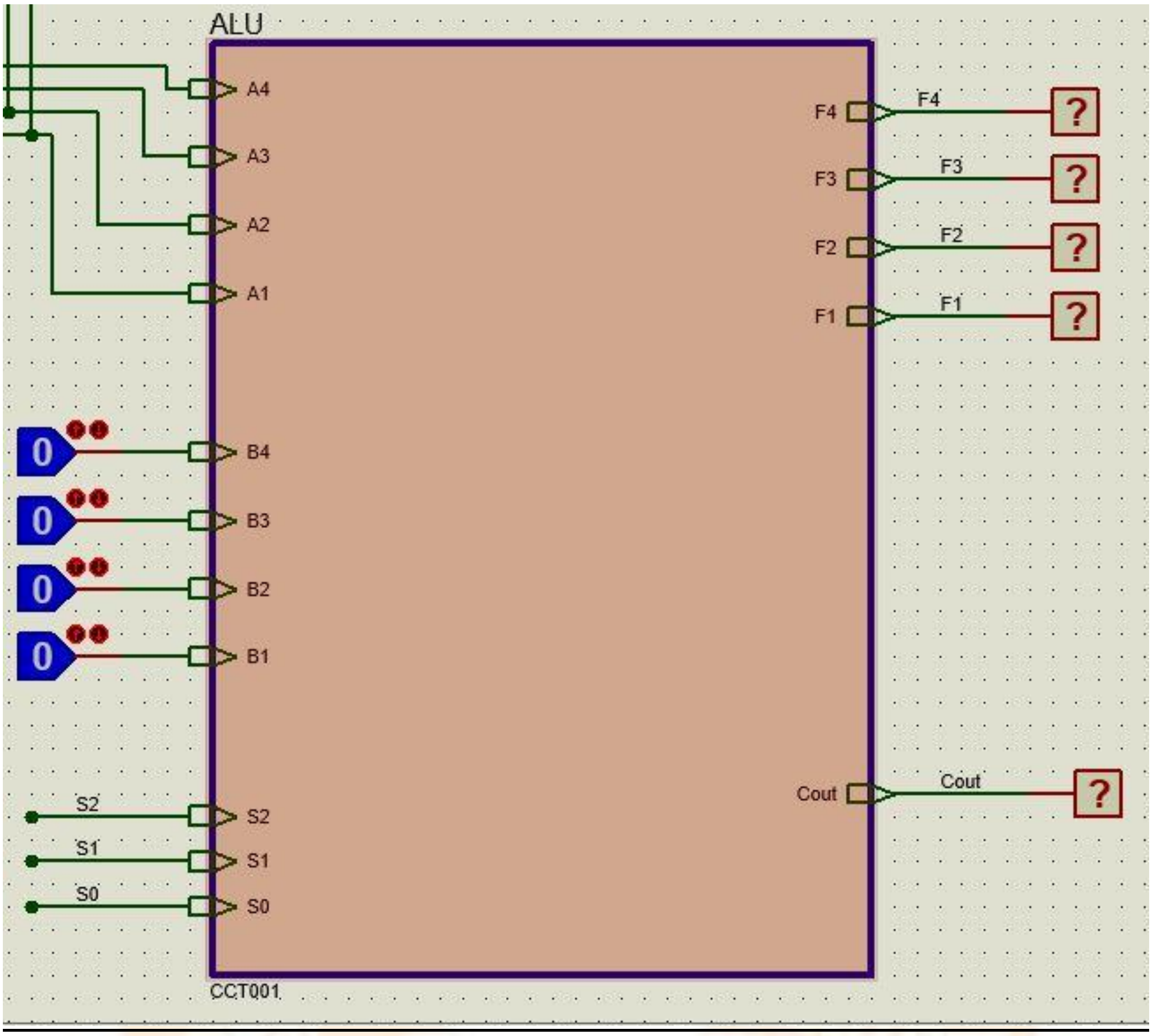
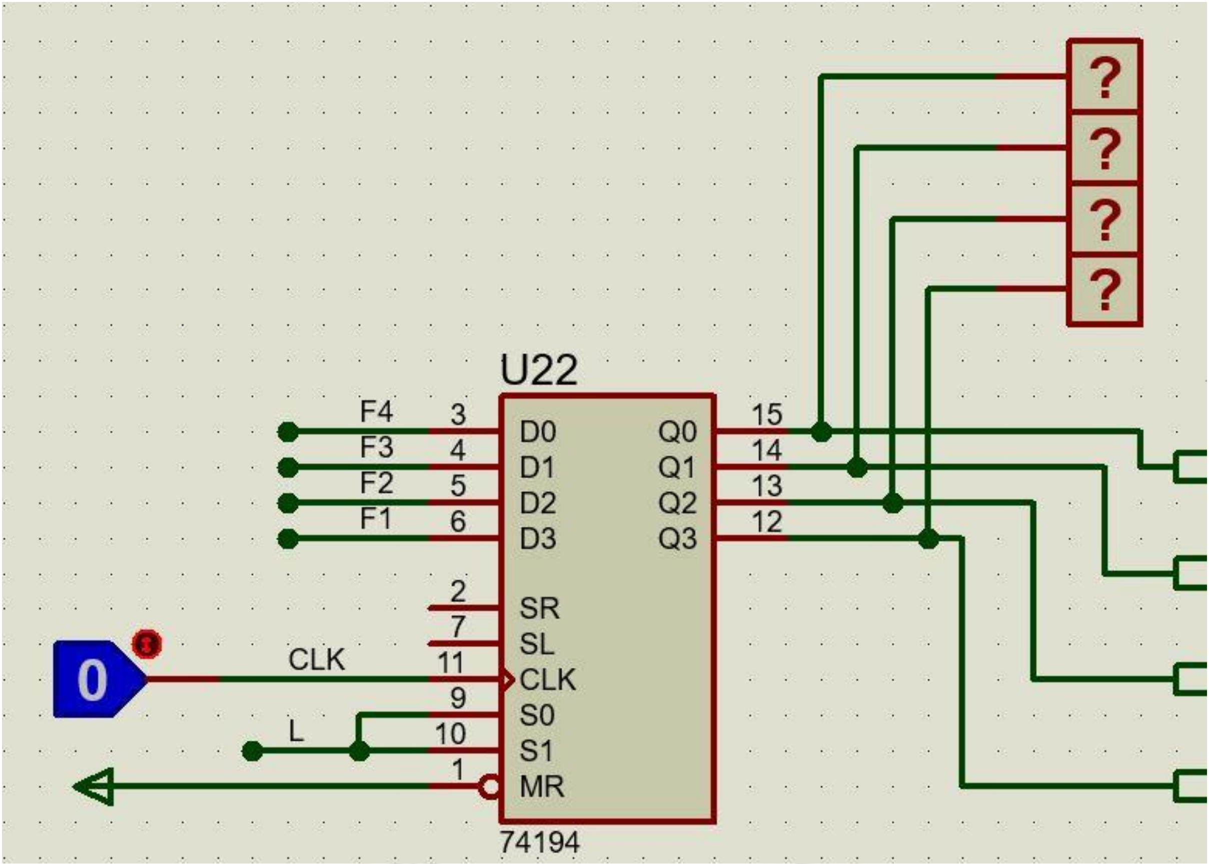
**Assignment Name:** Addition Subtraction of Signed Numbers

<u>Step 1: ALU Sub-circuit</u>



## Step 2: Accumulator Sub-circuit

We will be using a universal shift register (74194).




The shift register operates as follows-

$S_1S_0$ = 00 → Hold value

$S_1S_0$ = 11 → Parallel Load

Step 3: State transition

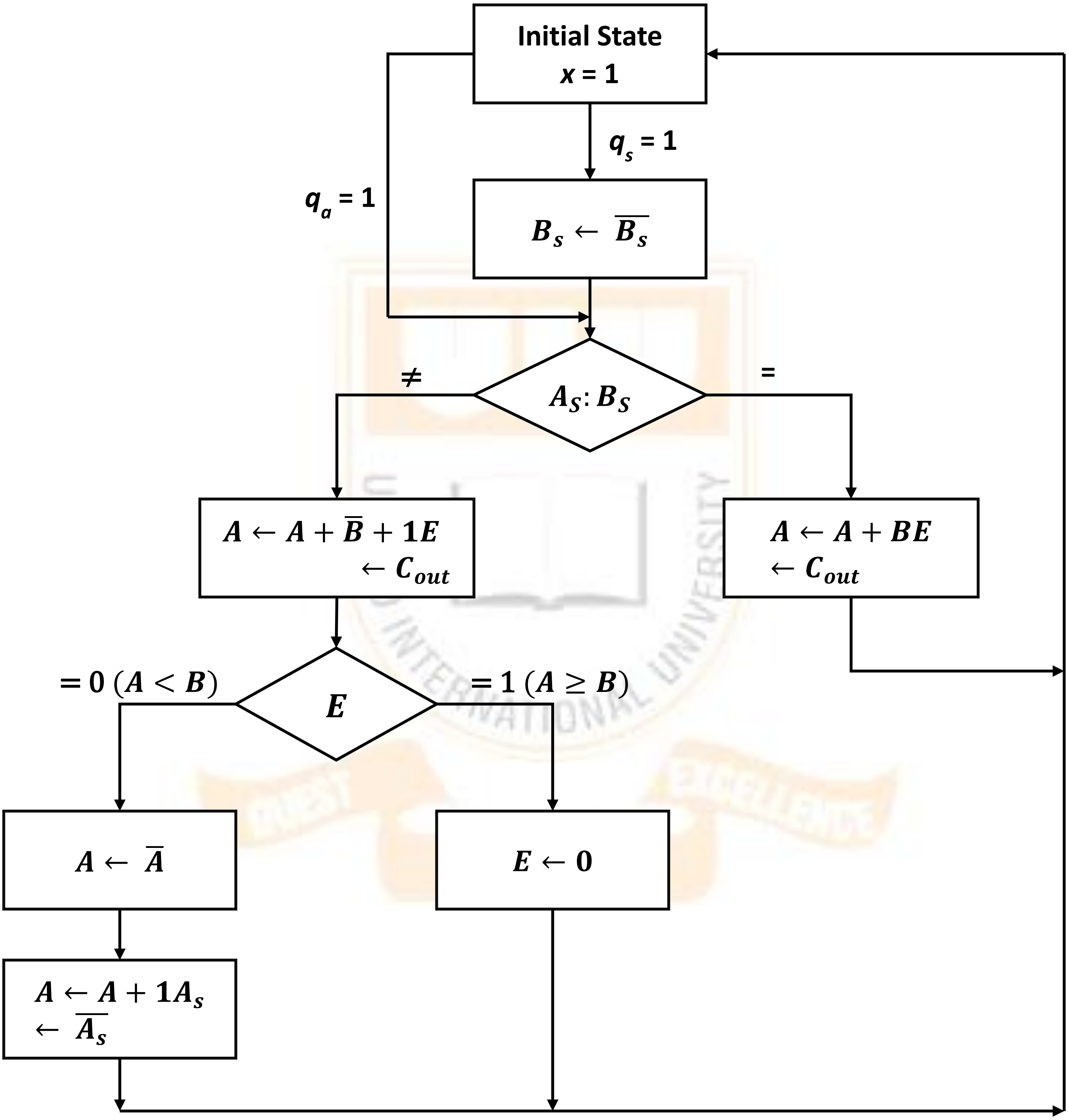
- **Derivation of algorithm:**

| | **if A ≥ B ($C_{out}$ =1)** | **if A < B ($C_{out}$= 0)** |
|---|---|---|
| (+A) + (+B) = + (A+B) | | |
| (+A) + (-B) = | + (A-B) | - (B-A) |
| (- A) + (+B) = | - (A-B) | + (B-A) |
| (- A) + (-B) = - (A+B) | | |

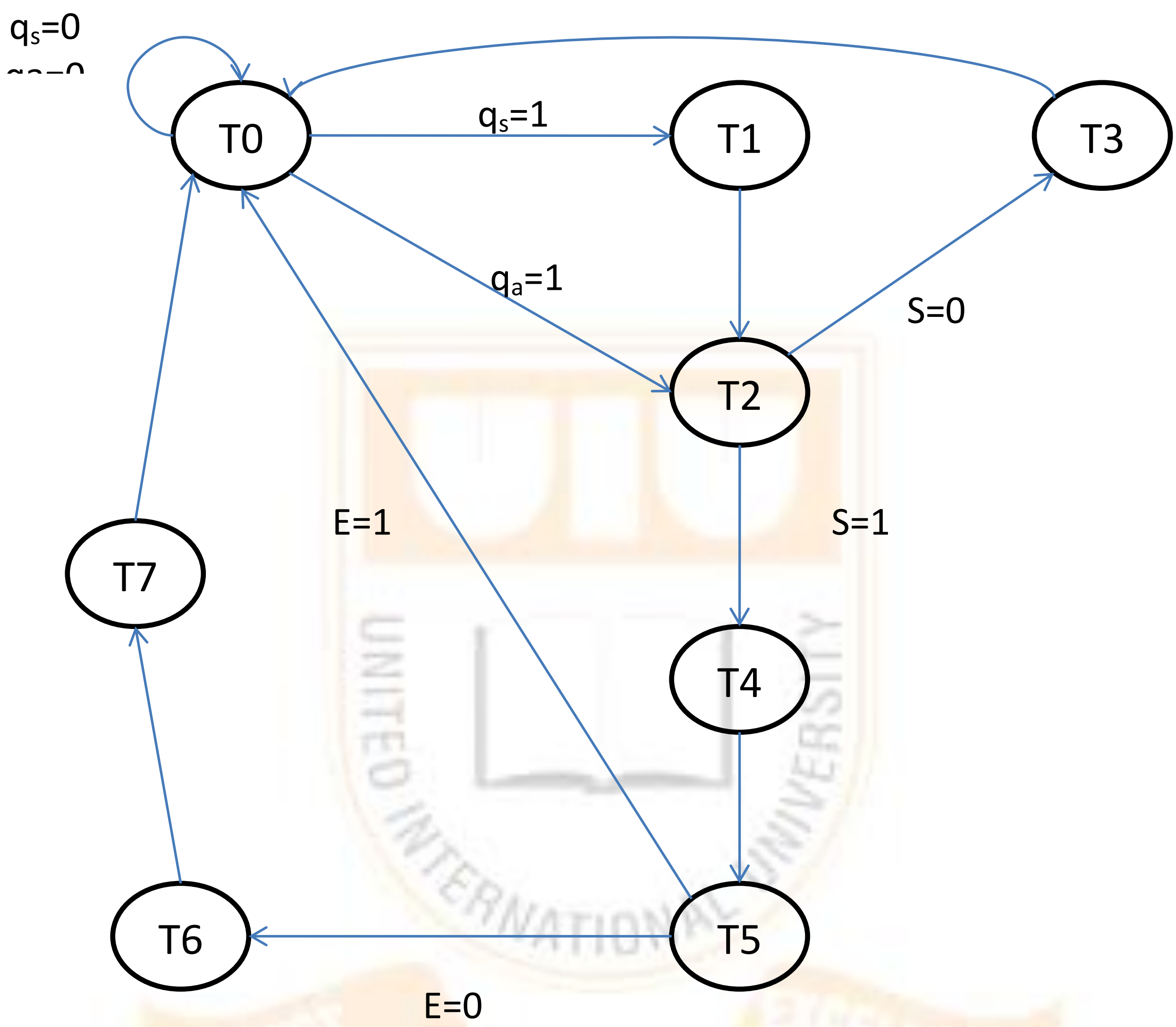
- **Algorithm:**

1. If subtraction, complement the sign of B
2. If the sign of A and B are equal- A = A + B, E = $C_{out}$ , end of process
3. Else –
   I. A = A – B, E = $C_{out}$
   II. Check if the result (A) is positive, if so set E = 0 and end
   III. Otherwise change A to –A by performing 2's complement. Also complement the sign of A, and end process.

- **Flowchart:**


Initial State
x = 1
q_s = 1
q_a = 1
B_s ← B̄_s
A_S: B_S
≠
=
A ← A + B̄ + 1E
← C_out
A ← A + BE
← C_out
E
= 0 (A < B)
= 1 (A ≥ B)
A ← Ā
E ← 0
A ← A + 1A_s
← Ā_s

- **State Diagram:**



- **Control Signal:**

| | X | S2 | S1 | S0 | Cin | L | y | z | w |
|---|---|---|---|---|---|---|---|---|---|
| T0:Ininitial state x=1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| T1: $B_s = B_s'$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| T2: nothing | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| T3: A =A+B $E=C_{out}$ | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| T4: A+B'+1 $E=C_{out}$ | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| T5: E=0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| T6: A=A' | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| T7:A=A+1 $A_s=A_s'$ | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |

| Flip-flop input functions | Output control functions |
|---|---|
| $DT_0 = q_a'q_s'T_0 + T_3 + ET_5 + T_7$ | $x = T_0$ |
| $DT_1 = q_sT_0$ | $s_2 = T_6$ |
| $DT_2 = q_aT_0 + T_1$ | $s_1 = T_3 + T_4$ |
| $DT_3 = S'T_2$ | $s_0 = T_3 + T_6$ |
| $DT_4 = ST_2$ | $L = T_3 + T_4 + T_6 + T_7$ |
| $DT_5 = T_4$ | $y = T_1$ |
| $DT_6 = E'T_5$ | $z = T_7$ |
| $DT_7 = T_6$ | $w = T_5$ |

## Step 4: Implement transition logic:

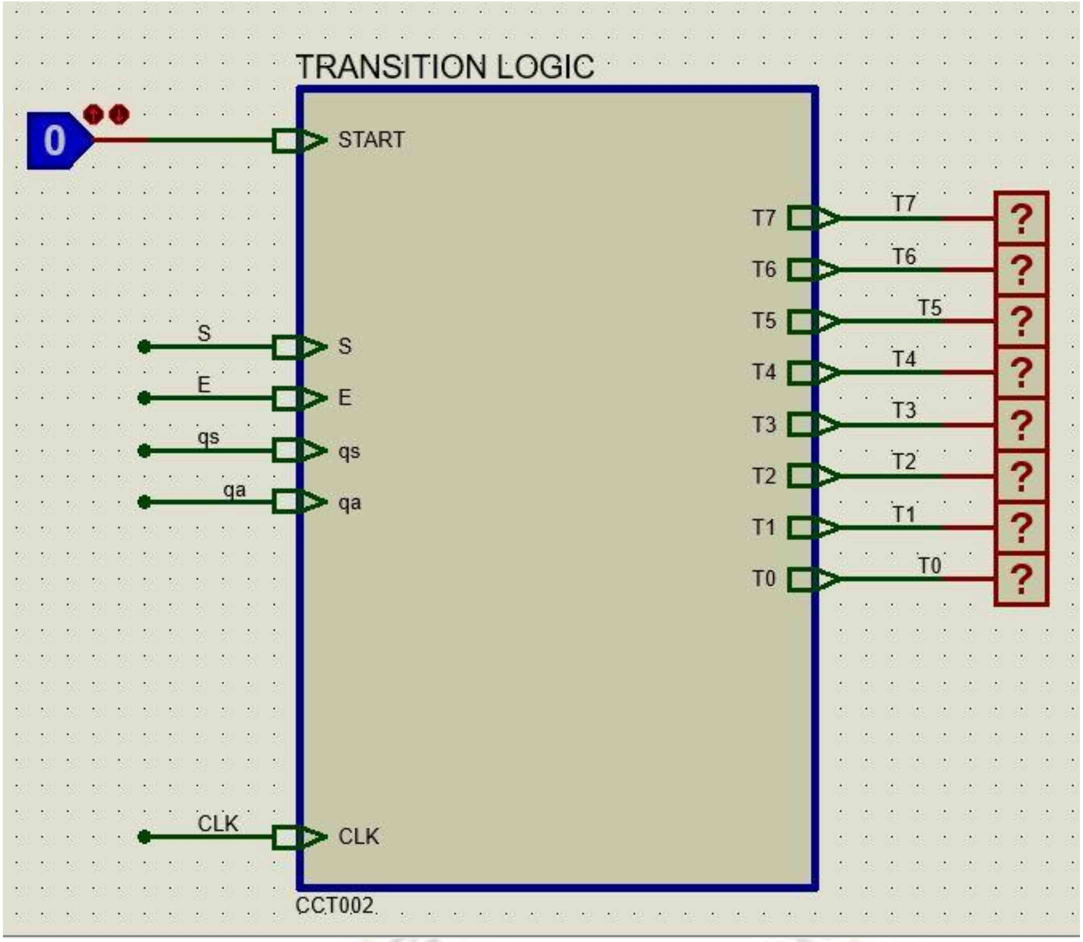



Fig: Transition Logic Parent Sheet

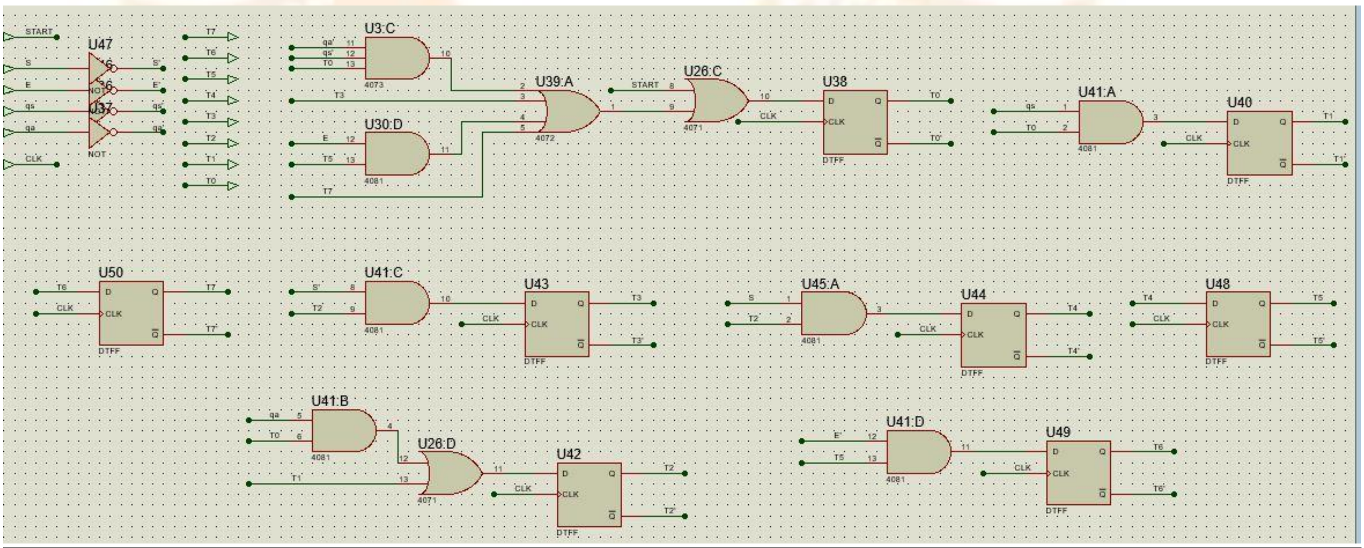
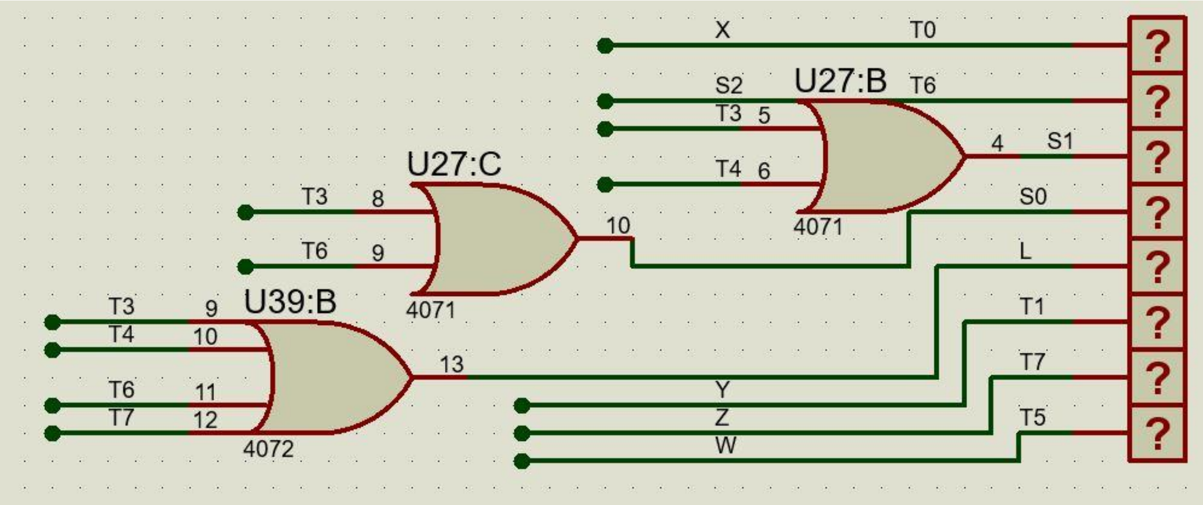



Fig: Transition Logic Child Sheet

## Step 5: Implement the control logic:




## Step 6: Implement $A_S$, $B_S$ and E:

| Signal | $JA_s$ | $KA_s$ |
|---|---|---|
| x = 1 | Input | Input' |
| z = 1 | 1 | 1 |
| $JA_s$ = xInput + z<br>$KA_s$ = xInput' + z | | |

| Signal | $JB_s$ | $KB_s$ |
|---|---|---|
| x = 1 | Input | Input' |
| y = 1 | 1 | 1 |
| $JB_s$ = xInput + y<br>$KB_s$ = xInput' + y | | |

| Signal | JE | KE |
|---|---|---|
| L = 1 | $C_{out}$ | $C_{out}'$ |
| w = 1 | 0 | 1 |
| JE = $LC_{out}$<br>KE = $LC_{out}'$ + w | | |

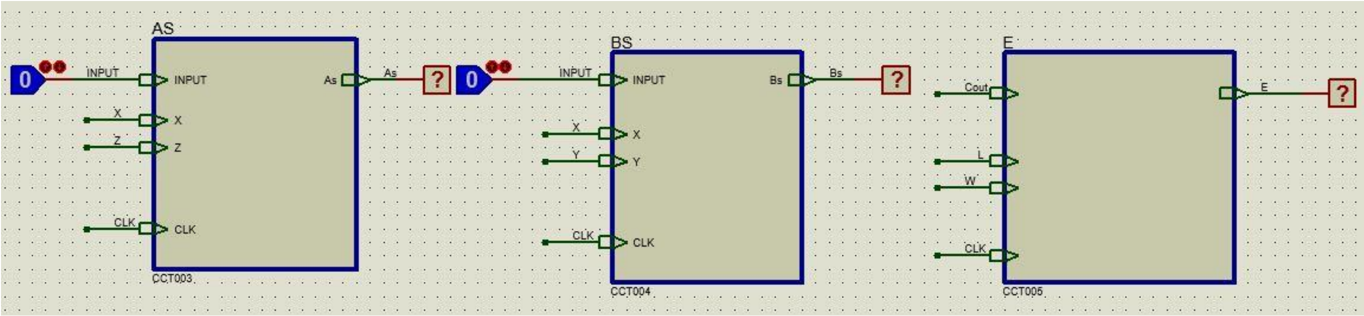



Fig: $A_s$, $B_s$ and E Parent Sheet

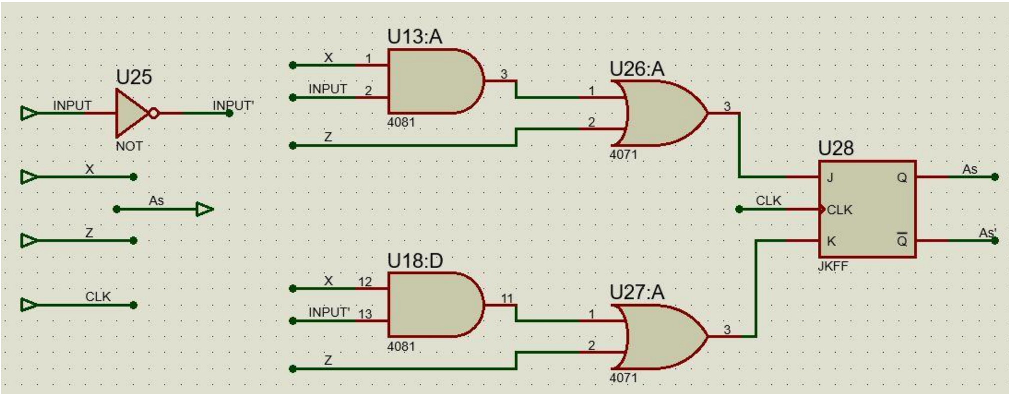



Fig: $A_s$ Child Sheet

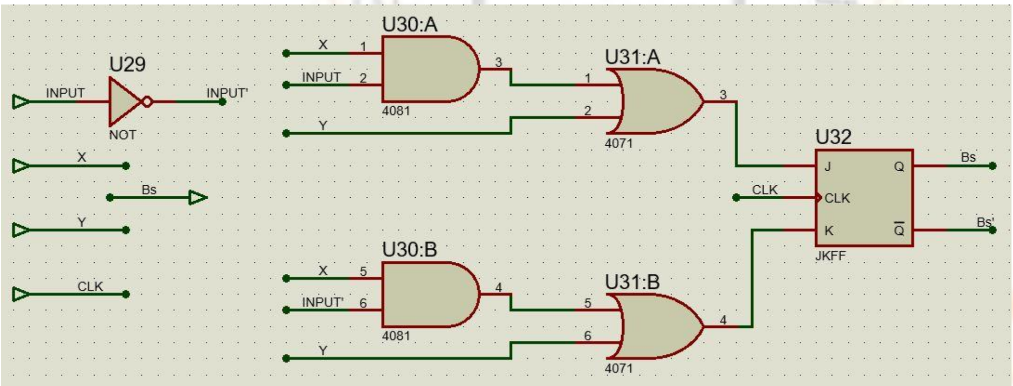



Fig: $B_s$ Child Sheet

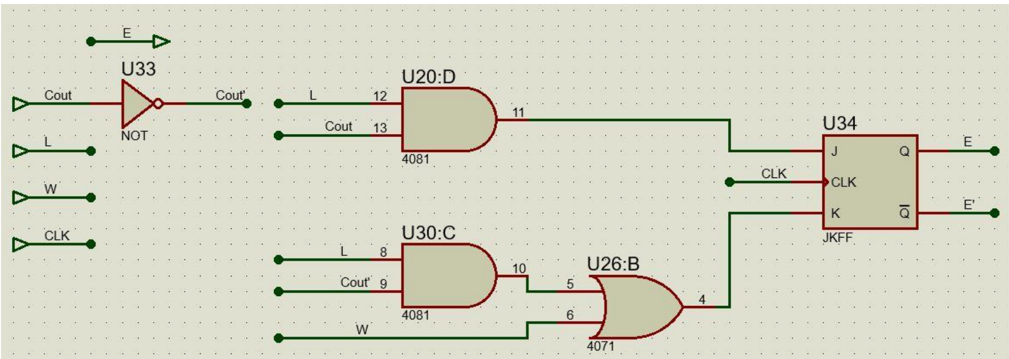



Fig: E Child Sheet

## Step 8: Final Step