

Microelectronics & VLSI

VLSI → Very Large Scale Integration

VLSI Technology, S. M Sze, McGraw Hill

VLSI Fabrication Principles, S. K Grandhi, Wiley

VLSI Design, Pucknell & Eshregian

Discrete circuit - A circuit which consists of discrete components such as resistors, capacitors & transistors etc.

Integrated circuit - In contrast, in an integrated circuit the entire circuit which contains active and passive elements is housed on the same substrate.

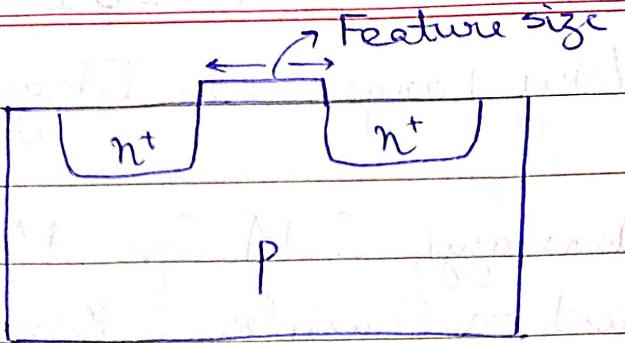
BJT vs MOSFET

Faster in application

Less power is consumed

Bi-CMOS - This is a hybrid VLSI technology which may have some active elements as BJT and some elements as FET wherever we require high speed functionality we put BJT active element & whenever we require high packing density & low power consumption we put CMOS.

Feature size



1. SSI - Small scale integration ($10 - 100$)

3 to 30 logic gates can be fabricated using $10 - 100$ transistors.

2. MSI - Medium scale integration ($100 - 1000$)

Flip flops, counters, adders, multipliers etc.

3. LSI - Large scale integration ($1000 - 10000$)

PLD Programmable logic device.

4. VLSI - Very large scale integration ($10000 - 100000$)

Complex PLD's

5. ULSI - Ultra large scale integration (10^6 to 10^7)

8 bit / 16 bit Microprocessors

6. GSI - Giga scale integration ($> 10^7$)

Pentium IV

The SSI, MSI, VLSI etc are process of integrating thousands of transistors on single semi conductor chip. They came into existence one after another as a result of technology advancement after 1970. As size of transistors reduced it became easier to integrate more & more transistors on a single chip.

Silicon is base for 95% of chips.

GaAs - Gallium arsenite

Greater than 95% chips are made of silicon due to its desirable characteristics & the years of consistent effort made by a large number of people over the years.

Theory proposed

Jack S. Kilby

Si MOSFET

1900 - 1910 - 1920 - 1930 - 1950 - 1960 + 1970

Triode, Diode
(1906)

MOSFET (1928)

IC (1958)

LST

oscillator

BJT (1947)

chip

Intel 4004

4-bit

Bardan & Schokly

- 1990 - 2000 - Present

VLSI VLSI GSI

Requirements

Low power consumption.

Speed, (High Speed).

High integration density.

Reliability

Moore's Feature Size is the minimum distance btw.

Source & drain on a MOS transistor or it is the half the distance between the cells in a DRAM chip.

Moore's law: So number of transistors on a chip doubles in a certain period of time for example: every 18 months in 1980's.

The device miniaturization results in reduced unit cost per junction and improved performance.

The cost per bit is decreasing because of miniaturization.

$$\text{Delay} \propto \frac{\text{Channel length}}{\text{Carrier velocity}}$$

As device dimension decreases the intrinsic switching times in MOSFET's decreases linearly.

Another benefit of miniaturization is reduced power consumption as device becomes smaller it consumes less power therefore device miniaturization also reduces energy used for each switching operation.

④ Crystal structure: $\text{Si} = \text{Ge}$ in zinc blende structure
 GaAs = InP = wurtzite structure

Si & GaAs have zinc blende structure.

In order to fabricate any device the requirement is a single crystal wafer. The structure of a Si crystal is given by zinc blende structure.

Si is a degenerate form of zinc blende structure also known as diamond lattice. There is no difference between two sub lattices which comprise of Si atom itself.

$$\left(\frac{1}{4}, \frac{1}{4}, \frac{1}{4} \right), \left(\frac{1}{4}, \frac{3}{4}, \frac{3}{4} \right), \left(\frac{3}{4}, \frac{3}{4}, \frac{1}{4} \right),$$

$$\left(\frac{3}{4}, \frac{1}{4}, \frac{3}{4} \right)$$

$$D = \sqrt{\left(\frac{1}{4}a - 0\right)^2 + \left(\frac{1}{4}a - 0\right)^2 + \left(\frac{1}{4}a - 0\right)^2}$$

$$D = \frac{\sqrt{3}}{4}a \quad \text{and radius } r_e = \frac{D}{2}$$

$$r_e = \frac{\sqrt{3}}{8}a$$

The total atoms in the zinc blende structure are :

$$\text{Corner atoms} = \frac{1}{8} \times 8 = 1$$

$$\text{Face atoms} = 6 \times \frac{1}{2} = 3$$

$$\text{Atoms on diagonal inside} = 4$$

$$V = 8 \times \frac{4}{3} \pi r_e^3$$

$$V = 8 \times \frac{4}{3} \pi \times \frac{3\sqrt{3}}{8 \times 64} \times a^3$$

$$V = \frac{\pi \sqrt{3} a^3}{16}$$

$$\text{Packing density} \Rightarrow V = \frac{\pi}{6} a^3 \approx 34.1\%$$

The packing density of the zinc blende structure can be calculated by dividing the volume occupied by all the contributing spheres by the volume of the cubic structure.

For FCC:

$$D = \sqrt{\left(\frac{a}{2}\right)^2 + \left(\frac{a}{2}\right)^2 + \left(\frac{a}{2}\right)^2}$$

$$D = \frac{a}{\sqrt{3}}$$

$$r = \frac{a}{2\sqrt{2}}$$

Total atoms = 4

$$\text{Volume of the cube} = V = 4 \times 4 \times \pi \times \frac{a^3}{16\sqrt{2}} = \pi a^3$$

$$= \frac{\pi a^3}{3\sqrt{2}}$$

$$\text{Packing density} = \frac{V}{a^3} = \frac{\pi}{3\sqrt{2}} = 74.1\%$$

The packing density of FCC structure is much more as compared to the zinc blende structure.

* In Blende :

$$V_0 = \frac{\sqrt{3}}{8} a^3$$

$$\text{Si, } a = 5.43 \text{ \AA}$$

$$r_0 \approx 1.18 \text{ \AA}$$

Impurities used: P As Sb B

$r_{\text{imp.}}$	→	1.1	1.18	1.36	0.88
ϵ	→	0.068	0	0.15	0.25

$\epsilon \rightarrow$ Misfit factor

$$r_0(1 + \epsilon) = r_{\text{imp.}}$$

n-p-n is preferred over p-n-p as Boron is difficult to dope heavily in Silicon due to high misfit factors.

The impurity atoms should replace Si atoms this is called substitutional introduction of dopants. Si has a particular tetrahedral radius. The impurity atom may or may not have same tetrahedral radius, which can result in strain in the lattice & will effect the electronic activity.

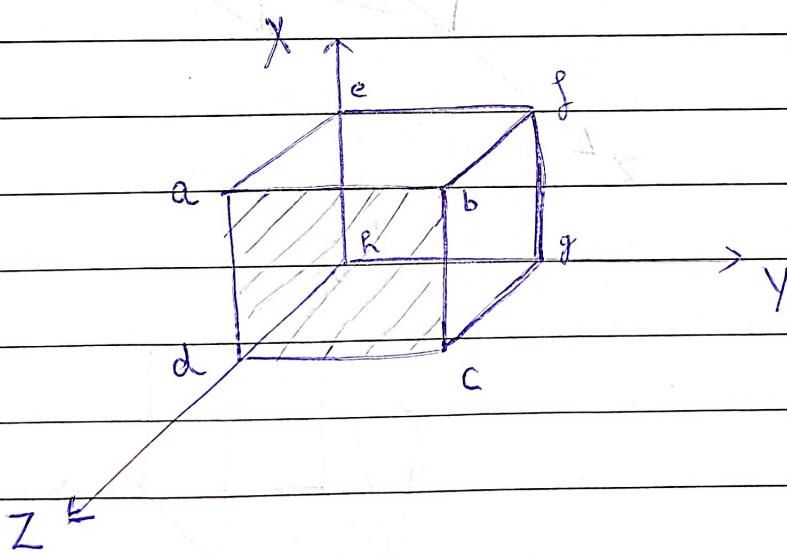
The dopants will contribute to the electronic activity only when they have substituted Si atoms.

The tetrahedral radius dictates dopants that how much electrically activated, the resulting structure is going to be. It is difficult to heavily dope Si p-type as compared to n⁺ region in the Silicon. So it is easier to fabricate a npn transistor than a pnp transistor. For IC's the npn transistor's are preferred.

④ Crystal planes or orientations :

{1, 0, 0} MOS

{1, 1, 1} BJT



$$\text{Eqn of a plane: } \frac{x}{a} + \frac{y}{b} + \frac{z}{c} = 1$$

$$a = \infty, b = \infty, c = 1$$

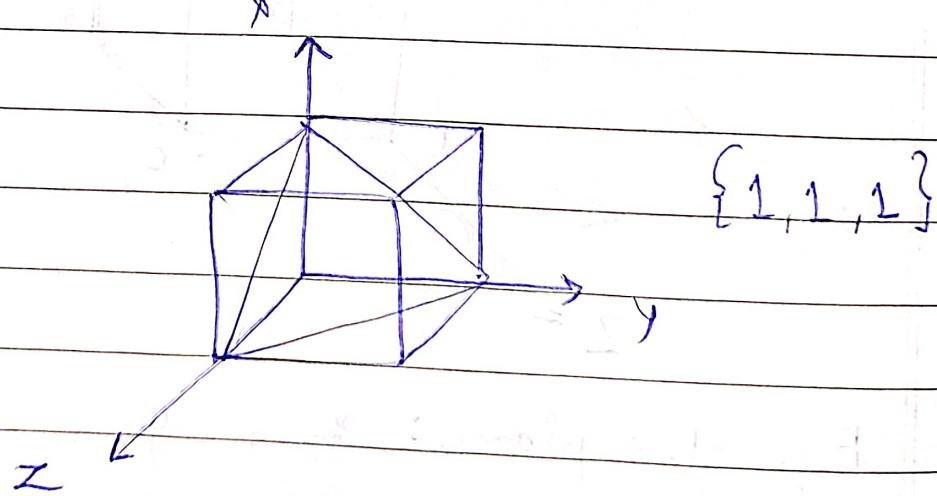
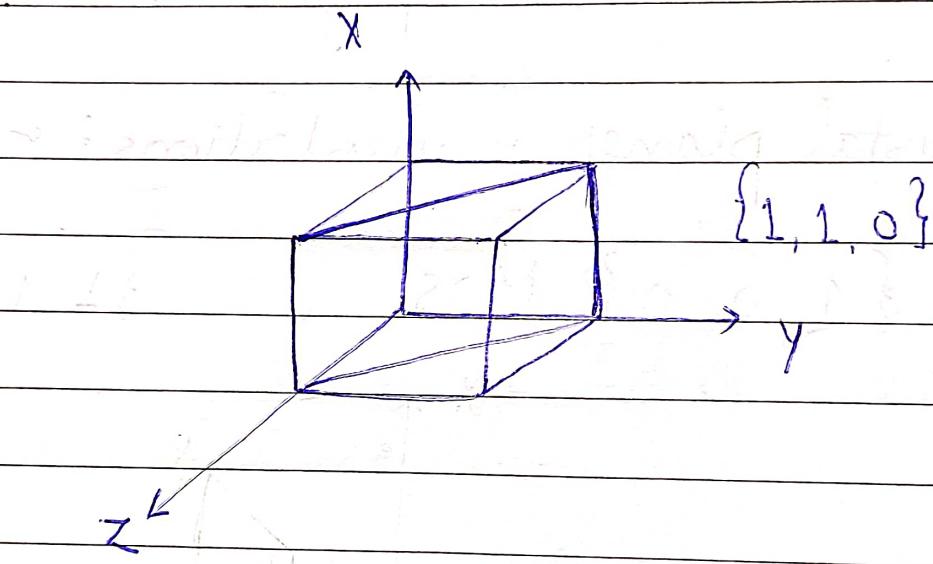
$$\frac{1}{a} = h, \frac{1}{b} = k, \frac{1}{c} = l$$

$\langle hkl \rangle$ Miller indices. $\langle 001 \rangle$

$$hx + Ky + lz = 1$$

$$\frac{x}{a} + \frac{y}{b} + \frac{z}{c} = 1, \text{ where } a, b, c \text{ are intercepts}$$

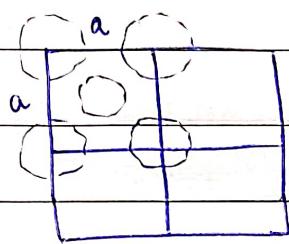
with x, y & z axis respectively. The entire family of $\{1, 0, 0\}$ planes which makes intercepts on only 1 axis & are parallel to other two axis will be represented by $\{1, 0, 0\}$.



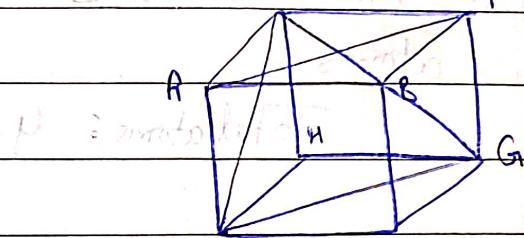
The family of planes which makes intercept with 2 axes & is parallel to 1 axis is represented as $\{1, 1, 0\}$

The family of planes which makes intercept with all three axis are $\{1, 1, 1\}$

$$1. \{1, 0, 0\}$$



$$S = a^2$$



$$\text{Corner atoms} = 4 \times \frac{1}{4} = 1 \rightarrow 1 \text{ atom}$$

$$\text{Face atom} = 1$$

$$\text{Total: } 2 \text{ atoms}$$

While considering Si as single crystal material these 3 types of crystal planes are mostly encountered & influence the properties of Si.

$$\text{Area} = a^2$$

$$\text{Density} = \frac{2}{a^2}$$

$$M = \rho \cdot S = \text{constant}$$

$$\frac{M}{a^2} = \text{constant}$$

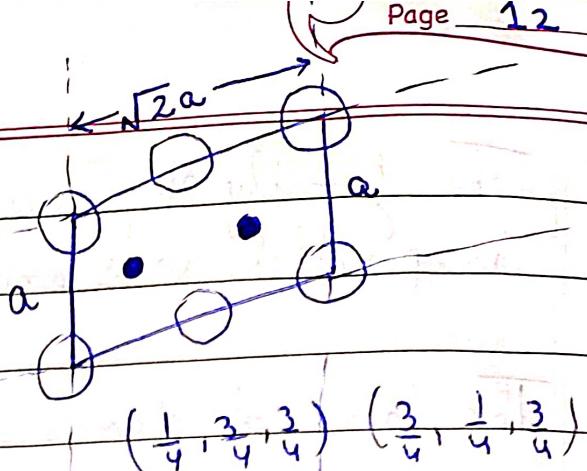
2. $\{1, 1, 0\}$

$$\text{Corner atoms} = \frac{1}{4} \times 4 = 1$$

$$\text{Face centered} = \frac{1}{2} \times 2 = 1$$

$$\text{2nd sublattice} = 2$$

$$\text{Total atoms: } 4$$

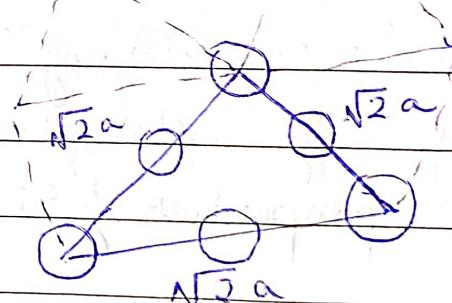


$$\text{Area} = a \times \sqrt{2}a = \sqrt{2}a^2$$

$$\text{Density} = \frac{4}{\sqrt{2}a^2} = \frac{2\sqrt{2}}{a^2}$$

3. $\{1, 1, 1\}$

$$\text{Corner atoms} = 3 \times \frac{1}{6} = \frac{1}{2}$$



$$\text{Face atoms} = 3 \times \frac{1}{2} = \frac{3}{2}$$

$$\text{Total Atoms} = 2$$

$$\text{Area} = \frac{\sqrt{3}}{4} \times 2a^2 = \frac{\sqrt{3}}{2}a^2$$

$$\text{Density} = \frac{2 \times 2}{\sqrt{3}a^2} = \frac{4}{\sqrt{3}a^2}$$

$$\text{Area} = \frac{1}{2} \times 2 \times \frac{\sqrt{3}}{2}a^2 = \frac{\sqrt{3}}{2}a^2$$

The packing density in $\{1,0,0\}$ plane is the lowest whereas planes $\{1/1,0\}$ and $\{1,1,1\}$ have relatively higher packing density.

Miller indices of two planes $\{U_1, V_1, W_1\}$ & $\{U_2, V_2, W_2\}$

$$\cos \theta = \frac{U_1 U_2 + V_1 V_2 + W_1 W_2}{\sqrt{(U_1^2 + V_1^2 + W_1^2)(U_2^2 + V_2^2 + W_2^2)}}$$

Coordinates of lines:

$$U = U_1 W_2 - U_2 W_1, \text{ Reciprocal of planes are also}$$

$$V = V_1 W_2 - V_2 W_1, \text{ if } \theta = 90^\circ \text{ then } \sin \theta = 1$$

$$W = W_1 V_2 - W_2 V_1, \text{ if } \theta = 90^\circ \text{ then } \cos \theta = 0$$

Distance btw similar planes:

$$\{1,0,0\}$$

$$\text{Distance} = \frac{1}{\sqrt{U^2 + V^2 + W^2}} \text{ at } \theta = 90^\circ$$

$\{1,1,0\}$ suggest it will be constant for all planes $\{1,1,k\}$

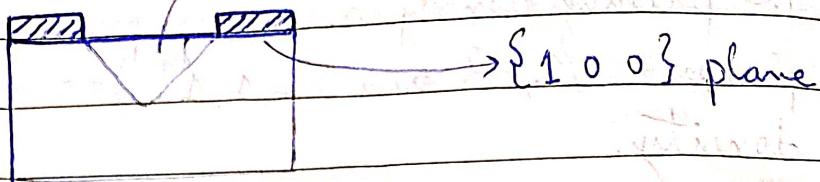
the above figure shows \Rightarrow $1/\sqrt{2}$ at 20 MV to normalize it.

Normalized distance of $\{1,1,0\}$ is $\sqrt{2}/2$ normalized by $\sqrt{3}$.

Thus, $\{1,1,0\}$ is constant for all planes $\{1,1,k\}$.

Now $\{1,0,0\}$ & $\{1,1,0\}$ are same for $\theta = 90^\circ$ but for $\theta = 0^\circ$ they are different.

So, $\cos \theta = 1 \Rightarrow \theta = 0^\circ$ $\Rightarrow \theta = 54.74^\circ$ when $\theta = 0^\circ$

Etching

At particular L etching is done to achieve UMOS.

\angle btw $\{100\}$ & $\{111\}$ is 54.74° .

$\{111\}$ is also called cleavage plane.

When etching is performed on a surface with plane configuration $\{100\}$ the cleavage plane which will appear underneath is $\{111\}$ plane as $\theta = 54.74^\circ$ for $\{100\}$ & $\{111\}$ plane so etching is also inclined at same \angle w.r.t

The height is determined by the width of the window this leads to self limiting etching.

The notable applications of this V groove etching are :

1. Fabrication of VMOS & VMOs which requires reduced no. of fabrication steps as compared to other mos technologies.
2. It can be used for isolation btw two devices. It is difficult to etch $\{111\}$ plane due to spacing btw adj parallel planes further $\{111\}$ has the highest tensile strength

& modulus of elasticity so it is hard to crack as compared to other planes so it is harder to fabricate.

$$\{1, 0, 0\}$$

$$\{1, 1, 1\}$$

$$u = v_1 w_2 - v_2 w_1$$

$$v = w_1 v_2 - w_2 v_1$$

$$w = v_1 v_2 - u_2 v_1$$

$$u = 0 - 0$$

$$v = 1 - 1 \quad \text{Because } w = 1 - 0 \quad \text{①}$$



Cut in circular form.

$$\text{dir. family } \{01\bar{1}, -1\bar{1}\}$$

$$\text{dir. family } \{1\bar{1}0, 0\bar{1}1\}$$

Belongs to family of lines $\{1 \bar{1}0 - 0\bar{1}1\}$

It is very imp. to scribe the wafer along the line of intersection of two planes. The scribing process is usually carried out using a diamond tip tool. While scribing the $\{1, 0, 0\}$ wafer the $\{1, 1, 1\}$ plane appears underneath it. The scribing has to be carried out along the direction of the line of intersection of $\{1, 0, 0\}$ plane & $\{1, 1, 1\}$ plane in order to get smooth edges of resulting rectangular chip.

$$(1, \bar{1}, 1) \nparallel (1, 1, \bar{1})$$

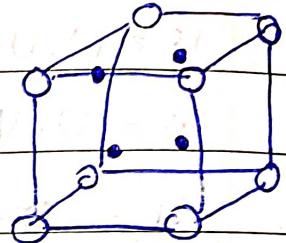
$$\cos \theta = \frac{1}{3} \quad u = -1 - 1 = -2 \quad v = 1 - 1 = 0$$

$$\theta = 70.53^\circ \quad w = 1 + 2 = 2$$

Belongs to family of line $\{1, 1, 0\}$.

Further some other steps also such as oxidation & diffusion are influenced by properties of these individual planes.

In $\{1\ 10\}$ we will get $\{1\ 11\}$ plane but at nearly 90° .



* Defects in crystal structures:

1. Point defects
2. Line defects - 1D
3. Area defects - 2D
4. Volume defects - 3D

1) To cause point defects energy required ranges from 1-2 eV

- (i) Schottky
- (ii) interstitial
- (iii) Frankel

In Blende is a loosely packed structure the packing density is only 34.1%. So there is lot of empty space inside these empty spaces are called interstitial sites. They are not occupied by atoms in a perfect crystal but can be occupied by atoms in case of non ideal crystal.

Di Vacancy only 6 bonds need to be broken so it is much easier to create a di Vacancy instead of two isolated Schottky vacancies.

defect

Frankel has vacancy interstitial pair. It is a combination of two defects Schottky & interstitial defects.

1. When temperature is rising these defects may arise.
2. Due to doping
3. Due to non perfect crystal growth process.

The impurities may influence electronic properties of the material.

The Lithium atoms can sit at interstitial sites & act as a donor & contribute to the electronic activity. Si itself sitting at interstitial sites can behave as donor & can give away four electrons to the conduction band.

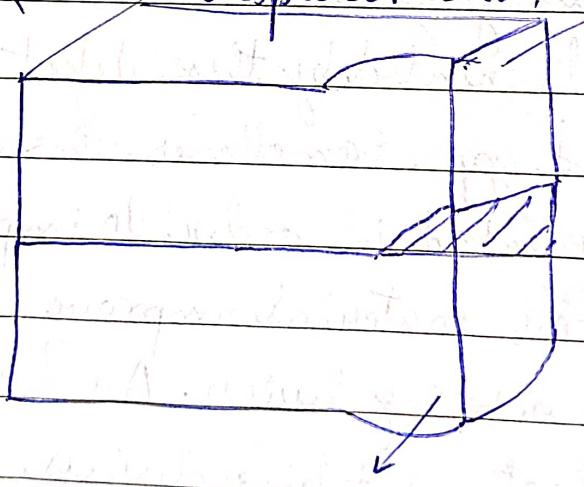
Energy levels created by these defect will be deep in the energy band gap. Sometimes these deep energy levels are deliberately created in order to improve switching speed of devices. This material improve can be used to make fast switching devices. Au & Pt can also be used to make fast switching devices.

① Line defects: A dislocation is formed when material is subjected to shear stress which is greater than elastic limit of material. We need 10-20 ev energy to cause this defect in order to cause this defect.

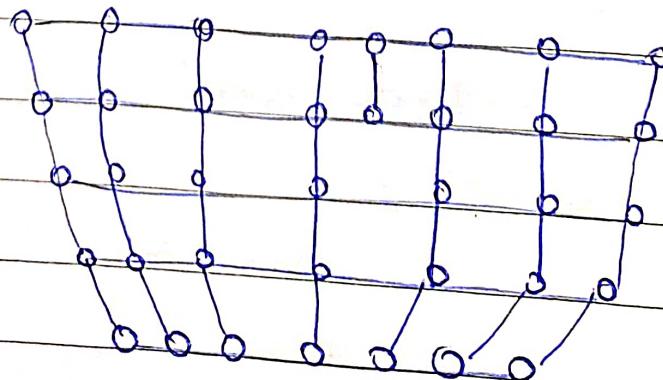
- 1) During crystal growth
- 2) Material subjected to stress
- 3) Excess impurity

Types: 1. Screw dislocation 2. Edge dislocation

1. The motion of screw dislocation is due to shear stress but defect line movement is perpendicular to direction of the stress & atom displacement.



2.



It can be visualized as extra half plane of atoms in the lattice, the dislocation is called line defect because defect caused by dislocation is caused along line.

* Area Defects:

1. Twining
2. Grain Boundary

We should not worry so much about area dislocations as wafer will be rejected and will not be used for IC fabrication. The material should be free from area dislocation.

1. Twining: It is a change in crystal orientation. It is not a single crystalline structure. Two parts of some structure have different crystal orientation.

2. Grain Boundary: Due to some process problem the substrate is a polycrystalline material there are various crystalline orientations in the same substrate. A highly defective region is known as having same crystal orientation in the substrate is known as grain & the boundary of this region is known as grain boundary.

④ Volume Defects: Volume defects are usually caused by precipitates every material has a solubility limit in other material. If a material is introduced in excess of solubility limit it will cause precipitates. The solubility decreases with reduction in temperature so extra material precipitates are formed inside the crystal for example metallic impurities give rise to silicides which has different thermal expansion coefficient which will cause strain further precipitates will also act as host for more dislocations.

→ Crystal Growth: Si is the most abundant ^{material} element on earth in the form of sand. The starting material SiO_2 is reduced to form Si. It is reduced to polysilicon. After this polysilicon is melt then solidified in controlled condition in order to grow single crystal Si.

Two methods to convert to polysilicon:

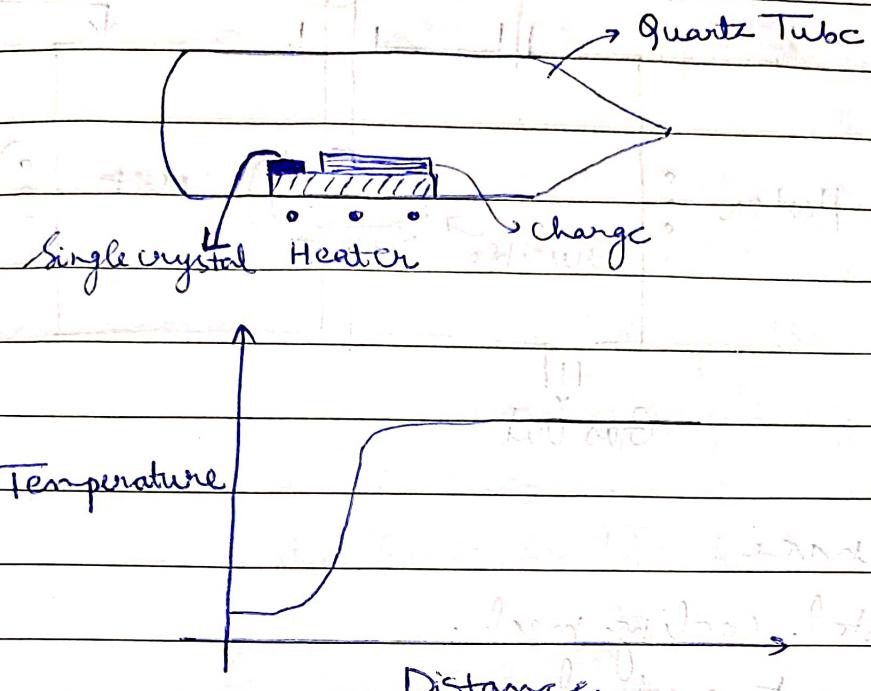
1. Carbothermic
2. Metallothermic

In metallothermic there is possibility of unwanted doping.

1. Bridgman method

2. Czochralski (CZ) method

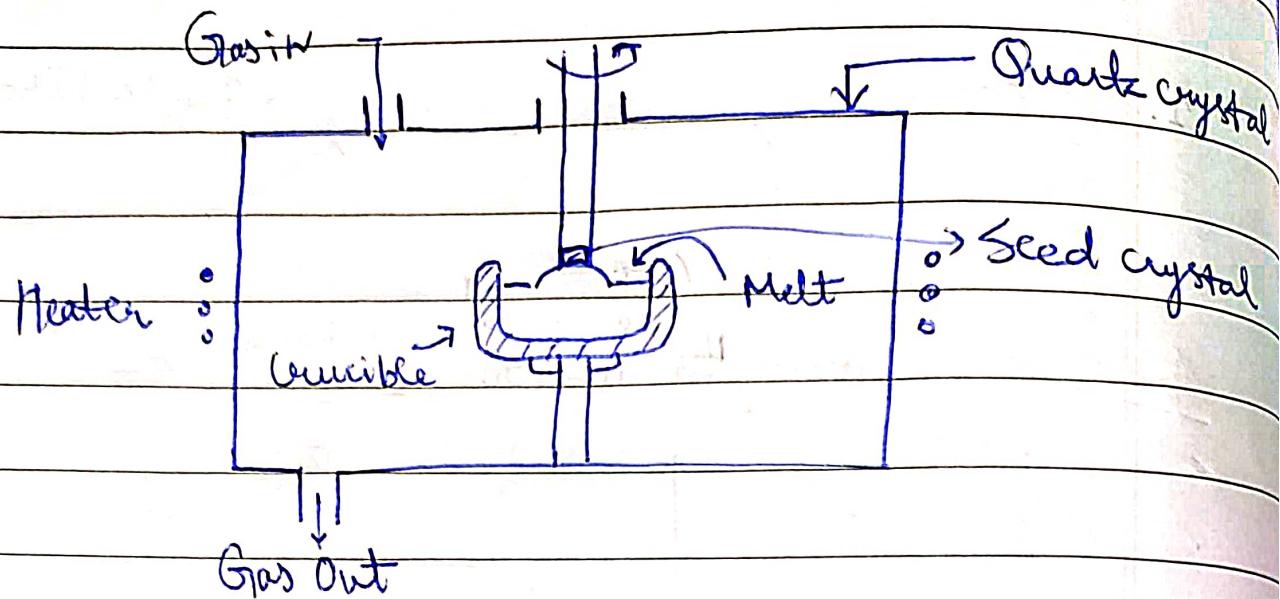
1.



The seed is placed alongside the polysilicon charge inside the quartz tube. The charge is heated to its melting point however it is made sure that seed crystal itself is not melted. The temperature profile is to be carefully maintained in the bridgeman method. When the charge is in molten state heater is moved in right direction.

The melt on the left side becomes cooler & it will solidify & since it is in contact with seed crystal it will adopt some orientation. The limitation of Bridgeman technique is its confining boundary of the quartz tube that will cause stress during solidification of the charge. So this will lead to lot of dislocations.

Czochralski method:



1. Furnace

2. Crystal cooling mech.

3. Ambient control

4. Control system.

Advantage:

Disadvantage: 1. Crucible is made of SiO_2 so there is possibility of impurity. Using O_2 can get trapped in Zn blende structure.

There is an opening through which the pull rod is suspended inside the chamber. The chamber may be water or oil cooled. The crucible is a cup in which charge is going to be placed & it is made up of quartz. The crucible is used only once as it cracks during cooling. The crucible is placed inside a

graphite susceptor. RF or resistor heating is used in order to heat the charge. At the end of ~~total~~^{pull} rod a seed crystal is fixed. The pull rod is pulled up during crystal growth. The chamber is evacuated & filled with some inert ambient gas. After charge gets molten then pull rod is gradually lowered till seed crystal touches the melt surface. Then very slowly pull rod is pulled up. The pull rate should be carefully selected in order to grow single crystal silicon.

$$L \frac{dn}{dt} + K_s \frac{dT}{dx_1} A_1 = K_s \frac{dT}{dx_2} A_2$$

as $\frac{dT}{dx}$ thermal gradient in melt $\frac{dT}{dx}$ thermal gradient in solid

$$L \frac{dn}{dt} = K_s \frac{dT}{dx_2} A_2 \quad \left[\frac{dn}{dt} = A \times \phi \frac{dn}{dt} \right]$$

Mass solidification
rate

$$A \phi \frac{dn}{dt} = K_s \frac{dT}{dx_2} A_2 \quad \left[\text{let } A = A_1 = A_2 \right]$$

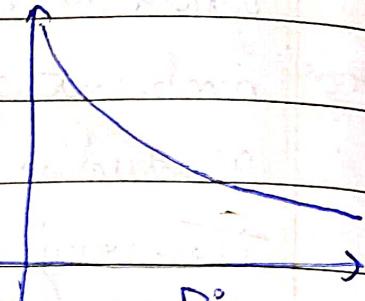
$\frac{dn}{dt} = \frac{K_s}{L \phi} \frac{dT}{dx_2}$
--

In reality or practical life $\frac{dt}{dm}$ is not zero but $\pm 0.5^\circ C$.

$$H_i - H_o = L \frac{dm}{dt}$$

$$LA\phi \frac{dn}{dt} = H_i - H_o$$

Pull
rate



$$\frac{dn}{dt} = \frac{H_i - H_o}{LA\phi}$$

In actual the pull rate is less than maximum pull rate. There can be variation in temp. of the melt. The pull rate is going to vary inversely with area for $H_i - H_o$. In other words larger is your crystal smaller should be the pull rate. The pull rate also has effects on the defects. It is much easier to draw smaller diameter single crystal wafer with low defect density.

Every impurity will have solid solubility in crystal & equilibrium solubility in the melt. This difference is represented by segregation coefficient represented by K_s .

The segregation coeff. is the ratio of solid solubility of dopant in Si to equilibrium solubility in the melt. For most of the impurities K_s is less than 1 which implies $C_s < C_L$.

The implication is that these impurities are left inside melt they don't enter solidification phase. A crystal is grown, the melt becomes richer in impurity so doping concentration will vary from one end to another end of the grown rod.

For O_2 $K_s > 1$ for $\approx 5 \times 10^{17}/cm^3$ $\sim 450^\circ C$ to $500^\circ C$

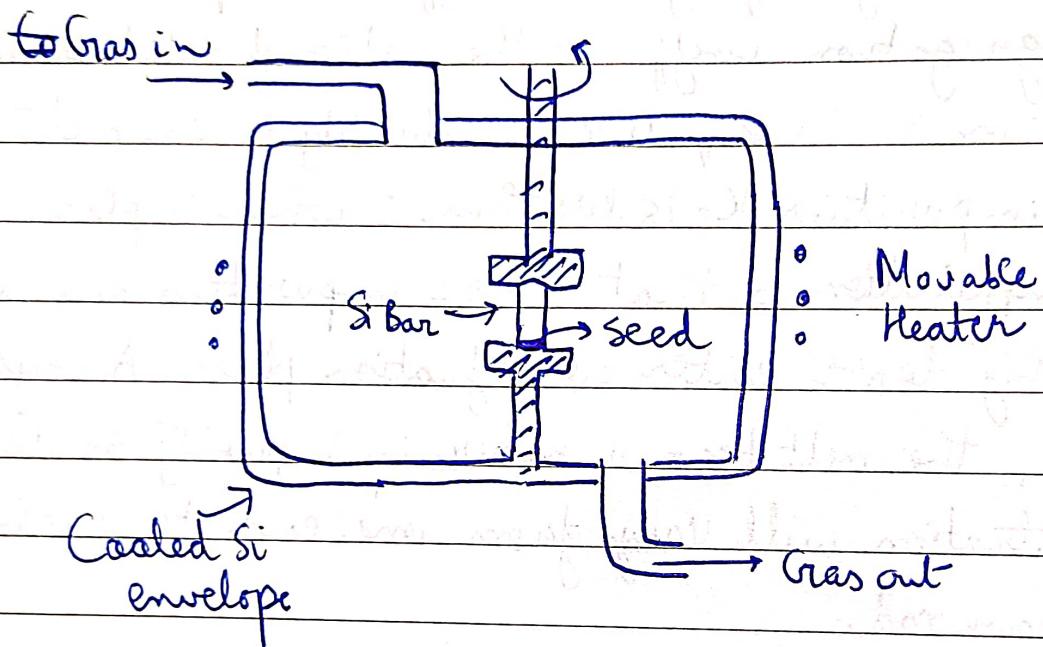
If the above conditions fulfilled 95% will enter interstitial site & 5% of O_2 will form complexes such as SiO_4 (this will act as a donor). It is effect the resistivity of the formed crystal.

~~A 5% of~~

The remedy is to cut into slices. Heat upto $600^\circ C$, SiO_4 complexes will be dissolved when it is rapidly cooled. It is much easier to cool down the wafer than entire large single crystal.

If oxygen conc. is greater than $6.4 \times 10^{17} / \text{cm}^3$. It will dissolve in oxygen precipitates these precipitates act as sink for metallic impurities & they give rise to more dislocations.

④ Zone refining technique:



The Si bar is held on a chuck on one side a small is provided. The heating starts at seed crystal end of the rod. At retreating end of the heater it will leave a solidified portion which is in contact with seed crystal

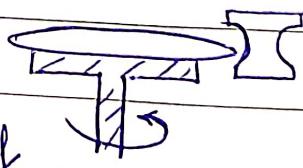
- Advantages:
1. No need of SiO_2 crucible so no O_2 impurity.
 2. Oxygen content can be reduced by at least 10% and in multiple passes 90-100% can be achieved.
 3. Repeated passages can be used to further improve the quality.

c) **Marking flat:** One or more flats are ground along the length of the ingot. The largest flat is called major or primary flat which is relative to specific crystal direction. It is used as mechanical locator in the automated processing equipment to position wafer and to orient IC devices relative to crystal.

d) **Cutting into wafers:** This step involves slicing of ingot into the wafers. The slicing determines the orientation, thickness, taper and other ~~for~~ parameters. The wafer is cut ⁱⁿ into a particular orientation. The thickness of the wafers is also decided by this step. Slightly thick wafers are cut which are able to subsequent thermal processes.

Wafer Loss : It is a loss which occurs due to blade width which is around $325\text{ }\mu\text{m}$.

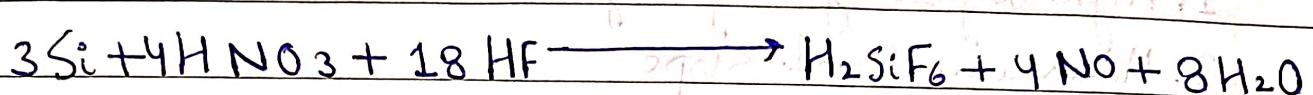
e) **Edge Contouring:**



The radius is ground on the rim of the wafer. Process is carried out in cassette fed high speed equipment. Edge rounded wafers develop lesser defect during device fabrication.

Etching: ~~etching is the process of removing material from a surface by chemical or physical action.~~

1. Acidic Etching: It is a mixture of hydrochloric, nitric & acetic acid.



Acetic acid acts as a diluent if more acetic acid less

rate of rxn. ~~rate of rxn. increasing with decrease of gas chamber~~

~~rate of rxn. constant Acet. & OIC. After rate decreases as~~

~~If solution is standardized at 2 within HCl~~

The etching involves oxidation reduction process followed by dissolution of oxidation product. The rotating wafer maintains uniformity of the etching process. Depending on the acid mixture & temp. etching can be isotropic or anisotropic. For HNO_3 rich solns isotropic etching is there, HF rich solns, anisotropic etching will be there.

4 : 1 : 3
 $\downarrow \quad \uparrow \quad \downarrow$
 $\text{HNO}_3 \quad \text{HF} \quad \text{CH}_3\text{COONa}$

to remove mechanical impurities.

Polish:

It is the final step in wafer preparation. Purpose is to provide smooth surface on which device features can be photo engraved. Requirements from for operations are:

1. High degree of surface freshness
2. Minimum local slope.

Process can be single wafer or batch process. Polishing pad is made up of artificial fabric polyester / polyurethane. Slurry is a colloidal soln. with SiO_2 (100 Å diameter) NaOH. The NaOH oxidises Si & mechanical step. Silica particles remove oxidised part away.

Epitaxy

1) Homo

2) Hetero

A thin layer with width upto few micrometer is grown on top of bulk substrate.

The epitaxy can be categorised into homo epitaxy & hetero epitaxy.

So in homo epitaxy same type of material is grown on top of bulk material but the grown material may have different doping concentration or resistivity & homoepitaxy is very simple process & it is not very challenging.

Heteroepitaxy involves growth of a dissimilar region on top of a particular substrate material. This is a much more complex process. Eg: Si on top of sapphire.

The three cardinal rules for heteroepitaxy are:

1. There should be no chemical rxn b/w the substrate & epitaxial layer
2. There should be no lattice mismatch.
3. Coefficient of thermal expansion should match.

Epitaxy

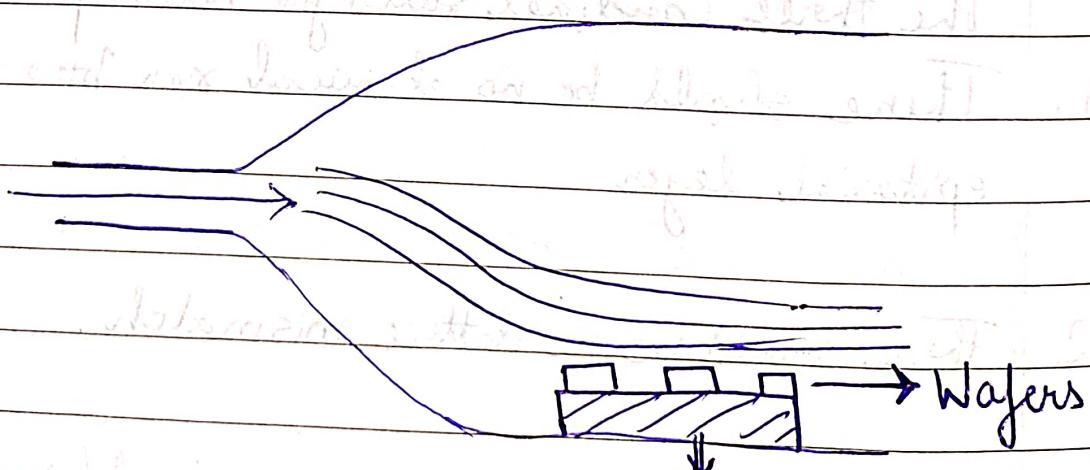
Liquid phase epitaxy

Vapour phase epitaxy

Molecular Beam epitaxy

For Si liquid phase epitaxy is not much used. For Si vapour phase or molecular beam epitaxy are preferred.

The liquid phase epitaxy is carried out in liquid phase for example. GaAs soln. is mixed in Ga soln. When this combination is cooled this will result in precipitation of GaAs. When GaAs bulk material is brought into contact inside the precipitate it will be deposited on GaAs bulk substrate. It is not very useful for Si. As Si is very difficult to dissolve.



In vapour phase epitaxy, the material transport is in form of vapour. We need to use gas reactants the liquid with

high vapour pressure i.e. it can be vapourised very easily. The gas also contains reactants. The gas flow is controlled using mass flow controllers. The reactants flow over the sample they react & their will be deposition on top of the samples.

1. Laminar flow
 $NR < 2000$

2. Turbulent flow
 $NR > 2000$

$$NR = \frac{d v S}{\mu}$$

where d = diameter of the tube v = velocity of gas + reactants
 S = density of the gas μ = viscosity

During vapour phase epitaxy in the horizontal type reactor stagnant layer is formed which is known as boundary layer. The flow of gas is characterized by reynolds number which is further dependent on the diameter of the tube, the velocity, density & viscosity of the gas plus reactant mixture. The reynolds no. has to be within certain limit. If it is less than 2000 the flow is characterized as laminar for. If $NR > 2000$ then turbulent flow.

For a typical vapour phase epitaxy is much less than 2000. Typical values are 100, 200 at max 500.

$$y = \sqrt{\frac{dn}{N_R}}$$

$$y = \sqrt{\frac{dn \mu}{dvs}}$$

$$y = \sqrt{\frac{n \mu}{v_s}}$$

The velocity & distance can be controlled to minimize the boundary layer growth.

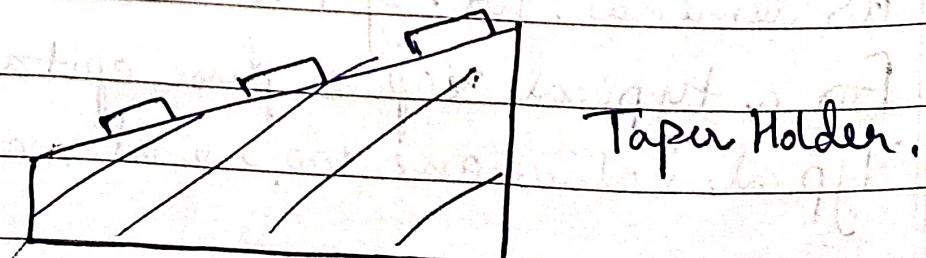
$$J = (N_g - N_s) \times (-D)$$

$y \rightarrow$ Boundary layer thickness

Conc. of reactants in gas

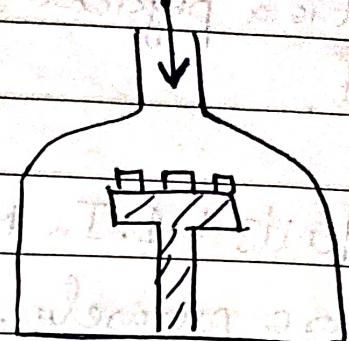
$$J = -D(N_g - N_s)$$

The flux should be as high as possible for the deposition.
 y should be as small as possible.



1. The gas flow is parallel to the surface of the sample. The samples are placed on an inclined plane.

2. Vertical phase epitaxy



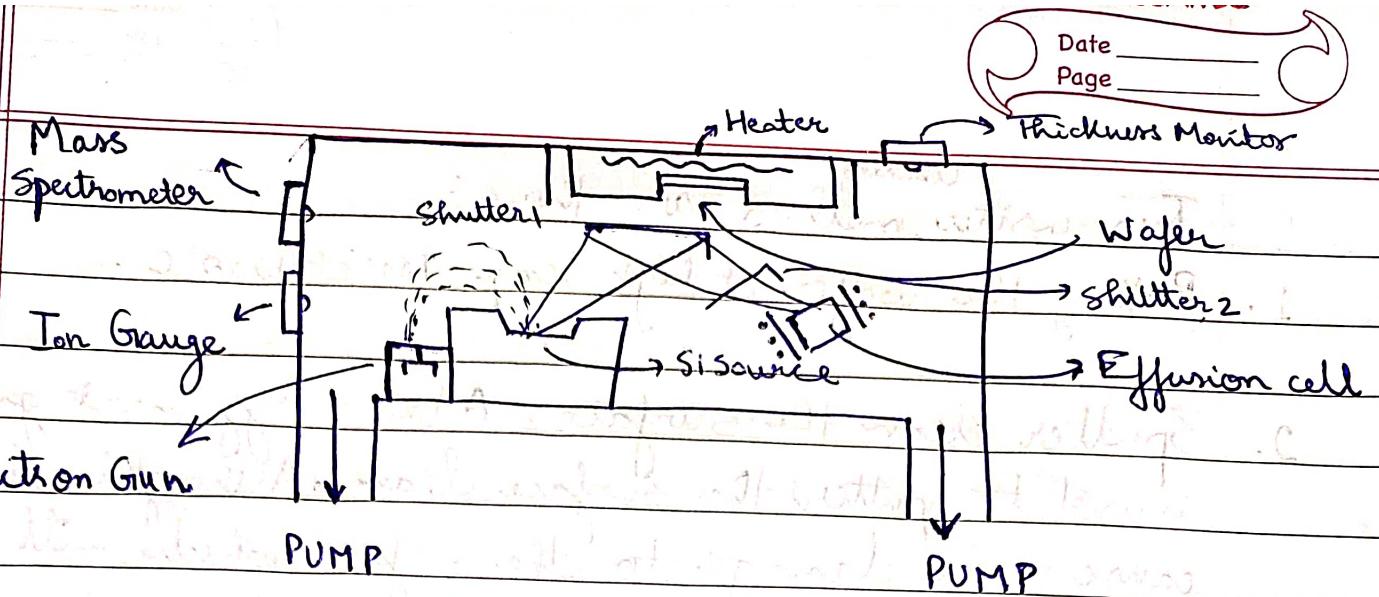
The gas flow is normal to the surface of the sample hence prob. of boundary layer is less critical. But the system is slightly complex & throughput is also less.

Barrel: The reactor holder is a barrel or drum. Small grooves are carved out in the drum which can hold samples or silicon wafers. The barrel type reactor can be used for mass production. Essentially it is a horizontal reactor as gas flows in parallel direction to the semiconductor sample surface. Better uniformity can be achieved by rotating the barrel.

Molecular Beam epitaxy : ~~volatilization & condensation~~
It is a physical evaporation process with no ~~rxn~~ involved in it.

- Merits : 1. In MBE the growth rate can be controlled more precisely. ($0.01 \mu\text{m/min}$ to $0.3 \mu\text{m/min}$ for Si).
2. There is no boundary layer problem.
3. MBE is comparatively low temperature processing. So auto doping is less.
- Auto doping is because of out diffusion from the substrate layer to the epitaxial layer & vice versa.
4. Precise control of doping is possible. As no chemical rxn is involved measured quantity can be vapourised & deposited.

Demerits : Sophisticated & expensive set up required.
Pressure req is 10^{-8} to 10^{-10} torr.



Evaporation is done under high vacuum condition to minimize contamination & avoid collisions. An e⁻ beam is focused on Si Source & Si is evaporated. The Si was placed inside a crucible type structure. In order to introduce dopants an effusion cell is heated. Shutter 1 & shutter 2 which are controlled using p processor are used to control epitaxial layer thickness & amount of dopants. The wafer is placed in Sample holder & its heated to temp. upto 400°C to 800°C.

It is very imp. to maintain vacuum condition in a MBE reactor so in between runs there will be too much time. Every time a substrate is introduced the chamber has to be opened at atmospheric pressure level, then again it has to be taken down to 10^{-13} - 10^{-20} torr. The soln. is a load lock system with multi chamber structure so without breaking the vacuum the substrate can be introduced in the MBE reactor.

Two insitu method are there:

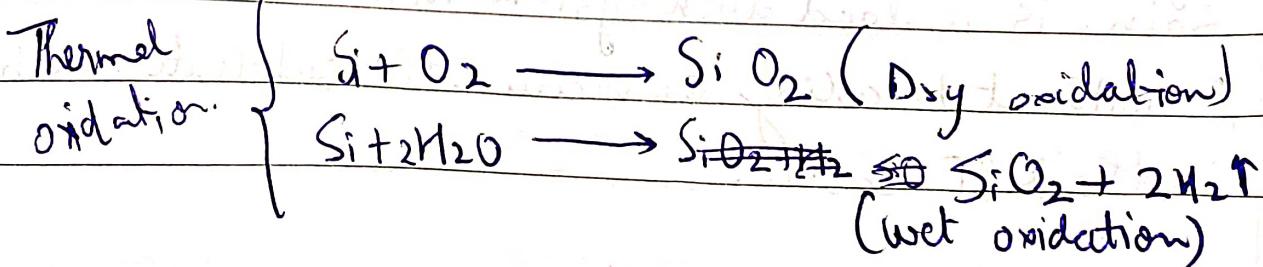
1. Baking the wafer at high temp. 1000°C to 200°C .
2. Sputter clean the surface. A low energy inert gas beam is used to sputter the surface clean. Although it may cause some damage to the surface which will require additional step of heat treatment.

- (i) RHEED - Reflection High energy electron diffraction.
- (ii) X-Ray Photoelectron spectroscopy (For compound like AlGaAs but not for Si).

* Oxidation: It is the process related to growing an oxide layer on top of Si substrate.

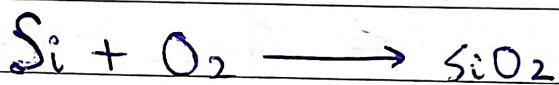
They are used as mask. The oxide layer can be used to protect regions through which we do not want doping to take place.

As an active element: It can be used as gate oxide in the MOS structure. In this a thin oxide layer with good interface quality is required.



The anodic oxidation put Si in electrolyte & bath used Si as anode & a nobel metal as cathode. Apply voltage an oxide layer will form on the Si substrate.

The thermal oxidized oxidation: It involves putting silicon samples inside the furnace increasing the temp by allowing O_2 or H_2O to flow. The Si will react with O_2 or water to form SiO_2 .



$$28 \text{ Area} \times 32 = 60$$

$$t_{SiO_2} = \frac{60}{Area \times 2.27}$$

$$V \times D_{Si} = W_{Si}$$

$$Area \times t_{Si} \times D_{Si} = 28$$

$$t_{Si} = \frac{28}{Area \times 2.33}$$

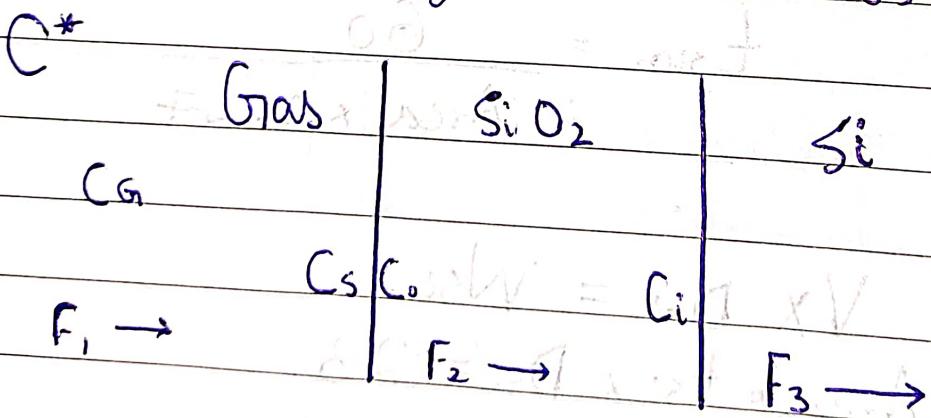
$$\frac{t_{Si}}{t_{SiO_2}} = \frac{28}{60} \times \frac{2.27}{2.33} \approx 0.45$$

The significance is that assume 1000 Å of SiO_2 is grown then it has consumed 450 Å of Si.

The movement of oxidising species into the Si causes the oxidation. So by radioactive tracing it has been found that it is the movement of oxidising species into the Silicon & not movement of Si out. whereas in anodic oxidation the Si moves out & starts at the outer surface.

⇒ Thermal oxidation has better oxide layer than anodic oxidation.

In thermal oxidation the contamination on outer layer doesn't effect the interface that's why thermal oxide is used as gate oxide in MOS device.



C_G is conc. of oxidising species in the gas.

C_s is diff. of C_G at boundary right next to gas SiO_2 surface.

C_o " " " " " outer surface of oxide layer.

C_i " " " " " inner oxide surface.

$$\text{Flux } F_1 = h_G (C_G - C_s) \quad \partial \Omega = \mathbb{D}$$

h_G = gas phase mass transfer coefficient.

$$PV = nKT$$

(conc)

$$C_G = \frac{P_G}{kT} \Rightarrow C_s = \frac{P_s}{kT}$$

$$F_1 = \frac{h_G}{kT} (P_G - P_s)$$

$$F_1 = h (P_G - P_s)$$

$$h = \frac{h_G}{nKT}$$

The flux from bulk gas right next to boundary of the SiO_2 layer is governed by conc. difference at two different points.

$$(e) \leftarrow [D_{\text{eff}} = ?]$$

As per Henry's law the eq. conc. of a species within a solid is proportional to partial pressure of that species in the surrounding gas.

$$C^* \propto P_G$$

$$C_0 \propto P_S$$

$$C^* = H P_G$$

$$C_0 = H P_S$$

$$F_1 = h (C^* - C_0) \rightarrow ①$$

F_2
This is related to movement of oxidizing species through the existing oxide layer. The movement is because of conc. gradient.

$$\frac{dF}{dT} = F_2 \propto C_0 - C_i$$

$$F_2 = D \frac{(C_0 - C_i)}{n} \rightarrow ②$$

\downarrow
 SiO_2 layer thickness

The F_3 is related to reaction of Si with oxidizing species

$$F_3 \propto C_i$$

$$F_3 = K_s C_i$$

→ ③

At equilibrium: $F_1 = F_2 = F_3$

Comparing ② & ③

$$F_2 = F_3$$

$$\frac{D(C_o - C_i)}{\pi} = K_s C_i$$

$$DC_o - DC_i = \pi K_s C_i$$

$$C_i = \frac{DC_o}{D + \pi K_s}$$

$C_i = \frac{C_o}{\left(1 + \frac{\pi K_s}{D}\right)}$
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If π is very small thin oxide layer, $C_i \approx C_o$.

For thicker oxide layer C_i becomes smaller than C_o .