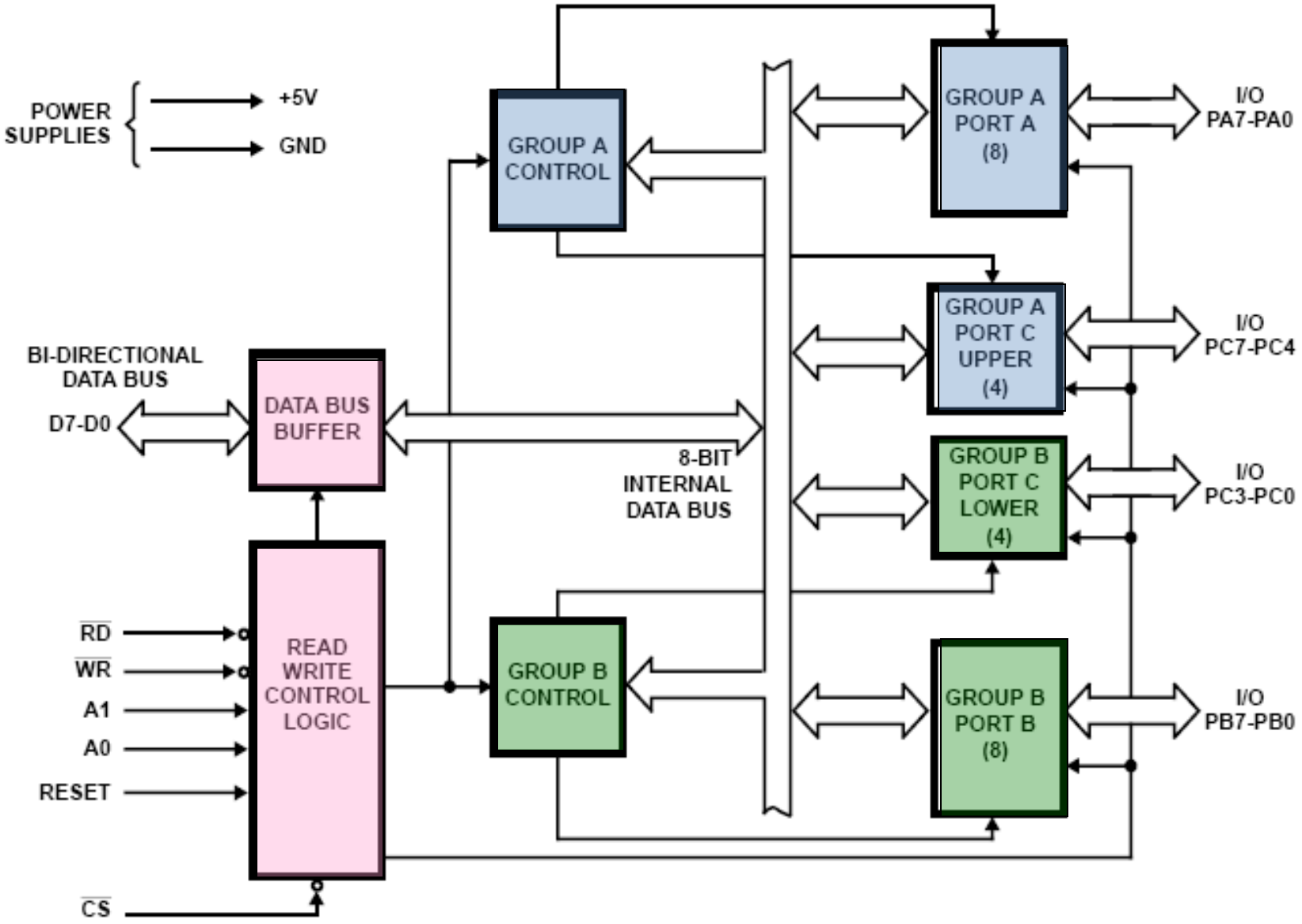
PPI

PROGRAMMABLE PERIPHERAL INTERFACE

8255

PPI

Functional Diagram



Functional Description

- **Data Bus Buffer**

  This three-state bi-directional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

- **Read/Write and Control Logic**

  The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Contd….

- **(CS)**

  Chip Select. A “low” on this input pin enables the communication between the 82C55A and the CPU.
- **(RD)**

  Read. A “low” on this input pin enables 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to “read from” the 82C55A.
- **(WR)**

  Write. A “low” on this input pin enables the CPU to write data or control words into the 82C55A.

Contd…

- **(A0 and A1)**

  Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).
- **(RESET)**

  Reset. A “high” on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode. “Bus hold” devices internal to the 82C55A will hold the I/O port inputs to a logic “1” state with a maximum hold current of 400mA.

Contd….

- **Group A and Group B Controls**

  The functional configuration of each port is programmed by the systems software. In essence, the CPU “outputs” a control word to the 82C55A. The control word contains information such as “mode”, “bit set”, “bit reset”, etc., that initializes the functional configuration of the 82C55A. Each of the Control blocks (Group A and Group B) accepts “commands” from the Read/Write Control logic, receives “control words” from the internal data bus and issues the proper commands to its associated ports. Control Group A - Port A and Port C upper (C7 - C4) Control Group B - Port B and Port C lower (C3 - C0) The control word register can be both written and read as shown in the “Basic Operation” table. Figure shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic “1”, as this implies control word mode information.

Operational Modes

The operation of the can be classified into two broad groups

- I/O mode and
- Bit Set/ reset mode

I/O Mode

Operational Description

Mode Selection

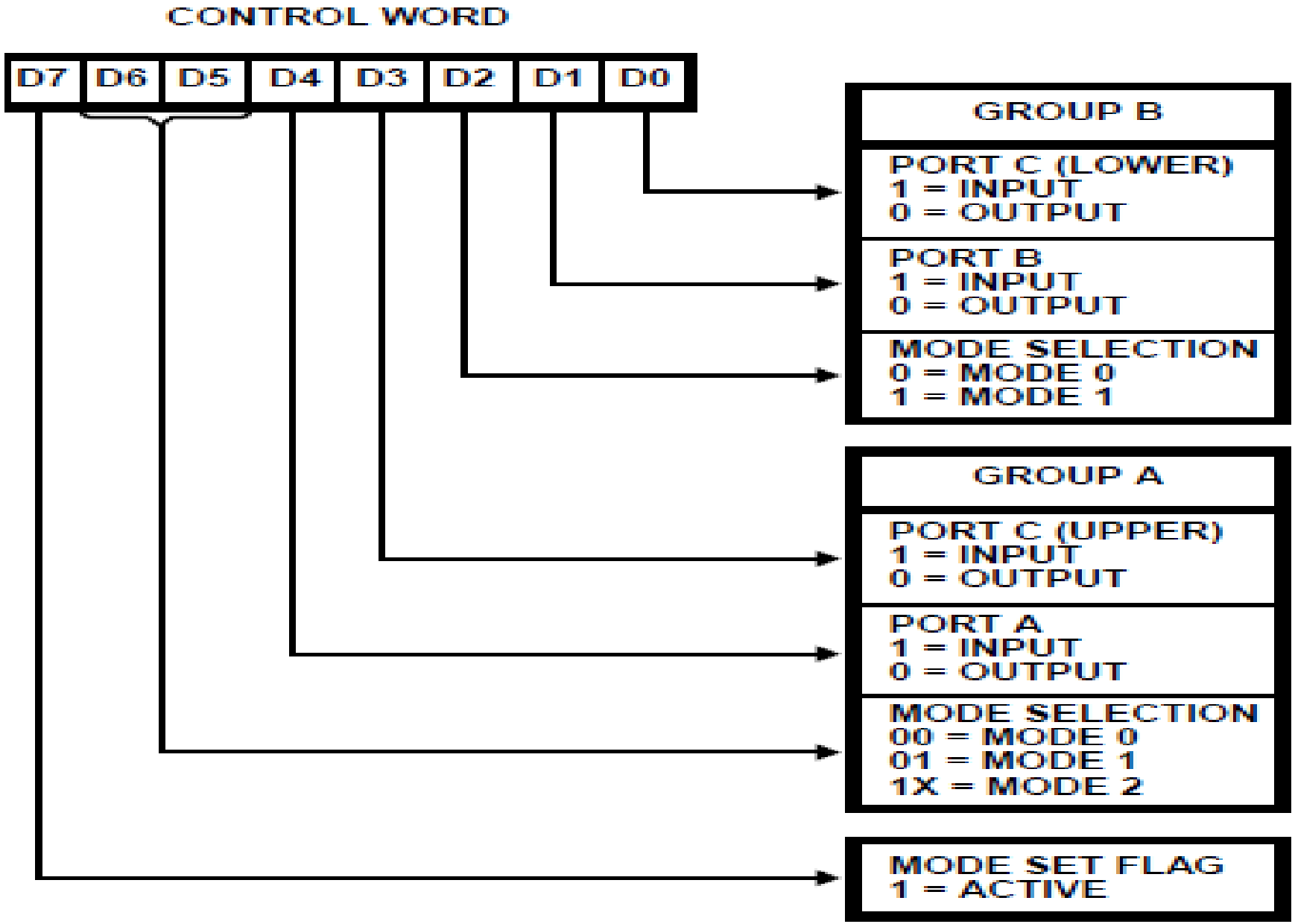
There are three basic modes of operation than can be selected by the system software:

- Mode 0 - Basic Input/Output
- Mode 1 - Strobe Input/Output
- Mode 2 - Bi-directional Bus

Contd…

- When the reset input goes “high”, all ports will be set to the input mode with all 24 port lines held at a logic “one” level by internal bus hold devices.
- After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required.
- This eliminates the need to pullup or pulldown resistors in all-CMOS designs.
- The control word register will contain 9Bh.

MODE DEFINITION FORMAT



Single *Bit Set/Reset* Feature

- Any of the eight bits of Port C can be Set or Reset using a single Output instruction. This feature reduces software requirements in control-based applications.
- When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were output ports.

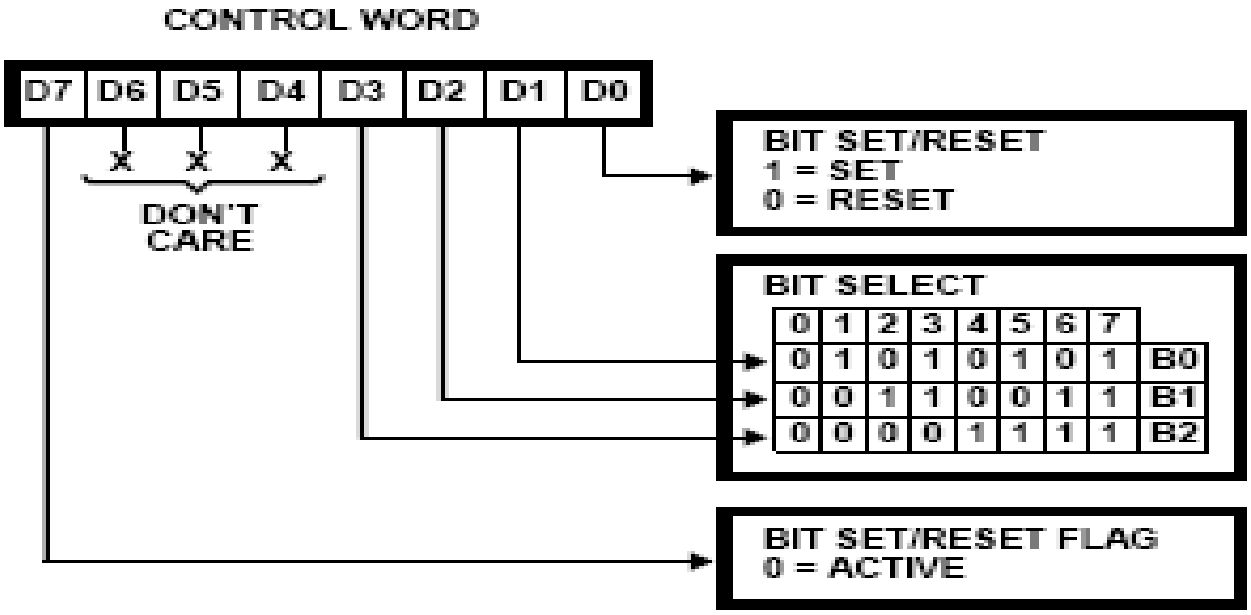


FIGURE 5. BIT SET/RESET FORMAT

Mode o

- **Mode 0** (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

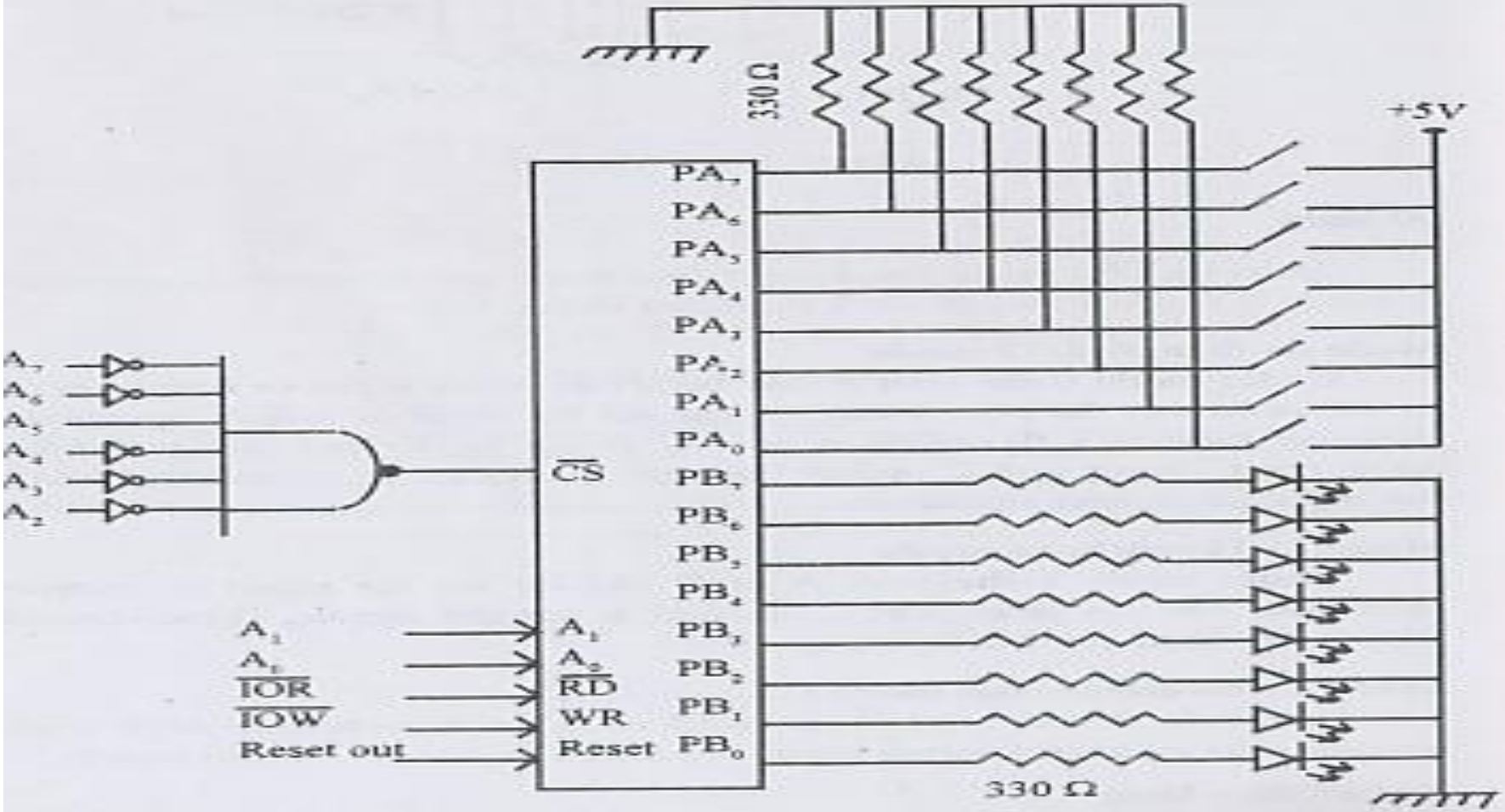
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any Port can be input or output
- Outputs are latched
- Input are not latched
- 16 different Input/Output configurations possible

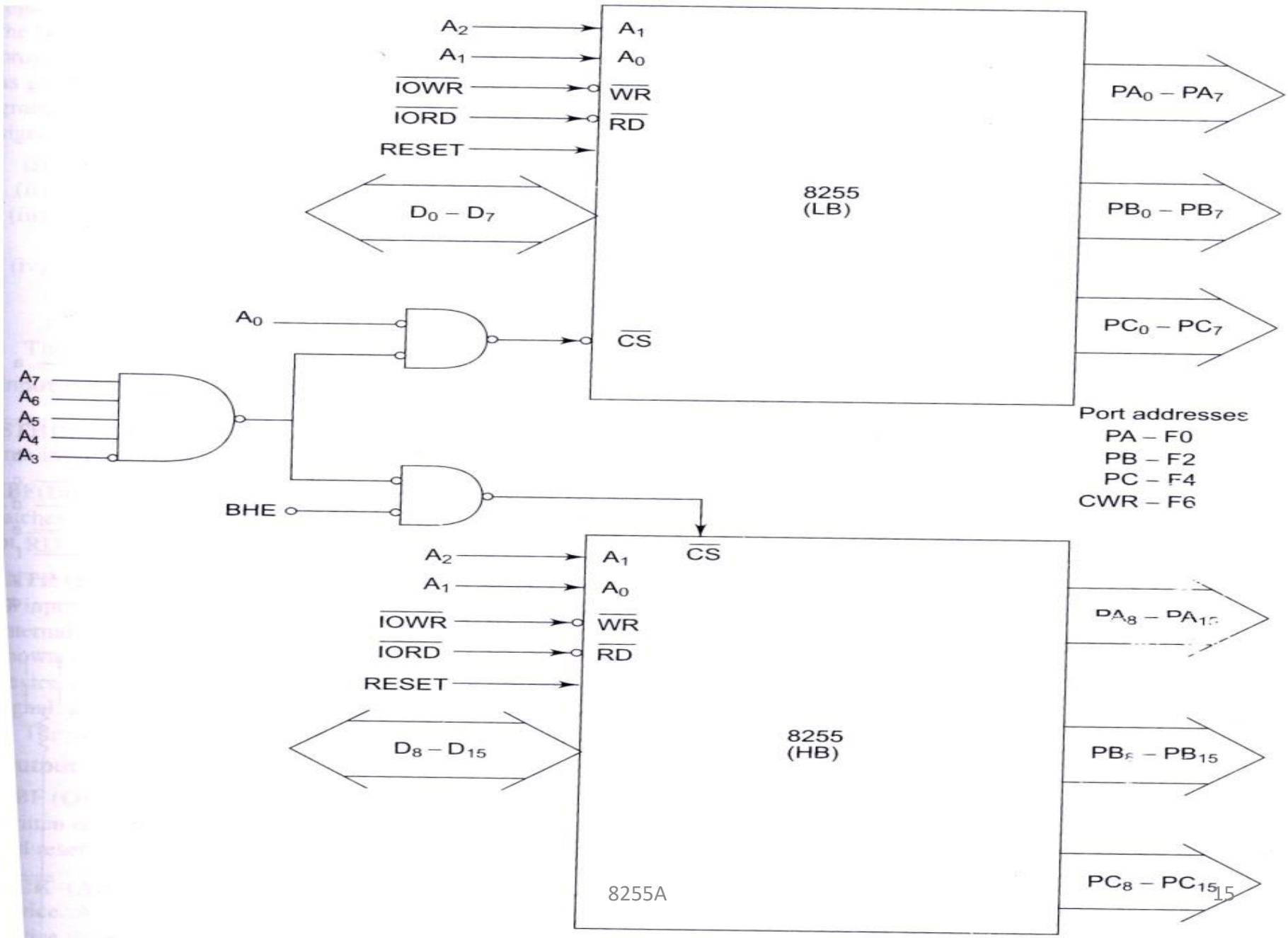
9.4 A MODE 0 APPLICATION—A SIMPLE I/O CIRCUIT

The application involves interfacing eight switches at the input port and eight LEDs at the output port. Port A is used for input and port B for output as shown in Fig.9.4.

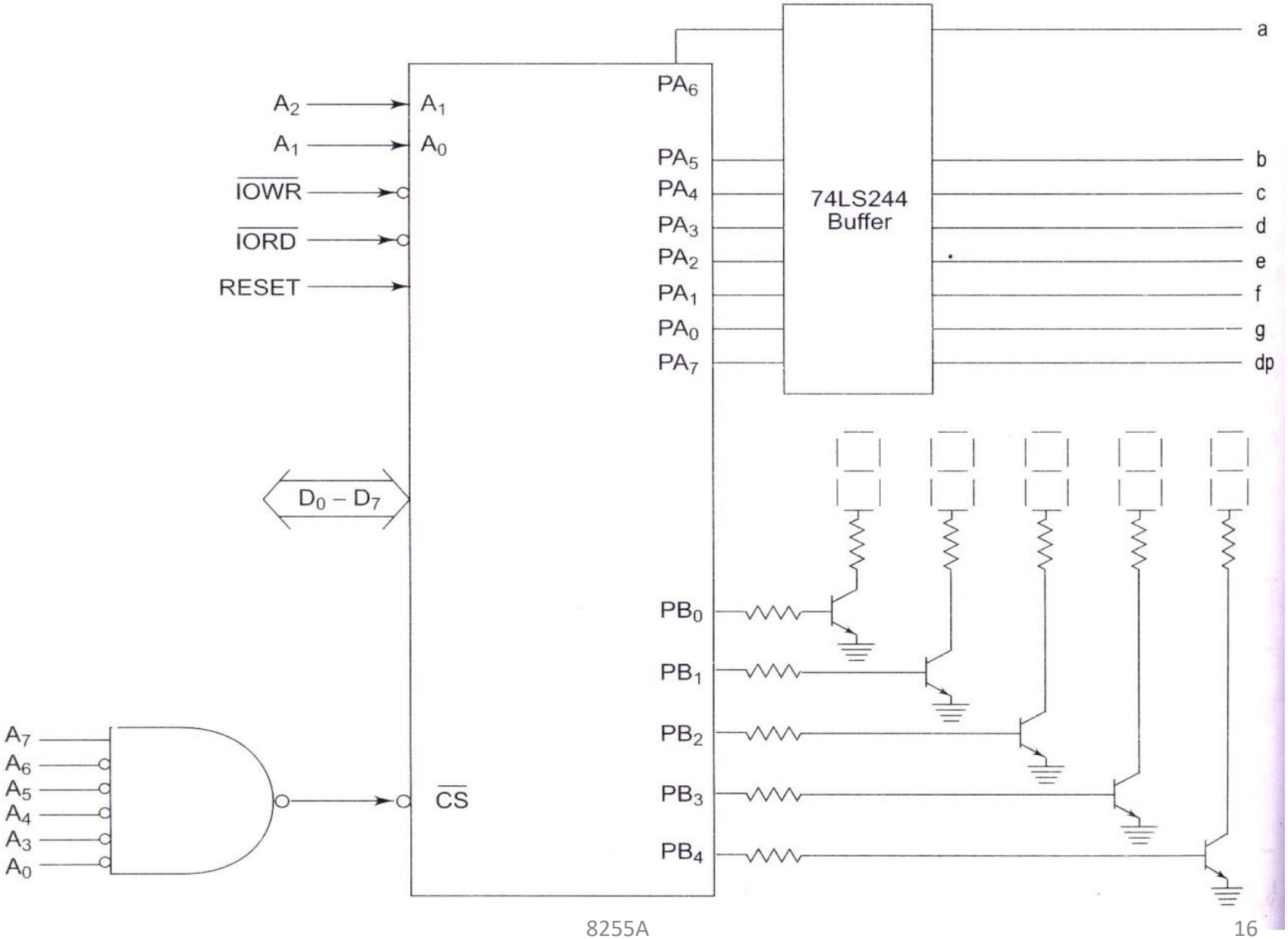
The device is operated in I/O mapped I/O mode, and $\overline{RD}$, and $\overline{WR}$ lines are connected to the $\overline{IOR}$ and $\overline{IOW}$ control signals of the bus.



Mode 0 example



Mode 0 example



Mode 1 Operation

- The details of mode 1 is illustrated with an example of interfacing a peripheral.

As an example interfacing with printer…….

- The printer is an electromechanical device. Its printing speed is much slower than the CPU's operating speed. Though printer can receive data from CPU at any rate, it can print the data only at slower rate. Therefore the data transfer between the CPU and the printer proceeds as follows…….

Mode 1 Operation

- The printer has a memory buffer within it.
- The CPU sends out a *byte* of data to printer
- The printer receives it stores it in the buffer, then sends out an acknowledgement to the CPU
- The CPU sends out one more byte. The process repeats until the memory buffer is full.
- Then the printer stops sending the acknowledgement.
- The stops sending further data.
- The printer prints the part of the buffer content.
- Then it starts sending acknowledgement and then the CPU sends data.
- This process of data transfer is known as *Handshake* method.

Mode 1

- **Mode 1** - (Strobed Input/Output)-

  This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or “hand shaking” signals. In mode 1, port A and port B use the lines on port C to generate or accept these “hand shaking” signals.

Mode 1 Basic Function Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

MODE 1 INPUT

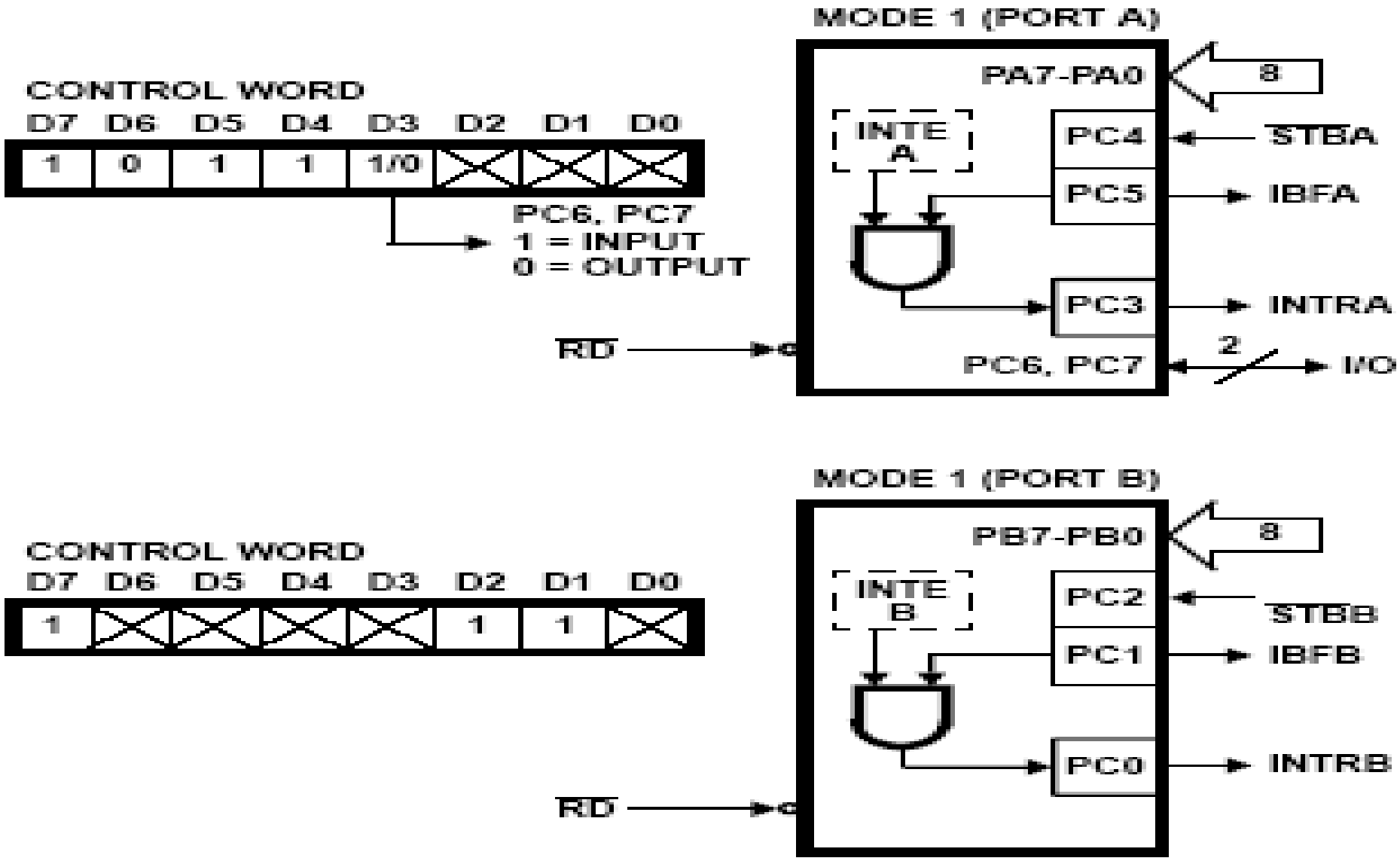


FIGURE 6. MODE 1 INPUT

Input Control Signal Definition

- **STB (Strobe Input)**

  This signal (active low) is generated by a peripheral device to indicate that it has transmitted a byte of data. The 8255A, in response to STB, generates IBF and INTR**.**

  "A "low" on this input loads data into the input latch."

- **IBF (Input Buffer Full F/F)**

  A "high" on this output indicates that the data has been loaded into the input latch: in essence, and acknowledgment. IBF is set by STB input being low and is reset by the rising edge of the RD input.

Input Control Signal Definition

- **INTR (Interrupt Request)**
  A “high” on this output can be used to interrupt the CPU when and input device is requesting service. INTR is set by the condition: STB is a “one”, IBF is a “one” and INTE is a “one”. It is reset by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.
- **INTE A**

Controlled by bit set/reset of PC4.

- **INTE B**

Controlled by bit set/reset of PC2.

Input Control Signal

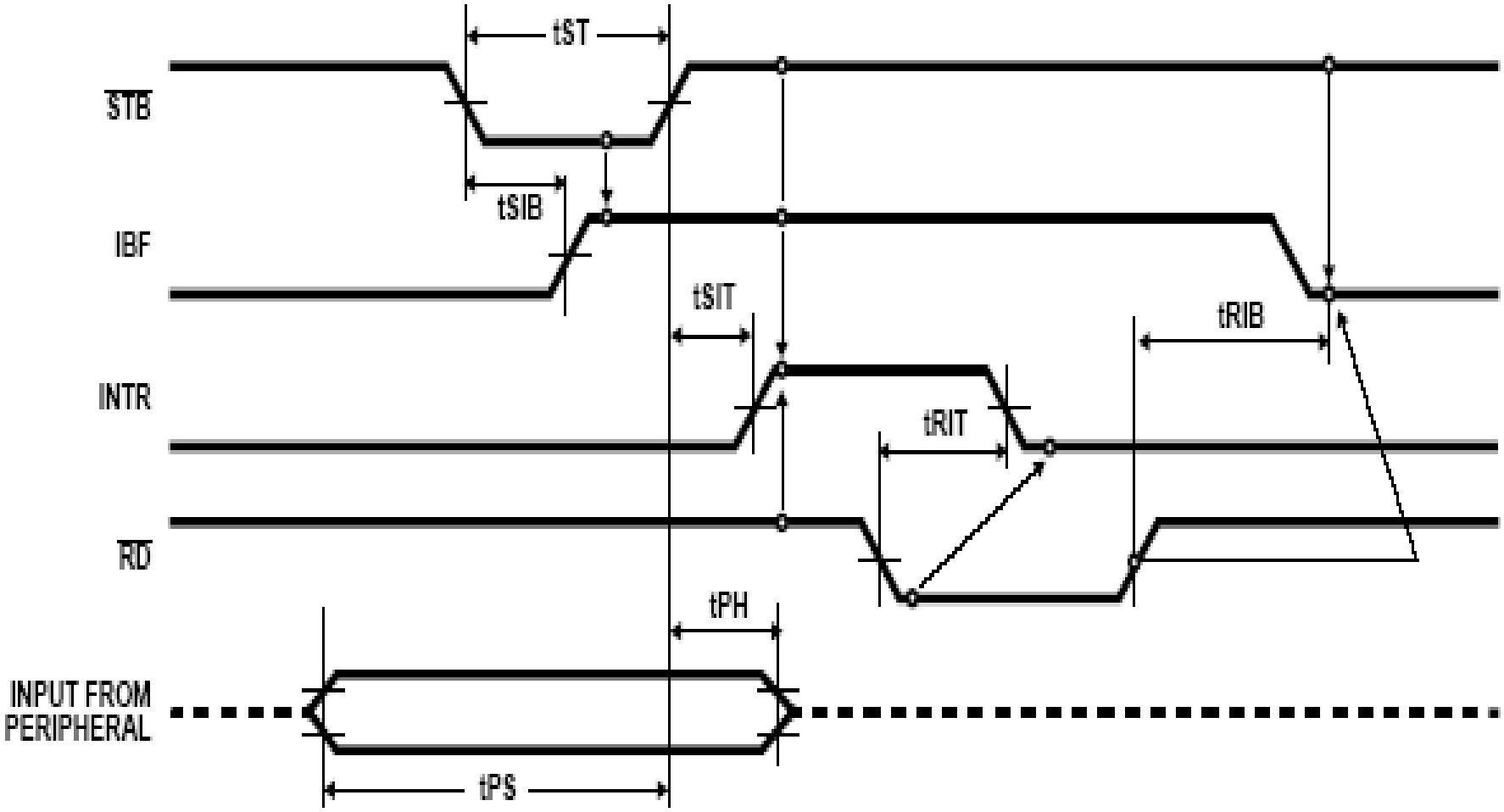


FIGURE 7. MODE 1 (STROBED INPUT)

MODE 1 OUTPUT

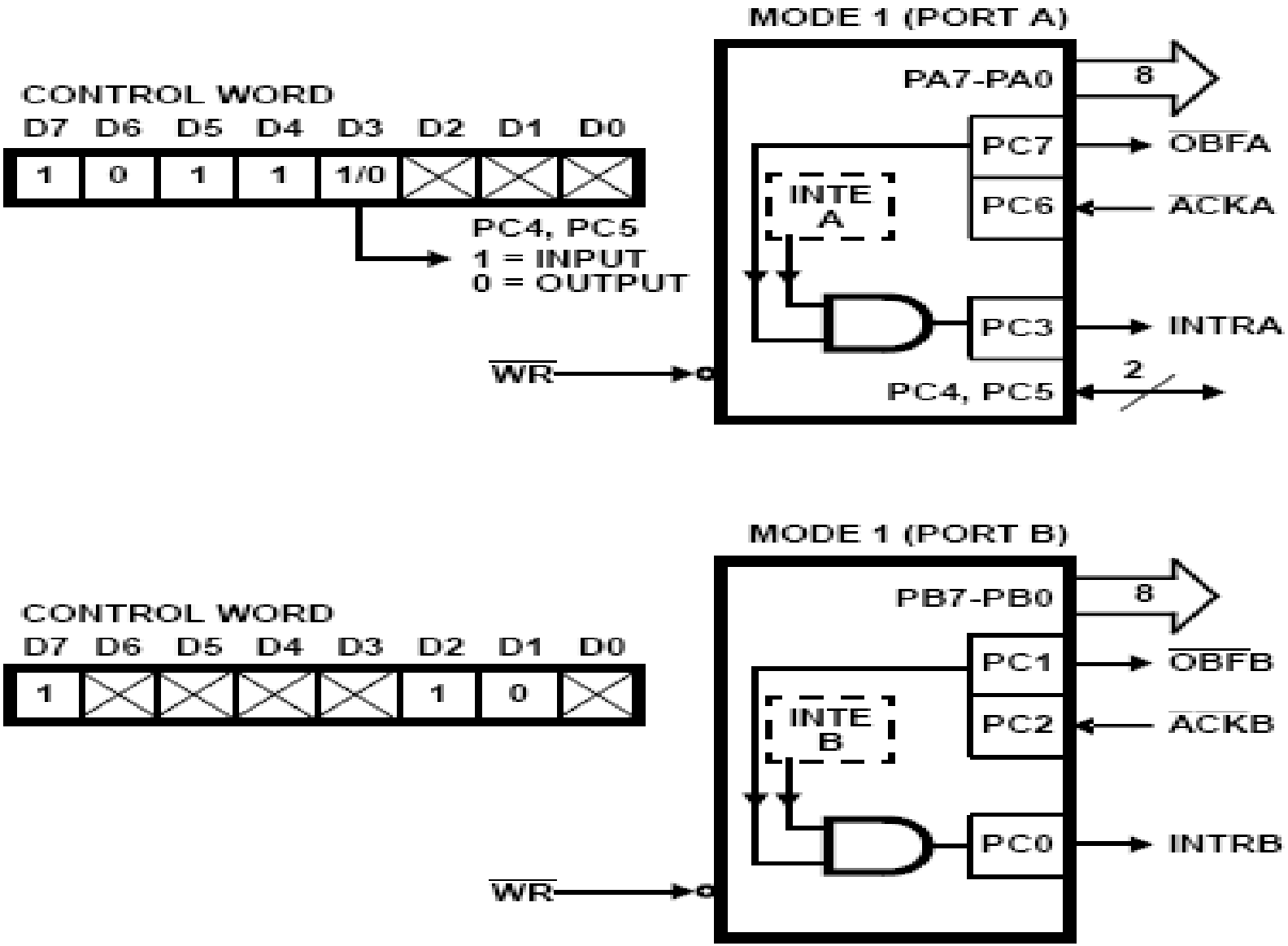


FIGURE 8. MODE 1 OUTPUT

Output Control Signal Definition

- **OBF** - Output Buffer Full F/F). The OBF output will go “low” to indicate that the CPU has written data out to be specified port. This does not mean valid data is sent out of the part at this time since OBF can go true before data is available. Data is guaranteed valid at the rising edge of OBF. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

- **ACK** - Acknowledge Input). A “low” on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data,

Output Control Signal Definition

- **INTR -** (Interrupt Request). A “high” on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a “one”, OBF is a “one” and INTE is a “one”. It is reset by the falling edge of WR.
- **INTE A**

Controlled by Bit Set/Reset of PC 6.

- **INTE B**

Controlled by Bit Set/Reset of PC 2.

- NOTE:

  To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send OBF to the peripheral device, generates an ACK from the peripheral device and then latch data into the peripheral device on the rising edge of OBF.

Output Control Signal

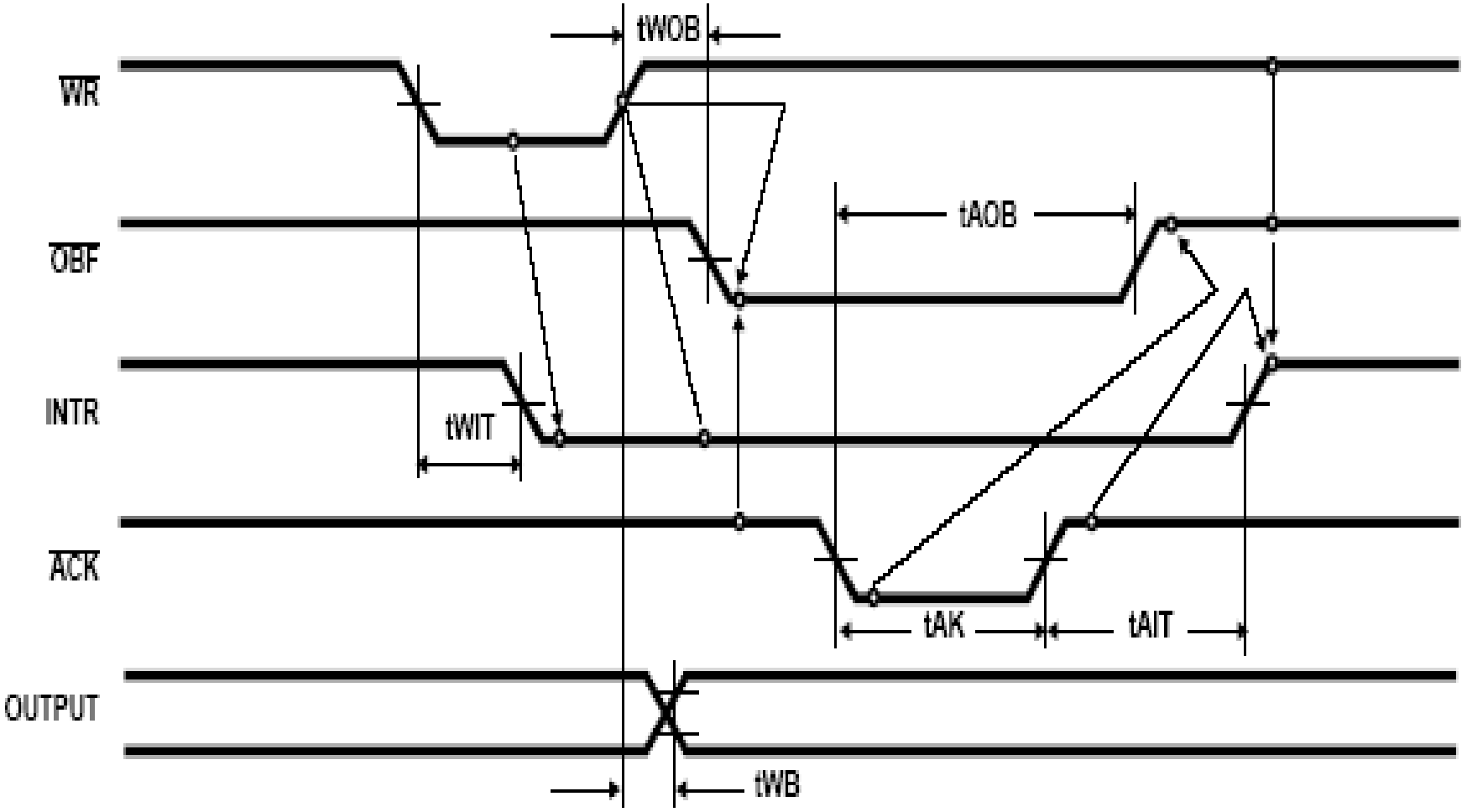
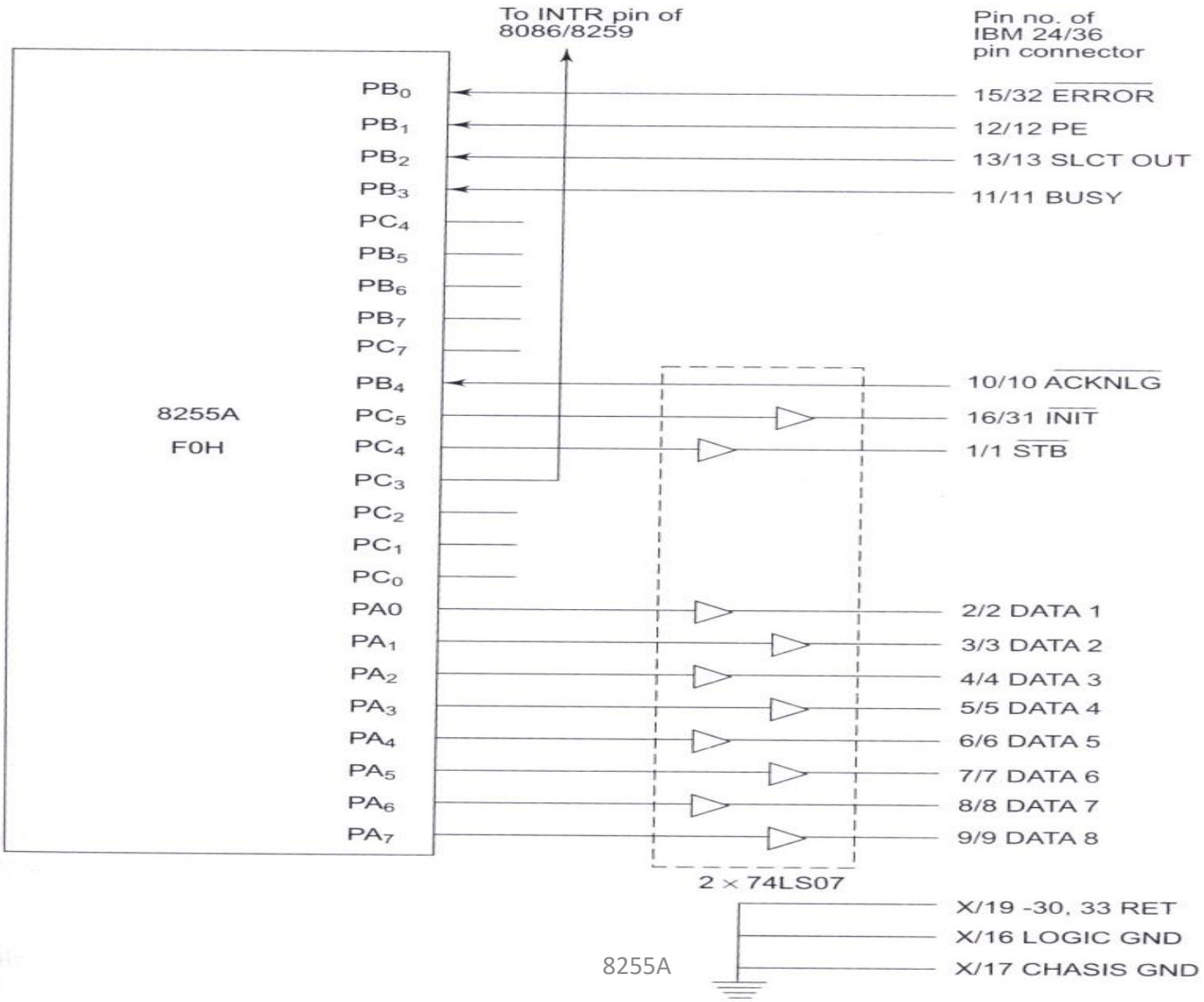


FIGURE 9. MODE 1 (STROBED OUTPUT)

Mode 1 example



Mode 2 (Strobed Bi-Directional Bus I/O)

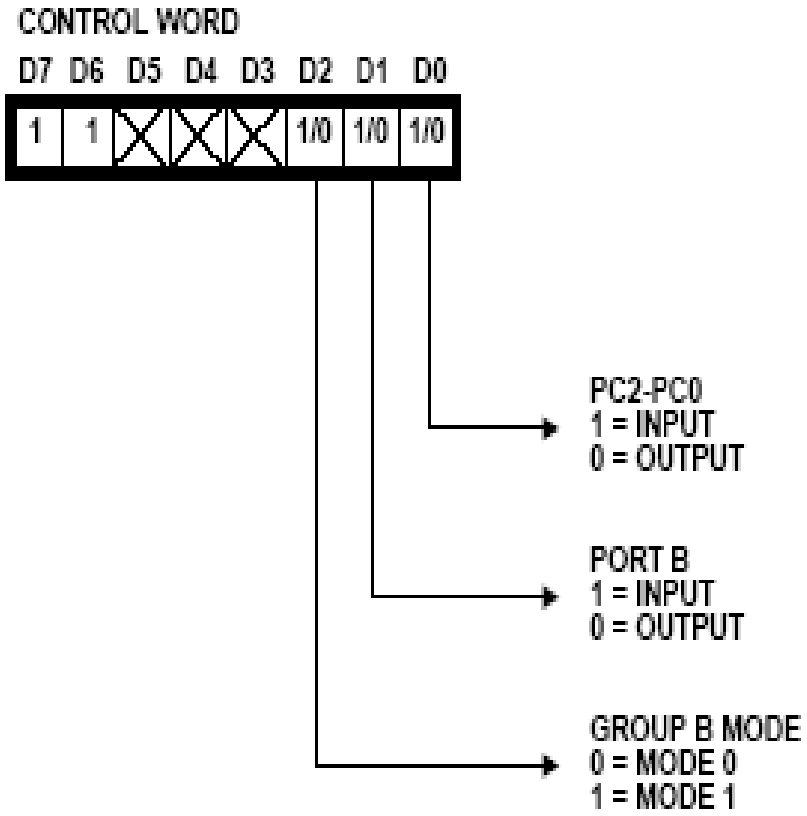


FIGURE 11. MODE CONTROL WORD

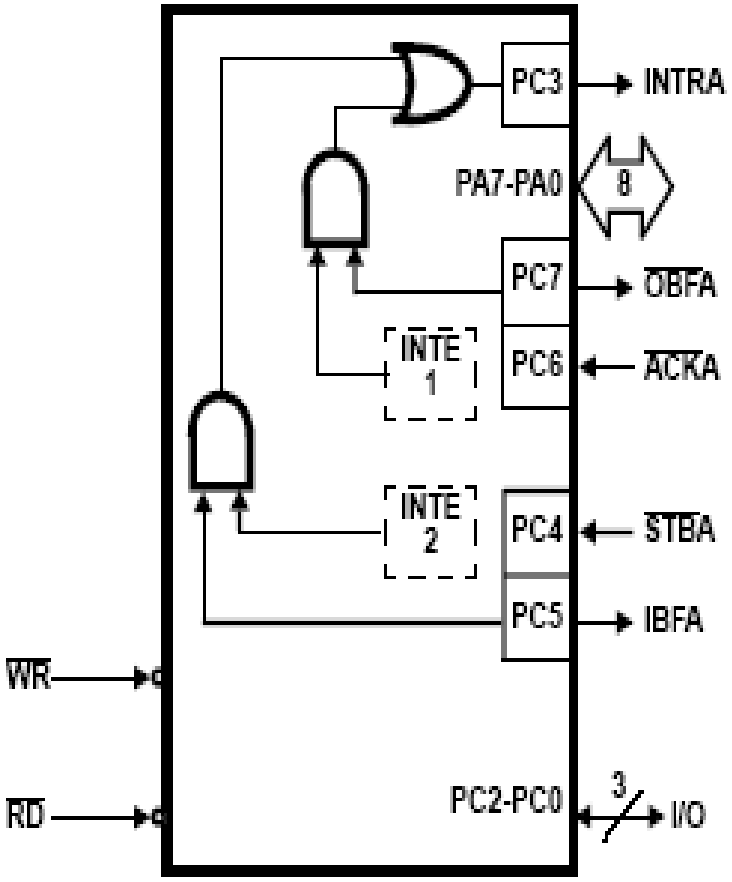


FIGURE 12. MODE 2

Mode 2 (Strobed Bi-Directional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). “Hand shaking” signals are provided to maintain proper bus flow discipline similar to Mode 1. Interrupt generation and enable/disable functions are also available

Mode 2 Basic Functional Definitions:

- Used in Group A only
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C)
- Both inputs and outputs are latched
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)

Bi-Directional Bus I/O Control Signal Definition

- **INTR** - (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

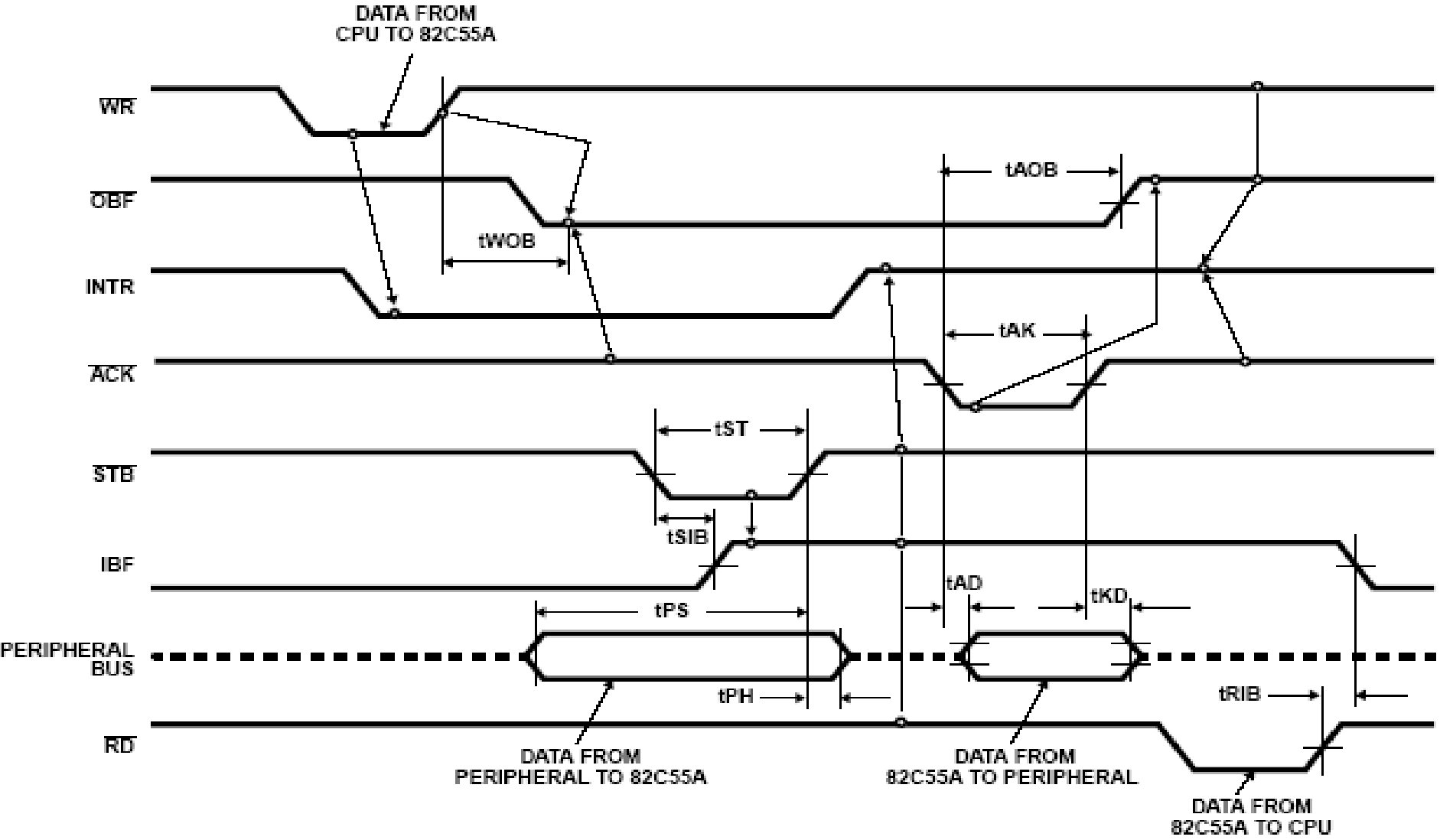
Output Operations

- **OBF** - (Output Buffer Full). The OBF output will go “low” to indicate that the CPU has written data out to port A.
- **ACK** - (Acknowledge). A “low” on this input enables the three-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.
- **INTE 1** - (The INTE flip-flop associated with OBF). Controlled by bit set/reset of PC4.

Input Operations

- **STB** - (Strobe Input). A “low” on this input loads data into the input latch.
- **IBF** - (Input Buffer Full F/F). A “high” on this output indicates that data has been loaded into the input latch.
- **INTE 2** - (The INTE flip-flop associated with IBF). Controlled by bit set/reset of PC4.

Bi-Directional Bus I/O Control Signal



NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before RD is permissible. (INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

FIGURE 13. MODE 2 (BI-DIRECTIONAL)

Mode 2

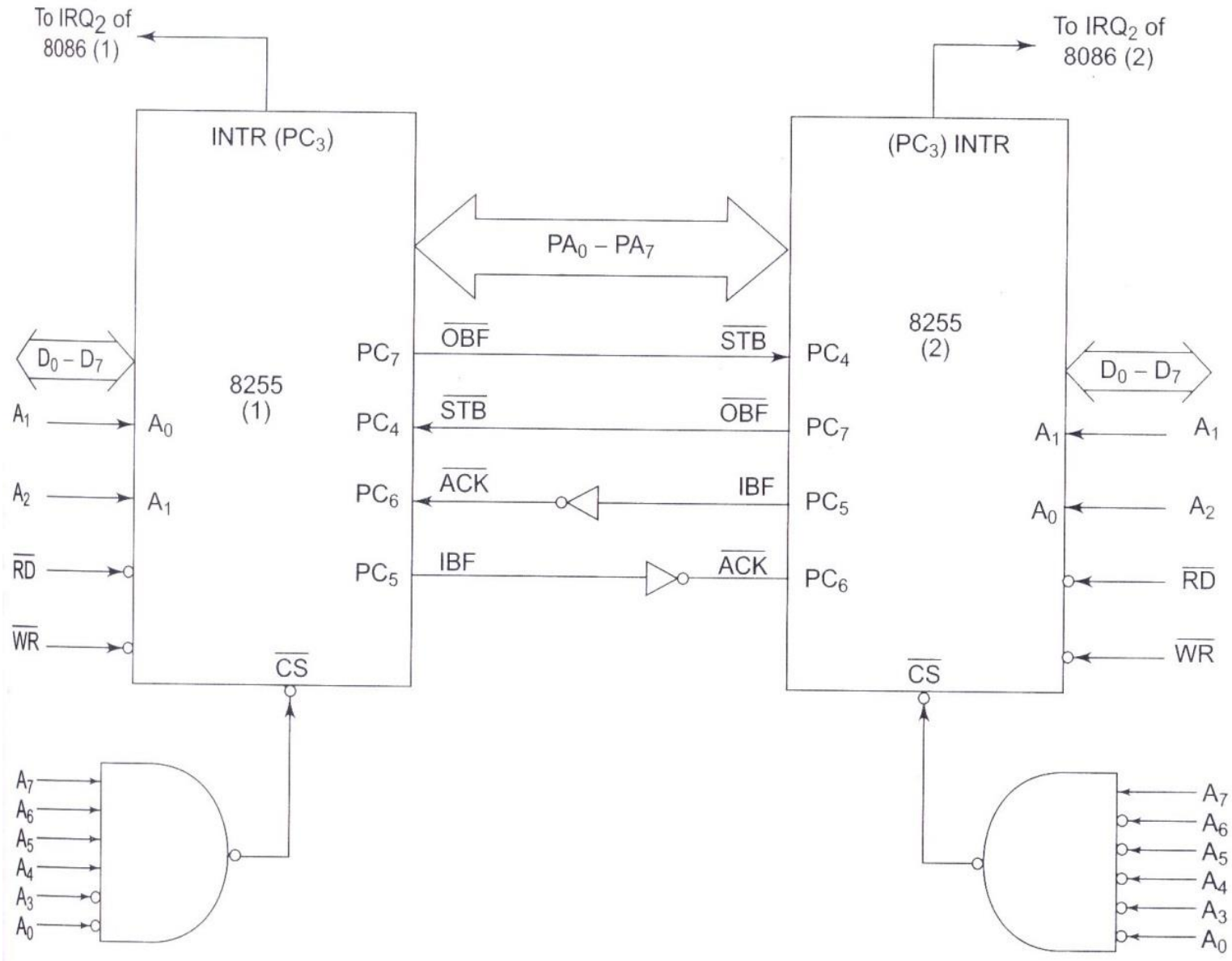


Fig. 5.36 *Interconnections between the two 8255s in Mode 2 for Problem 5.16*