

Timing Diagram of 8085

Timing Diagram is a graphical representation. It represents the execution time taken by each instruction in a graphical format. The execution time is represented in T-states.

Instruction Cycle:

The time required to execute an instruction .

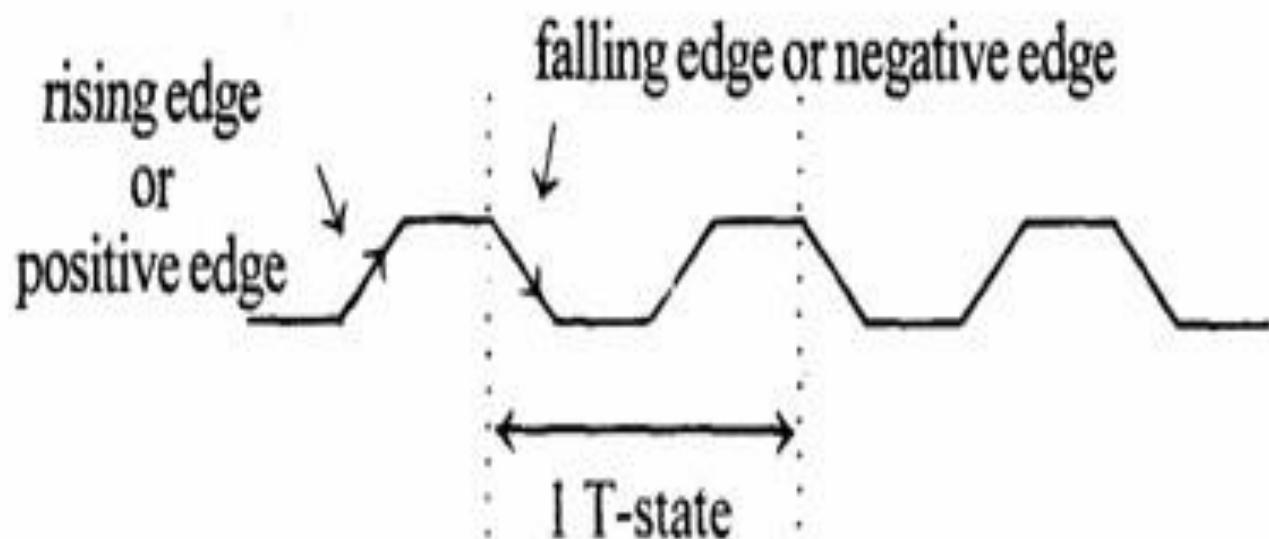
Machine Cycle:

The time required to access the memory or input/output devices .

T-State:

- The machine cycle and instruction cycle takes multiple clock periods.
- A portion of an operation carried out in one system clock period is called as T-state.

Note : Time period, $T = 1/f$; where $f = \text{Internal clock frequency}$



Timing diagrams

- The 8085 microprocessor has 7 basic machine cycle. They are
 1. Op-code Fetch cycle(4T or 6T).
 2. Memory read cycle (3T)
 3. Memory write cycle(3T)
 4. I/O read cycle(3T)
 5. I/O write cycle(3T)
 6. Interrupt Acknowledge cycle(6T or 12T)
 7. Bus idle cycle

Machine Cycle	Status			No. of Machine cycles	Control
	IO/ \overline{M}	S1	S0		
Opcode Fetch	0	1	1	4	$\overline{RD} = 0$
Memory Read	0	1	0	3	$\overline{RD} = 0$
Memory Write	0	0	1	3	$\overline{WR} = 0$
I/O Read	1	1	0	3	$\overline{RD} = 0$
I/O Write	1	0	1	3	$\overline{WR} = 0$
INTR Acknowledge	1	1	1	3	$\overline{INTA} = 0$

Opcode fetch cycle of 8085

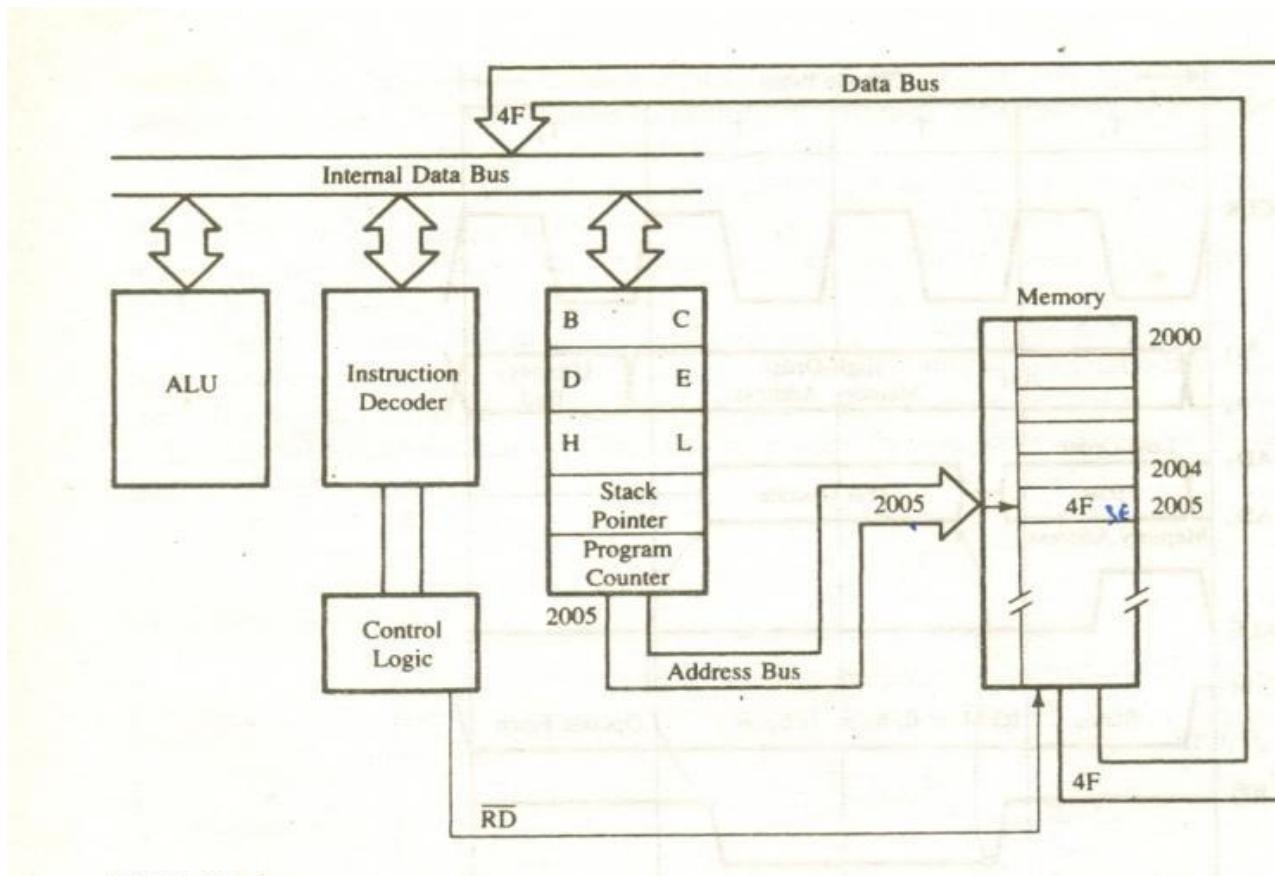
Instruction:

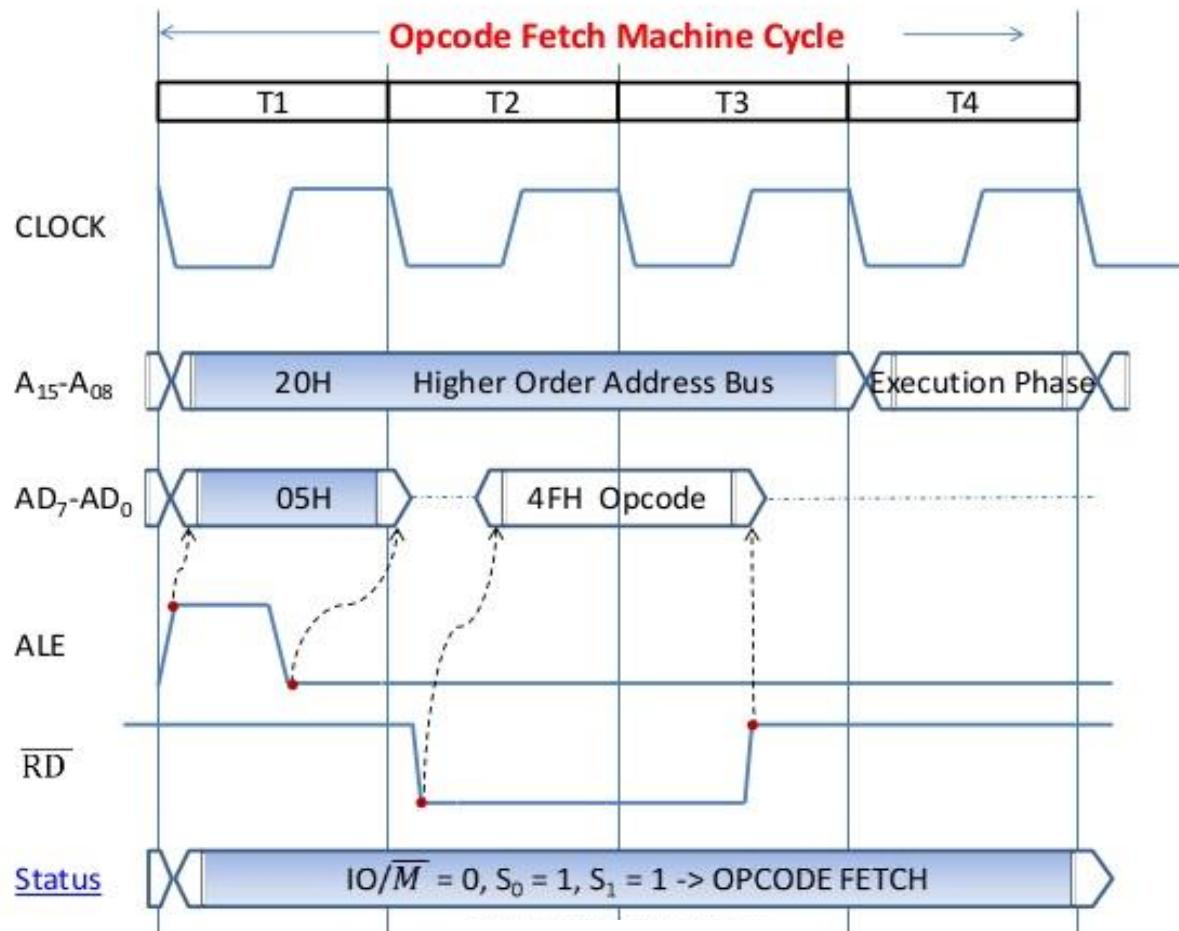
MOV A,C

OPCODE stored at 2005 as:

2005 4F

Opcode fetch cycle of





1-byte instruction

MOV A,B

ADD B

RLC

2-byte instruction

MVI

ADI

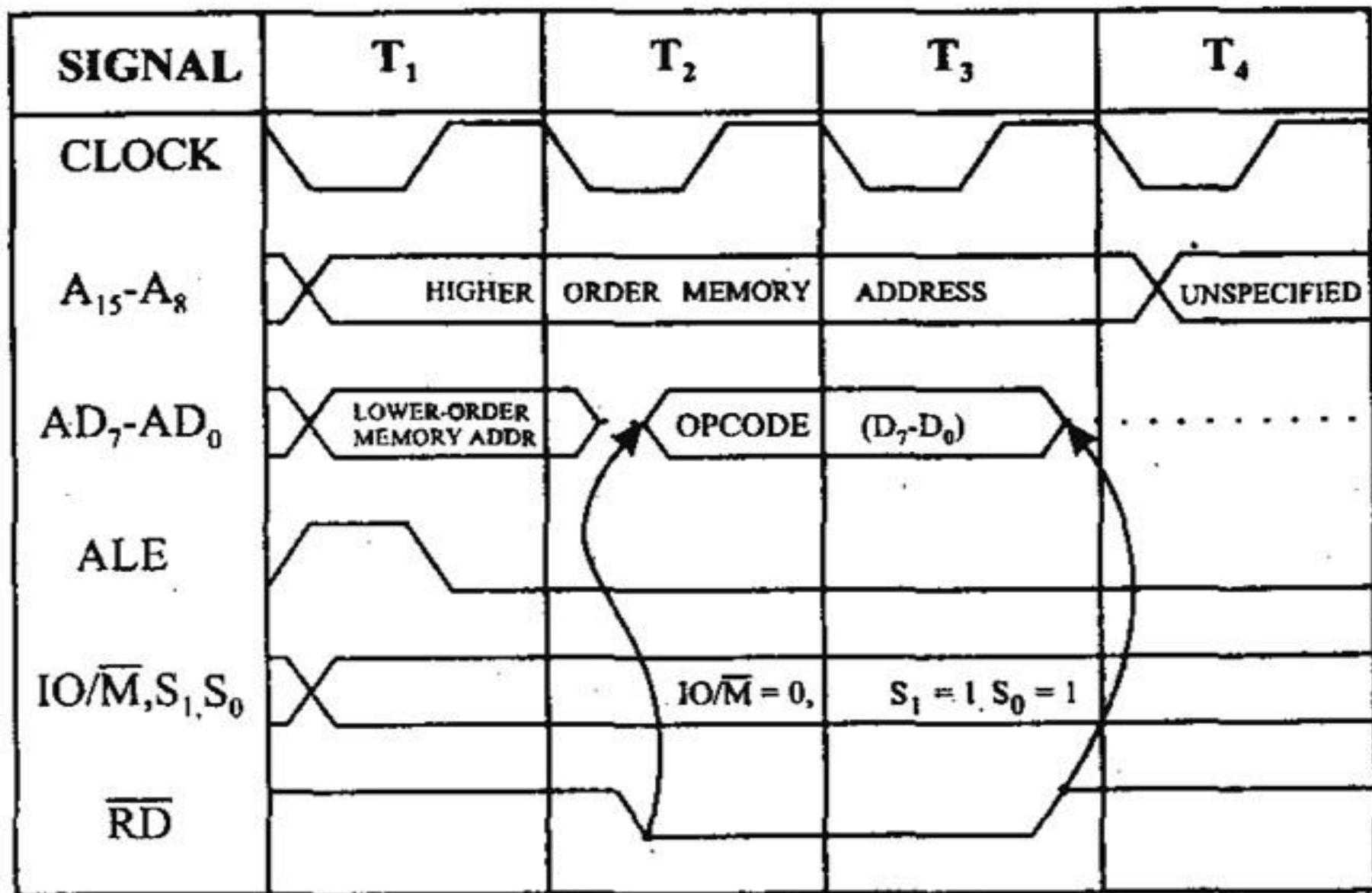
3-byte instruction

LDA

STA

LXI

1.Opcode fetch cycle(4T or 6T)



OPCODE FETCH

- The Opcode fetch cycle, fetches the instructions from memory and delivers it to the instruction register of the microprocessor
- Opcode fetch machine cycle consists of **4 T-states**.

T1 State:

During the T1 state, the contents of the program counter are placed on the 16 bit address bus. The **higher order 8 bits** are transferred to address bus (**A8-A15**) and **lower order 8 bits** are transferred to multiplexed A/D (**AD0-AD7**)bus.

ALE (address latch enable) signal goes **high**. As soon as ALE goes high, the memory latches the AD0-AD7 bus. At the middle of the Tstate the **ALE goes low**

T2 State:

During the beginning of this state, the **RD' signal goes low** to enable memory. It is during this state, the selected memory location is placed on D0-D7 of the Address/Data multiplexed bus.

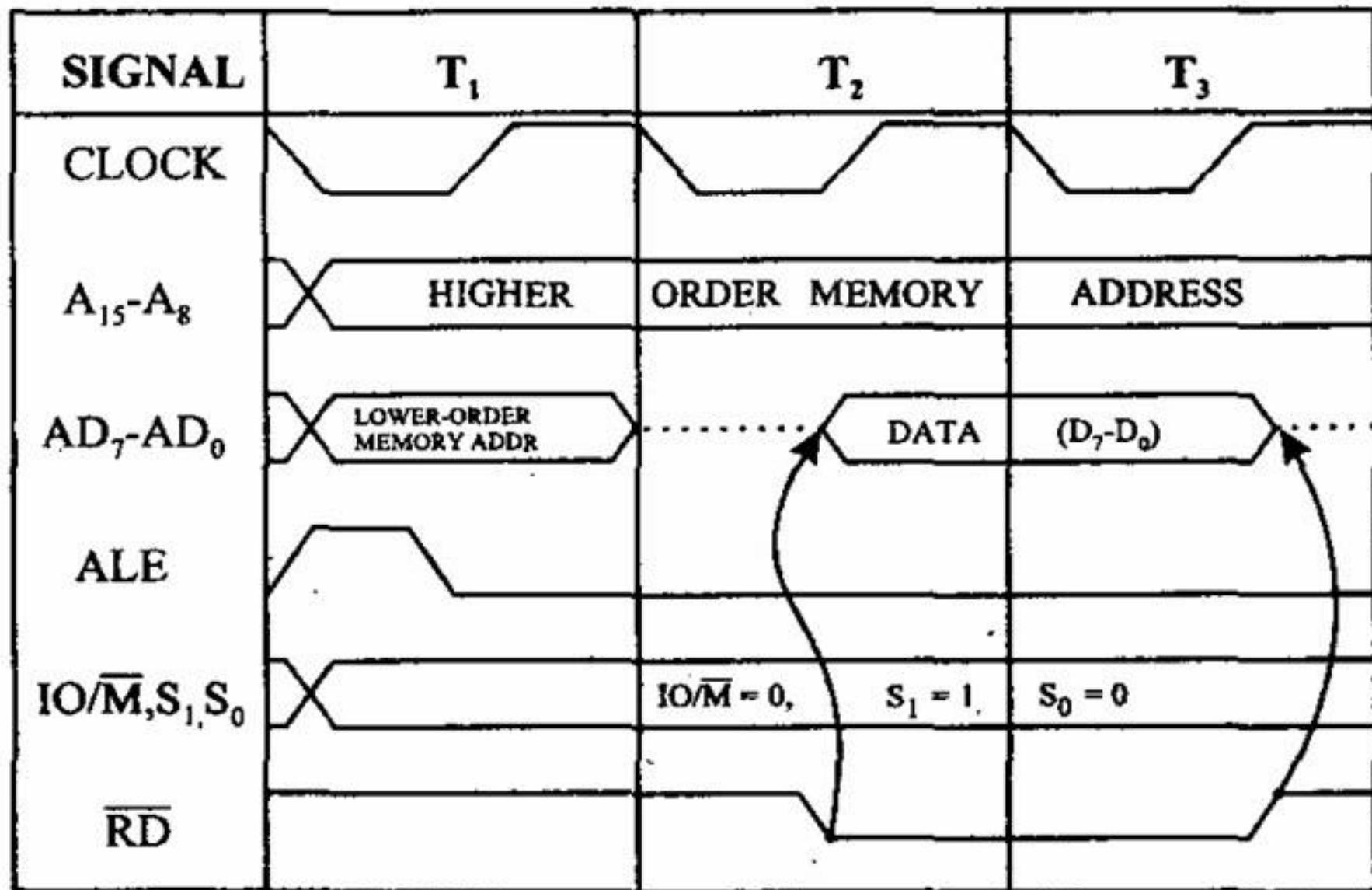
T3 State:

In the previous state the Opcode is placed in D0-D7 of the A/D bus. In this state of the cycle, the Opcode of the A/D bus is transferred to the instruction register of the microprocessor. Now the **RD' goes high** after this action and thus disables the memory from A/D bus.

T4 State:

In this state the Opcode which was fetched from the memory is decoded.

2. Memory read cycle (3T)



- These machine cycles have 3 T-states.

T1 state:

- The higher order address bus (**A8-A15**) and lower order address and data multiplexed (**AD0-AD7**) bus. **ALE goes high** so that the memory latches the (**AD0-AD7**) so that complete 16-bit address are available.

The mp identifies the memory read machine cycle from the status signals **IO/M'=0, S1=1, S0=0**. This condition indicates the memory read cycle.

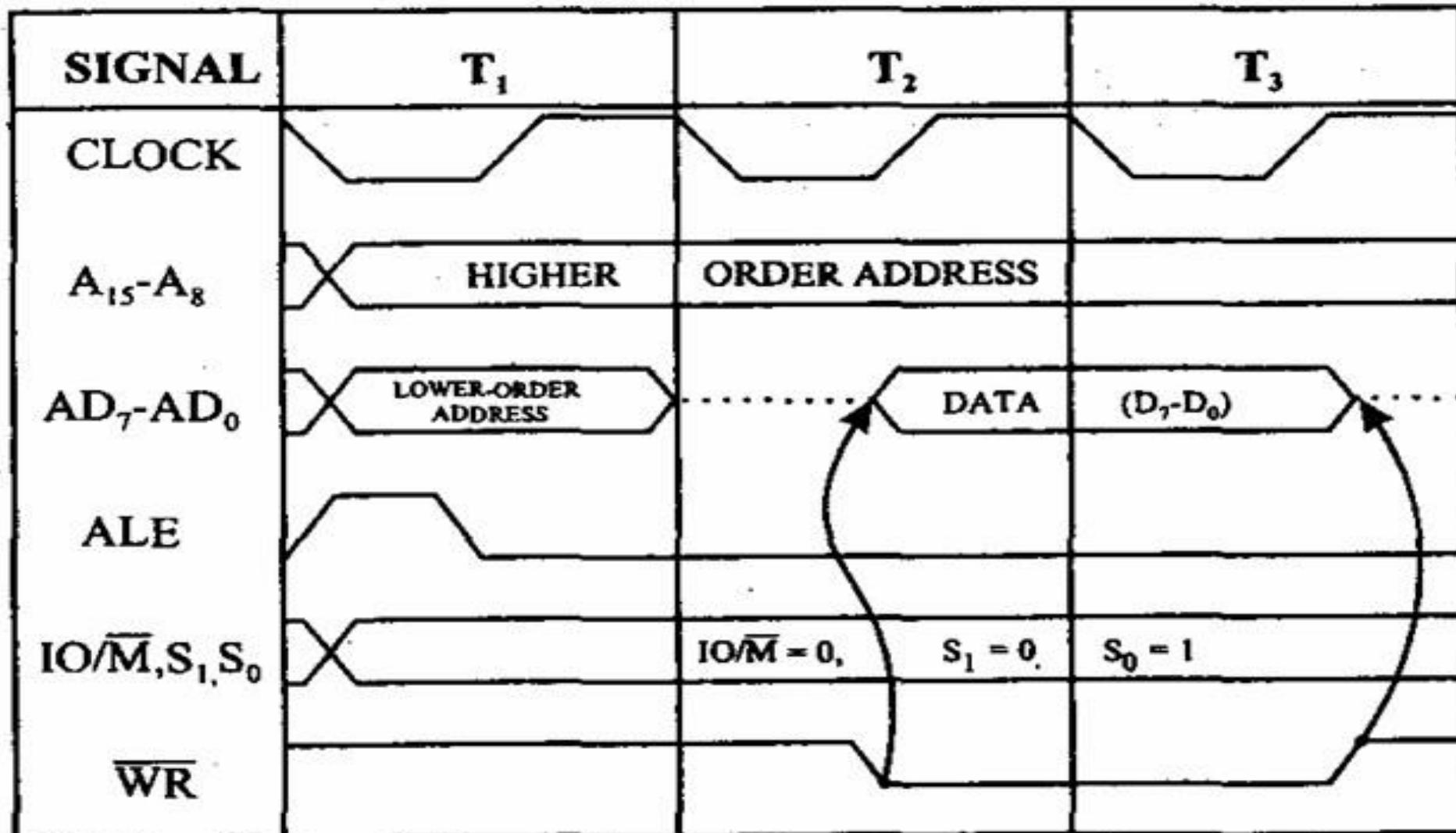
T2 state:

- Selected memory location is placed on the (**D0-D7**) of the A/D multiplexed bus. **RD'** goes **LOW**

T3 State:

- The data which was loaded on the previous state is transferred to the microprocessor. In the middle of the T3 state **RD'** goes high and disables the memory read operation. The data which was obtained from the memory is then decoded.

3. Memory write cycle (3T)



- These machine cycles have 3 T-states.

T1 state:

- The higher order address bus (**A8-A15**) and lower order address and data multiplexed (**AD0-AD7**) bus. **ALE goes high** so that the memory latches the (AD0-AD7) so that complete 16-bit address are available.

The mp identifies the memory read machine cycle from the status signals **IO/M'=0, S1=0, S0=1**. This condition indicates the memory read cycle.

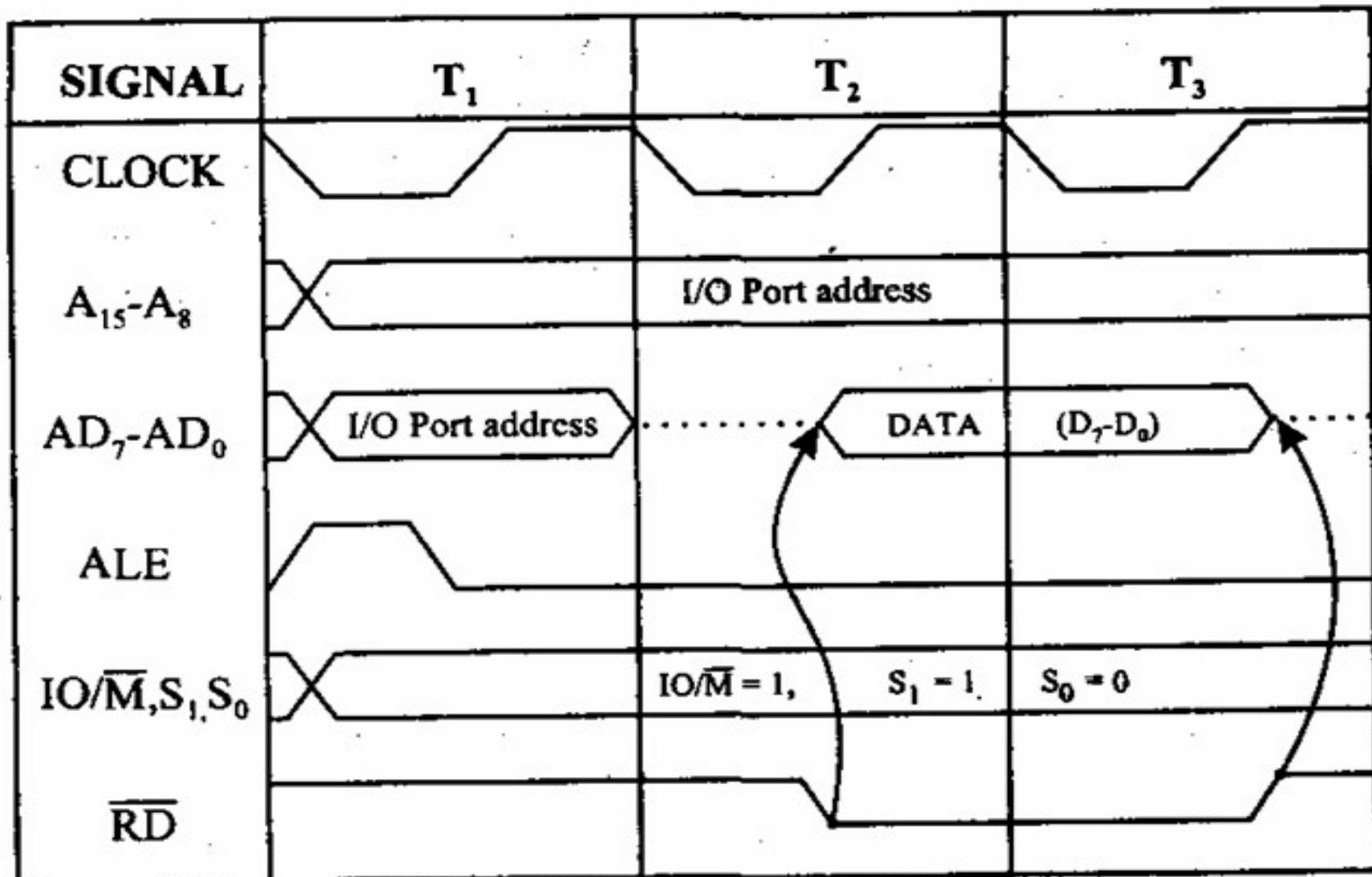
T2 state:

- Selected memory location is placed on the (D0-D7) of the A/D multiplexed bus. **WR'** goes **LOW**

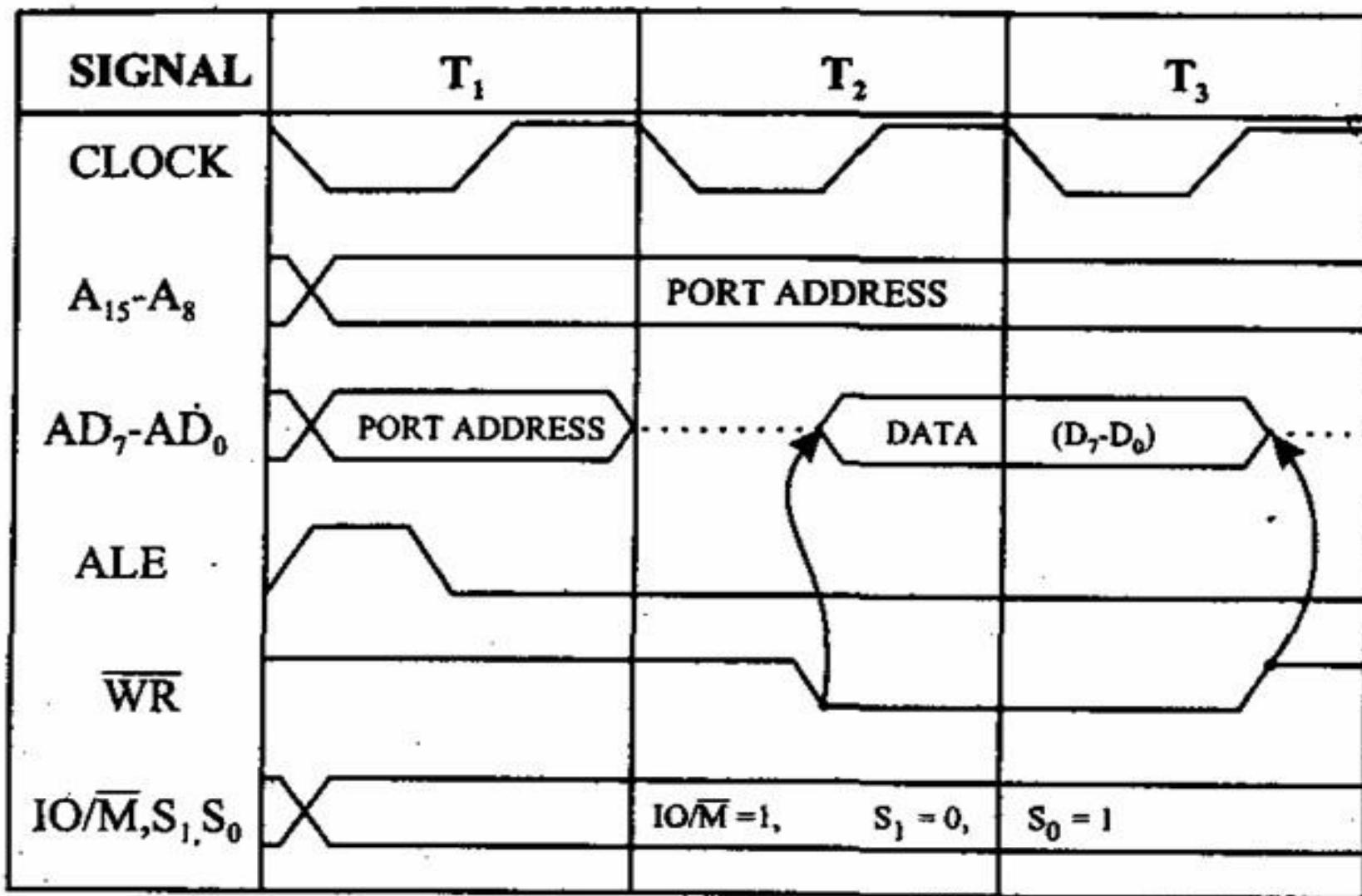
T3 State:

- In the middle of the T3 state **WR'** goes **high** and **disables the memory write operation**. The data which was obtained from the memory is then decoded.

4.I/O read cycle(3T)



5.I/O write cycle(3T)



STA instruction

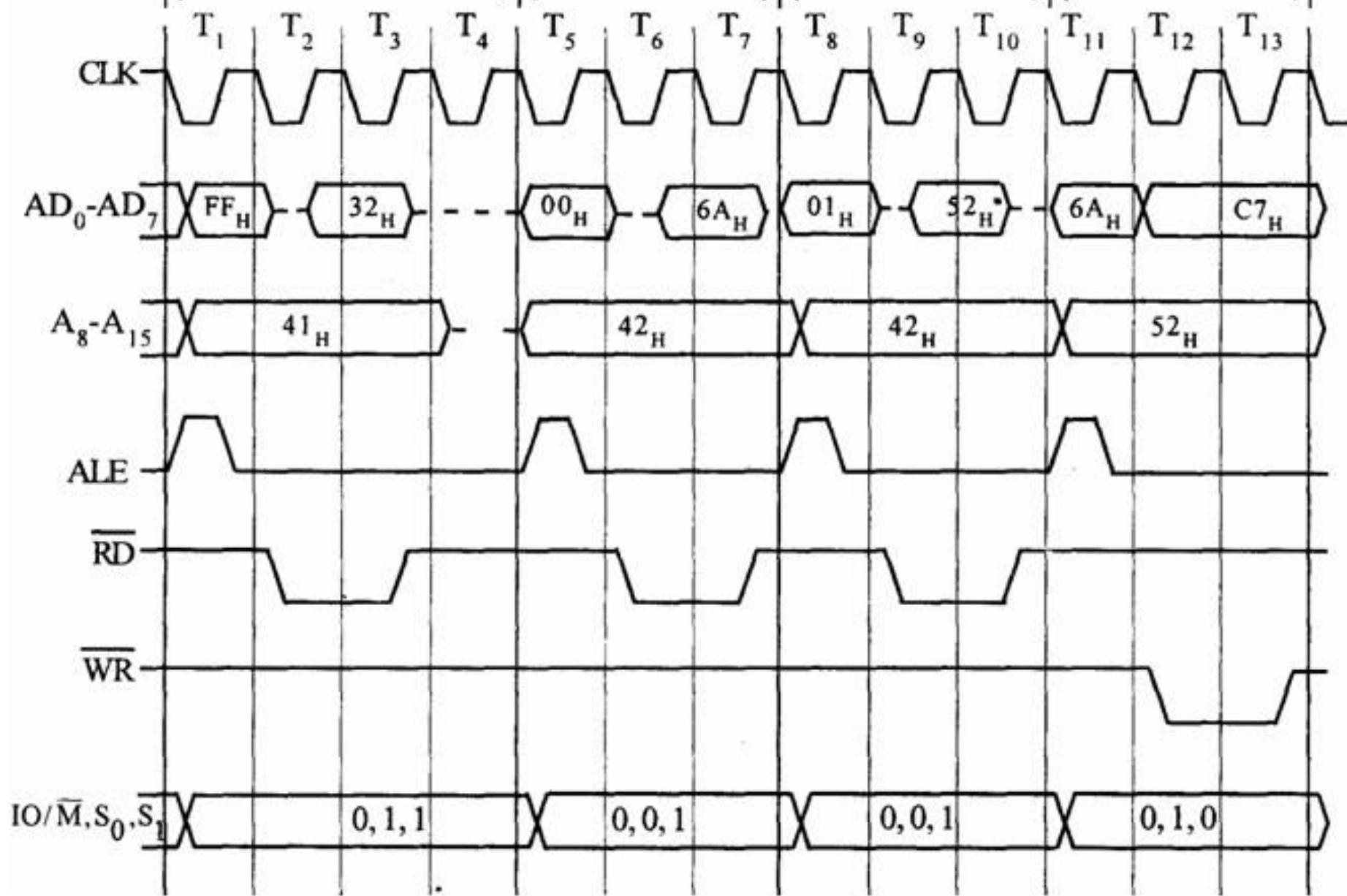
ex: **STA 526A**

Address	Mnemonics	Op code
41FF	STA 526AH	32H
4200		6AH
4201		52H

It require 4 m/c cycles 13 T states

- 1.opcode fetch(4T)
- 2.memory read(3T)
- 3.memory read(3T)
- 4.Memory write(3T)

Opcode fetch Memory read Memory read Memory write



Timing diagram for IN C0_H

- Fetching the Opcode DB_H from the memory 4125H.
- Read the port address C0_H from 4126H.
- Read the content of port C0_H and send it to the accumulator.
- Let the content of port is 5E_H.

It require 3 m/c cycles 10 T states

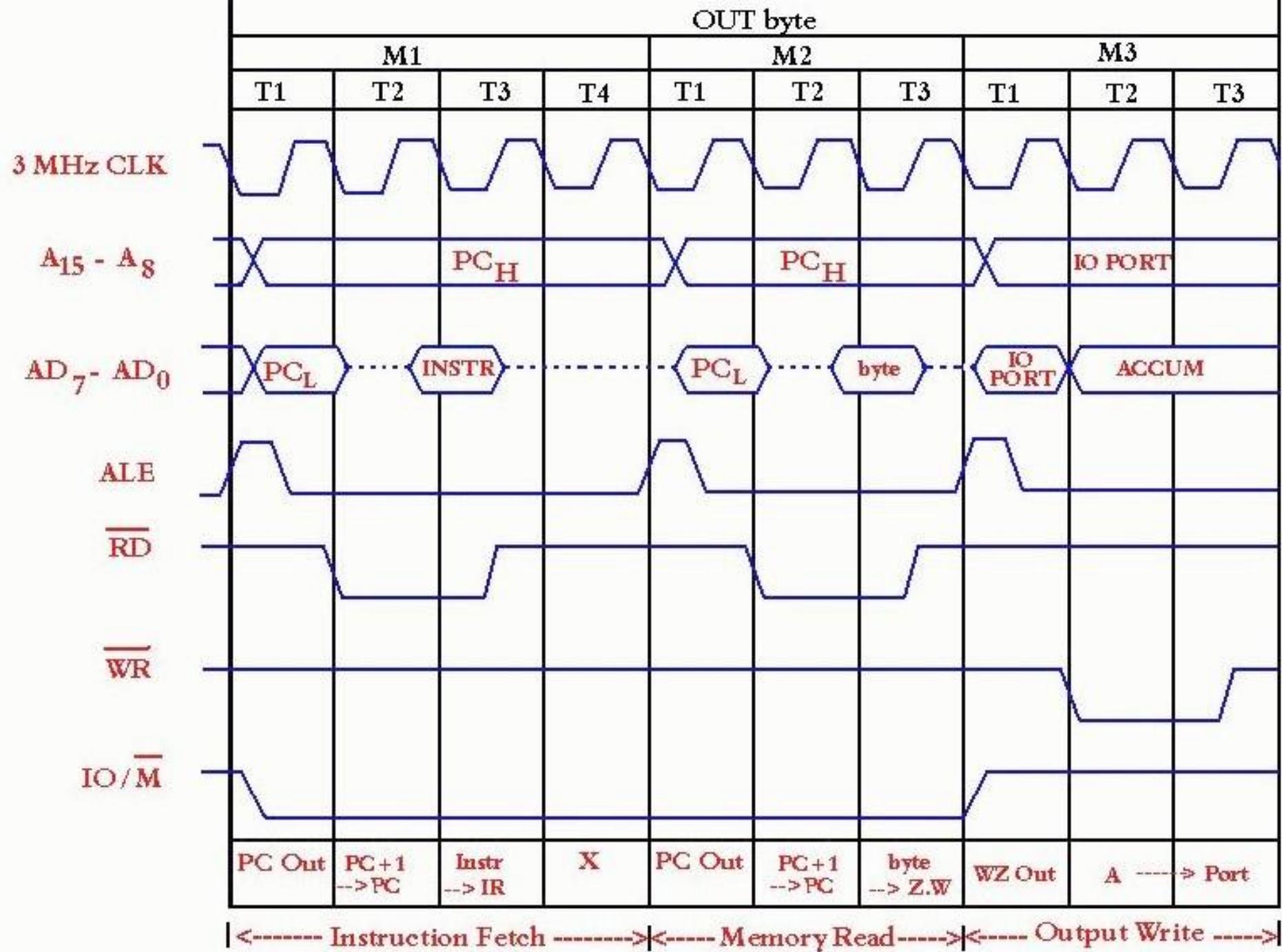
opcode fetch(4T) memory
read(3T) I/O read(3T)

Address	Mnemonics	Op code
4125	IN C0H	DBH
4126		C0H

OUT instruction

Machines Cycles(10T):

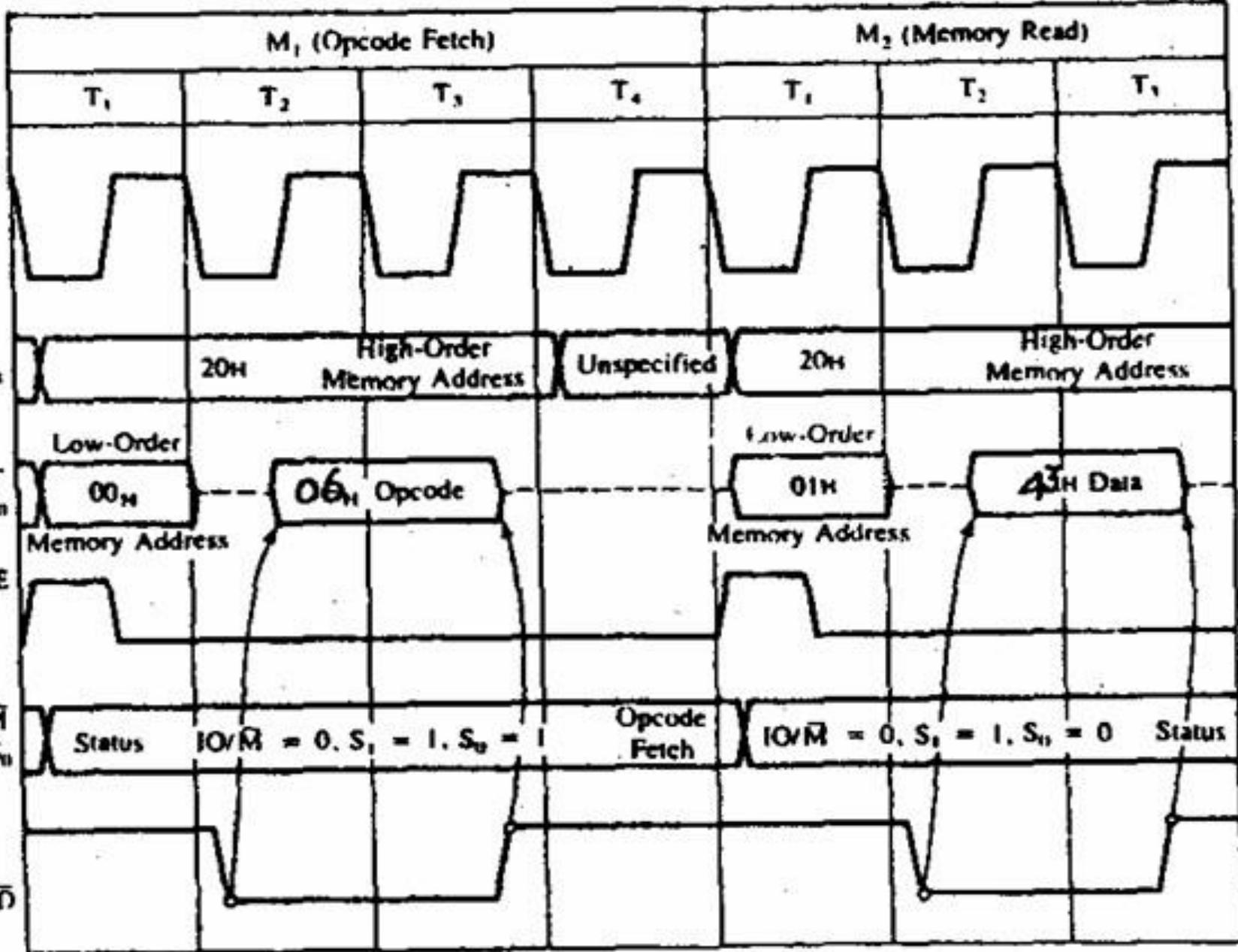
- 1.instruction fetch(4T)**
- 2.memory read (3T)**
- 3.IO write (3T)**

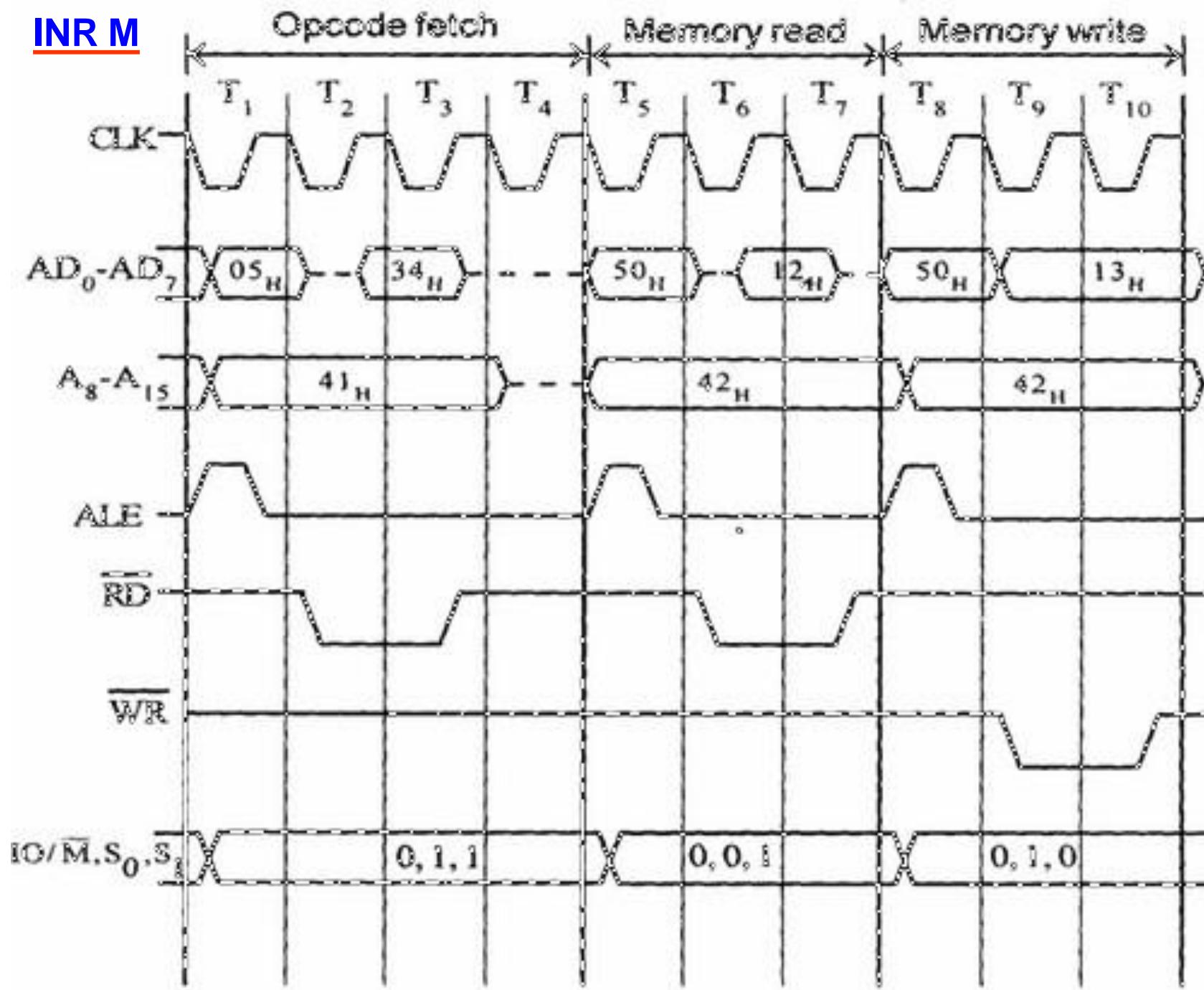


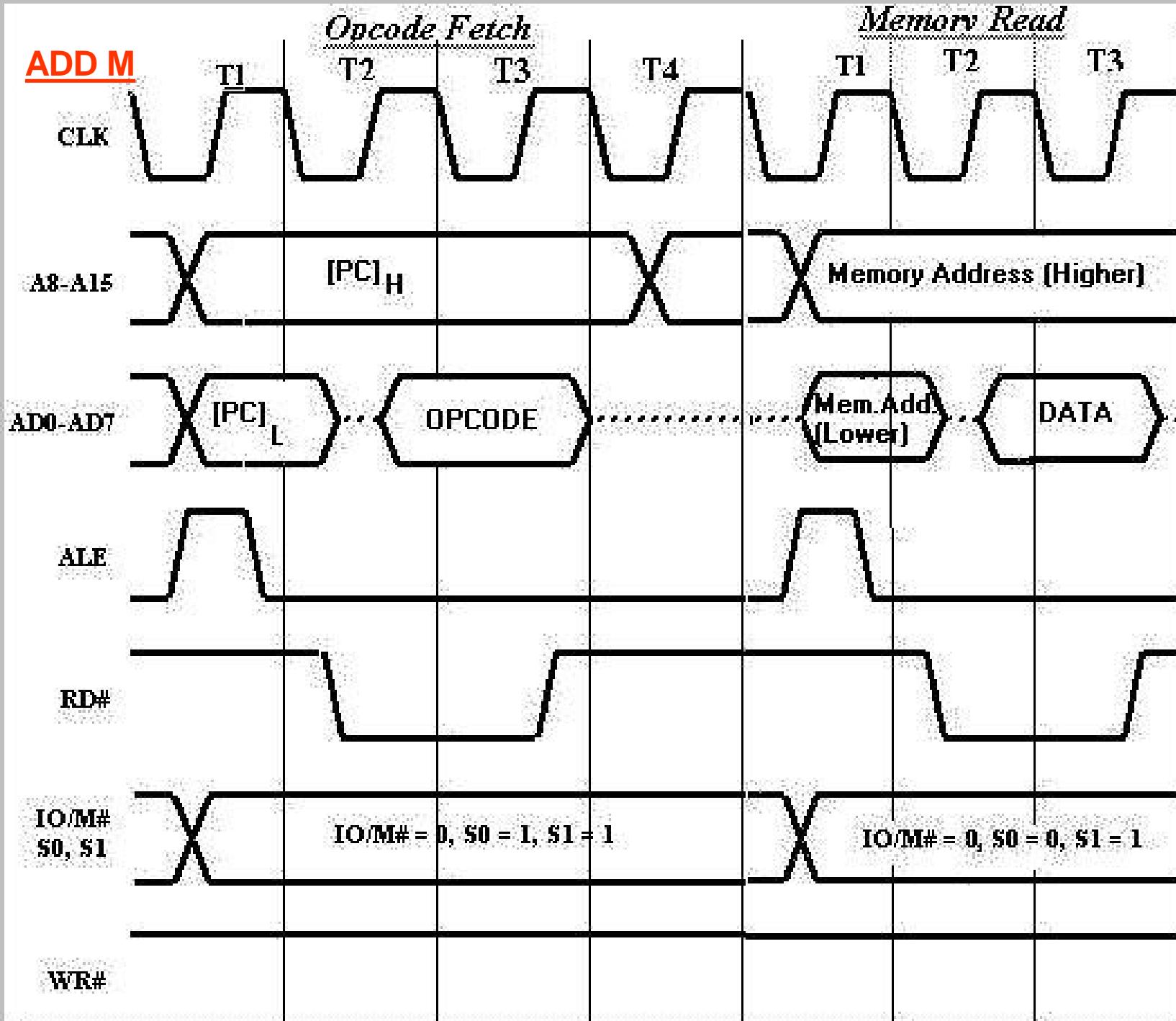
Timing diagram for MVI B, 43H

- Fetching the Opcode 06H from the memory 2000_H. (OF machine cycle)
- Read (move) the data 43H from memory 2001_H. (memory read)

Address	Mnemonics	Op code
2000	MVI B, 43 _H	06 _H
2001		43 _H







DCX

