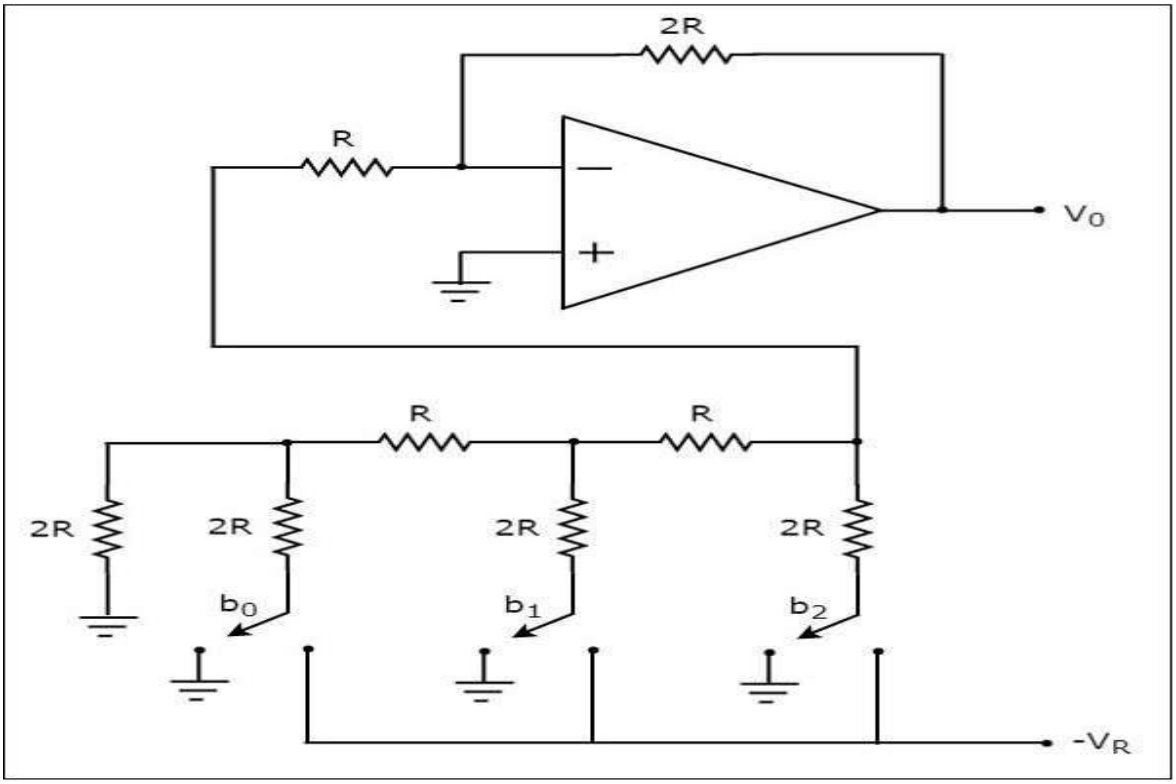
R-2R Ladder DAC

The R-2R Ladder DAC overcomes the disadvantages of a binary weighted resistor DAC. As the name suggests, R-2R Ladder DAC produces an analog output, which is almost equal to the digital (binary) input by using a **R-2R ladder network** in the inverting adder circuit.

The **circuit diagram** of a 3-bit R-2R Ladder DAC is shown in the following figure:



Recall that the bits of a binary number can have only one of the two values. i.e. either 0 or 1. Let the **3-bit binary input** is b2 b1b0. Here, the bits b2 and b0 denote the Most Significant Bit (MSB) and Least Significant Bit (LSB) respectively.

The digital switches shown in the above figure will be connected to ground, when the corresponding input bits are equal to‘0’. Similarly, the digital switches shown in above figure will be connected to the negative reference voltage, −*VR*−VR when the corresponding input bits are equal to ‘1’.

It is difficult to get the generalized output voltage equation of a R-2R Ladder DAC. But, we can find the analog output voltage values of R-2R Ladder DAC for

individual binary input combinations easily.

The **advantages** of a R-2R Ladder DAC are as follows:

- R-2R Ladder DAC contains only two values of resistor: R and 2R. So, it is easy to select and design more accurate resistors.
- If more number of bits is present in the digital input, then we have to include required number of R-2R sections additionally.

Due to the above advantages, R-2R Ladder DAC is preferable over binary weighted resistor DAC.

Resolution of DAC:

- The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter. For example, an 8-bit D/A converter has 2^8-1=255 equal intervals. Hence the smallest change in output voltage is(1/255) of the full scale output range.
- Resolution should be high as possible. It depends on the number of bits in the digital input applied to DAC. Higher the number of bits, higher is the resolution.
- It can also be defined as the ratio of change in analog output voltage resulting from a change of 1LSB at the digital input.

Resolution for n-bit DAC:

The **Resolution** in case of **DAC** is the smallest change in the analog voltage it can detect. This is also known as step size of the DAC. For an n bit **DAC resolution** is calculated by the **formula**;

Resolution= (Range/(2^n-1))

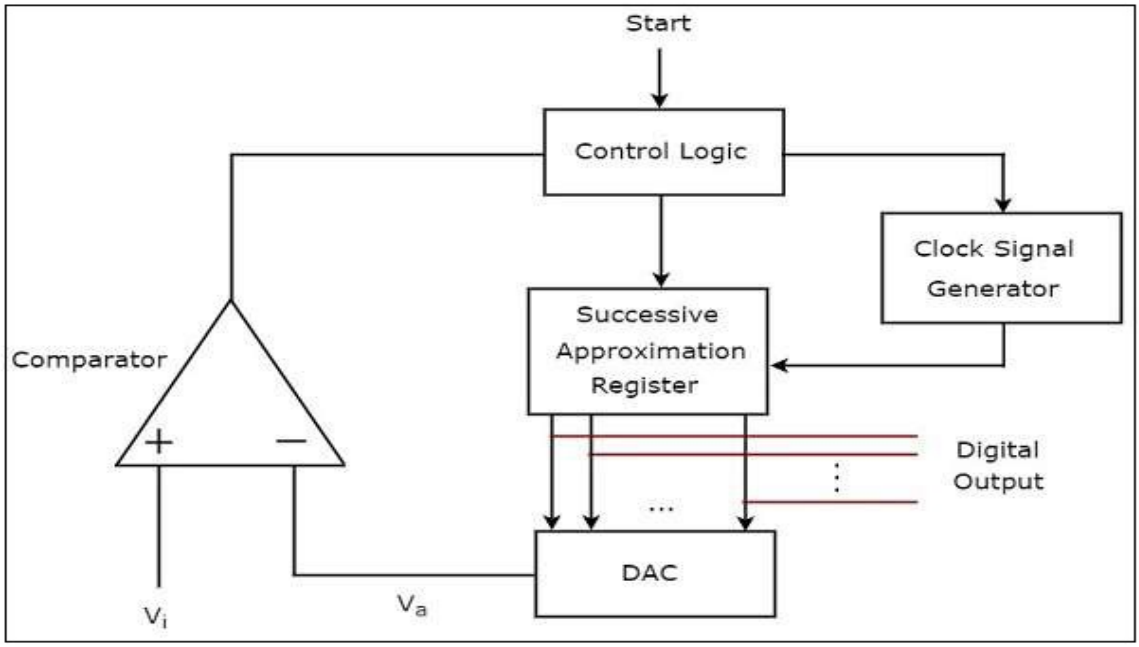
Accuracy:

- Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter outputs.
- Relative accuracy is the maximum deviation after gain and offset errors have been removed.

Successive Approximation ADC

A **successive approximation type ADC** produces a digital output, which is approximately equal to the analog input by using successive approximation technique internally.

The **block diagram** of a successive approximation ADC is shown in the following figure



The successive approximation ADC mainly consists of 5 blocks− Clock signal generator, Successive Approximation Register (SAR), DAC, comparator and Control logic.

The **working** of a successive approximation ADC is as follows –

- The **control logic** resets all the bits of SAR and enables the clock signal generator in order to send the clock pulses to SAR, when it received the start commanding signal.
- The binary (digital) data present in **SAR** will be updated for every clock pulse based on the output of comparator. The output of SAR is applied as an input of DAC.
- **DAC** converts the received digital input, which is the output of SAR, into an analog output. The comparator compares this analog value Va with the external analog input value Vi.
- The **output of a comparator** will be '1' as long as Vi is greater than Va. Similarly, the output of comparator will be '0', when Vi is less than or equal to Va.
- The operations mentioned in above steps will be continued until the digital output is a valid one.

The digital output will be a valid one, when it is almost equivalent to the corresponding external analog input value Vi.