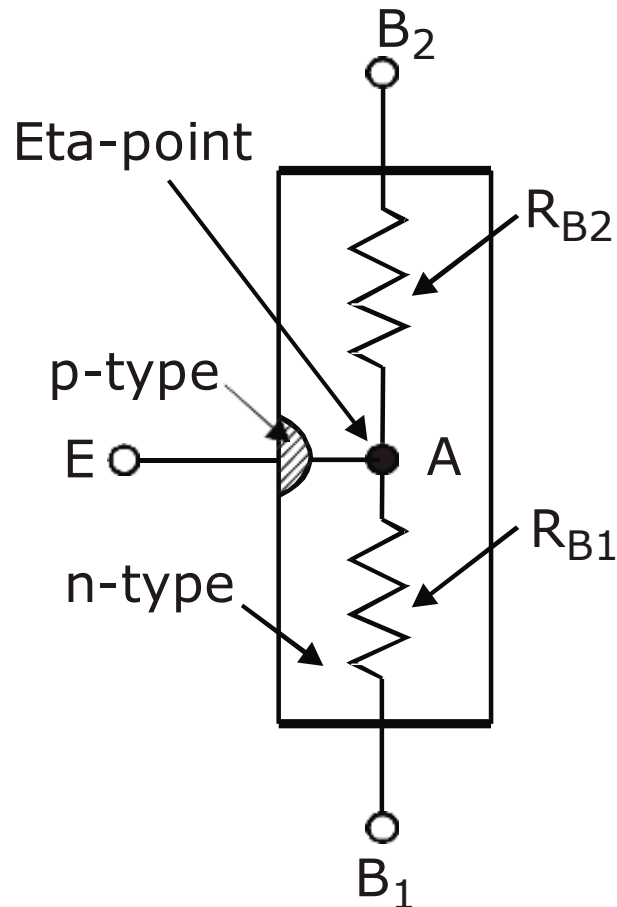


UJT Based Triggering Circuit

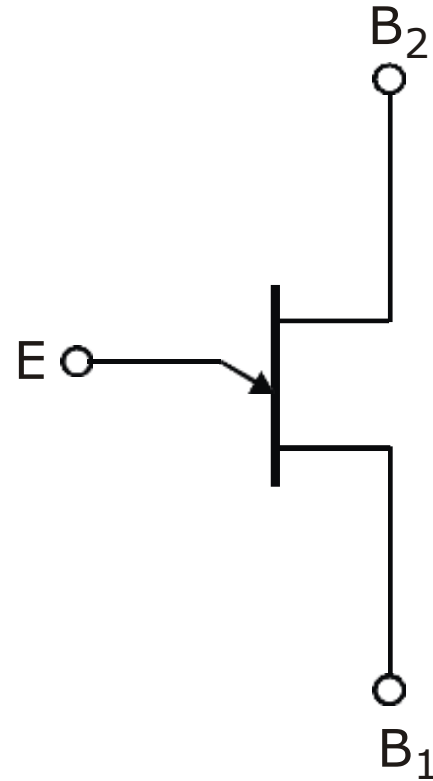
Introduction

- Three terminal single junction latching device*
- Different from either diode (due to 3 terminals) or the transistor (can't amplify)
- Wide range of applications like oscillators, **trigger circuits**, sawtooth generators, phase control
- Overcomes the limitations of previous trigger circuits like power dissipation & high dependability on the SCR characteristics
- Other variants include CUJT & PUT

Structure & Symbol

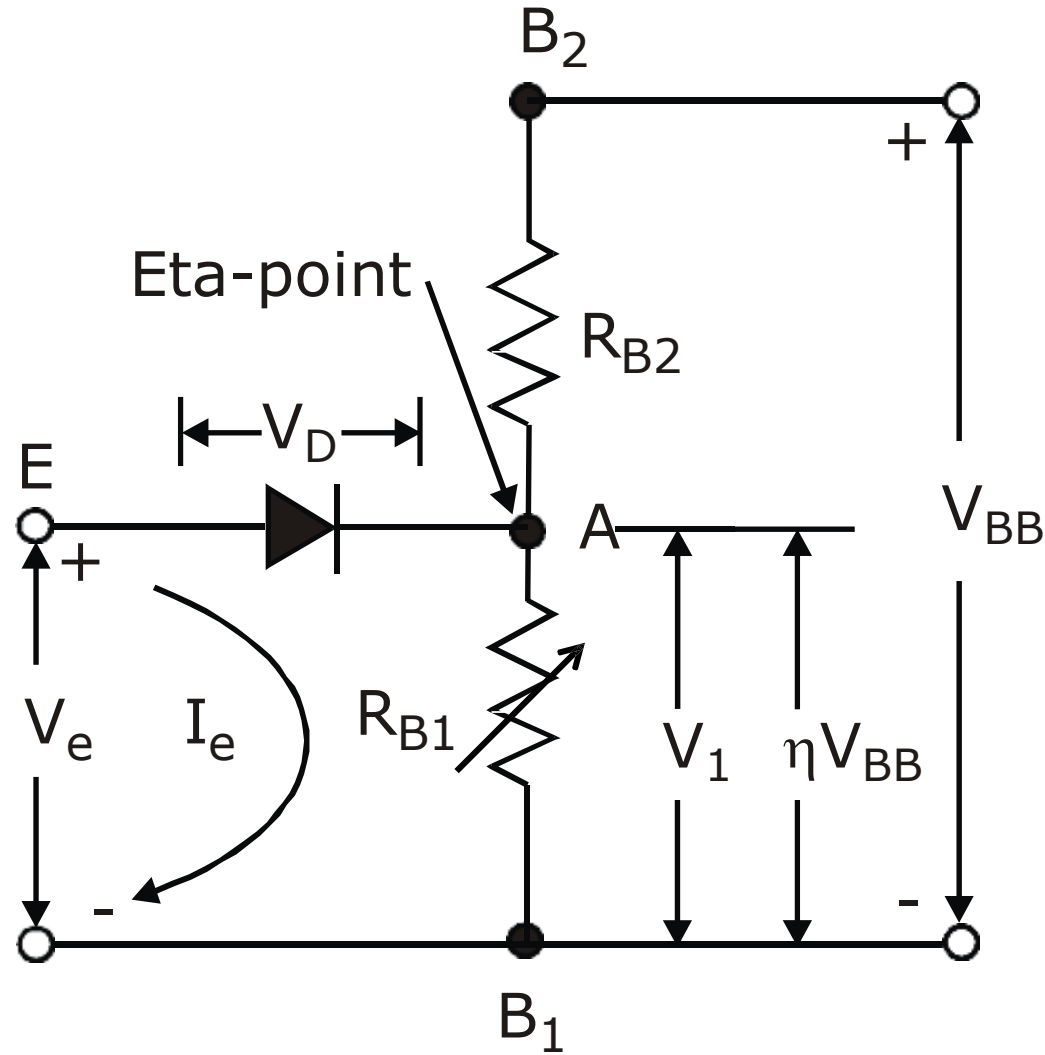


Basic Structure



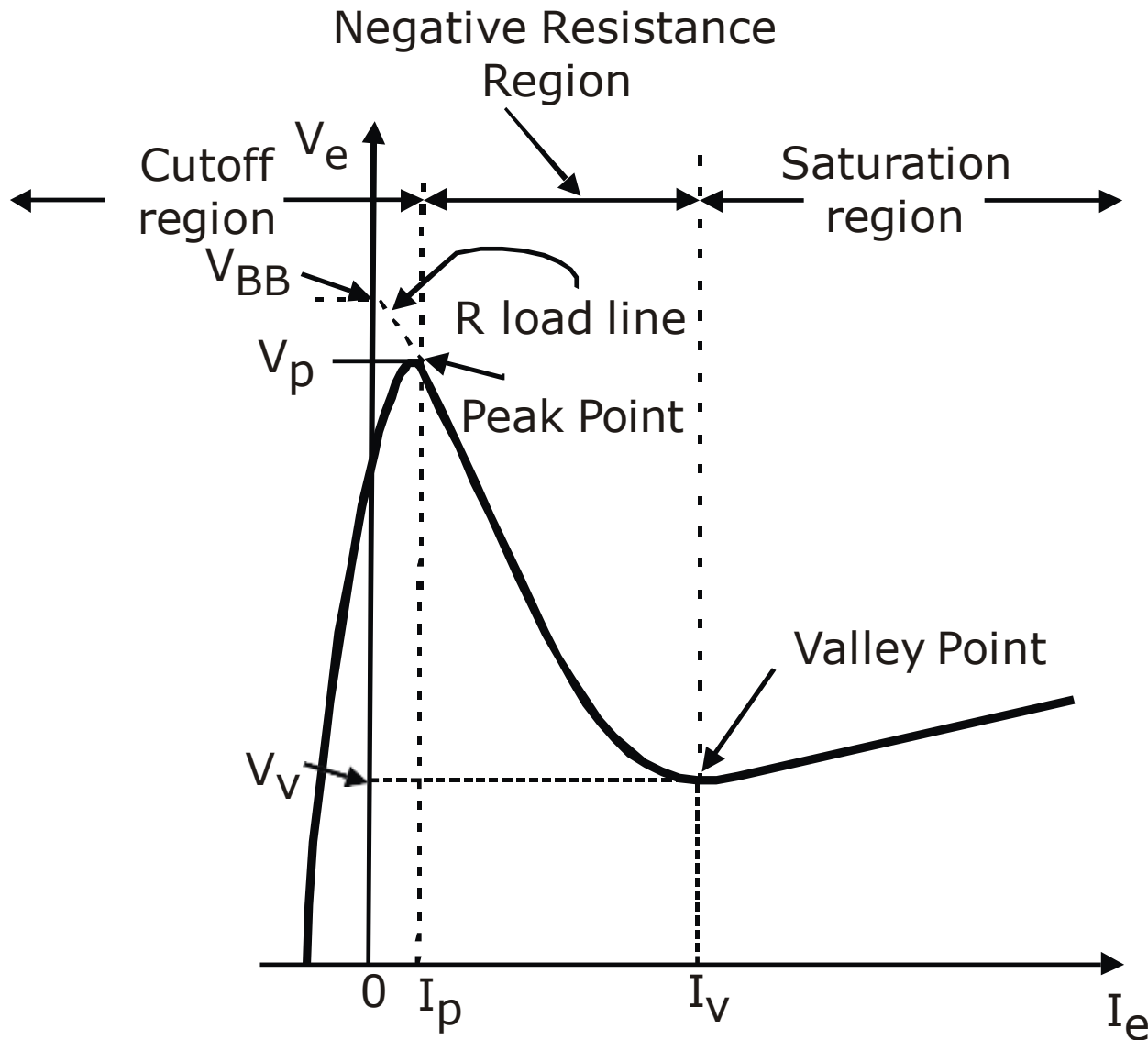
Symbol

Equivalent Circuit



Equivalent Circuit of UJT

Characteristics



Device Description & Operation

- Consists of a lightly doped n-type Si base to which heavily doped p-type emitter is embedded
- At the two ends, there are *ohmic* contacts designated as Base 1 & Base 2
- Thus the 3 terminals are: E, B_1 & B_2
- An interbase resistance $R_{BB} = R_{B1} + R_{B2} |_{I_E = 0}$ ($\sim 5\text{-}10\text{ k}\Omega$) exists between the two bases

Contd...

- Equivalent circuit consists of a pn junction diode and the interbase resistance divided into two parts R_{B1} & R_{B2}
- When a voltage V_{BB} is applied between the bases, the potential of point A w. r. t. B_1 is

$$V_{AB1} = \frac{R_{B1}}{R_{B1} + R_{B2}} V_{BB} = \frac{R_{B1}}{R_{BB}} V_{BB} = \eta V_{BB}$$

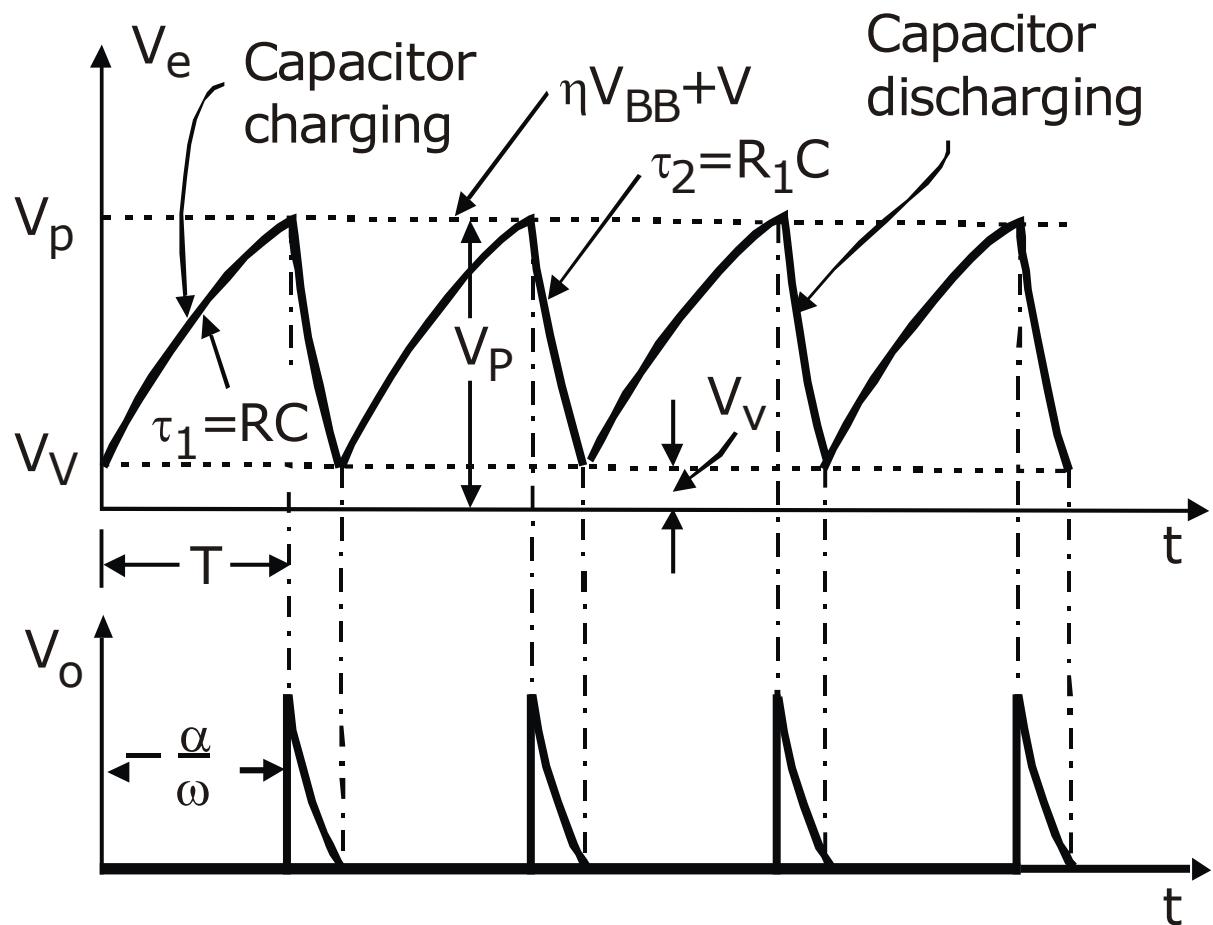
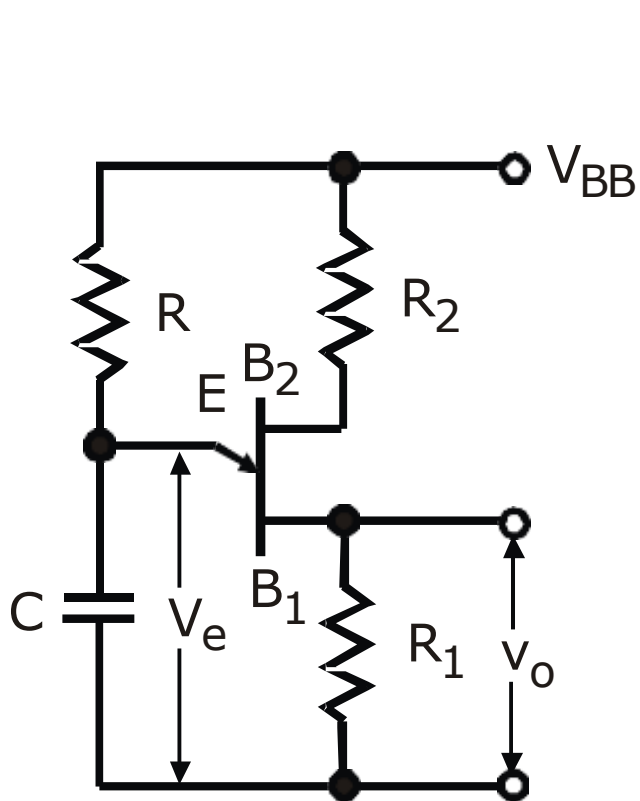
Contd...

- Where, η is known as *intrinsic stand off ratio* & ranges from 0.5-0.8
- When $V_E < V_1$, the equivalent diode is R. B. This is the OFF state of the device & is shown as very low current region on the V_E - I_E curve
- When $V_E > V_1 + V_D$, the diode becomes F. B. this is the ON state of the device
- $V_p = V_1 + V_D = \eta V_{BB} + V_D$ is known as the ***peak point voltage***

Contd...

- Due to the flow of I_E through R_{B1} , number of charge carriers in R_{B1} is increased which *reduces its resistance*, which in turn decrease V_1
- This causes diode to become more & more F. B. & I_E increases further leading to a *regenerative action*
- V_E decreases with increase in I_E & the device is said to exhibit ***negative resistance***
- Eventually, *valley point* will be reached after which there will be no further decrease of R_{B1}
- After valley point, device will reach into saturation state

UJT Relaxation Oscillator



Contd...

- The –ve resistance region of the UJT can be used to advantage in relaxation oscillator which can provide triggering pulses for SCR
- In the above ckt, R_1 & R_2 are chosen to be much smaller than the interbase resistances
- The charging resistance R should be such that its load line passes through the device characteristics in the negative resistance region

Contd...

- When a source voltage V_{BB} is applied to it, C begins to charge through R exponentially towards V_{BB} according to the equation

$$v_C = V_{BB} \left(1 - e^{-t/RC}\right)$$

- When v_C reaches the peak point voltage, E-B₁ junction breaks down & the UJT turns ON. Now C discharges rapidly through R₁
- $\tau_2 \ll \tau_1$
- UJT turns OFF when the voltage decays to valley voltage V_v

Expression for Time Period of Oscillation

- The time T required for C to charge from initial voltage V_v to peak-point voltage V_p thru R can be obtained as:

$$V_p = \eta V_{BB} + V_D = V_v + V_{BB} \left(1 - e^{-t/RC}\right)$$

- Assuming $V_D = V_v$, $\eta = \left(1 - e^{-t/RC}\right)$

or

$$T = \frac{1}{f} = RC \ln \left(\frac{1}{1 - \eta} \right)$$

Contd...

- If T is taken as the time pd. of the O/P pulse duration (neglecting small discharge time), then firing angle is given by

$$\alpha = \omega T = \omega RC \ln \left(\frac{1}{1-\eta} \right)$$

- Design considerations include selection of R_1 , R_2 & R

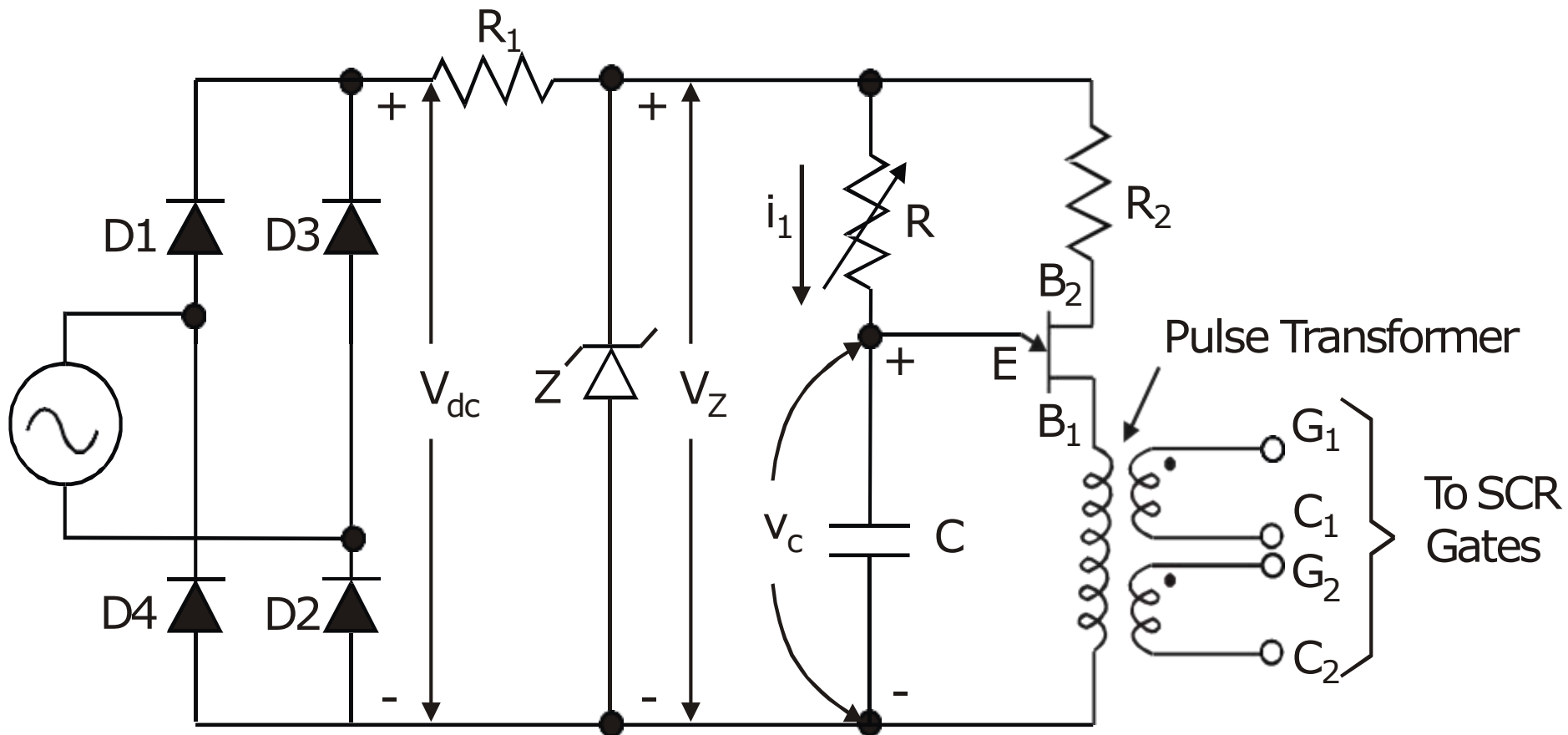
Resistance Values

$$R_{\max} = \frac{V_{BB} - V_p}{I_p}; R_{\min} = \frac{V_{BB} - V_v}{I_v}$$

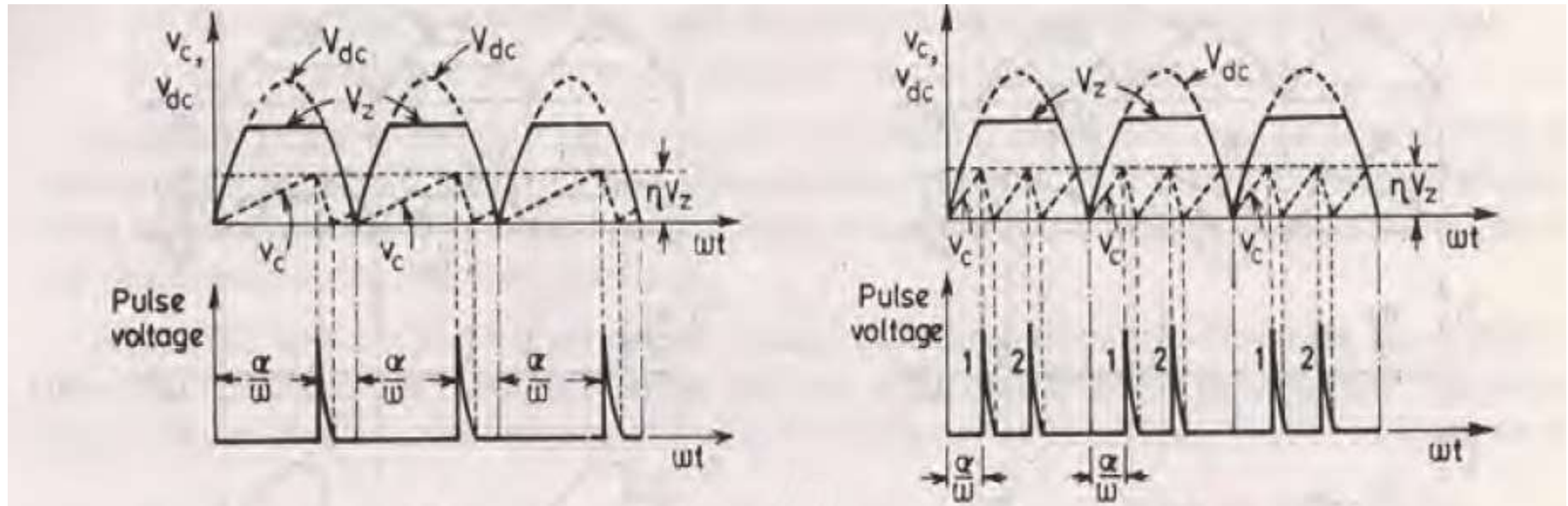
$$\frac{V_{BB} R_1}{R_{BB} + R_1 + R_2} < V_{GT}$$

$$R_2 = \frac{10^4}{\eta V_{BB}}$$

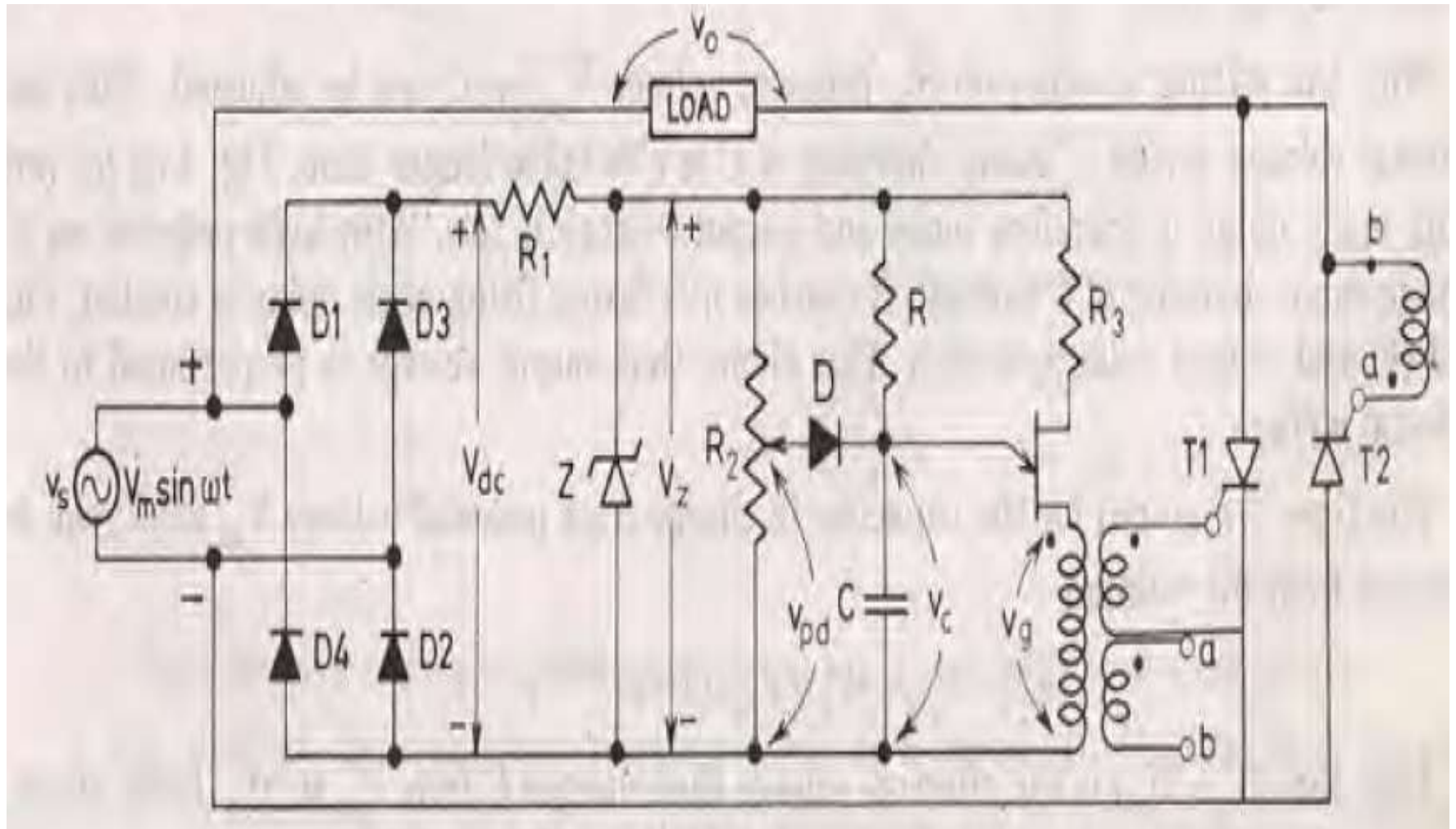
UJT Synchronized Triggering



Generation of Output Pulses



Ramp and Pedestal trigger circuit



Waveforms

