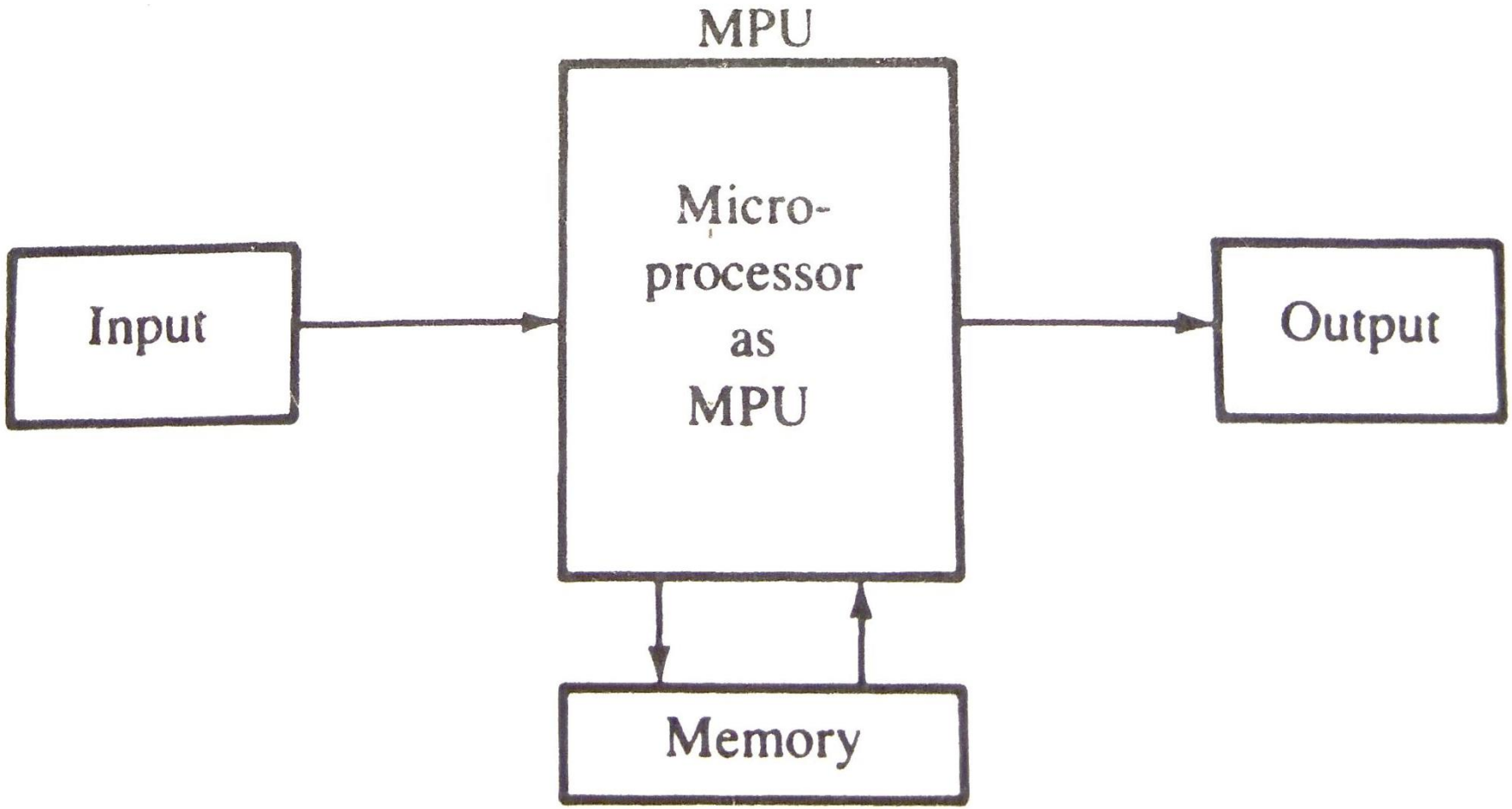
Microprocessors and Microcontrollers

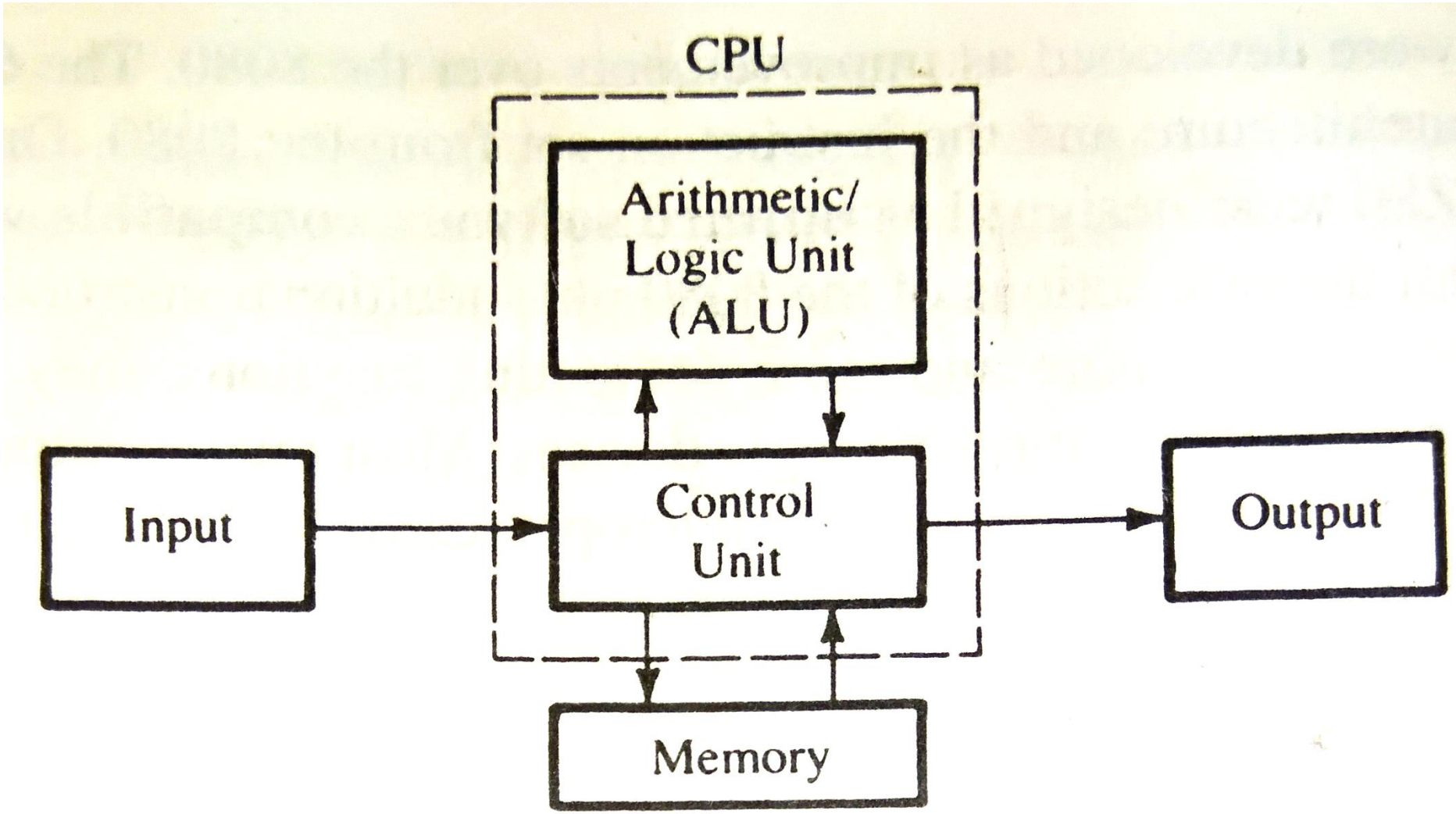
Lecture-2

8085 Architecture

Organisation of a Microprocessor based system



Organisation of a Microprocessor based system



Microprocessor

- The microprocessor is a clock-driven semiconductor device consisting of electronic logic circuits manufactured by using either LSI or VLSI technique.
- Microprocessor is capable of performing various computing functions and making decisions to change the sequence of program execution.

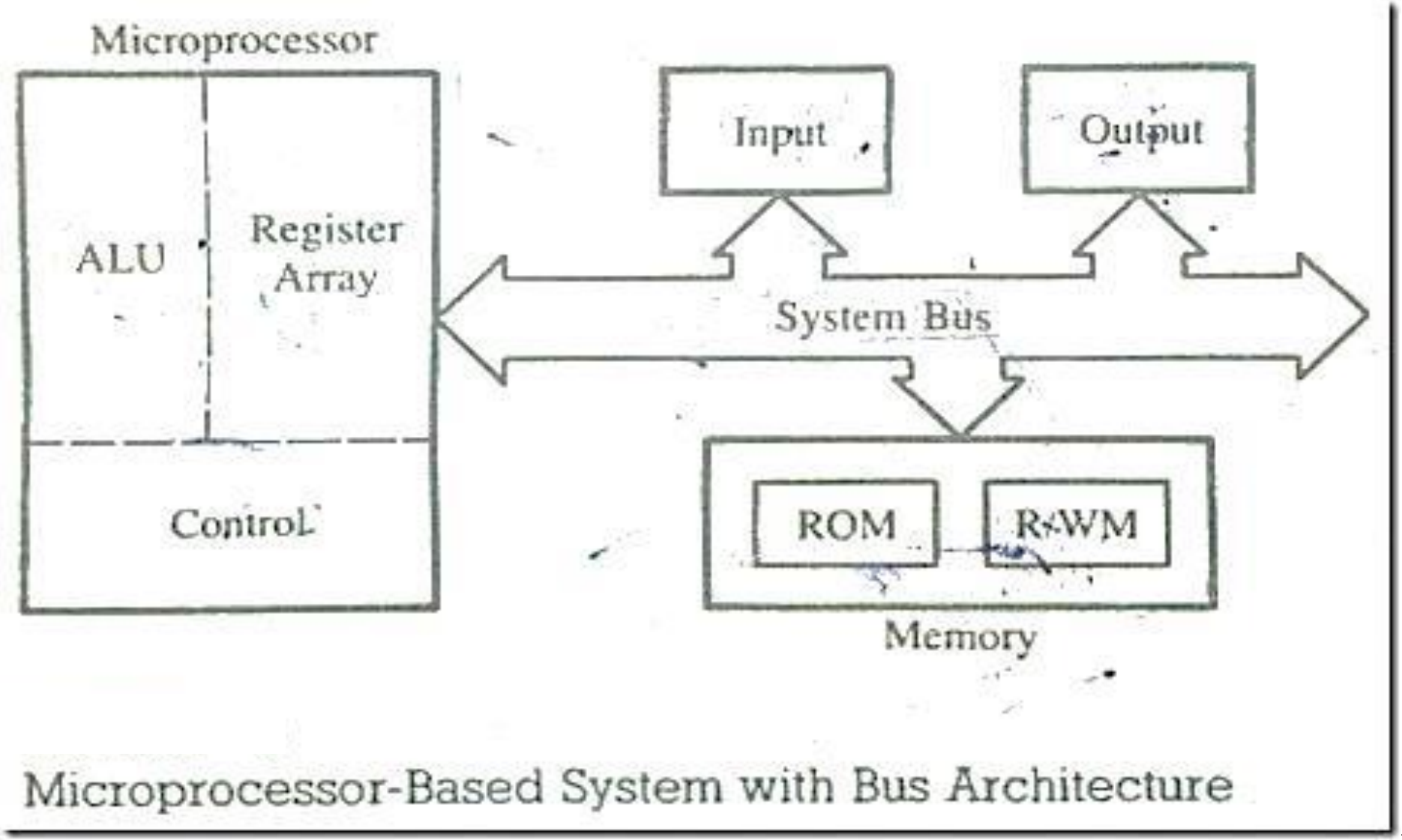
Arithmetic Logic Unit (ALU)

- This area of the microprocessor where various computing functions are performed on data (arithmetic or logical operations)

Control Unit

- The control unit provides the necessary timing and control signal to all the operations in the microcomputer.
- It controls flow of data between microprocessor and memory and peripherals.

Organisation of a Microprocessor based system



Microprocessor-Based System with Bus Architecture

Classification of Microprocessor

- Based on size of data that microprocessor can handle:
  - 4-bit
  - 8-bit
  - 16-bit
  - 32-bit
  - 64-bit

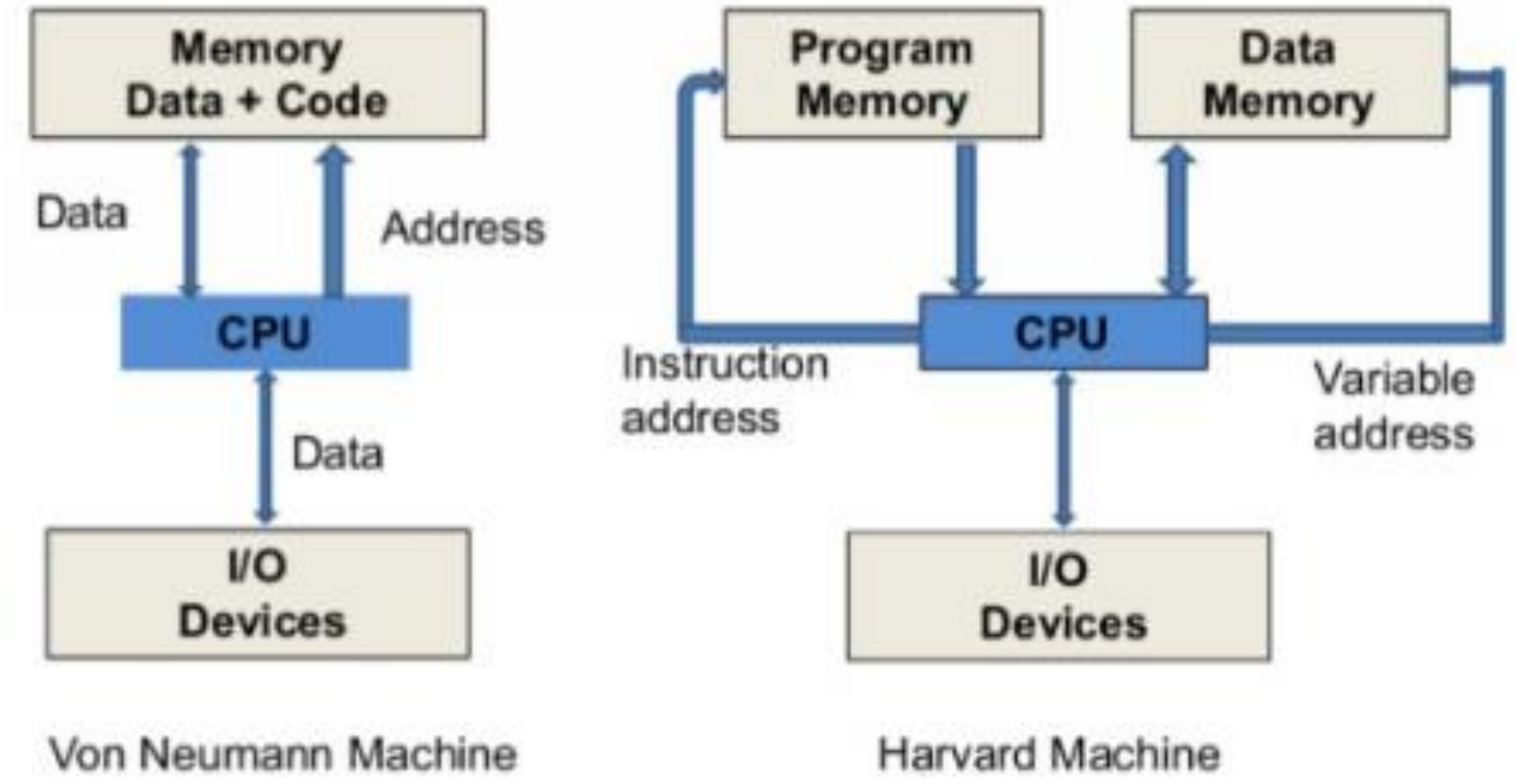
Classification of Microprocessor

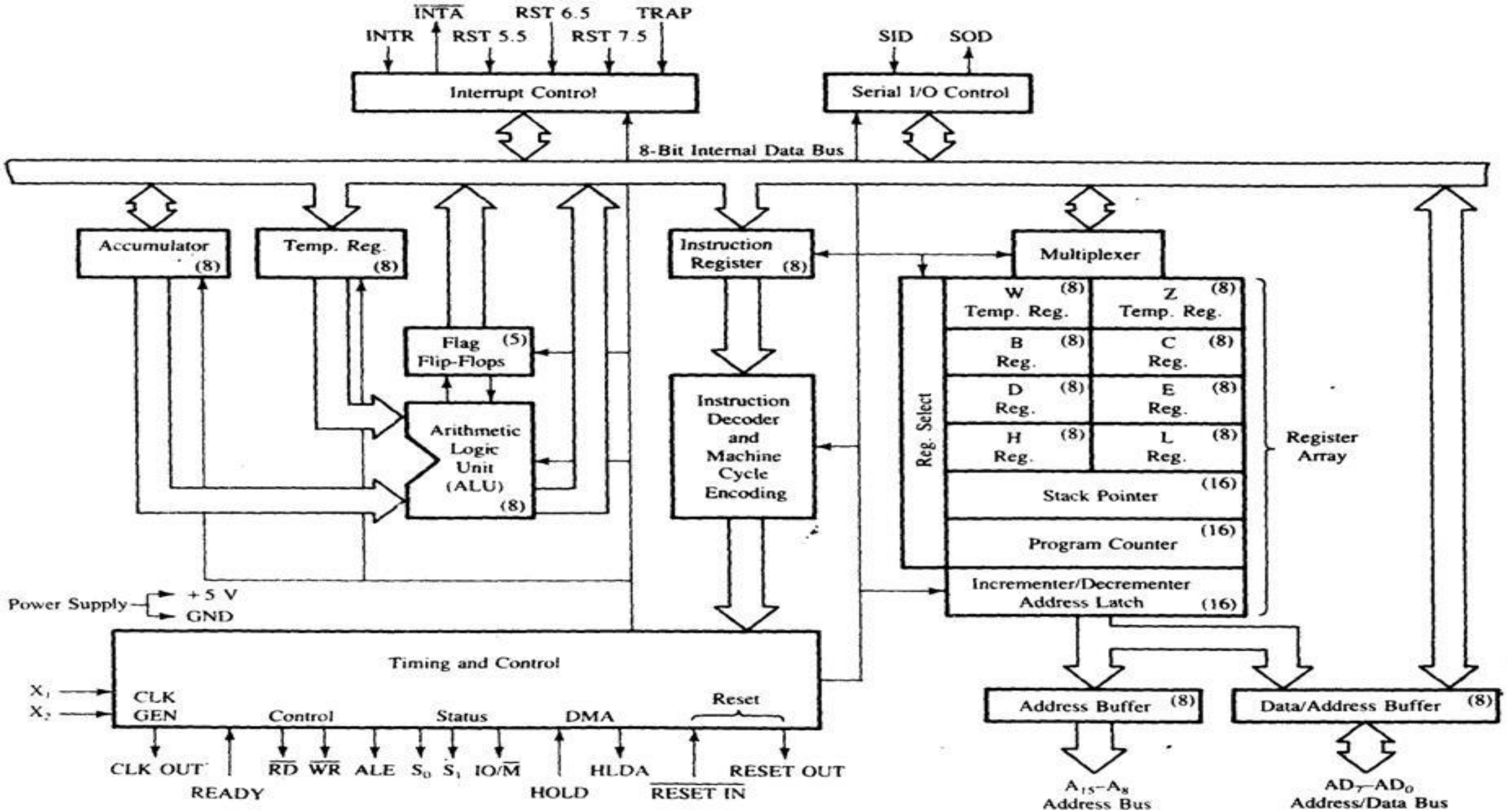
- Based on application
  - General purpose processor: These are used in general computer system integration and can be used by programmer for any application.
  - Microcontroller: These microprocessor chip with inbuilt hardware for the memory and ports can be programmed by user for any generic control application.
  - Special purpose processor: These are designed specifically to handle special function required for an application. DSP processor are example of special purpose processor

Classification of Microprocessor

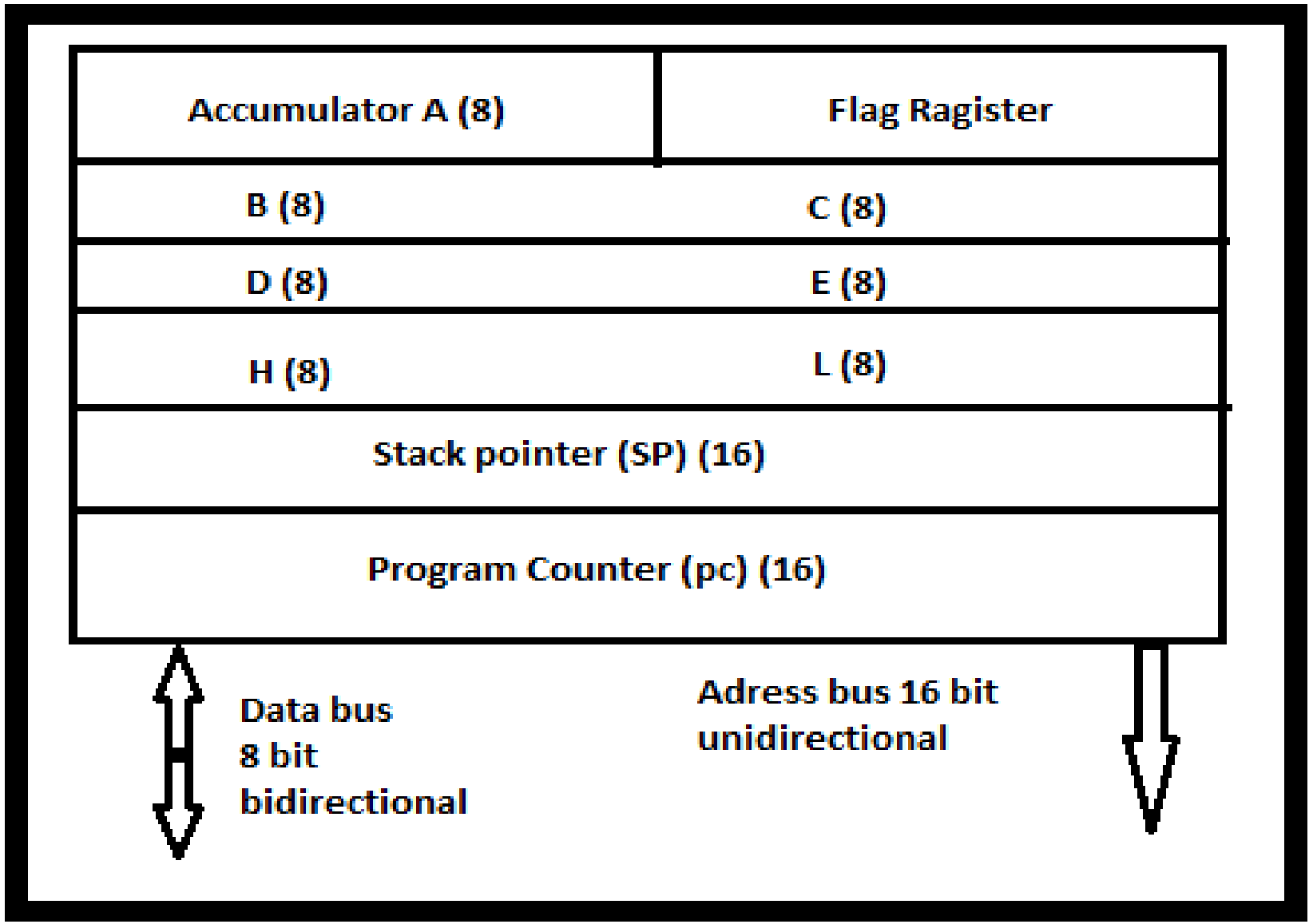
- Based on architecture and hardware of the processor:
  - **RISC processor:** This a processor architecture that supports limited language instruction. (Reduce instruction set computer)
  - **CISC processor:** (complex instruction set computer) is slower more expansive than RISC
  - **VLIW processor** (very long instruction word) have instructions composed of many machine operations. These instruction can be executed in parallel. Their parallel execution is called instruction level parallelism.
  - **Superscaller processor :** use complex hardware to achieve parallelism.

Von-Neuman architecture & Harvard architecture

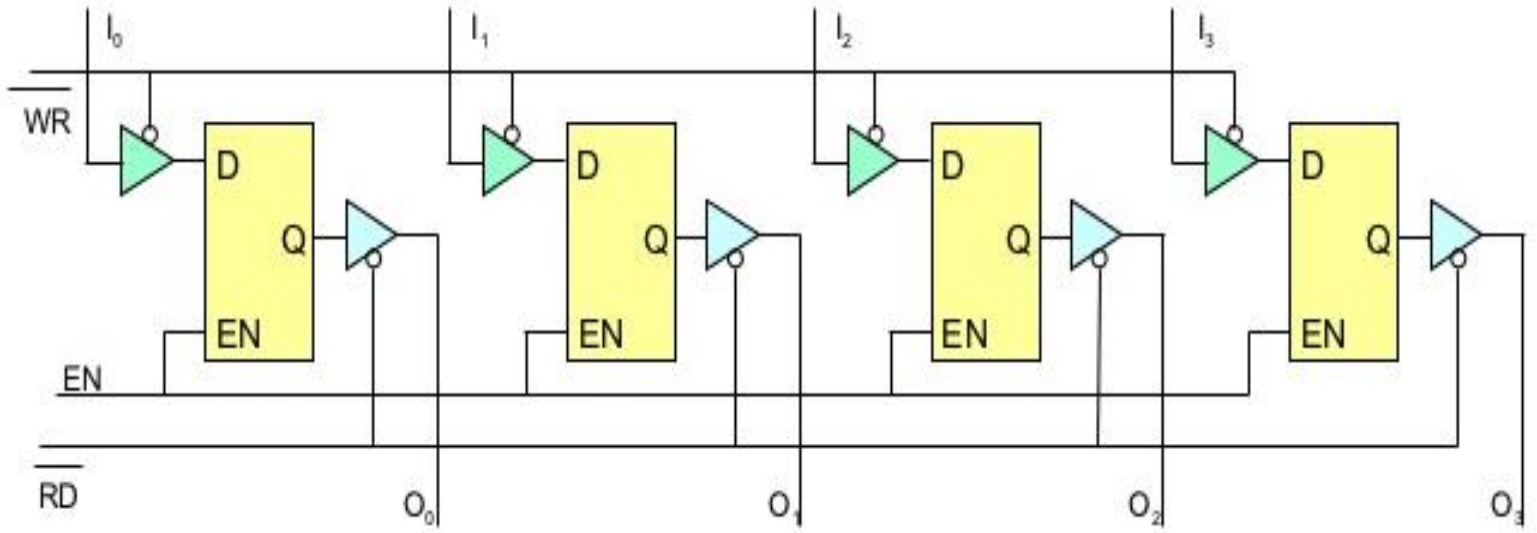



INTA
INTR
RST 5.5
RST 6.5
RST 7.5
TRAP
Interrupt Control
SID
SOD
Serial I/O Control
8-Bit Internal Data Bus
Accumulator (8)
Temp. Reg. (8)
Flag Flip-Flops (5)
Arithmetic Logic Unit (ALU) (8)
Instruction Register (8)
Instruction Decoder and Machine Cycle Encoding
Multiplexer
Reg. Select
W Temp. Reg. (8)
Z Temp. Reg. (8)
B Reg. (8)
C Reg. (8)
D Reg. (8)
E Reg. (8)
H Reg. (8)
L Reg. (8)
Register Array
Stack Pointer (16)
Program Counter (16)
Incrementer/Decrementer Address Latch (16)
Power Supply
+5 V
GND
Timing and Control
X1
X2
CLK GEN
Control
Status
DMA
Reset
CLK OUT
READY
RD
WR
ALE
S0
S1
IO/M
HOLD
HLDA
RESET IN
RESET OUT
Address Buffer (8)
Data/Address Buffer (8)
A15–A8
Address Bus
AD7–AD0
Address/Data Bus

8085 Registers....



4- bit Register



8085 Microprocessor

- The salient features of 8085 μp are :
- It is a 8 bit microprocessor.
- It is manufactured with N-MOS technology.
- It has 16 bit address bus and hence can address upto $2^{16} = 65536$ bytes (64KB) memory locations through A_0-A_{15}.
- The first 8 lines of address bus and 8 lines of data bus are multiplexed $AD_0 - AD_7$.

8085 Microprocessor (cont..)

- Data bus is a group of 8 lines $D_0 - D_7$.
- It supports external interrupt request.
- A 16 bit program counter (PC)
- A 16 bit stack pointer (SP)
- Six 8-bit general purpose register arranged in pairs: BC, DE, HL.
- It requires a signal +5V power supply and operates at 6.144 MHZ single phase clock.
- It is enclosed with 40 pins DIP (Dual in line package).

8085 Microprocessor (cont..)

Memory:

- Program, data and stack memories occupy the same memory space. The total addressable memory size is 64 KB.
- **Program memory** - program can be located anywhere in memory. Jump, branch and call instructions use 16-bit addresses, i.e. they can be used to jump/branch anywhere within 64 KB. All jump/branch instructions use absolute addressing.

8085 Microprocessor (cont..)

- **Data memory** - the processor always uses 16-bit addresses so that data can be placed anywhere.
- **Stack memory** is limited only by the size of memory. Stack grows downward.
- First 64 bytes in a zero memory page should be reserved for vectors used by RST instructions.

8085 Flag Register...

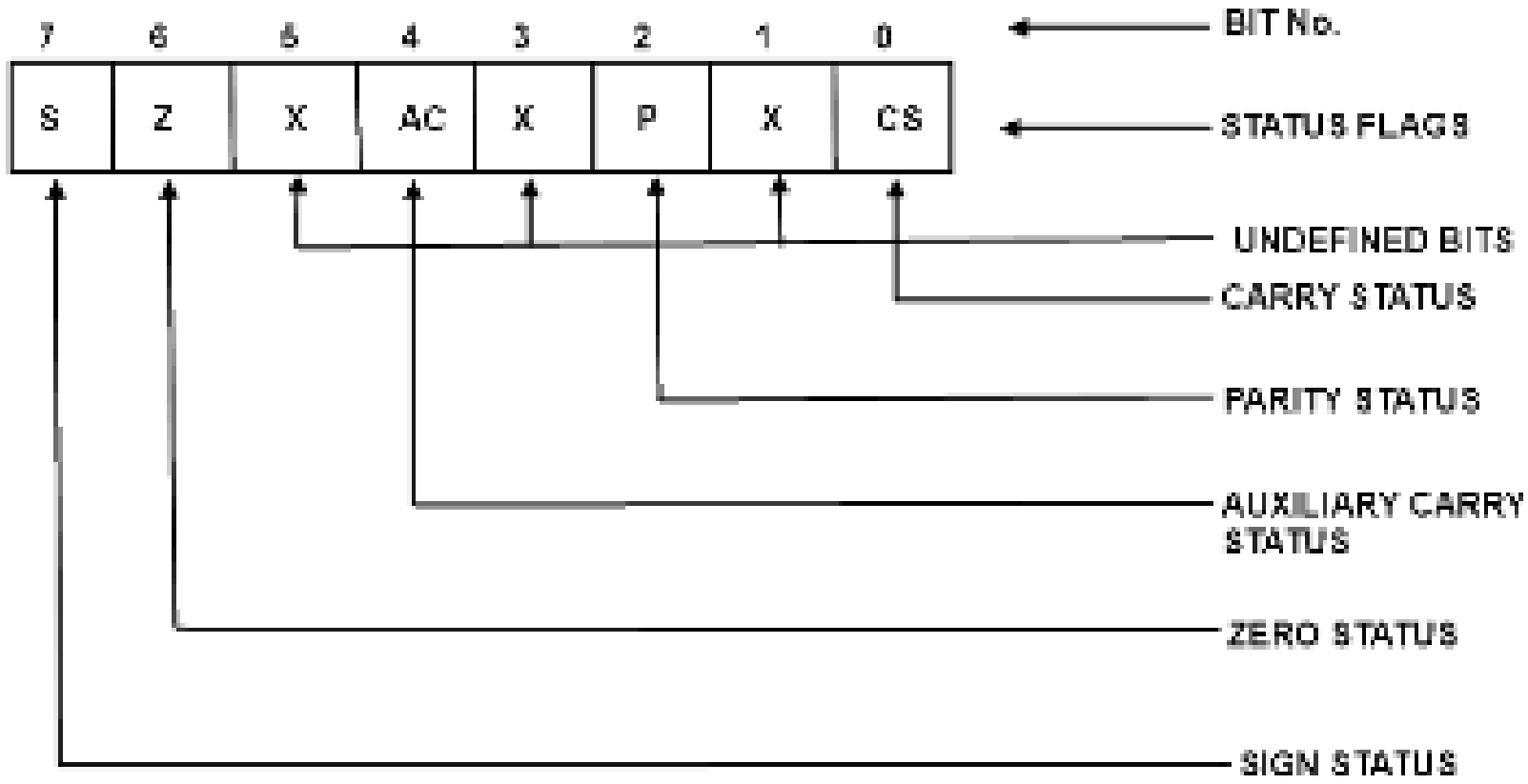
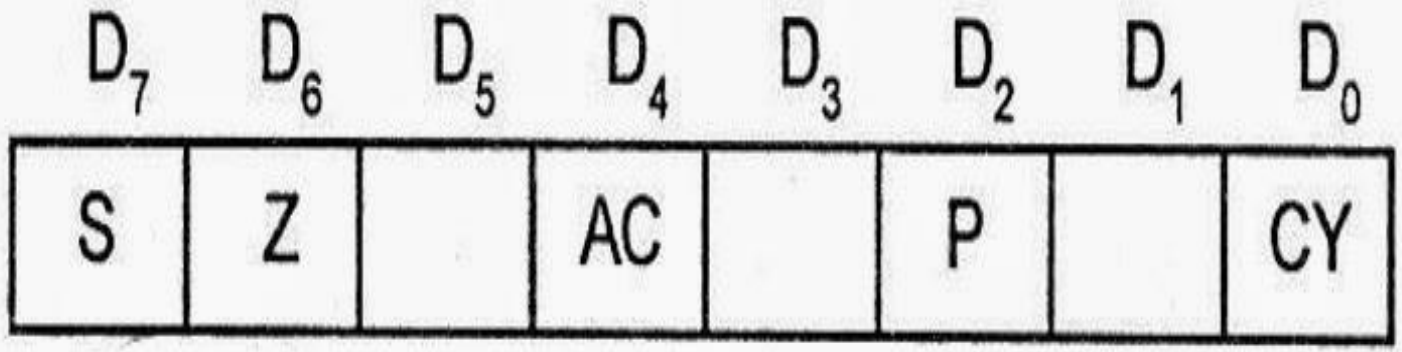


Figure 2: Status Flags of Intel 8085

FLAG REGISTER OF 8085



Flag is an 8-bit register containing 5 1-bit flags:

Sign - set if the most significant bit of the result is set.

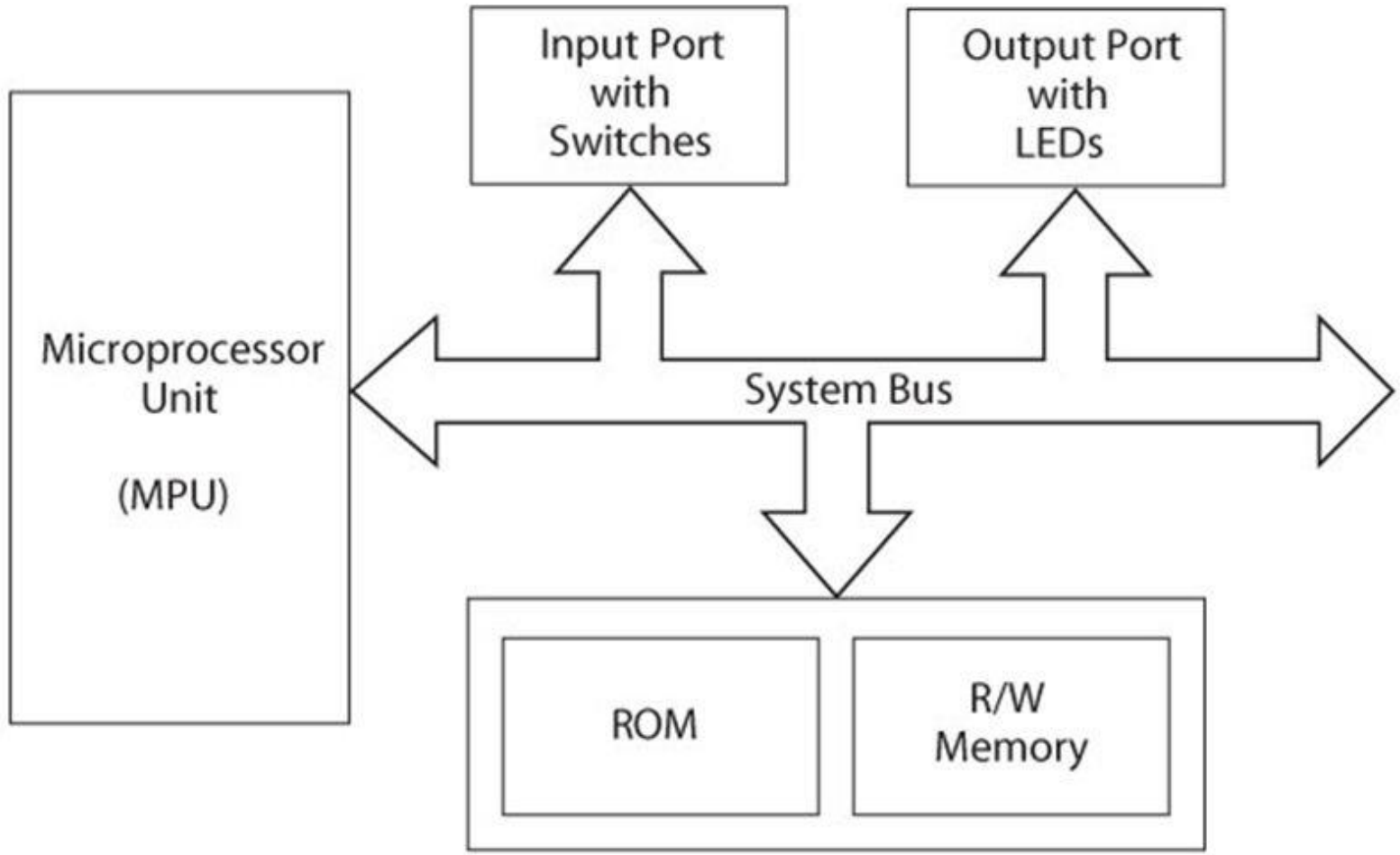
Zero - set if the result is zero.

Auxiliary carry - set if there was a carry out from bit 3 to bit 4 of the result.

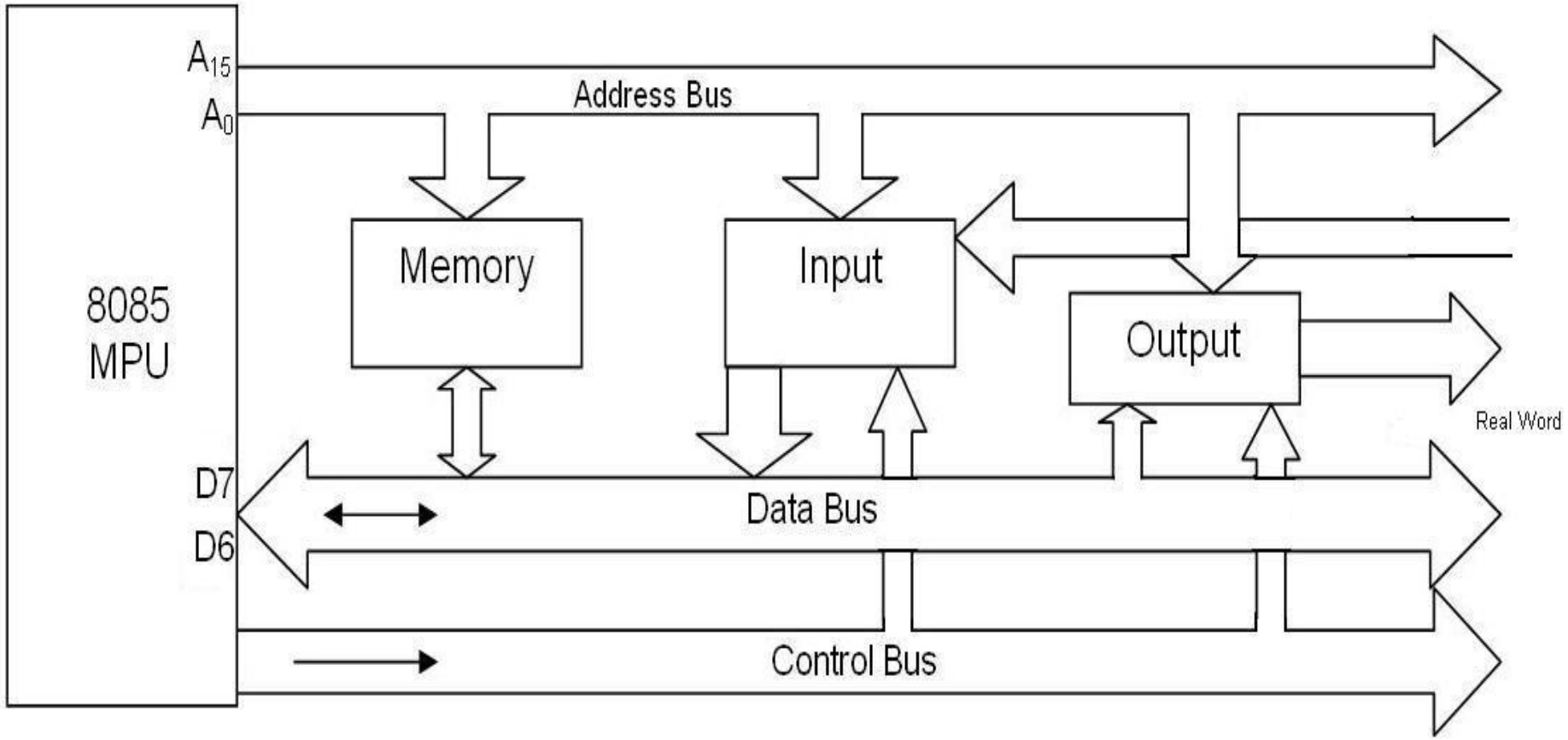
Parity - set if the parity (the number of set bits in the result) is even.

Carry - set if there was a carry during addition, or borrow during subtraction/comparison.

Microprocessor-Based System with Bus Architecture

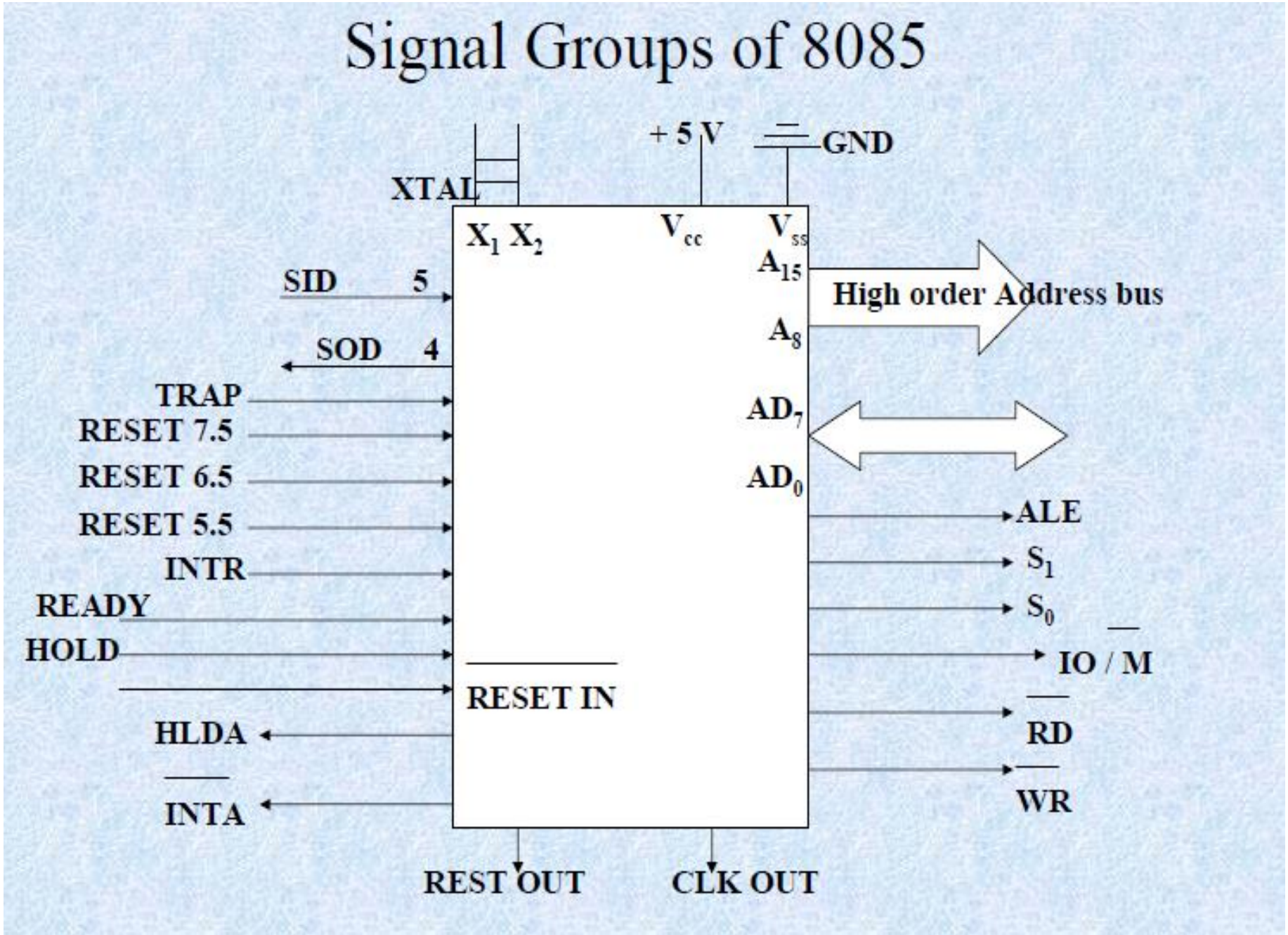


8085 bus structure



8085 Signals

Signal Groups of 8085



AD7-AD0

- The following signal descriptions are common for both modes.
- **AD7-AD0 :**
  - These are the time *multiplexed* memory I/O address and data lines.

– Address remains on the lines during T1 state, while the data is available on the data bus during T2, T3 and T4. These lines are active high and float to a tristate during interrupt acknowledge and local bus hold acknowledge cycles.

A15-A8

- These are the higher order address bus.

Control and Status signal

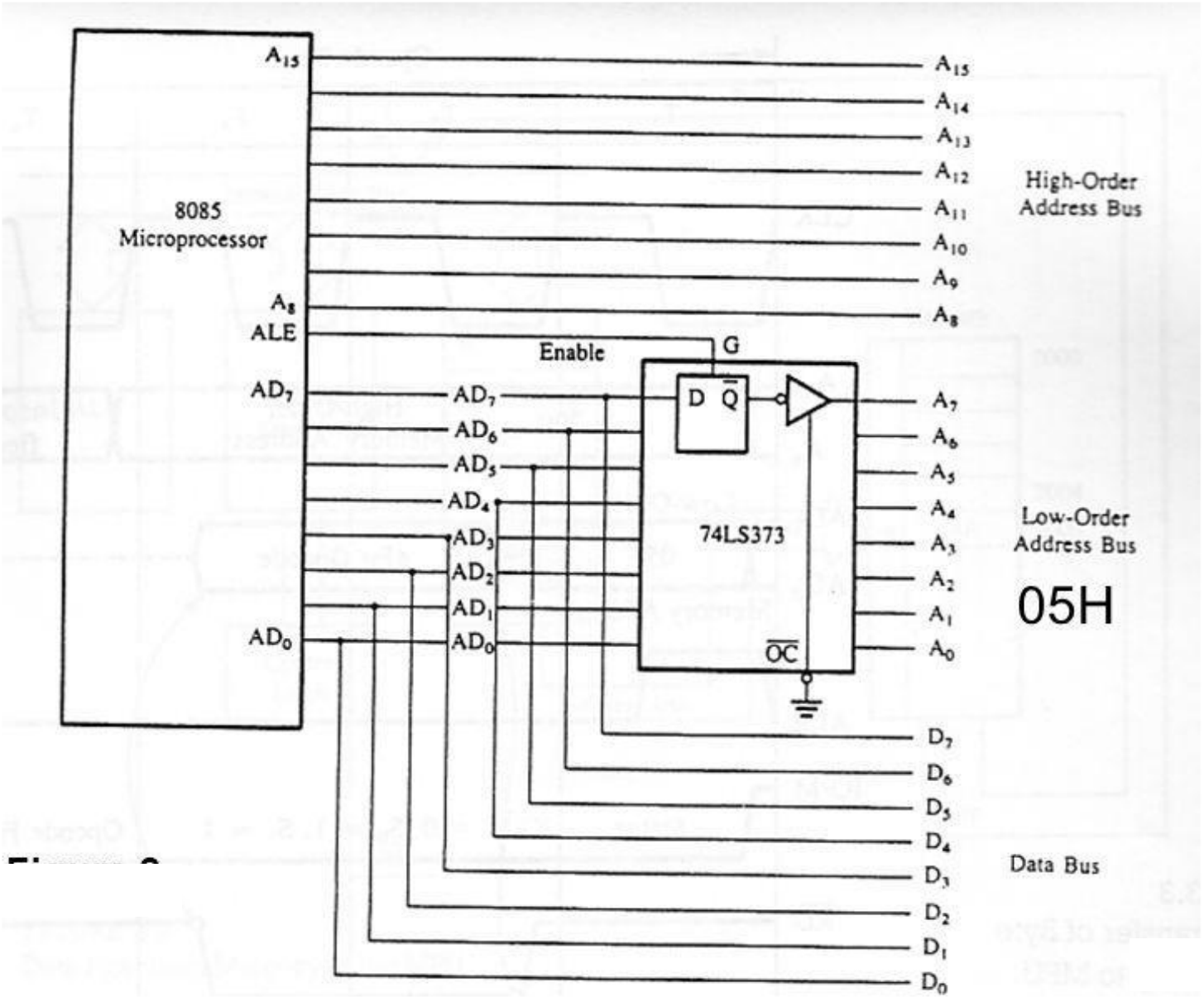
ALE

Address Latch Enable

This is a positive going pulse generated every time the 8085 begins an operation (machine cycle)

It indicates that the bits on AD7-AD0 are address bit.

- Schematic diagram to latch low order address bus.



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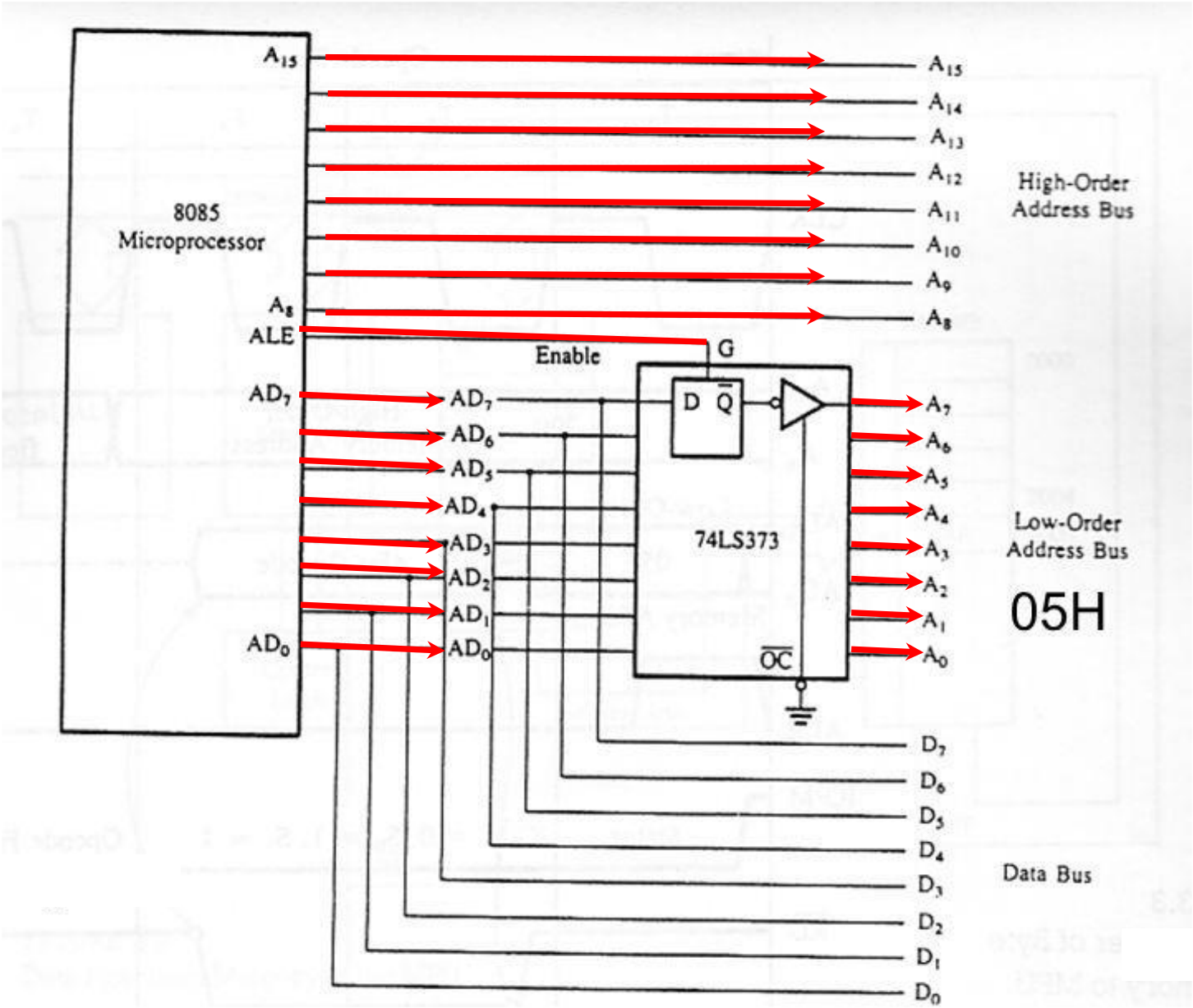

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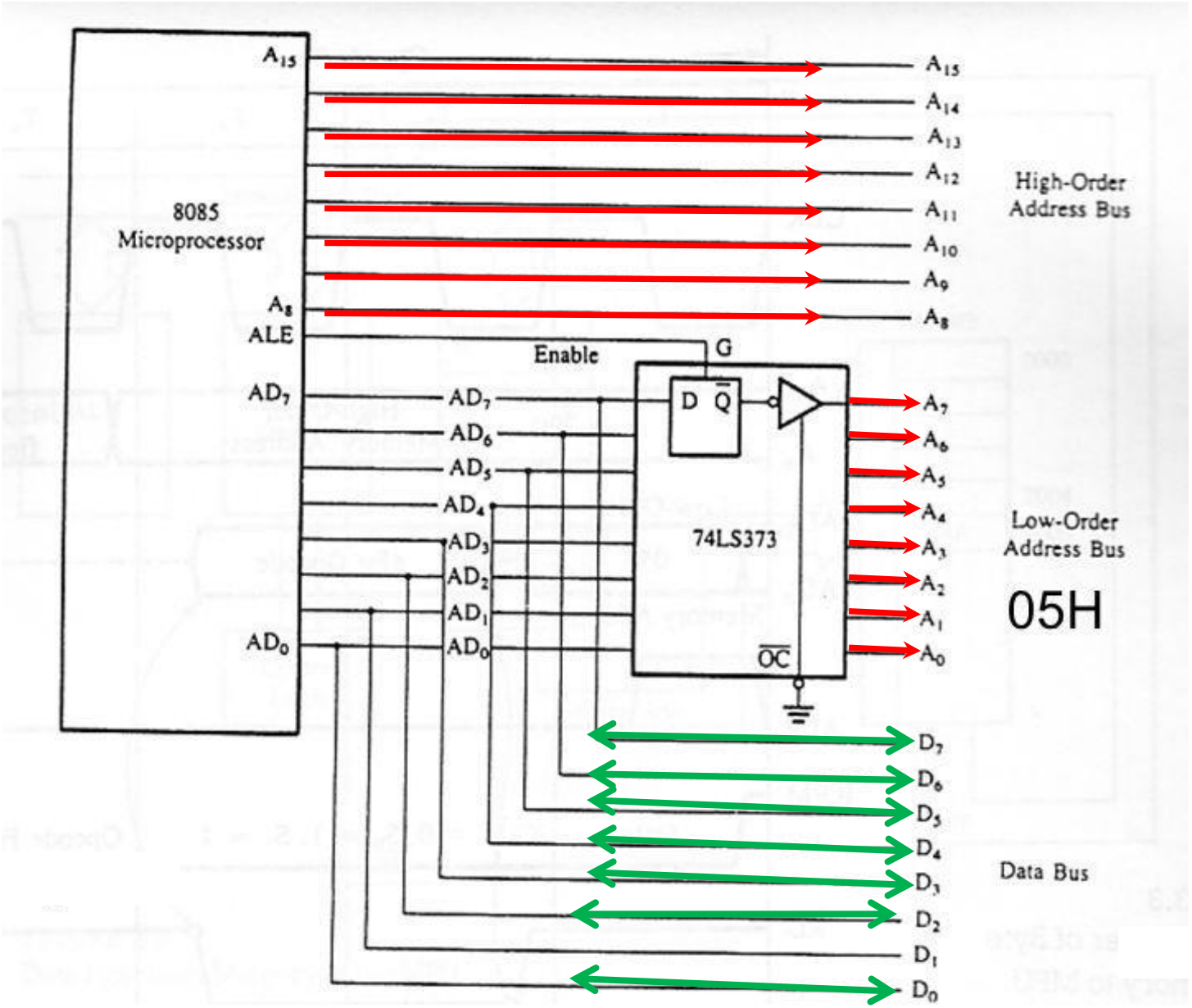

$\overline{RD}$

(Read)

- This is a read control signal (active low).
- This signal indicates that the selected I/O or memory device is to be read and data are available on the bus.

$\overline{WR}$

(write)

- This is a write control signal.
- This signal indicates that the data on the data bus are to be written into a selected memory or I/O location.

$IO/\overline{M}$

- This is a status signal used to differentiate between I/O and memory operation.
- When it is high, it indicates a I/O operation
- When it is low, it indicates memory operation.

S1 and S0

- These status signals are used to specify the kind of operation being performed.

S1	S0	Operations
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

S1 and S0

- The status signal combines with I/O signals to govern various operations.

IO/M(Active Low)	S1	S0	Data Bus Status(Output)
0	0	0	Halt
0	0	1	Memory WRITE
0	1	0	Memory READ
1	0	1	IO WRITE
1	1	0	IO READ
0	1	1	Opcode fetch
1	1	1	Interrupt acknowledge

Externally initiated Signals

INTR

(Interrupt Request)

- This used as a general purpose interrupt.
- When an interrupt is detected by the processor it suspend the execution of current program and execute the interrupt service routine.

Externally initiated Signals

$\overline{\text{INTA}}$

(Interrupt Acknowledgement)

- It is used to acknowledge the interrupt.

Restart Interrupts

RST 7.5, RST 6.5, RST 5.5 and TRAP

- These are vectored interrupts that transfer the program control to specific memory location.

$\overline{\text{RESET IN}}$

- When the signal on this pin goes low the program counter (PC) is set to zero (0) and processor is reset.
- Now the program execution begins at zero address.

RESET OUT

- The signal can be used to reset other device that are connected to the processor.

HOLD

- This signal indicates that peripheral such as DMA controller is requesting the use of the address bus and data bus.

HLDA

- It is an acknowledgement signal that sent in response to the HOLD request

READY

- It is a signal that serves to delay the microprocessor.
- If this signal goes low, then the processor is allowed to wait for an integrated number of clock cycles until READY becomes high.

X1 and X2

- A crystal oscillator is connected at these two pins.
- The frequency is internally is divided by two; therefore to operate a system at 3 MHz, the crystal should have a frequency of 6 MHz.

CLK (out)

Clock Out

- This signal can be used as the system clock for other device

SID

- Serial Input Data

SOD

- Serial Output Data