ADC Interfacing with pt-51 using SPI

24^{th} September, 2018

Introduction

In this experiment we are using the ADC TLV1543. The ADC can be given single ended or differential analog inputs and it produces 10 bit digital output. This 10 bit digital output is available on the Dout pin of the ADC serially. We are interfacing this with Pt 51 microcontroller. The microcontroller takes this 10 bit input and modifies data appropriately.

Steps to configure SPCON register

1. Free the SS pin for a general-purpose
2. Select one of the Master clock rates (by choosing appropriate values of SPR0, SPR1, SPR2 we can get different baud rates. Select the appropriate baud rate)
3. Configure the SPI module as Master (in this case)
4. Selects serial clock polarity and phase(1,1) or (0,0)
5. Enable the SPI module (SPEN = 1)

ADC interfacing with pt-51

Pin	Function	Description
P1.7	MOSI	Serial Output
P1.6	SCK	Serial Clock
P1.5	MISO	Serial Input
P1.4	$\overline{SS}$	Chip Select

Table 1: SPI pins

The pins on the Pt-51 board marked SPI can be used for connecting wires to the ADC

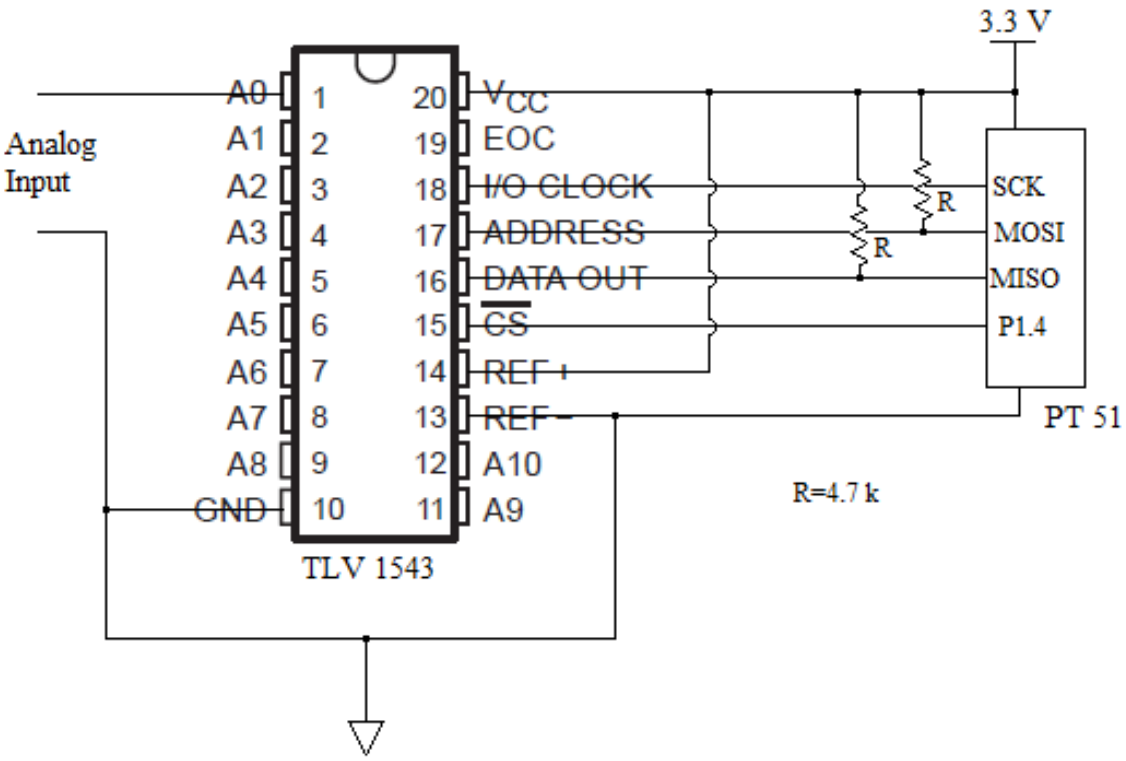
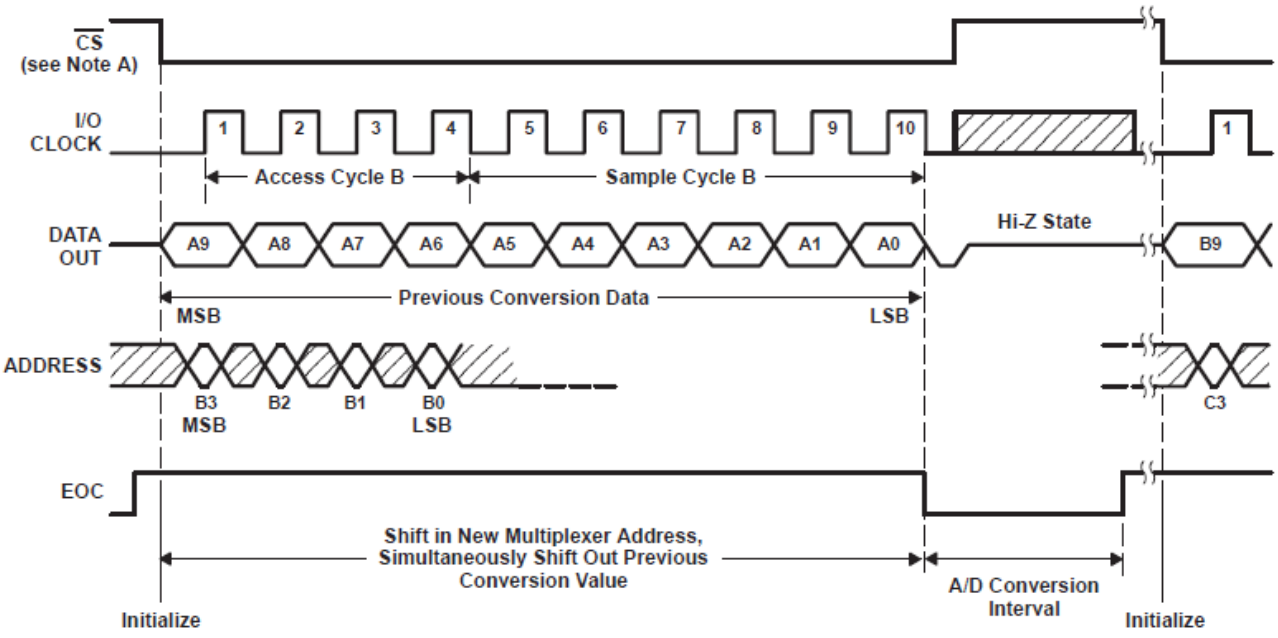


Figure 1: Connection Diagram

Steps for ADC interfacing

1. Configure the SPCON register as described in the section steps to configure SPCON register.
2. Enable SPI communication.
3. Make CS pin of ADC low to select it.
4. As shown in timing diagram send channel selection for ADC input. First four cycles will take 4 bits. We should send these four bits (MSB first) according to the channel where we are giving input. As there are 11 channels, we will require 4 bits to represent them. Also there are three test modes.
5. The MSB of the previous conversion appears on DATA OUT on the falling edge of CS in mode 1, mode 3, and mode 5, on the rising edge of EOC in mode 2 and mode 4, and following the 16th clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host through DATA OUT.
6. In short, in mode 1,3 and 5 we will receive digital output of the previously selected channel as well as we will give address of the channel of which we want to do the conversion. We will get digital output of this channel at the next CS falling edge(MSB). Refer TLV1543 datasheet for more details.



NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$

Figure 2: timing diagram

7. After the successful reception of 10 bit of data CS pin of ADC is made high.

8. The data bits transmission and reception from microcontroller should be done as per the alignment shown in timing diagram.

Important formulae for voltage conversion calculations

$$LSB\,Size = \frac{V_{REF}}{1024}$$

$$Digital\,Output\,Code = \frac{1024 \times V_{IN}}{V_{REF}}$$

Where,
V_{IN} = Analog input voltage
V_{REF} = Analog Reference voltage

SPCON Register

SPCON - Serial Peripheral Control Register (0C3H)

7	6	5	4	3	2	1	0
SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0

Bit Number	Bit Mnemonic	Description
7	SPR2	**Serial Peripheral Rate 2** Bit with SPR1 and SPR0 define the clock rate.
6	SPEN	**Serial Peripheral Enable** Cleared to disable the SPI interface. Set to enable the SPI interface.
5	SSDIS	**$\overline{SS}$ Disable** Cleared to enable $\overline{SS}$ in both Master and Slave modes. Set to disable $\overline{SS}$ in both Master and Slave modes. In Slave mode, this bit has no effect if CPHA = "0".
5	MSTR	**Serial Peripheral Master** Cleared to configure the SPI as a Slave. Set to configure the SPI as a Master.
4	CPOL	**Clock Polarity** Cleared to have the SCK set to "0" in idle state. Set to have the SCK set to "1" in idle low.
3	CPHA	**Clock Phase** Cleared to have the data sampled when the SCK leaves the idle state (see CPOL). Set to have the data sampled when the SCK returns to idle state (see CPOL).
2	SPR1	**SPR2 SPR1 SPR0 Serial Peripheral Rate** 0 0 0 Invalid 0 0 1 $F_{CLK\ PERIPH}/4$ 0 1 0 $F_{CLK\ PERIPH}/8$
1	SPR0	0 1 1 $F_{CLK\ PERIPH}/16$ 1 0 0 $F_{CLK\ PERIPH}/32$ 1 0 1 $F_{CLK\ PERIPH}/64$ 1 1 0 $F_{CLK\ PERIPH}/128$ 1 1 1 Invalid

Reset Value = 0001 0100b

Figure 3: SPCON Register