ECE451 Lab 2: 3-bit ALU in Verilog

Digital System Design

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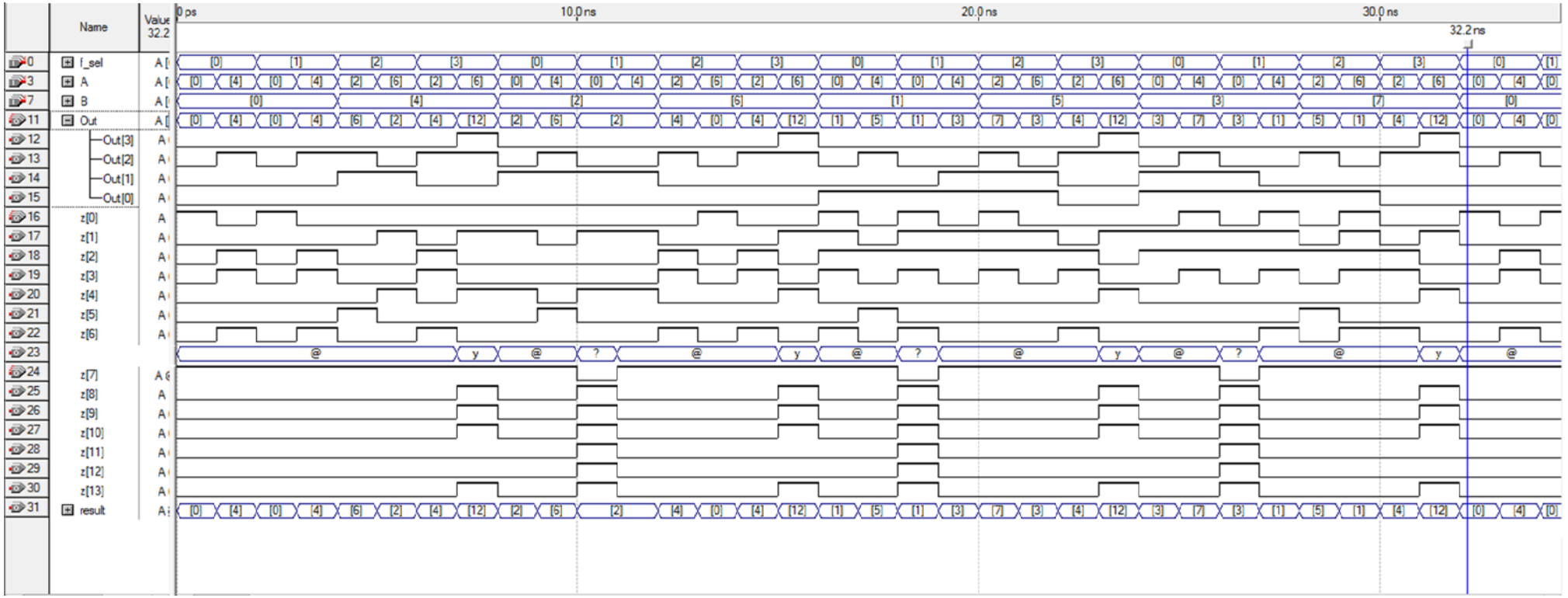
Verilog Code:

```
module threealu(
        input [2:0]          A,B,
        input [1:0]          Sel,
        output[3:0]          Out,
        output reg[3:0]      result,
        output reg[13:0]      z
        );

    wire[3:0] tmp;
    assign Out = result;



    always
    begin
        case(Sel)
            2'b00: result = A+B;
            2'b01: result = A-B;
            2'b10: result = A^B;
            2'b11: result = A<<1;

         endcase


     // Purpose: Creates a case statement for all possible input binary numbers.
  // Drives r_Hex_Encoding appropriately for each input combination.

        case (result[3:0])
              4'b0000 :                                 //Hexadecimal 0
              z = 14'b10000001000000;

              4'b0001 :                                 //Hexadecimal 1
              z = 14'b10000001111001  ;

              4'b0010 :                                 //Hexadecimal 2
              z = 14'b10000000100100 ;

              4'b0011 :                                 //Hexadecimal 3
              z = 14'b10000000110000 ;

              4'b0100 :                                 //Hexadecimal 4
              z = 14'b10000000011001 ;

              4'b0101 :                                 //Hexadecimal 5
              z = 14'b10000000010010 ;

              4'b0110 :                                 //Hexadecimal 6
              z = 14'b10000000000010 ;

              4'b0111 :                                 //Hexadecimal 7
              z = 14'b10000001111000;

              4'b1000 :                                 //Hexadecimal 8
              z = 14'b10000000000000;

              4'b1001 :                                 //Hexadecimal 9
              z = 14'b10000000010000;
```


Name
Value
32.2
0 ps
10.0 ns
20.0 ns
30.0 ns
32.2 ns
f_sel
A
B
Out
Out[3]
Out[2]
Out[1]
Out[0]
z[0]
z[1]
z[2]
z[3]
z[4]
z[5]
z[6]
z[7]
z[8]
z[9]
z[10]
z[11]
z[12]
z[13]
result