

Dc characteristics of CMOS Inverter:-

Digital ckt analysis

DC analysis
(Voltage Transfer Characteristics)

V_{in} Vs V_{out}

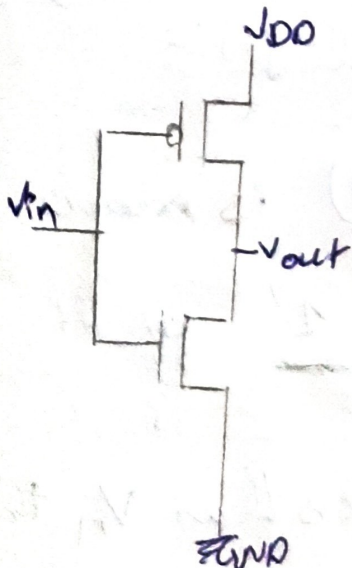
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wherever we apply i/p voltage it will take enough time to settle.

Transient Analysis
(V_{out} Vs time)

V_{out} Vs time

i) CMOS Inverter:-

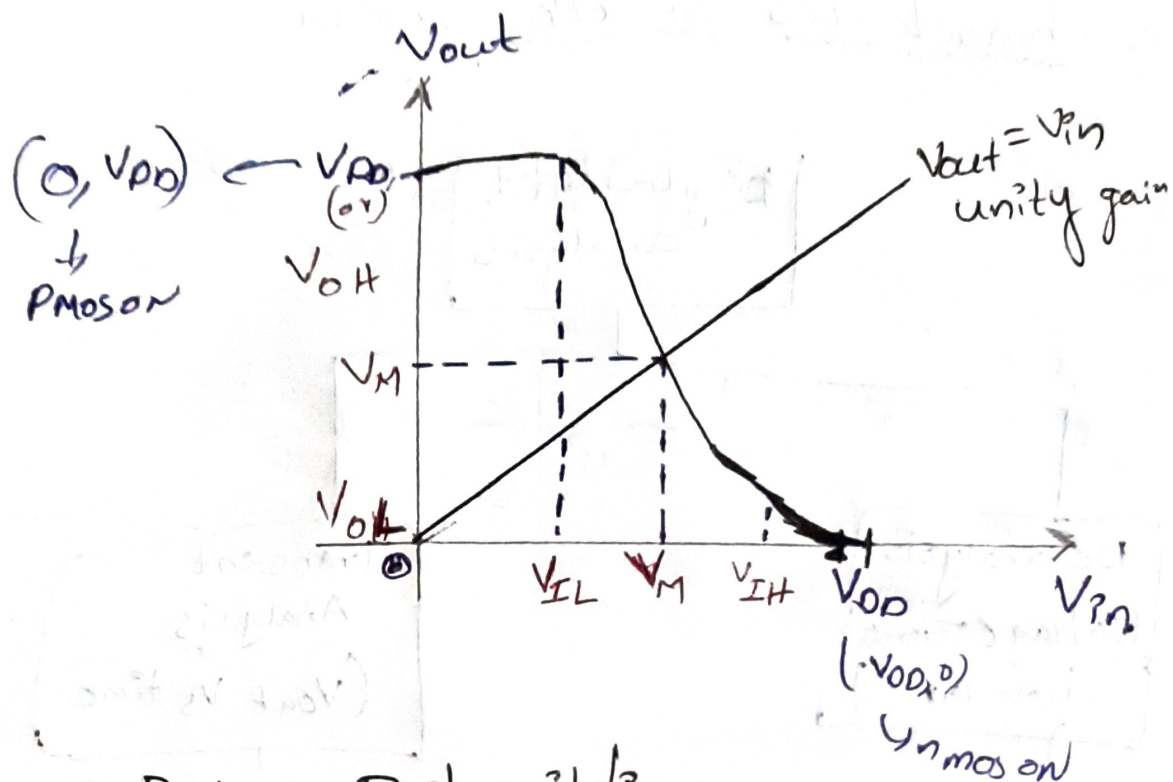


when $V_{in} = 0$; nmos OFF, pmos ON

$V_{out} = V_{DD} = V_{OH}$ at high i/p voltage
(V_{in}, V_{out}) = (0, V_{DD})

when $V_{in} = V_{DD}$, nmos ON, pmos OFF

$V_{out} = 0 = V_{OL}$ at low i/p voltage
(V_{in}, V_{out}) = (V_{DD} , 0)



● Rail to Rail switching:-

→ Swing at o/p = $V_{OH} = V_{OL} = V_{DD}$. This

is known as Full rail o/p. And this type of switching is known as Rail to Rail Switching.

(Operating point at which $V_{out} = V_{in} = V_M$)
Significance of V_M (Mid point Voltage):-

→ If operating point (V_{out}) is above the V_M then it is logic "1" or if the ~~the~~ is the operating point (V_{out}) is less than V_M then it is logic "0"

operating regions for nmos and pmos

$$V_{in} = V_{out} = V_m$$

for saturation (nmos)

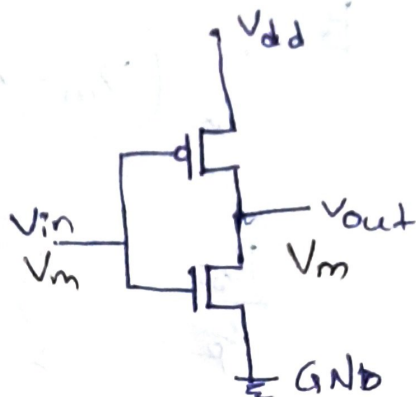
$$V_{GS} \geq V_{GS} - V_T$$

$$\therefore V_m \geq V_m - V_T$$

\Downarrow

True

\therefore nmos is in Saturation



(pmos) :-

$$V_{SD} \geq |V_{SG}| = |V_T|$$

$$V_S = V_{dd}$$

$$\cancel{V_{dd} - V_{in} \geq V_{dd} - V_m} \quad V_D = V_{out}$$

$$V_{dd} - V_{out} \geq V_{dd} - V_m - |V_T|$$

$$\Rightarrow \underline{V_{dd} - V_m \geq V_{dd} - V_m - V_T}$$

\Downarrow

True

\therefore pmos is in Saturation

Current is same from source (pmos) to GND.

for,

nmos

$$I = \frac{B_n}{2} (V_{GS} - V_{Tn})^2 = \frac{B_n}{2} (V_m - V_{Tn})^2 \quad \text{--- (1)}$$

for,

pmos

$$I = \frac{B_p}{2} (V_{SG} - V_{TP})^2 = \frac{B_p}{2} (V_{dd} - V_m - |V_{TP}|)^2 \quad \text{--- (2)}$$

Equating ① & ②

$$\frac{\beta_n}{2} (V_m - V_{Tn})^2 = \frac{\beta_p}{2} (V_{DD} - V_m - |V_{Tp}|)^2$$

$$V_m = \frac{V_{DD} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

At $\beta_n = \beta_p$ & $V_{Tn} = |V_{Tp}|$

then $V_m = \frac{V_{DD}}{2}$

To make

$$\beta_n = \beta_p$$

$\left(\frac{W}{L}\right) \rightarrow$ aspect ratio

$$\beta_n = \mu_n C_{ox} \frac{W}{L} \quad \beta_p = \mu_p C_{ox} \frac{W}{L}$$

but ~~mobility of electrons are high than mobility of holes~~

but mobility of electrons are high than mobility of holes. So, width of pmos should be higher to make equal to n-mos.

\therefore pmos \uparrow than nmos.

Q) $k_n' = 100$; $V_{Tn} = 0.70V$; $k_p' = 42$; $V_{Tp} = -0.80$
 and power supply of $V_{DD} = 3.3V$ is used. Find the
 V_M if $(W/L)_n = 10$ & $(W/L)_p = 14$

Sol:-

$$\frac{B_n}{B_p} = \frac{k_n' (W/L)_n}{k_p' (W/L)_p} = \frac{100 (10)}{42 (14)}$$

$$= \frac{1000}{588} = \underline{\underline{0.1698}}$$

$$V_M = \frac{V_{DD} - |V_{Tp}| + \sqrt{\frac{B_n}{B_p}} V_{Tn}}{1 + \sqrt{\frac{B_n}{B_p}}} = \frac{3.3 - 0.8 + \sqrt{0.1698} (0.7)}{1 + 0.412}$$

$$V_M = \frac{3.3 - 0.8 + (1.304)(0.7)}{1 + 1.304} \quad \boxed{V_M = 1.699}$$

$$\boxed{V_M = 1.481}$$