

I-V relation :-

G_+ V_{GS}

Q) why ~~do~~ don't we have current at Gate? 

Ans: Between the Gate & Drain source terminal we have oxide layer (insulating layer) so current no will flow through Gate region.

Advantage of having no current at Gate.

For BJT we will write I/P & O/P loop

But here we will write only one equation

(as no current in $I_Q = 0$)

* V_{GS} is like a load, V_{DS} is like a cap.

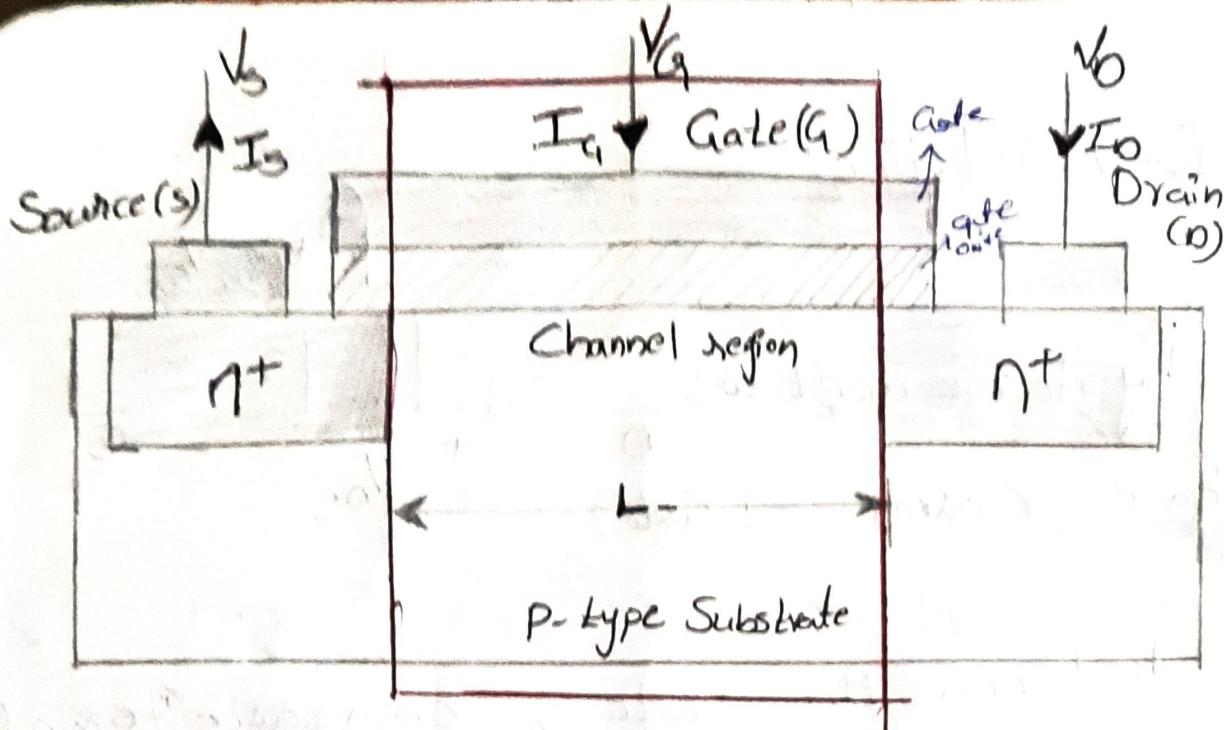
→ If we won't have road, we can't ride a car!

→ In the same way : if we don't have V_{GS}

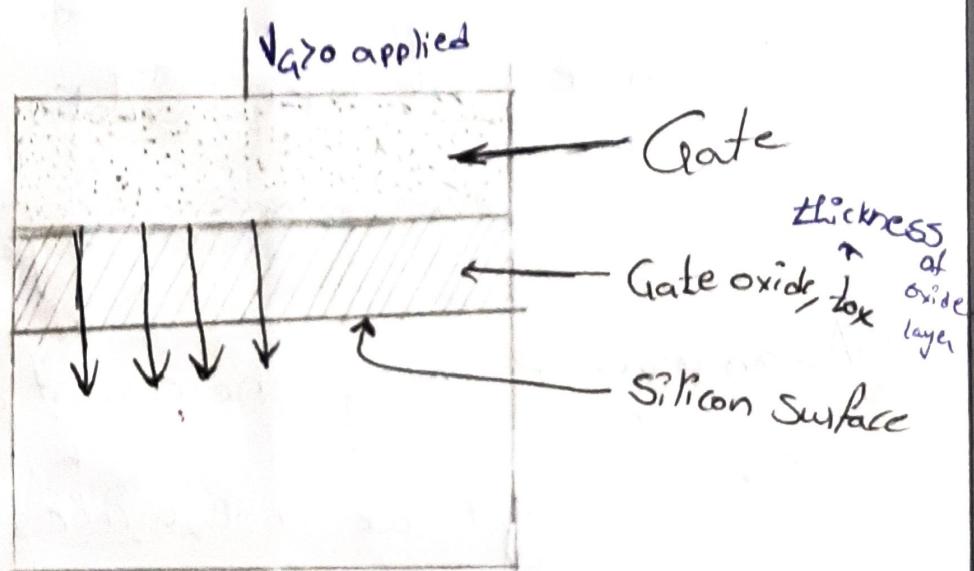
then no channel is formed, then no current

will flow from V_D to V_S . So,

$$I_{Dn} = f(V_{DS}, V_S)$$



(i) $V_G > 0$



* Mosfet is a Surface device, because all the current flowing in this device dependent on the how much ~~the~~ charge is accumulated in the x P-type Surface of the substrate.

WKT,

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

permittivity of the oxide
thickness of oxide layer

→ C_{ox} determines the how much charge
accumulated in the Silicon Surface

$$Q_s = -C_{ox} V_g$$

Surface
charge

$-V_g$ represents
electrons are
accumulated
(n-type)

$$V_s = V_{ox} + Q_s \rightarrow \text{Surface potential.}$$

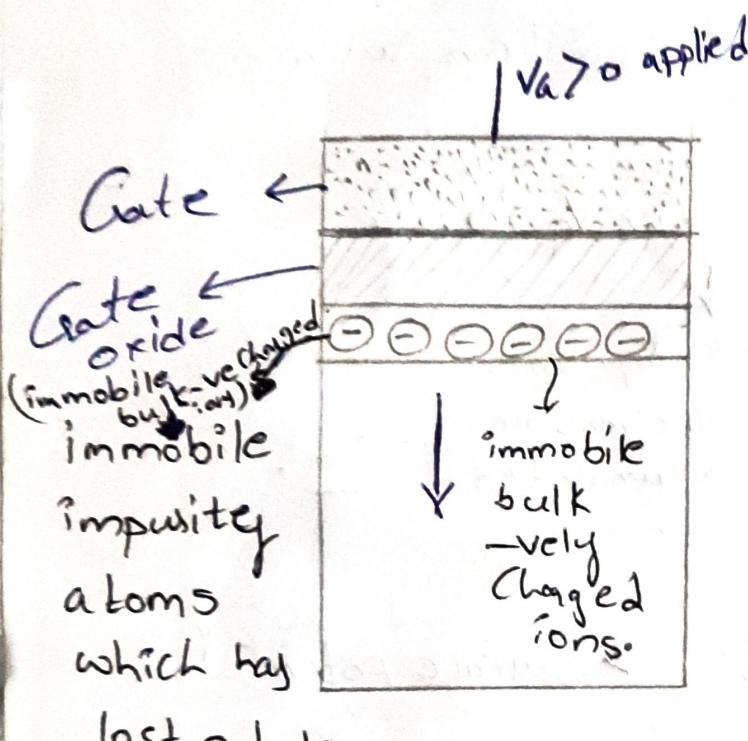
↓
Gate Oxide voltage

Direction of electric field:-

→ As $V_g > 0$; so current flows from high voltage to low voltage, so current (\downarrow) flows down.

→ Current (\downarrow) electrons moves up (electrons are accumulated at the silicon surface)
{ holes moves down (in the direction of current)}

(ii) $V_G < V_{TH}$ \Rightarrow Depletion mode of operation



\rightarrow Current flows down (\downarrow)
electrons (\uparrow), holes (\downarrow)

\rightarrow holes pushed down (\downarrow)
then electrons are
not get attracted
(need more voltage
to attract them).

so immobile bulk

-ve very charged ions
are formed

Contribute to current but they are blocked
inside the silicon crystal; they cannot move

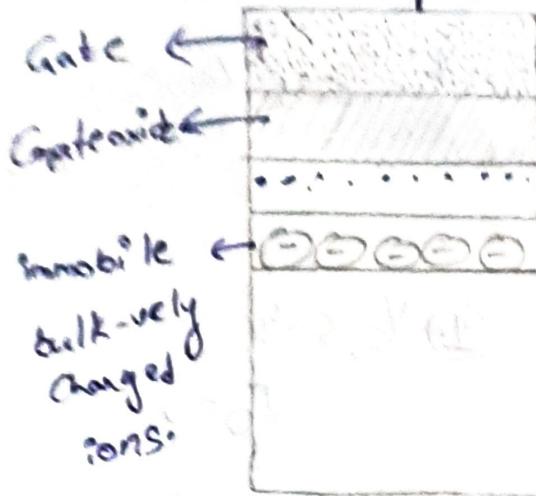
So they cannot contribute to current.

* This mode of operation is known as Depletion mode of operation.

Bulk charge

$$Q_B = -C_{ox} V_G$$

(iii) $V_G > V_{Tn}$, $V_D > 0$ Applied



→ As V_G (applied voltage)

increases (greater than V_{Tn})

then "very charged ions" (e^-)
will attract towards
the Silicon surface.

then channel is formed

Surface charge Q_s

$$Q_s = Q_B + Q_e$$

where,

$$Q_e = -C_{ox} (V_G - V_{Tn})$$

Purpose of V_{GS} & V_{DS} :

V_{GS} : → is used to create the channel

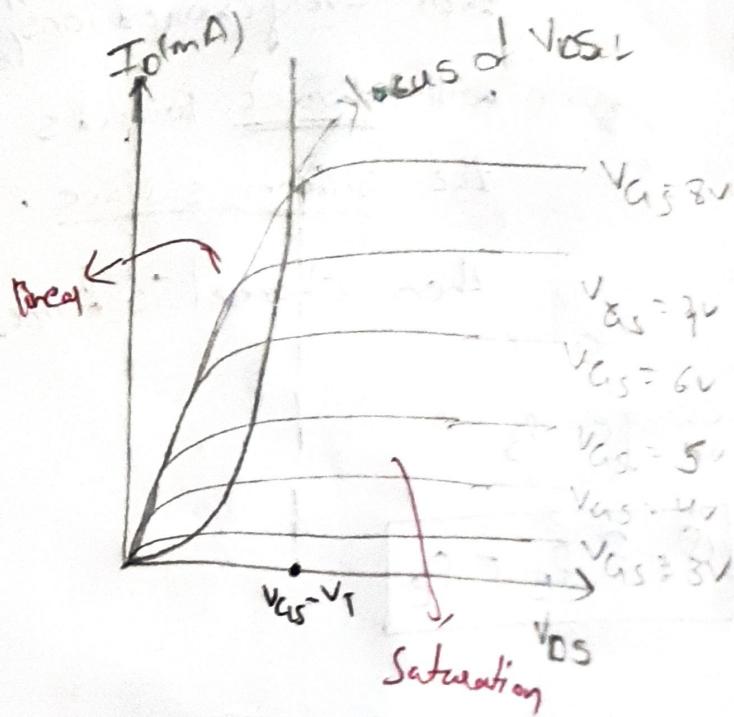
V_{DS} : → provides the potential difference b/w

the source and drain. So
Electrons can move

* V_{DS} : → Voltage difference b/w drain & source

↳ So, Voltage is distributed across
the channel. So, high voltage

will be at Drain terminal and voltage goes on decreasing, low voltage at Source terminal



- ① $V_{GS} < V_T$
 $I_D = 0$
- ② $V_{GS} > V_T$
 - (i) $V_{DS} < V_{GS} - V_T$

① $V_{GS} < V_T \rightarrow I_D = 0$

② $V_{GS} > V_T$

(i) $V_{DS} < V_{GS} - V_T \Rightarrow$ Linear region

$$I_D = \frac{\mu n C_{ox}}{2} \frac{W}{L} [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2]$$

(ii) $V_{DS} > V_{GS} - V_T \Rightarrow$ Saturation
(a)

without
channel
length
modulation

$$I_D = \frac{\mu n C_{ox}}{(sat)} \frac{W}{2} \frac{C_0}{L} [V_{GS} - V_T]^2$$

(b) $V_{DS} > V_{GS} - VT \rightarrow \text{saturation}$

with
channel $\subset \left\{ I_D(\text{sat}) = \frac{\mu_p C_{ox}}{2} \frac{W}{L} [V_{GS} - VT]^2 (1 + \lambda V_{DS}) \right.$

length modulation