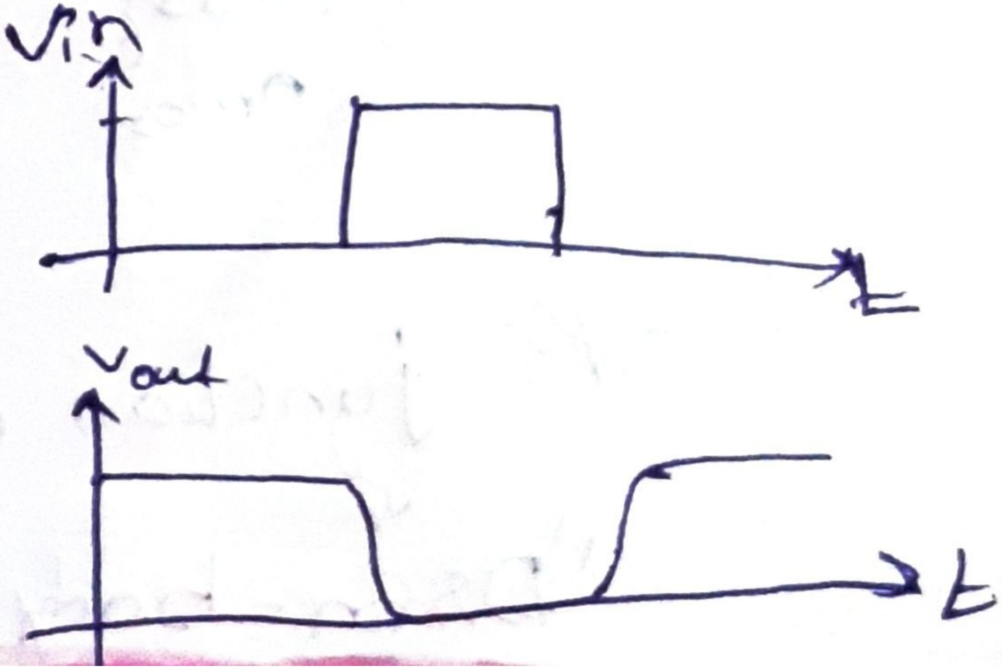
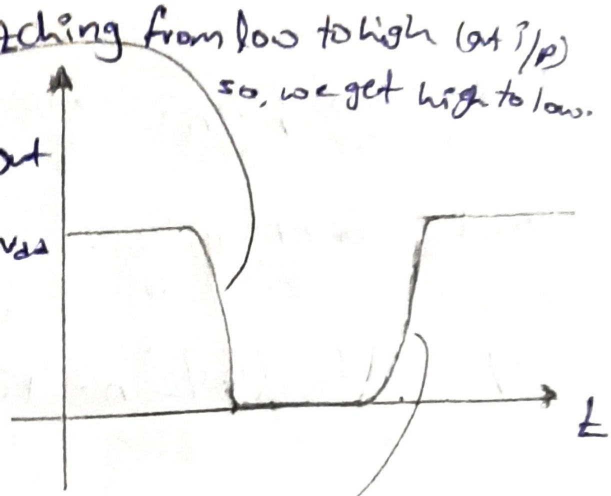
Inverter switching characteristics:-

Switching wave forms:-

Cmos inverter CKT →



→ It takes some time for o/p to fall from Vdd to "0". This is known as Fall time.



It takes some time to rise from "0" to "Vdd" for o/p.

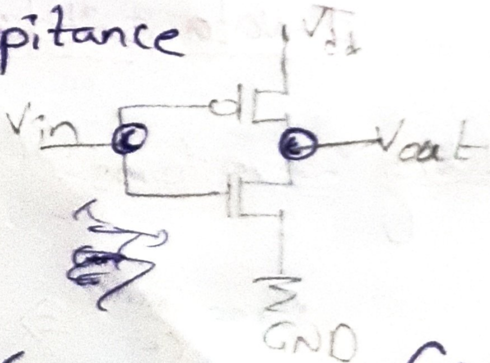
This is known as Rise time.

Reason behind delay in wave forms :- (why is not behaving ideally) Due to

Parasitic elements (ie parasitic capacitance, parasitic resistances).

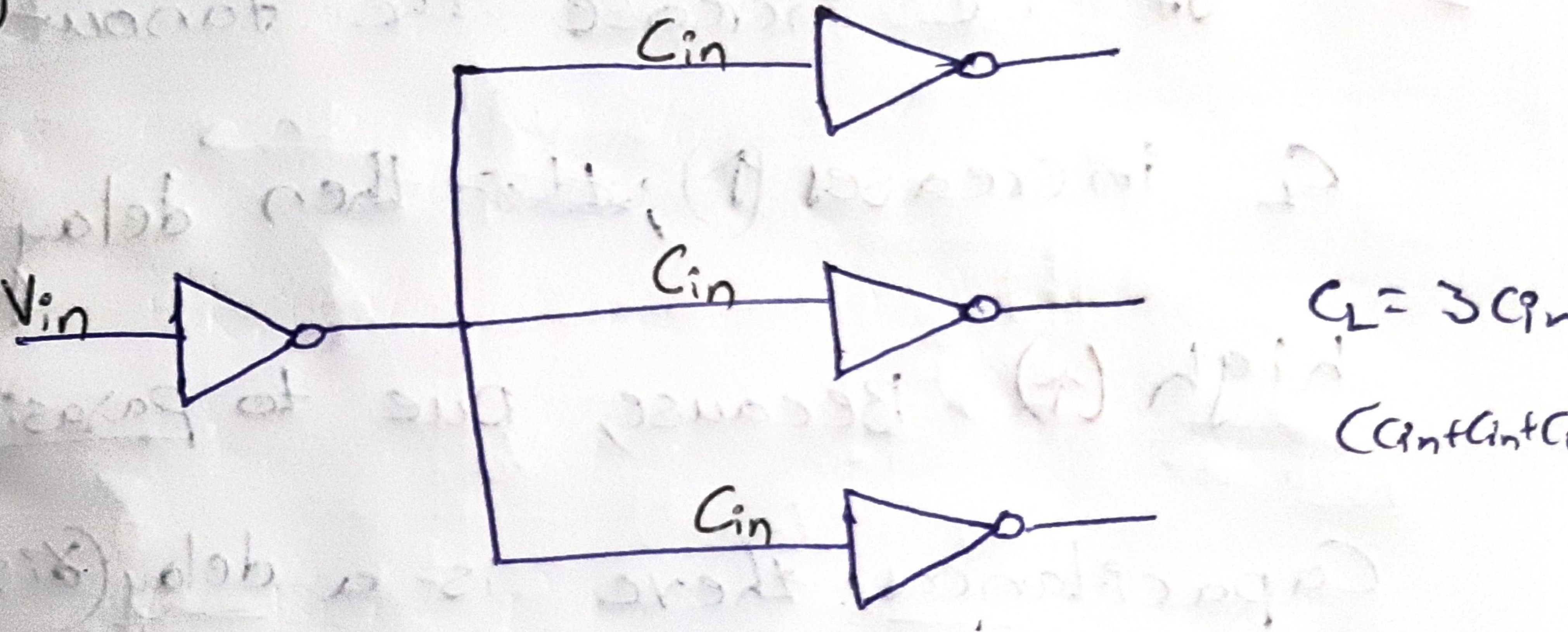
→ Capacitances are Gate & Junction

At i/p :- Gate capitance of Pmos & nmos



At o/p :- junction capacitance
"Drain - body capacitance" } Capacitance at the drain terminal of both Pmos & nmos.

Logic Chain:-



Fanout:-

Morethan "1" o/p. Connected to "1" gate. Then it is Known as "Fanout".

~~Cout~~ $\boxed{C_L = 3C_{in}}$

↓

Load observed by the inverter.

$\therefore \boxed{C_{out} = C_{OB} + C_L}$

Junction Capacitance.

4

Note:- If we increase the fanout then C_L increases (↑); ~~then~~ then delay becomes high (↑). Because, Due to parasitic Capacitances, there is a delay (rise time, Fall time). So, always there will be limitation for the no. of Fanouts Connected to gate.

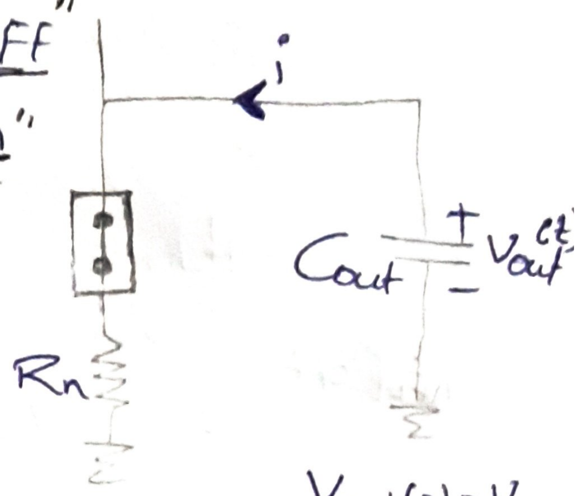
$$C_{out} = \underbrace{C_{FET}}_{\text{Junction}} + \underbrace{C_L}_{\text{Fanout}}$$

Fall time Calculation:-

Based on fall time and rise time we can say, how fast the invater is;

↪ If Fall time is less then the MOSFET is responding quickly. so, we can increase the operating speed of the device.

i/p high
so, Pmos "off"
& nmos "on"



$V_{out}(0) = V_{DD}$

→ Capacitor initially charged to V_{DD}, discharg. through the resistance "R_n"

$$i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{out}}{R_n}$$

$R_n \to$ (nmos / pmos)

$$\boxed{t = T_n \ln\left(\frac{V_{DD}}{V_{out}}\right)}$$

Total time

where $\boxed{T_n = R_n C_{out}}$

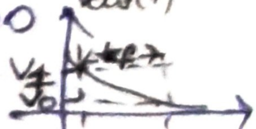
Note:-
so, Total time(t_n) is dependent on R_n

$$\left(t = R_n C_{out} \ln\left(\frac{V_{DD}}{V_{out}}\right)\right)$$

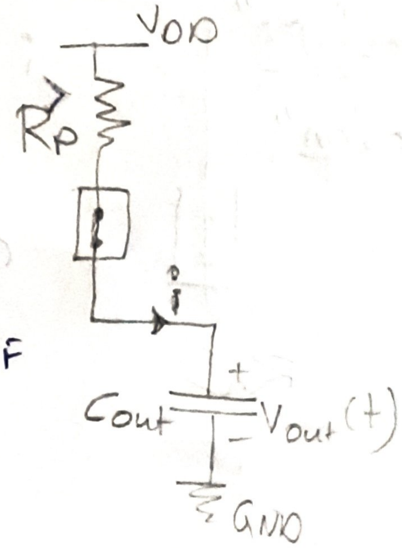
Fall time is from 90% to 10% of total time

∴ substituting $0.9\,V_{DD}$ & $0.1\,V_{DD}$

$$\boxed{t_f = 2.2\,T_n}$$

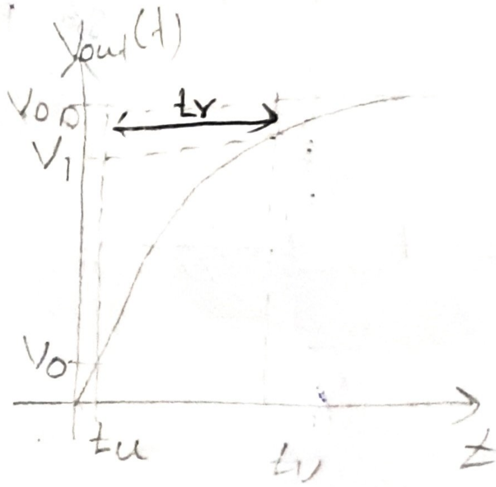


Rise time:-



nFET OFF

$V_{out}(0) = 0V$



Rise time $\leftarrow$ $\boxed{t_r = 2.2\,T_p}$ where $T_p = R_p C_{out}$.

$$f_{max} = \frac{1}{t_{HL} + t_{LH}} = \frac{1}{t_r + t_f}$$

Propagation Delay:- (t_p)

↳ fall upto 50% & rise from 50%

$$t_p = \frac{t_{pf} + t_{pr}}{2}$$

$$\boxed{t_p = 0.35(\underbrace{T_n}_{R_n C_{out}} + \underbrace{T_p}_{R_p C_{out}})}$$