Exp No: 4. 4-bit Down Counter

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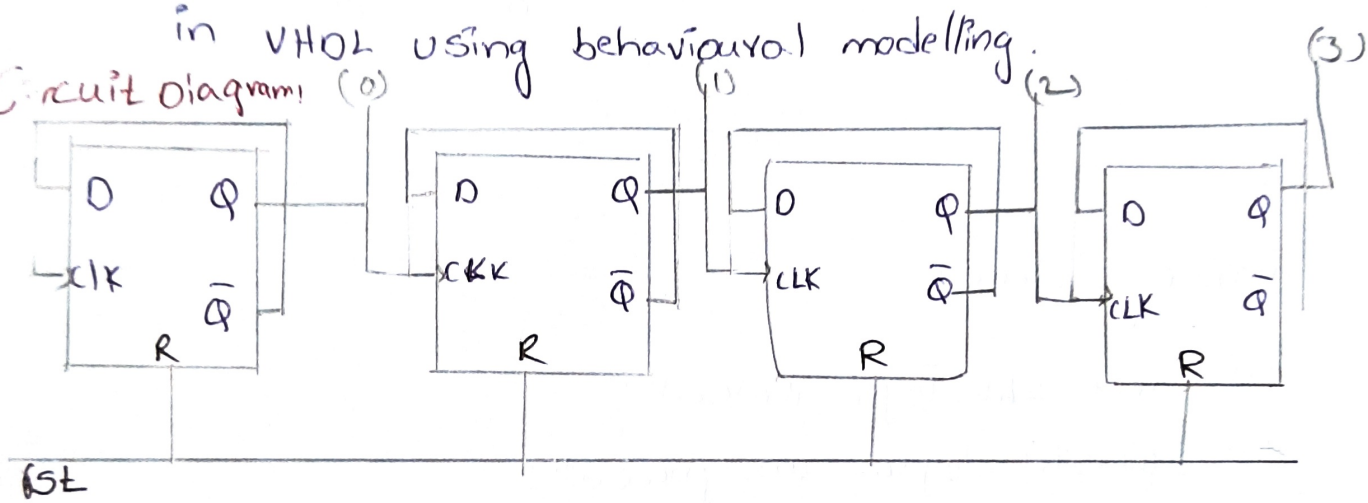
Aim:- Design and implementation of 4-bit down counter in VHDL using behavioural modelling.

Circuit diagram:



Truth table:-

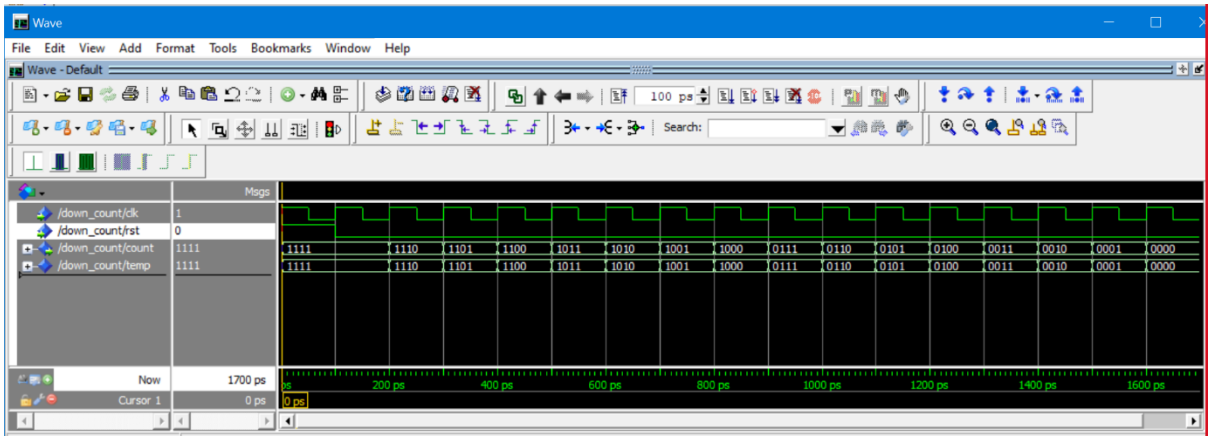
CLK	RST	(3)	(2)	(1)	(0)
↑	1	1	1	1	1
↑	0	1	1	1	0
↑	0	1	1	0	1
↑	0	1	1	0	0
↑	0	1	0	1	1
↑	0	1	0	1	0
↑	0	1	0	0	1
↑	0	1	0	0	0
↑	0	0	1	1	1
↑	0	0	1	1	0

CLK	rst	(3)	(2)	(1)	(0)
↑	0	0	1	0	1
↑	0	0	1	0	0
↑	0	0	0	1	1
↑	0	0	0	1	0
↑	0	0	0	0	1
↑	0	0	0	0	0

Code:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_Arith_all;
entity down_count is
    Port (CLK, rst :in std_logic;
          Count : out std_logic (3 down to 0));
end down_count
architecture down_count_a of down_count is
signal temp: std_logic_vector (3down to 0);
begin
process (clk, rst)
begin
if (rst = '1') then
```

```
temp <= "1111";
elsif (rising_edge (CLK)) then
temp <= temp-1;
end if
end process;
Count <= temp;
end down_ count _a;
```


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/down_count/clk
/down_count/rst
/down_count/count
/down_count/temp
1
0
1111
1111
1111 1110 1101 1100 1011 1010 1001 1000 0111 0110 0101 0100 0011 0010 0001 0000
Now
1700 ps
Cursor 1
0 ps
200 ps 400 ps 600 ps 800 ps 1000 ps 1200 ps 1400 ps 1600 ps

Inference:

VHDL code for 4-bit down counter is implemented using modelsim and the outputs was verified.

*** END ***