EXP NO: 6 Dynamic Simulation of CMOS circuits in Winspice

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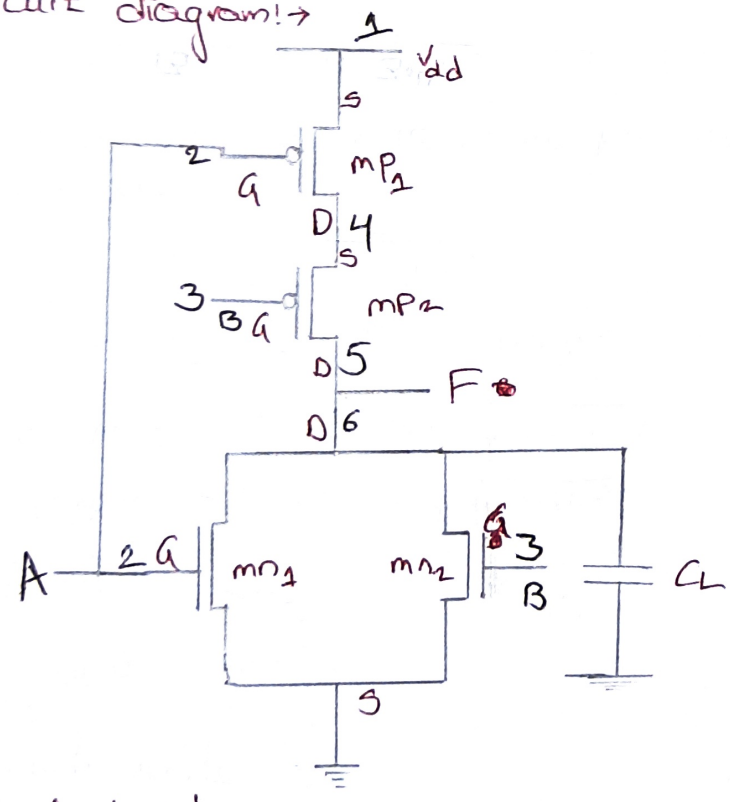
ROLL NO: CB.EN.U4ECE18211	Marks out of 15

Aim:→

To Simulate and analyse transient analysis for 2 input NOR gate and to plot both the input and output for all possible combinations.

Circuit diagram:→



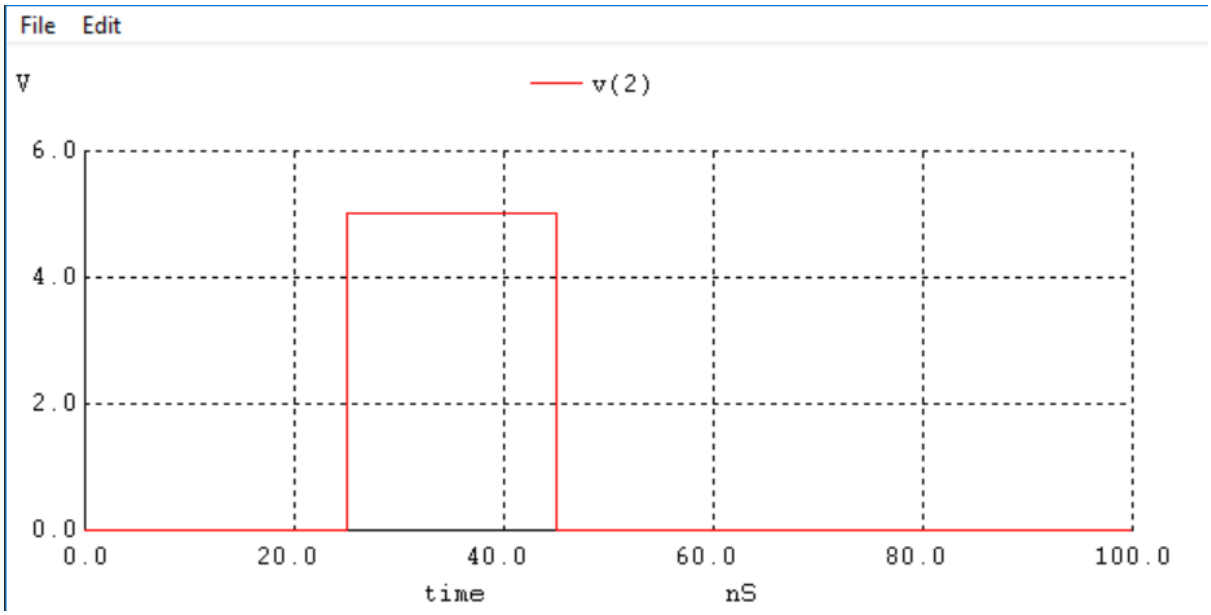
Truth table:-

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

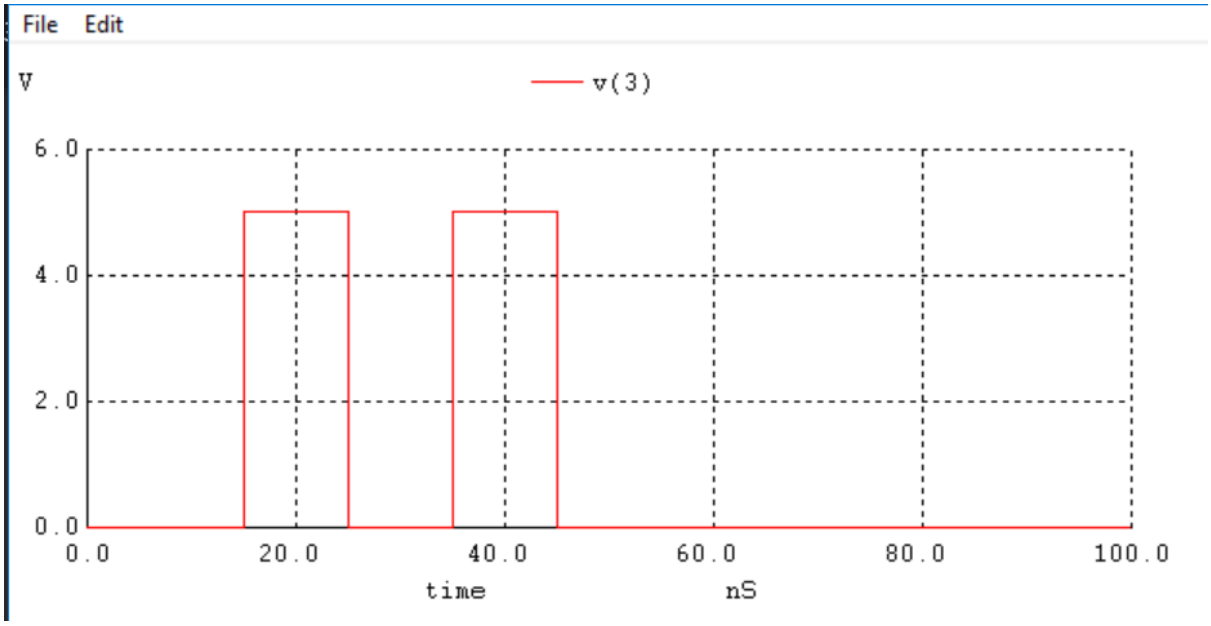
Code:→

```
* cmos transient charac
Vdd 1 0 dc 5
Vin 1 2 0 dc 0 pwl (5ns,0)(15ns,0) (15.001ns,0)
(25ns,0) (25.001ns,5) (35ns,5) (35.001ns,5)
(45ns,5) (45.001ns,0) (55ns,0)
Vin 2 3 0 dc 0 pwl (5ns,0) (15ns,0) (15.001ns,5)
(25ns,5) (25.001ns,0) (35ns,0), (35.001ns,5), (45ns,5)
(45.001ns,0) (55ns,0)
Vdum 5 6 dc 0
Mp1 1 2 4 1 MODp W=4U 1=1U
Mp2 4 3 5 1 MODP W=4U 1=1U
Mn1 6 2 0 0 MODn W=4U 1=1U
Mn2 6 3 0 0 MODn W=4U 1=1U
C 5 0 400fF
.tran 1ns 100ns
.plot tran V(2)
.plot tran V(3)
.plot tran V(5)
```

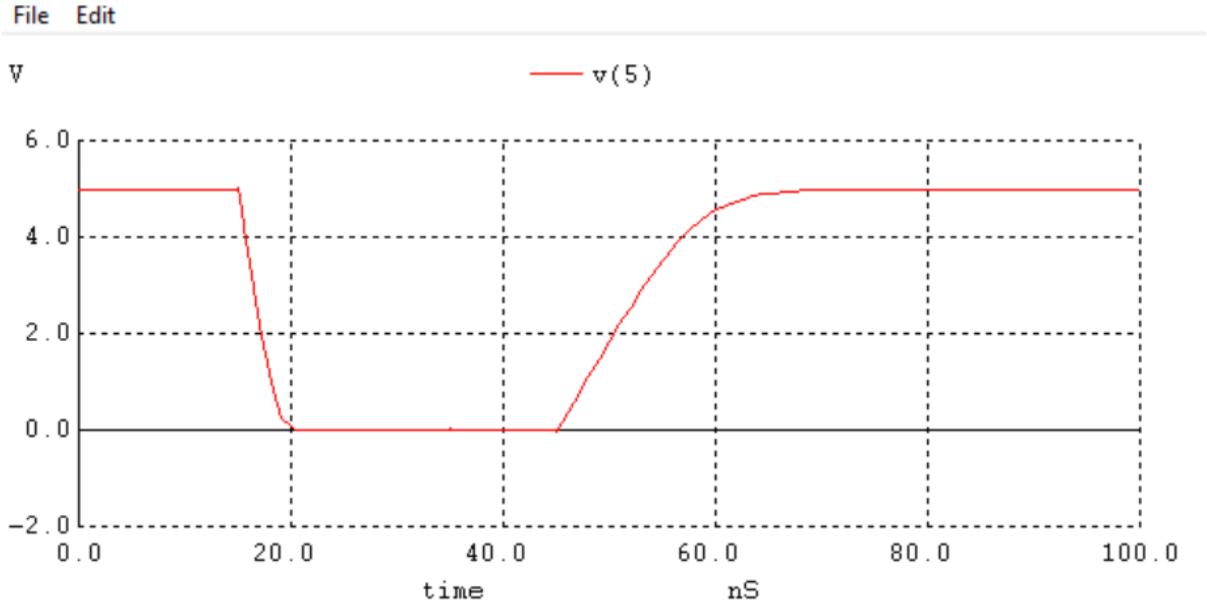
INPUT1



INPUT2



OUTPUT



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Calculation:→

Fall time

Voltage range (0-5)

10% of 5 = 0.5

90% of 5 = 4.5

0.5 volts is occured at 15.4ns

4.5 volts is occured at 18.8ns

∴ Fall time = 18.8ns - 15.4ns

= 3.4ns

Rise time

Voltage range (0-5)

10% of 5 = 0.5

90% of 5 = 4.5

0.5 volts is occured at 46.5ns

4.5 volts is occured at 59.5ns

∴ Rise time = 59.5ns - 46.5ns

= 13ns

Inference:

CMOS nor gate is implemented, rise time and fall time are 13ns and 3.4ns and transient analysis is done