Exp No:- 01

Design and Simulation of Combinational Circuit behavioural

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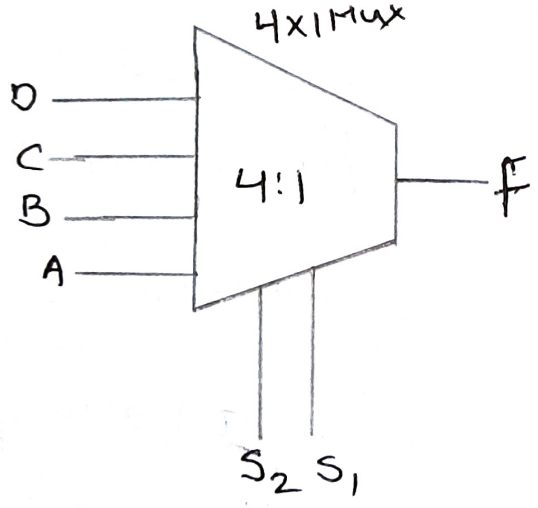
Aim:→

To understand the modelsim software and write the basic programs using different modellings.

Block/circuit Diagram:→



4-data points
D, C, B A

selection lines
S_2, S_1

Truth Table:

selection Lines		Data points				output
S_2	S_1	D	C	B	A	F
0	0	X	X	X	A	A
0	1	X	X	B	X	B
1	0	X	C	X	X	C
1	1	D	X	X	X	D

Code:

```
Library ieee;
use ieee.std_logic_1164.all;

Entity mux is
Port ( s1: in std_logic;
       s2: in std_logic;
       a: in std_logic;
       b: in std_logic;
       c: in std_logic;
       d: in std_logic;
       F: out std_logic
);
end mux;
architecture OR_arch of mux is
begin
    process(s1,s2,a,b,c,d)
    begin
        -- Compare to truth table
        if ((s1='0') and (s2='0')) then
            F<=a;
        elsif ((s1='0') and ((s2='1')) then
            F<=b;
        elsif ((s1='1') and ((s2='0')) then
            F<=c;
        Else
            F<=d;
```

```
        Endif;
    End process;

End   OR_arch;
```

4x1 Multiplexer

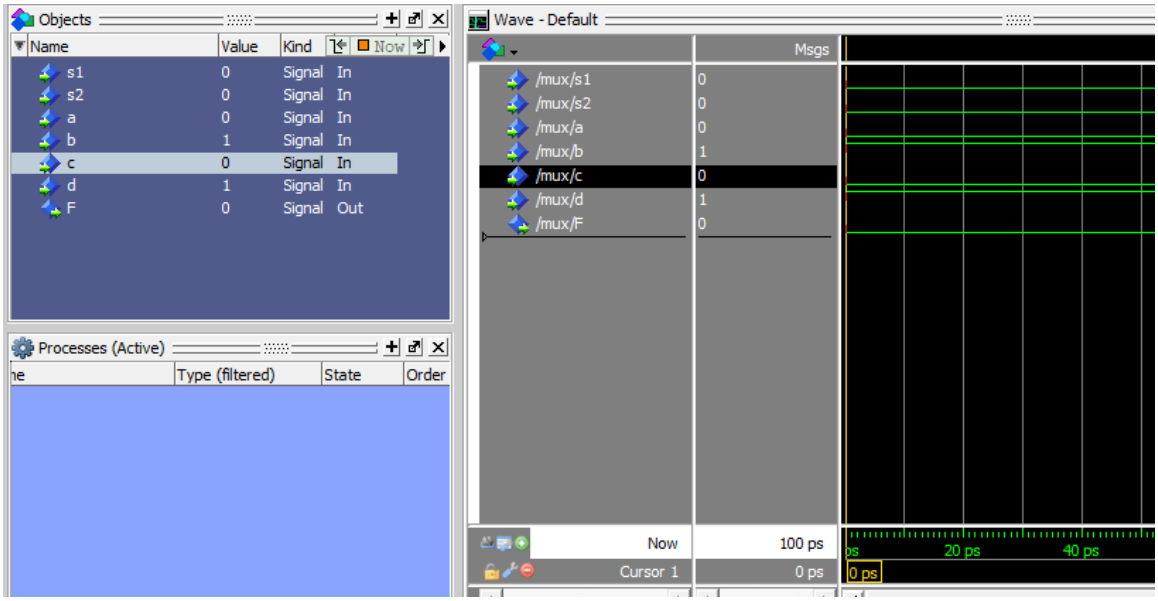
4x1 Multiplexer has four data inputs D,C,B & A two selection lines S2 & S1 and one output F

Select lines are **S2 S1** , where

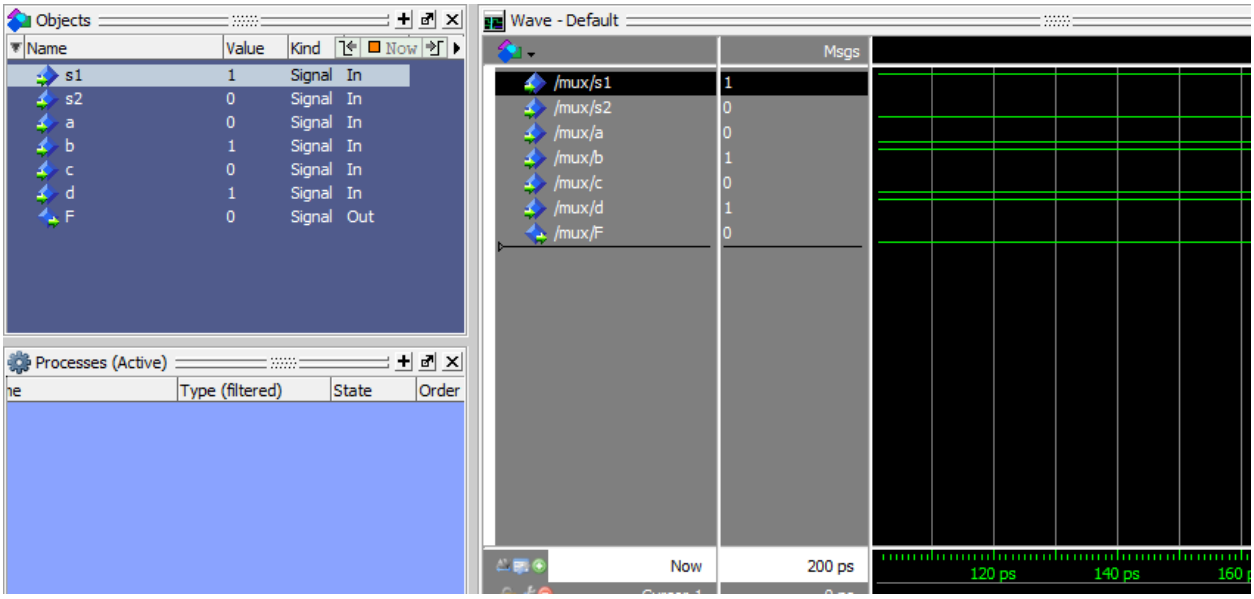
S2 is MSB

S1 is LSB

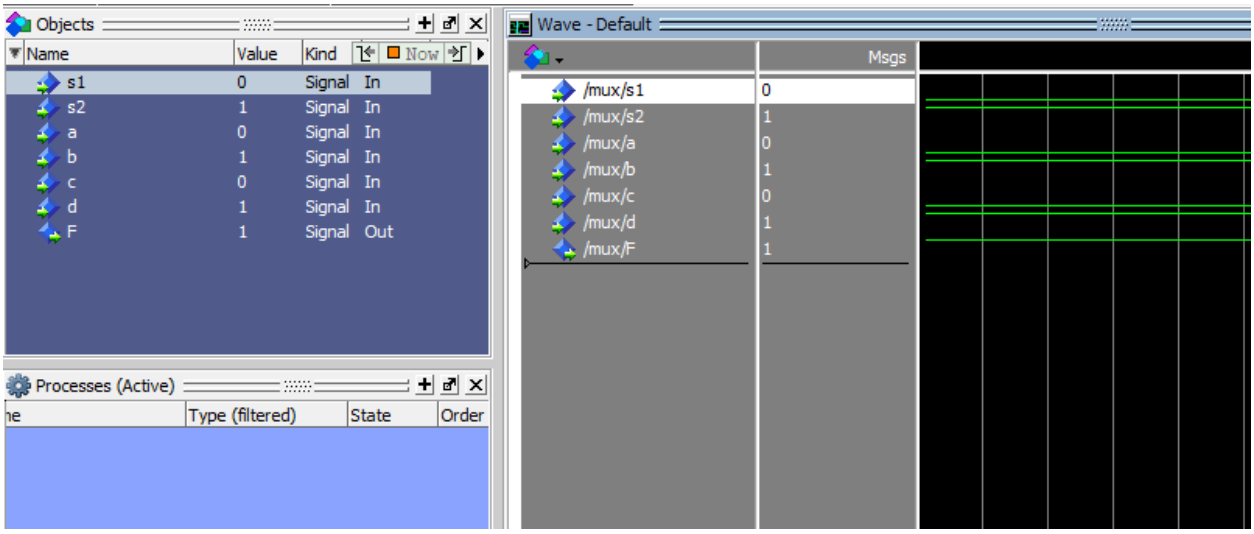
CASE-1:



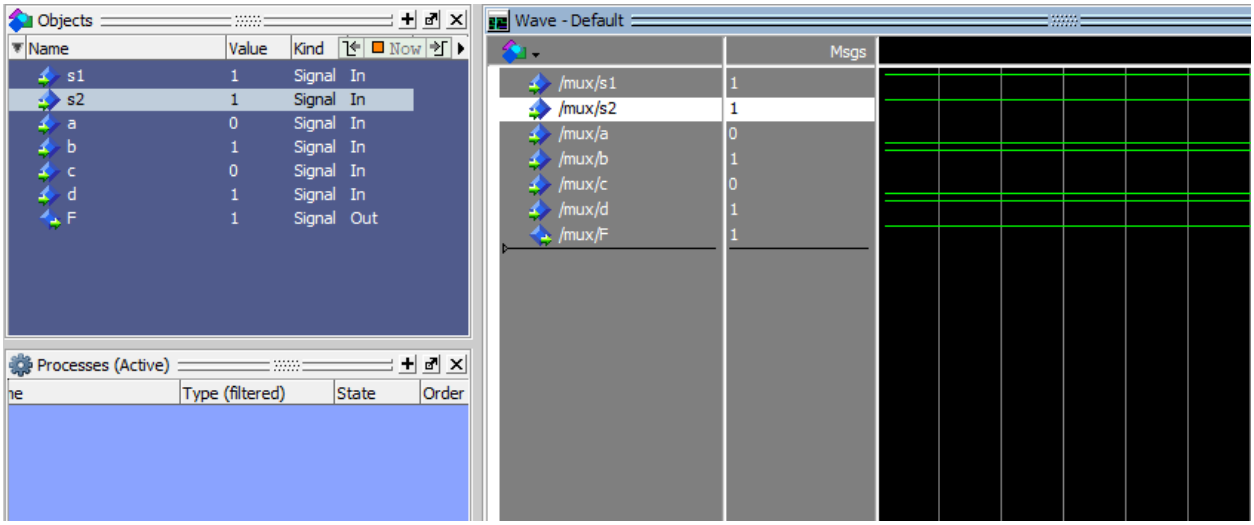
CASE-2:


Objects
Name
Value
Kind
Now
s1 1 Signal In
s2 0 Signal In
a 0 Signal In
b 1 Signal In
c 0 Signal In
d 1 Signal In
F 0 Signal Out
Processes (Active)
Type (filtered)
State
Order
Wave - Default
Msgs
/mux/s1 1
/mux/s2 0
/mux/a 0
/mux/b 1
/mux/c 0
/mux/d 1
/mux/F 0
Now
200 ps
120 ps
140 ps

CASE-3:


Objects
Name
Value
Kind
Now
s1 0 Signal In
s2 1 Signal In
a 0 Signal In
b 1 Signal In
c 0 Signal In
d 1 Signal In
F 1 Signal Out
Processes (Active)
Type (filtered)
State
Order
Wave - Default
Msgs
/mux/s1 0
/mux/s2 1
/mux/a 0
/mux/b 1
/mux/c 0
/mux/d 1
/mux/F 1

CASE-4:


Objects
Name
Value
Kind
Now
s1
1
Signal
In
s2
1
Signal
In
a
0
Signal
In
b
1
Signal
In
c
0
Signal
In
d
1
Signal
In
F
1
Signal
Out
Processes (Active)
Type (filtered)
State
Order
Wave - Default
Msgs
/mux/s1
/mux/s2
/mux/a
/mux/b
/mux/c
/mux/d
/mux/F
1
1
0
1
0
1
1

Inference:

Code was written on 4x1 mux and the output for the given inputs were verified and the graph values were accurate. We got familerized with the new software on digital circuits