

Exp No: 2

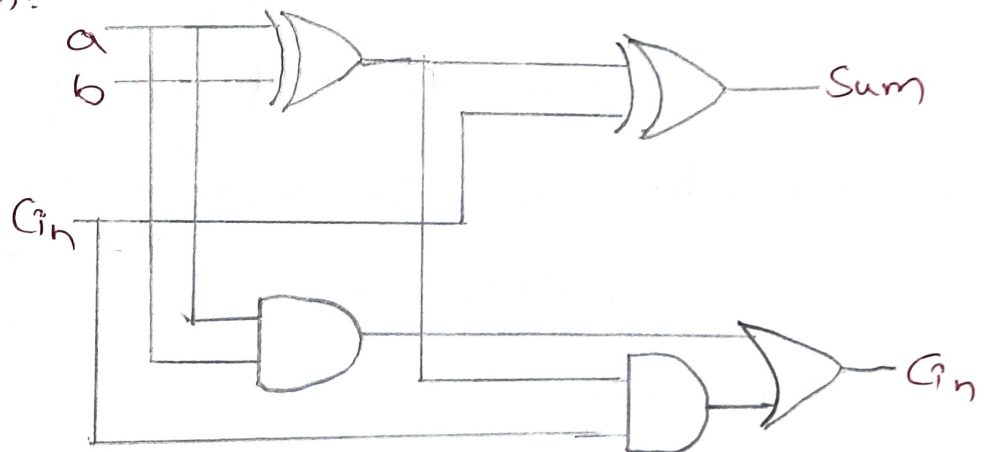
Full Adder

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Aim:- Design a full adder using VHDL.

Tools used:- modelsim

Block diagram:-



Truth Table:-

Input			output	
a	b	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Codes

```
library ieee;
```

```
use ieee.std_logic_1164.all;
```

```
entity xor2 is
```

```
    Port (a: in std_logic;
```

```
          b: in std_logic;
```

```
          c: out std_logic
```

```
    );
```

```
end xor2;
```

```
architecture xor2_a of xor2 is
```

```
begin
```

```
    c <= a xor b;
```

```
end xor2_a;
```

```
library ieee;
```

```
use ieee.std_logic_1164.all;
```

```
entity and2 is
```

```
    Port (a: in std_logic;
```

```
          b: in std_logic;
```

```
          c: out std_logic
```

```
    );
```

```
end and2
```

architecture and2a of and2 is

begin c<a and b;

end and2a;

library ieee;

use ieee.std_logic_1164.all;

entity or2 is

Port (a: in std_logic;

b: in std_logic;

c: out std_logic

);

end or2;

architecture or2_a of or2 is

begin

c<=a or b;

end or2_a;

library ieee;

use ieee.std_logic_1164.all;

entity full_adder is

Port (a: in std_logic;

b: in std_logic

cin: in std_logic;

Sum: out std_logic;

Carry: out std_logic;

);

architecture full-adder_a of full-adder is

Component xor2

Port (a: in std-logic;
b: in std-logic;
c: out std-logic

);

end component

Component or2

Port (a: in std-logic;
b: in std-logic;
c: out std-logic

);

End component;

Signal d: std-logic;

Signal e: std-logic;

Signal f: std-logic;

begin

u1 : xor2 port map (a => a, b => b, c => d);

u2 : xor2 port map (a => d, b => cin, c => Sum);

u3 : and2 port map (a => a, b => b, c => e);

u4 : and2 port map (a => d, b => cin, c => f);

u5 : or2 port map (a => f, b => e, c => carry)

end fulladder_a.

Objects

Name	Value	KI	123 ps
a	0	Signal	In
b	0	Signal	In
cin	1	Signal	In
sum	1	Signal	Out
carry	0	Signal	Out
d	0	Signal	Internal
e	0	Signal	Internal
f	0	Signal	Internal

Processes (Active)

Name	Type (filtered)	State

Wave - Default

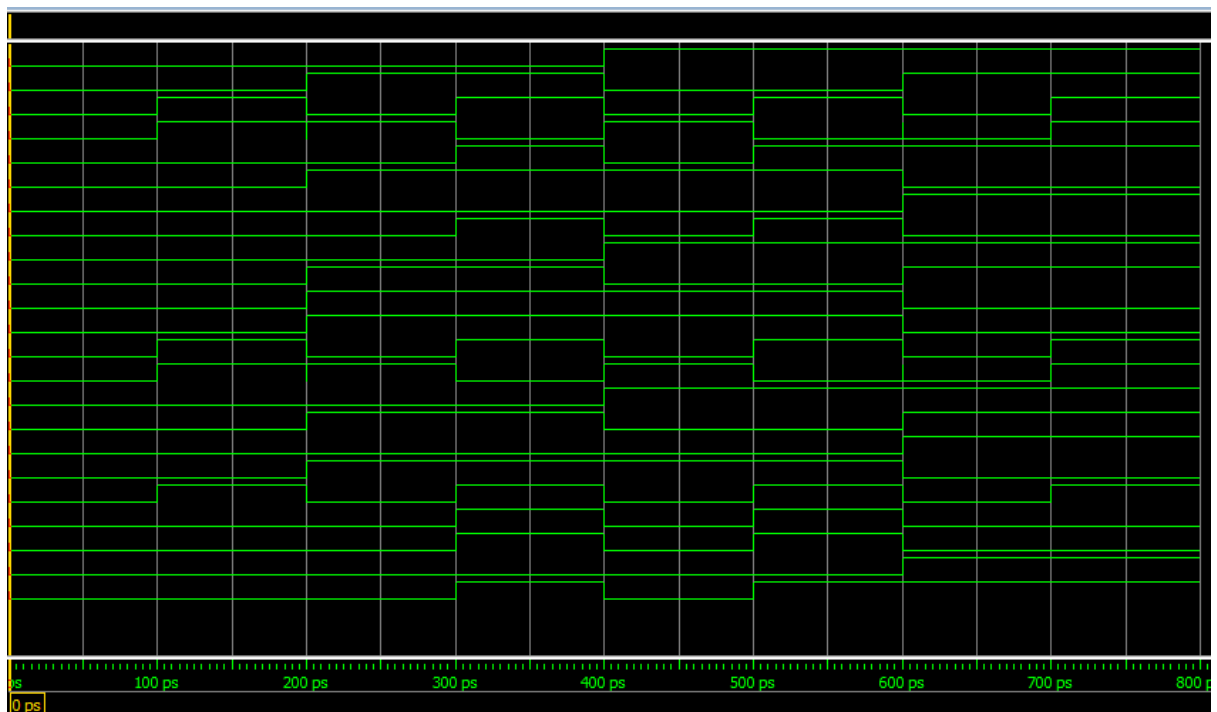
	Msgs
/full_adder/a	0
/full_adder/b	0
/full_adder/cin	1
/full_adder/sum	1
/full_adder/carry	0
/full_adder/d	0
/full_adder/e	0
/full_adder/f	0
/full_adder/u1/a	0
/full_adder/u1/b	0
/full_adder/u1/c	0
/full_adder/u2/a	0
/full_adder/u2/b	1
/full_adder/u2/c	1
/full_adder/u3/a	0
/full_adder/u3/b	0
/full_adder/u3/c	0
/full_adder/u4/a	0
/full_adder/u4/b	1

Now

800 ps

Cursor 1

123 ps



Order of inputs is corresponding to truth table .

Inference:

Full adder Code has been written and compiled using modelsim and the expected output is being observed and matched to truth table.

* * * END * * *