Exp No: 3

SR Flip Flop

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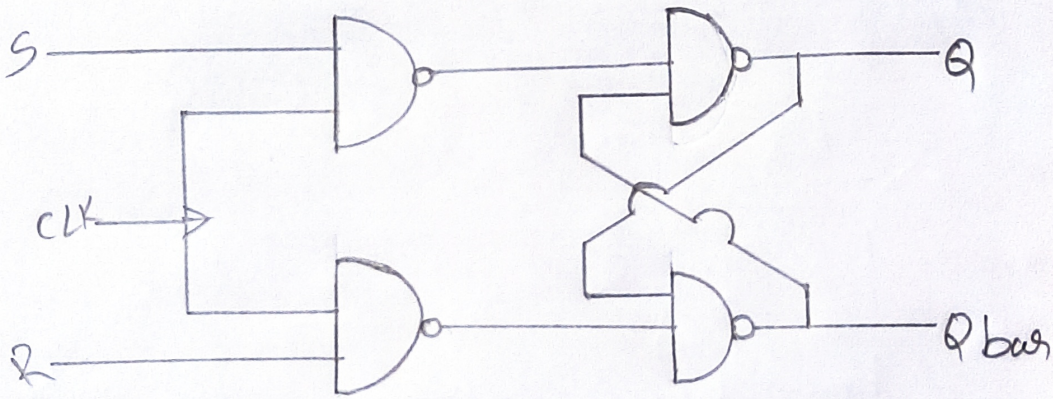
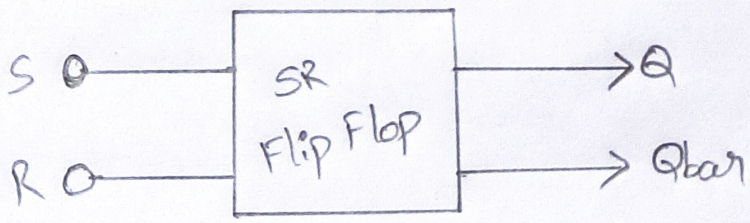
Aim: To implement SR Flip Flop by using VHDL Code

Circuit Diagram



Block diagram



Truth table:

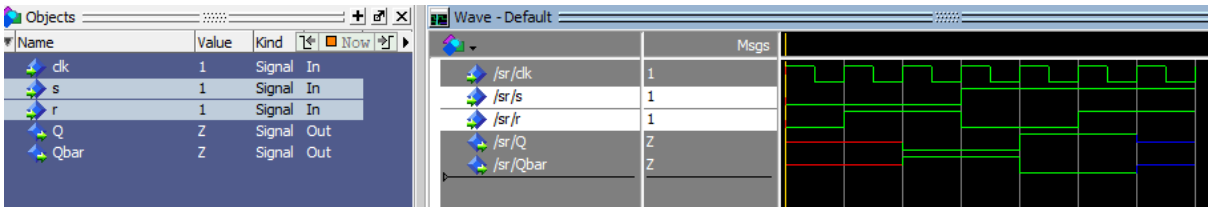
CLK	S	R	Q	Qbar
↑	0	0	0	1
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	-	-

Code :-

```
library ieee;
use ieee.std_logic_1164.all;
entity SR_flipflop is
Port ( clk : in std_logic;
       S : in std_logic;
       R : in std_logic;
       Q : out std_logic
       Qbar : out std_logic
end SR_flipflop;
architecture SR_flipflop_flow of SR_flipflop is
begin
    process (clk, S, R)
        begin
        if clk = '1' and clk'event ) then
            if (S = '0') and (R = '1')) then
                Q <= S;
                Qbar <= R;
            elsif (S = '1') and (R = '0')) then
                Q <= S;
                Qbar <= R;
```

```
elsif ((S = '1') and (r='1')) the
        Q<= 'Z';
        Qbar<= 'Z';
    end if;
  end if;
end process
end SR_flipflop_tbw;
```

OUTPUT



Inputs are in the order of

(I) S,R =(0,0)
(II) S,R =(0,1)
(III) S,R =(1,0)
(IV) S,R =(1,1)

Inference:

VHDL code for SR Flip Flop was written and Compiled. outputs corresponding to truthtable was observed and equal And the graphs are verified.

END