

**Problem Statement 1:** Implement 4-bit ripple carry adder. Optimize the adder for speed. Assume load capacitance to be 50 pF, VDD = 3.3 V. You may assume input capacitance to be 2 pF (for the input A[3:0], B [3:0] and Cin) if required in the calculation.

**Solution:** Designed a single bit full adder using LT Spice and then made its symbol and used it as an instance for 4-Bit FA by instantiating single bit FA four times and optimized for speed.

Below is the analysis of 1-Bit FA and delay calculations theoretically. Also sizing analysis is done in below attachments.

P.Y

Analysis of 1-bit Full Adder :-

Inputs  $\rightarrow A, B, Cin$   
 Outputs  $\rightarrow \text{Sum}(S)$  or  $\text{Sum}(\text{out})$ ,  
 Carry out (Carry-bit).

Truth Table

A	B	Cin(C)	Sumout	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sumout (Kmap)

$A' B' C' \quad 00\ 01\ 11\ 10$

$\bar{A}'$	0	1	0	1
$\bar{A}$	1	0	1	0

$\text{Sumout} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= A \oplus B \oplus C$

Carry out (Kmap)

$A' B' C' \quad 00\ 01\ 11\ 10$

$\bar{A}'$	0	0	1	0
$\bar{A}$	1	0	1	0

$Cout = AB + BC + AC$

Kmap for carry out

Simplified expression,

$\text{Sumout} = \overline{\text{Cout}}(A+B+C) + ABC$

$\text{Cout} = AB + C(A+B)$

Here, for level-3 SPICE, we have,

$M_n : M_p = 3 : 1$

$\therefore I_d = \frac{M_n}{2} \text{Cox} \left( \frac{W}{L} \right) (V_{GS} - V_{TH})$

current in saturation region

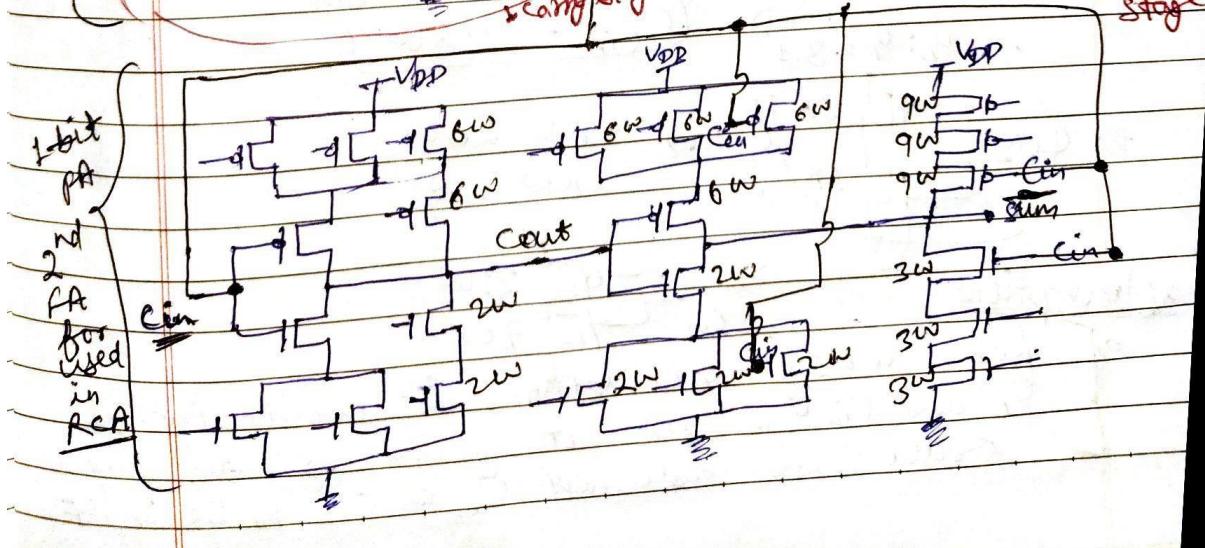
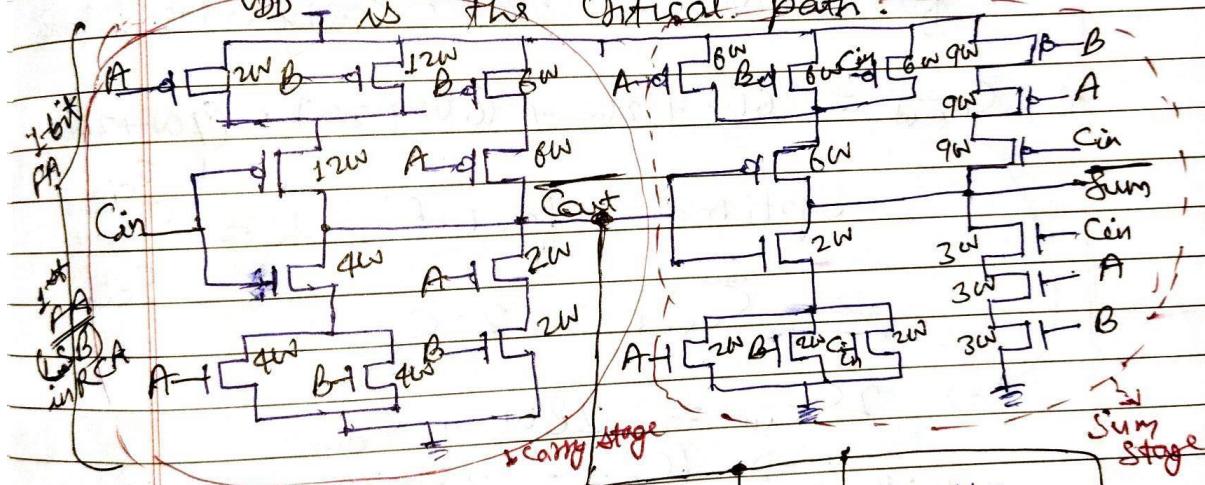
$\Rightarrow \left( \frac{W}{L} \right)_{PMOS} = 3 \times \left( \frac{W}{L} \right)_{NMOS}$

$C_{out}$  is fed to sum stage to obtain sum and also to the inverter to get  $C_{out}$ .

So, driver ckt. has its sizing twice that of load ckt. (twice of maintaining 3:1). Also, since for FA to give result, it's the carryin ( $C_{in}$ ) which must be available initially and at last  $C_{out}$  is the o/p which we get means path from  $C_{in}$  to  $C_{out}$  (or  $\bar{C}_{out}$ ) is the slowest path.

→ path from  $C_{in}$  to  $C_{out}$  (or  $\bar{C}_{out}$ )

$V_{DD}$  T is the critical path:



for minimum delay, we do 4-bit  
 delay calculation; generally,  
 Here, logical effect of carry  
 stage = 2.

$$\text{Stage Ratio} = \frac{\text{Cout of carry stage}}{\text{Cin}}$$

$$= 2$$

$\Rightarrow$  Optimal fanout is 2.

Calculating ifp capacitance ( $C_{out}$ ) at  
 carry in of next F.A. by finding  
 Capacitance at Cout node of F.A.

$\therefore$  Cout acts as carry in to the next  
 full adder in ripple carry adder (4-bit).

$$\Rightarrow C_{out} = 6w + 2w + (6w + 2w) + (9w + 3w)$$

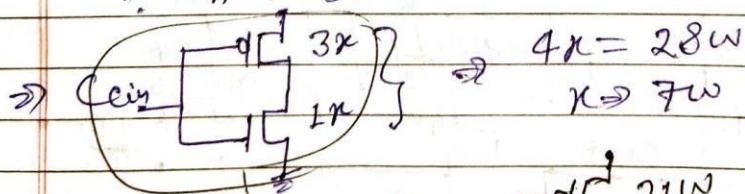
$$\therefore \text{optimal fanout} = 2 = \frac{C_{out}}{C_{in}}$$

$$\Rightarrow C_{out} = 2 C_{in}$$

$$\Rightarrow 2C_{in} = 28w + C_{in}$$

$$\Rightarrow C_{in} = 28w$$

$$\therefore M_h : M_p = 3:1$$

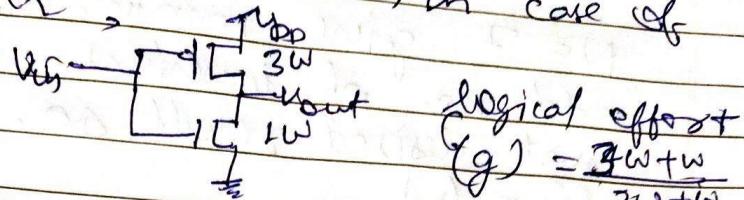


### Assumptions

$\Rightarrow$  for delay calculation, as while taking  
 $C_L$  and  $C_{in}$  is PF it gives  $(\frac{C_L}{C})$  of higher  
 order, so assumed  $C_L$  &  $C_{in}$  to be in FF.



Delay Calculation using logical effort:-  
for  $U_p: U_p = 3:1$ , in case of  
Inverter  $\rightarrow$



$$\text{logical effort } (g) = \frac{3w+w}{3w+w} = 1$$

$$C_{in} = (3w + w) = 4w$$

$\because$  given (assumed),

$C_L = 50 \text{ fF}$ , and  $C_{in} = 2 \text{ fF}$ .  
1-bit FA cell implemented has two stages named as,  $\rightarrow$  sum stage (I)  
 $\rightarrow$  carry stage (II)

Overall logical effort of  $C_{in}$ ,

$$G_1 = g_1 \cdot g_2 = \left( \frac{28w}{4w} \right) \times \left( \frac{6w+2w+9w+3w}{4w} \right) = 7 \times 5 = 35$$

Electrical effort,

$$H = \frac{C_{out}}{C_{in}} = \frac{50 \text{ fF}}{2 \text{ fF}} = 25$$

Overall path effort ( $F$ ),

$$F = GBH \quad (\because B=1)$$

$$\text{Delay Optimization} = 35 \times 25 = 875$$

$$\text{Optimal no. of stages} = \log_{3.59} F$$

$$P = 1+2+9+1+1+5+1+1 = 20$$

$$N = 5.30$$

So, for  $N=5$ ,

$$d = 5 \times (875)^{\frac{1}{15}} + 20 = 39.38 \text{ fT}$$

for  $N=6$ ,

$$d = 6 \times (875)^{\frac{1}{16}} + 20 = 38.59 \text{ fT}$$

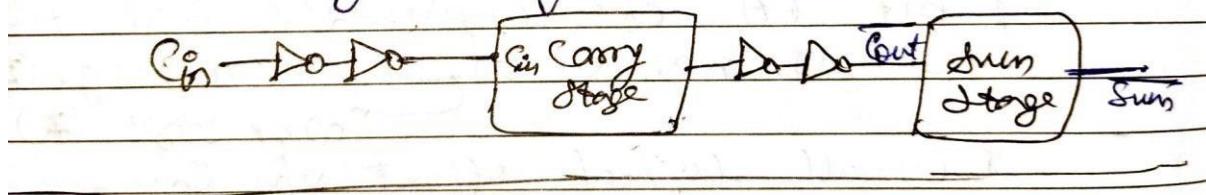
$$\text{for } N=7, d = 7 \times (875)^{\frac{1}{17}} + 20 = 38.42 \text{ fT}$$

$$\text{for } N = 8, d = 8 \times (875)^{1/8} + 20 \\ = (38.65)2$$

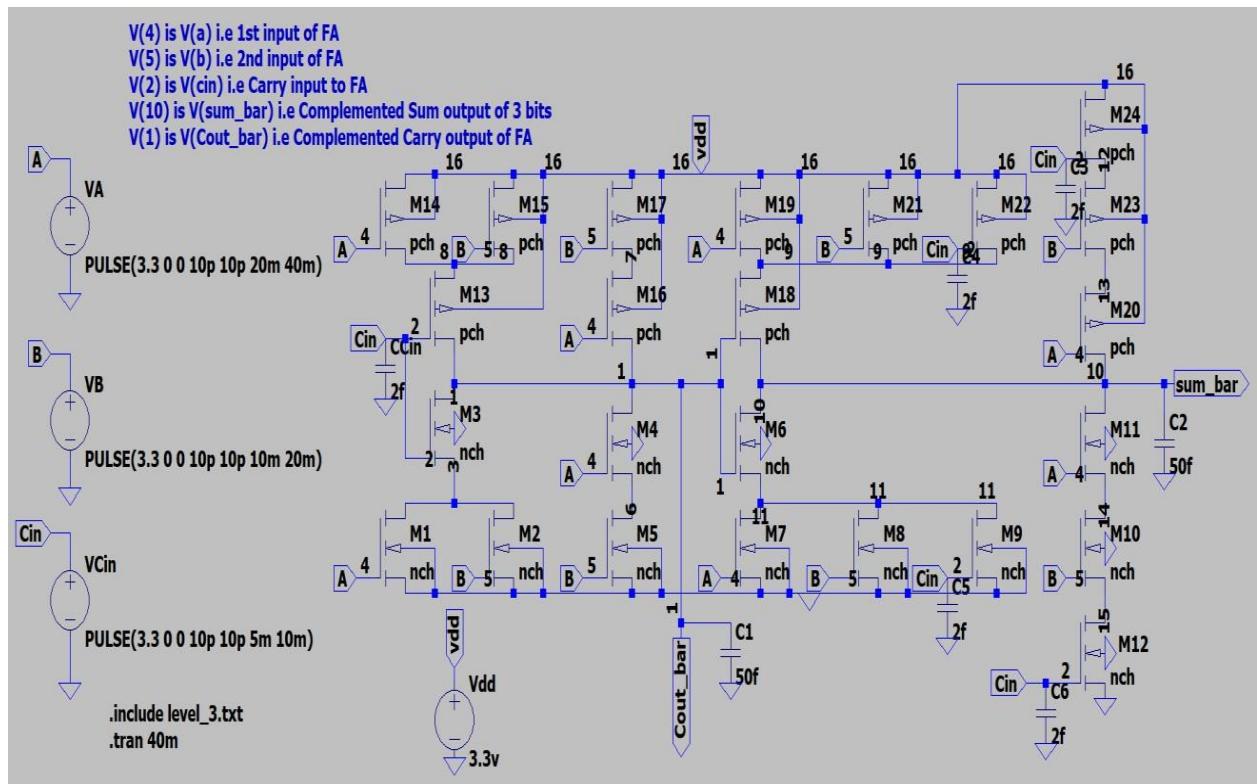
$N = 7$  give minimum delay, but odd no of inverters will result in not desired result so, we take.

$$(N = 6)$$

As already two stages there, so, we add 4 inverters for optimizing delay.



Below is the schematic of Single Bit Full Adder:



- Netlist (Without Optimization) of above schematic i.e Single Bit FA:

```

1bit_FA 1bit_FA
* SPICE Netlist for Single Bit Full Adder
*nmos model file
.model nch NMOS
+ LEVEL = 3
+ VTO = 0.70
+ UO = 660
+ TOX = 1.40E-08
+ NSUB = 3E+16
+ XJ = 2.0e-7
+ LD = 1.6E-08
+ NFS = 7e+11
+ VMAX = 1.8e5
+ DELTA = 2.40
+ ETA = 0.1
+ KAPPA = 0.15
+ THETA = 0.1
+ CGDO = 2.20E-10
+ CGSO = 2.20E-10
+ CGBO = 7.00E-10
+ MJ = 0.50
+ CJSW = 3.50E-10
+ MJSW = 0.38
*pmos model file
.model pch PMOS
+ LEVEL = 3
+ VTO = -0.70
+ UO = 210
+ TOX = 1.40E-08
+ NSUB = 6.00E+16
+ XJ = 2.0e-7
+ LD = 1.5E-08
+ NFS = 6e+11
+ VMAX = 2.00e5
+ DELTA = 1.25
-----
+ ETA = 0.1
+ KAPPA = 2.5
+ THETA = 0.1
+ CGDO = 2.20E-10
+ CGSO = 2.20E-10
+ CGBO = 7.00E-10
+ MJ = 0.50|
M1 3 4 0 0 nch l=1u w=4u
M2 3 5 0 0 nch l=1u w=4u
M3 1 2 3 0 nch l=1u w=4u
M4 1 4 6 0 nch l=1u w=2u
M5 6 5 0 0 nch l=1u w=2u
M6 10 1 11 0 nch l=1u w=2u
M7 11 4 0 0 nch l=1u w=2u
M8 11 5 0 0 nch l=1u w=2u
M9 11 2 0 0 nch l=1u w=2u
M10 14 5 15 0 nch l=1u w=3u
M11 10 4 14 0 nch l=1u w=3u
M12 15 2 0 0 nch l=1u w=3u
M13 8 2 1 16 pch l=1u w=12u
M14 16 4 8 16 pch l=1u w=12u
M15 16 5 8 16 pch l=1u w=12u
M16 7 4 1 16 pch l=1u w=6u
M17 16 5 7 16 pch l=1u w=6u
M18 9 1 10 16 pch l=1u w=6u
M19 16 4 9 16 pch l=1u w=6u
M21 16 5 9 16 pch l=1u w=6u
M22 16 2 9 16 pch l=1u w=6u
M20 13 4 10 16 pch l=1u w=9u
M23 12 5 13 16 pch l=1u w=9u
M24 16 2 12 16 pch l=1u w=9u

```

```

VA 4 0 PULSE(3.3 0 0 10p 10p 20m 40m)
VB 5 0 PULSE(3.3 0 0 10p 10p 10m 20m)
VCin 2 0 PULSE(3.3 0 0 10p 10p 5m 10m)
Vdd 16 0 3.3v
CCin 2 0 2f
C1 1 0 50f
C2 10 0 50f
C3 2 0 2f
C4 2 0 2f
C5 2 0 2f
C6 2 0 2f

.tran 40m
.end

```

- Netlist with optimization:

```

M1 3 4 0 0 nch l=1u w=7u
M2 3 5 0 0 nch l=1u w=7u
M3 1 2 3 0 nch l=1u w=7u
M4 1 4 6 0 nch l=1u w=2u
M5 6 5 0 0 nch l=1u w=2u
M6 10 1 11 0 nch l=1u w=2u
M7 11 4 0 0 nch l=1u w=2u
M8 11 5 0 0 nch l=1u w=2u
M9 11 2 0 0 nch l=1u w=2u
M10 14 5 15 0 nch l=1u w=3u
M11 10 4 14 0 nch l=1u w=3u
M12 15 2 0 0 nch l=1u w=3u
M13 8 2 1 16 pch l=1u w=21u
M14 16 4 8 16 pch l=1u w=21u
M15 16 5 8 16 pch l=1u w=21u
M16 7 4 1 16 pch l=1u w=6u
M17 16 5 7 16 pch l=1u w=6u
M18 9 1 10 16 pch l=1u w=6u
M19 16 4 9 16 pch l=1u w=6u
M21 16 5 9 16 pch l=1u w=6u
M22 16 2 9 16 pch l=1u w=6u
M20 13 4 10 16 pch l=1u w=9u
M23 12 5 13 16 pch l=1u w=9u
M24 16 2 12 16 pch l=1u w=9u

```

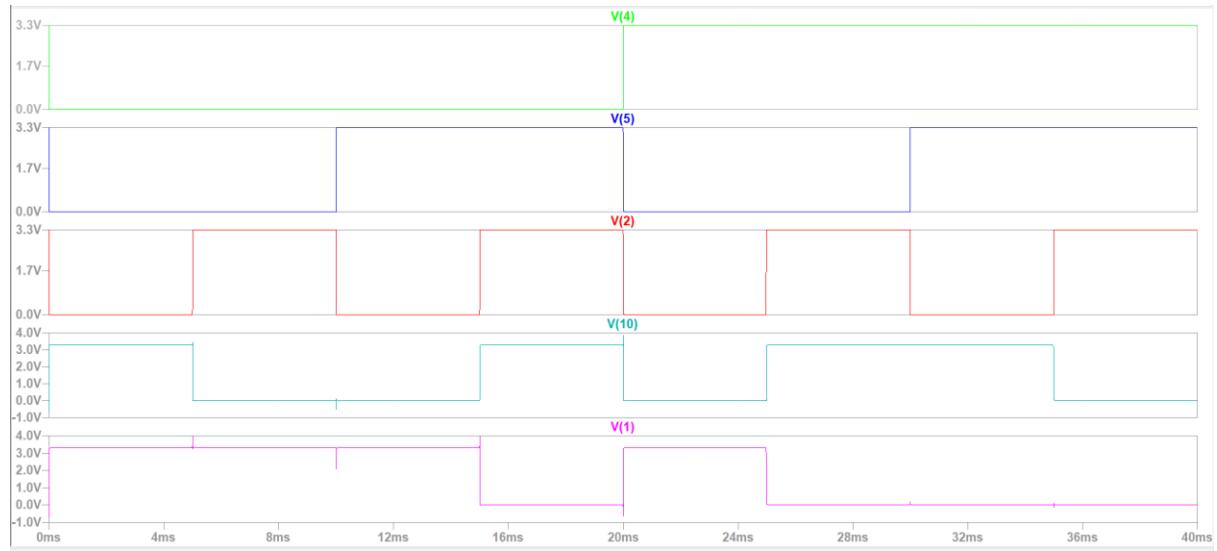
```

VA 4 0 PULSE(3.3 0 0 10p 10p 20m 40m)
VB 5 0 PULSE(3.3 0 0 10p 10p 10m 20m)
VCin 2 0 PULSE(3.3 0 0 10p 10p 5m 10m)
Vdd 16 0 3.3v
CCin 2 0 2f
C1 1 0 50f
C2 10 0 50f
C3 2 0 2f
C4 2 0 2f
C5 2 0 2f
C6 2 0 2f

.tran 40m
.end

```

- Waveform Without optimization:



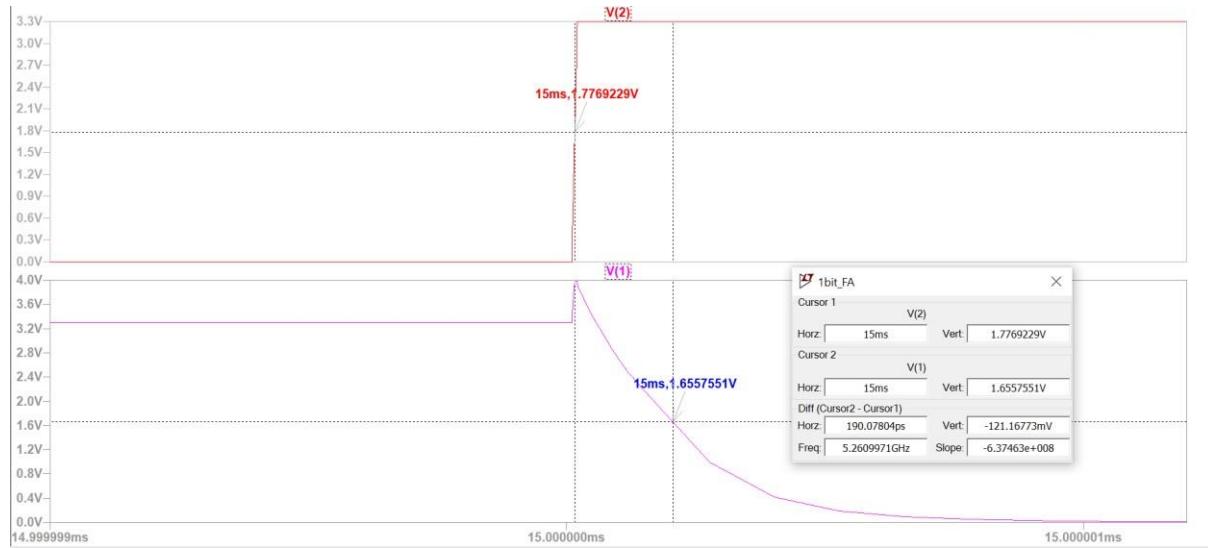
Green- A

Blue- B

Red- Cin

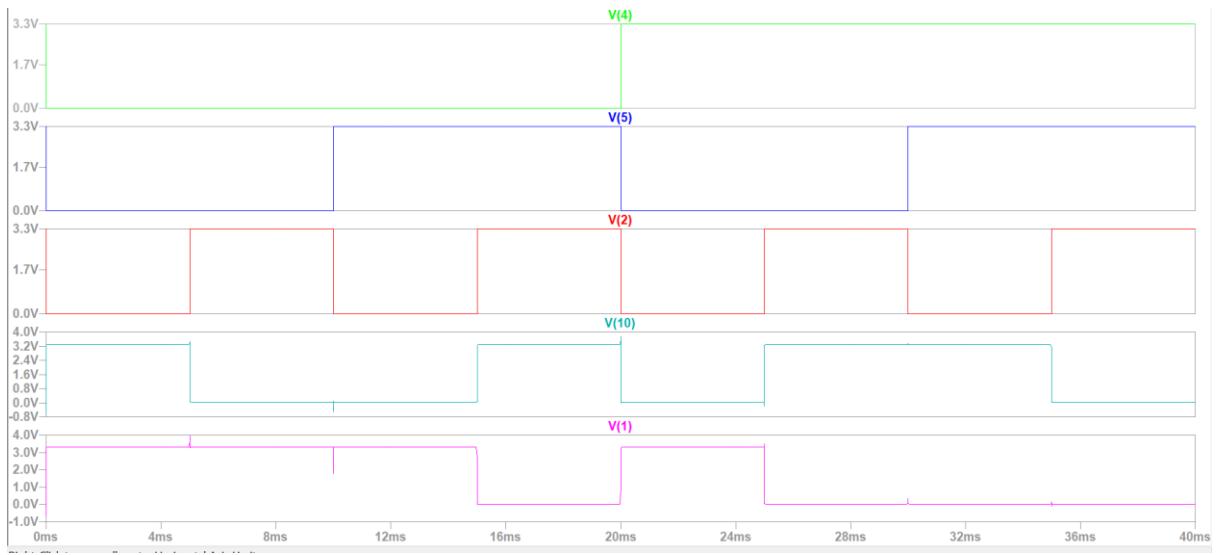
Light Blue- Sum\_bar

Pink- Cout\_bar



Delay=190 ps

- Waveform with optimization



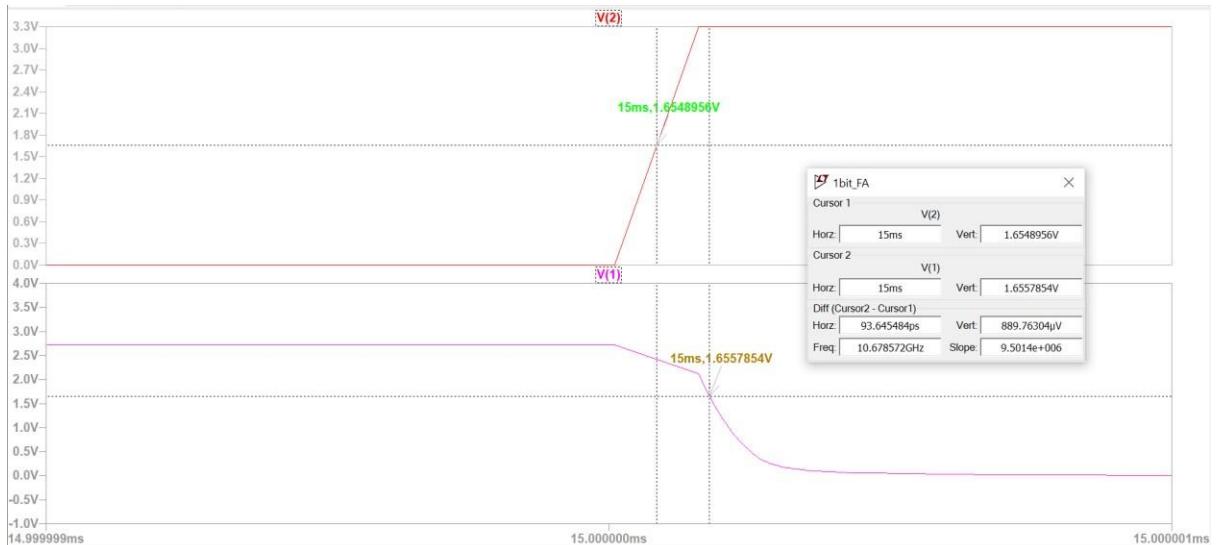
Green- A

Blue- B

Red- Cin

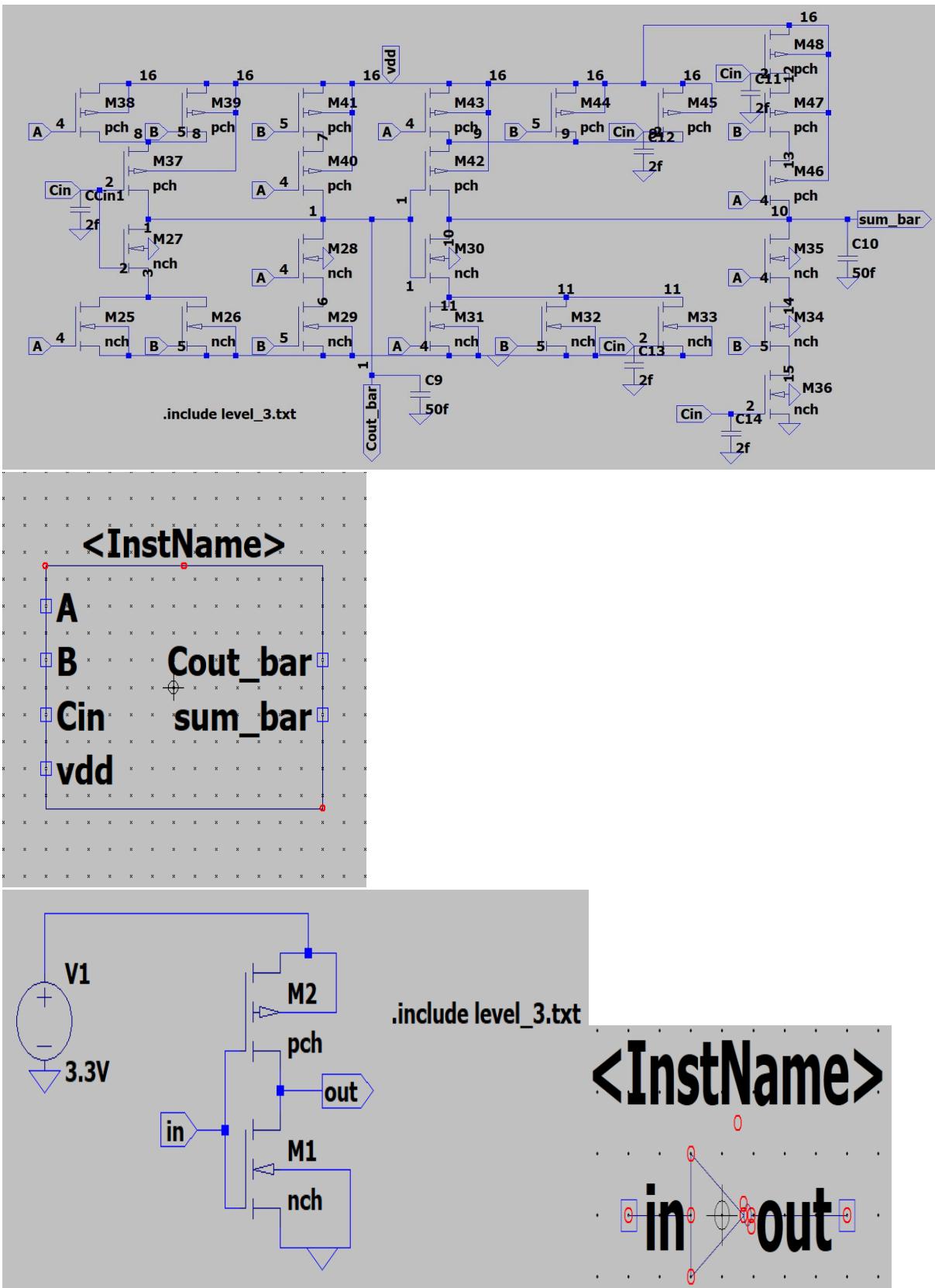
Light Blue- Sum\_bar

Pink- Cout\_bar

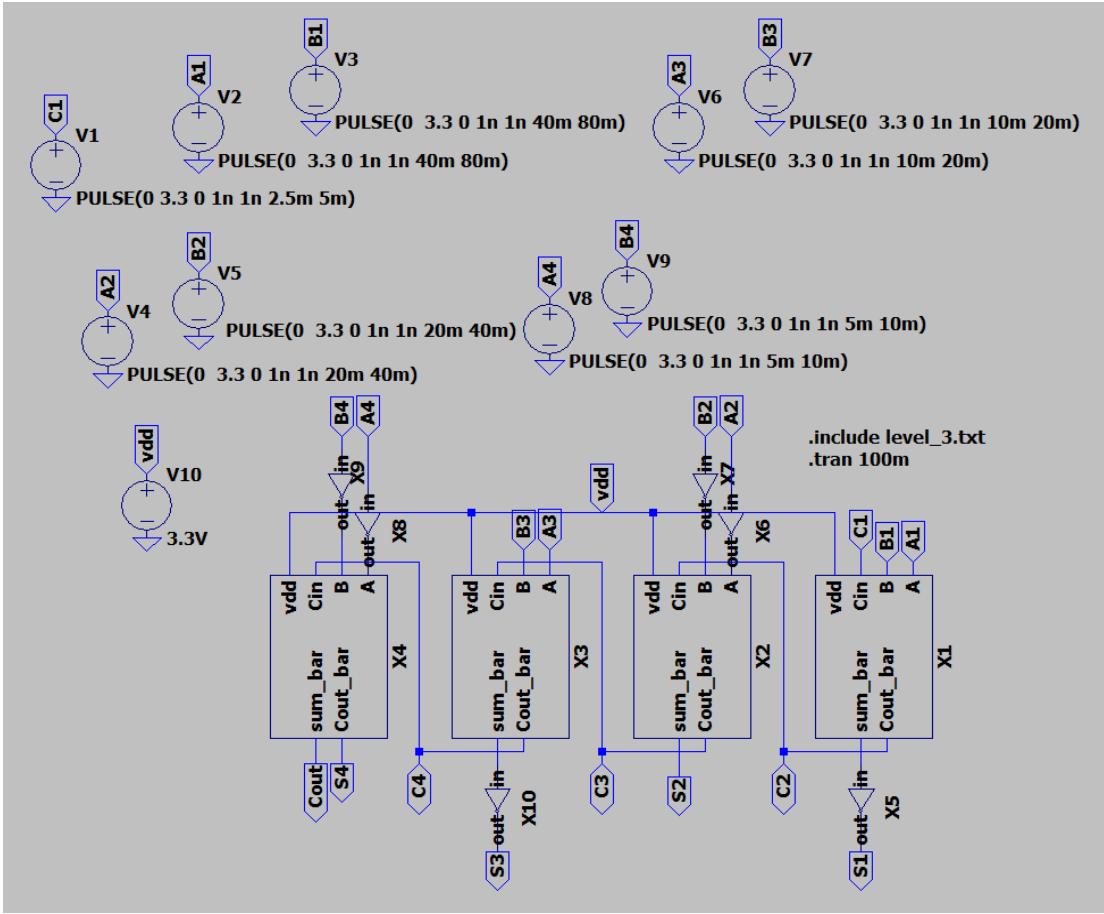


Delay=93.65 ps

- 1-Bit FA for symbol generation



- 4-Bit Ripple Carry Adder using 4 single bit FA as instances:



- Netlist for 4-Bit RCA:

```
* SPICE Netlist of 4-Bit Ripple Carry Adder Using 4 1-Bit FA
XX1 A1 B1 C1 vdd C2 N004 fa_1bit_for_symbol
XX2 P001 N002 C2 vdd C3 S2 fa_1bit_for_symbol
XX3 A3 B3 C3 vdd C4 N003 fa_1bit_for_symbol
XX4 P002 N001 C4 vdd S4 Cout fa_1bit_for_symbol
V2 A1 0 PULSE (0 3.3 0 1n 1n 40m 80m)
V3 B1 0 PULSE (0 3.3 0 1n 1n 40m 80m)
V4 A2 0 PULSE (0 3.3 0 1n 1n 20m 40m)
V5 B2 0 PULSE (0 3.3 0 1n 1n 20m 40m)
V7 B3 0 PULSE (0 3.3 0 1n 1n 10m 20m)
V8 A4 0 PULSE (0 3.3 0 1n 1n 5m 10m)
V1 C1 0 PULSE (0 3.3 0 1n 1n 2.5m 5m)
V6 A3 0 PULSE (0 3.3 0 1n 1n 10m 20m)
V9 B4 0 PULSE (0 3.3 0 1n 1n 5m 10m)
V10 vdd 0 3.3V
XX5 N004 S1 inverter_level3
XX6 A2 P001 inverter_level3
XX7 B2 N002 inverter_level3
XX8 A4 P002 inverter_level3
XX9 B4 N001 inverter_level3
XX10 N003 S3 inverter_level3

* block symbol definitions
.subckt fa_1bit_for_symbol A B Cin vdd Cout_bar sum_bar
M25 3 A 0 0 nch l=lu w=7u
M26 3 B 0 0 nch l=lu w=7u
M27 Cout_bar Cin 3 0 nch l=lu w=7u
M28 Cout_bar A 6 0 nch l=lu w=2u
M29 6 B 0 0 nch l=lu w=2u
M30 sum_bar Cout_bar 11 0 nch l=lu w=2u
M31 11 A 0 0 nch l=lu w=2u
M32 11 B 0 0 nch l=lu w=2u
M33 11 Cin 0 0 nch l=lu w=2u
M34 14 B 15 0 nch l=lu w=3u
.include level_3.txt
.tran 100m
```

```

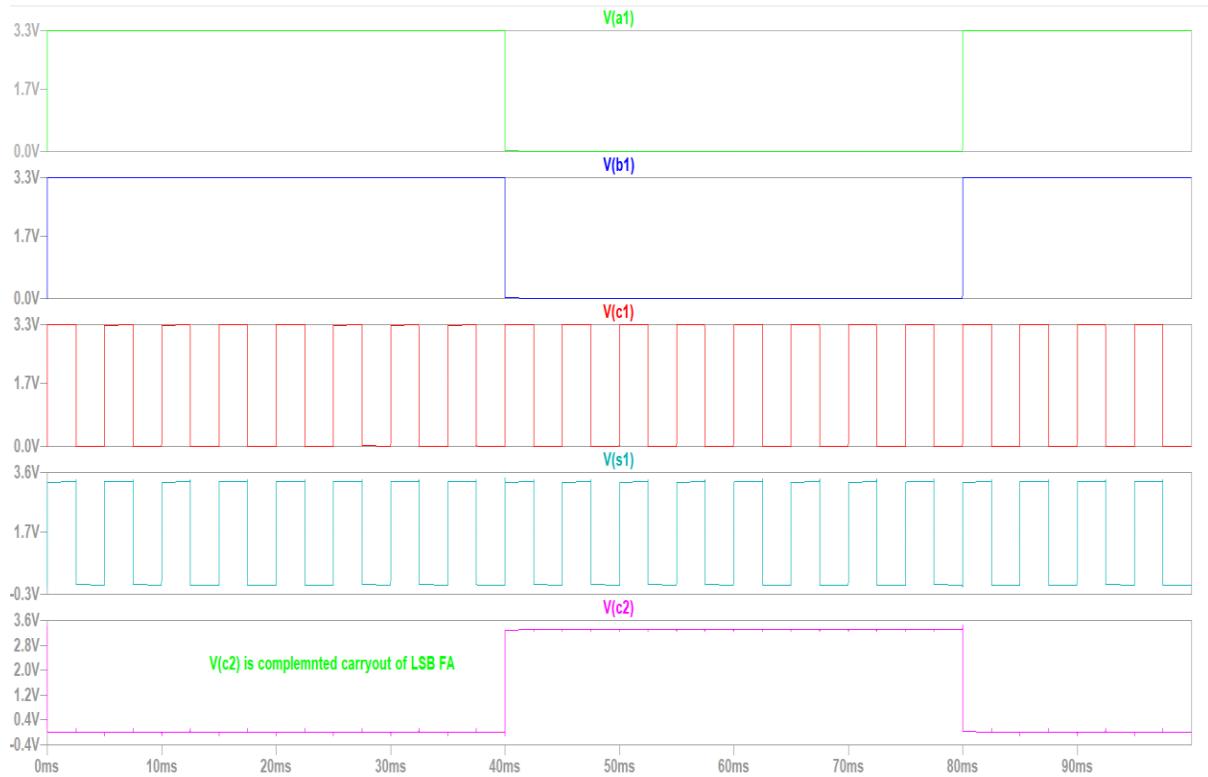
M35 sum_bar A 14 0 nch l=1u w=3u
M36 15 Cin 0 0 nch l=1u w=3u
M37 8 Cin Cout_bar vdd pch l=1u w=21u
M38 vdd A 8 vdd pch l=1u w=21u
M39 vdd B 8 vdd pch l=1u w=21u
M40 7 A Cout_bar vdd pch l=1u w=6u
M41 vdd B 7 vdd pch l=1u w=6u
M42 9 Cout_bar sum_bar vdd pch l=1u w=6u
M43 vdd A 9 vdd pch l=1u w=6u
M44 vdd B 9 vdd pch l=1u w=6u
M45 vdd Cin 9 vdd pch l=1u w=6u
M46 13 A sum_bar vdd pch l=1u w=9u
M47 12 B 13 vdd pch l=1u w=9u
M48 vdd Cin 12 vdd pch l=1u w=9u
CCin1 Cin 0 2f
C9 Cout_bar 0 50f
C10 sum_bar 0 50f
C11 Cin 0 2f
C12 Cin 0 2f
C13 Cin 0 2f
C14 Cin 0 2f
.include level_3.txt
.ends fa_1bit_for_symbol

.subckt inverter_level3 in out
M1 out in 0 0 nch l=1u w=1u
M2 N001 in out N001 pch l=1u w=3u
V1 N001 0 3.3V
.include level_3.txt
.ends inverter_level3

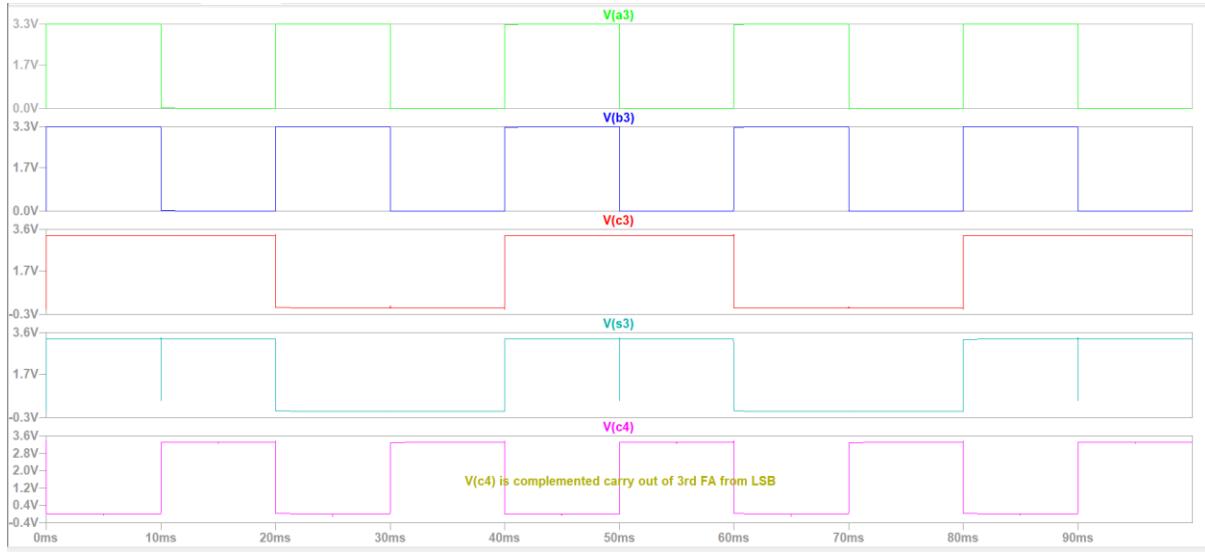
.include level_3.txt
.tran 100m
.end

```

- Waveform of LSB FA of RCA:



- Waveform for 3<sup>rd</sup> FA from LSB of RCA:



**Problem Statement 2:** Design a super buffer using CMOS inverters to drive a load of 100 pF, assume the input capacitance to be 2 pF.

**Solution:** Designed a super-buffer and optimised it along with sizing done.

Below attached is the analysis, delay calculation, sizing and optimizing done for super-buffer.

Q.2 Given,  $C_L = 100 \text{ fF}$  } we assumed in  
 $C_{in} = 2 \text{ fF}$  } FF for  
 We have to make smaller ( $\downarrow$ )  
 superbuffer,  $\because$  we are not concerned of output being normal or comple  
 to, we will consider optimal  $N$  for it is.

Optimal no of stages  $\Rightarrow \hat{N} = \log \frac{f}{3.57}$

in  $\boxed{\begin{array}{c} 4W \\ \boxed{3W} \\ \boxed{1W} \end{array}}$   $g_{out} = 1$ ,  $h = \frac{\text{Const} (C_L)}{C_{in}}$

$$= \frac{100}{2} = 50$$

$$\Rightarrow f = g \cdot h = 50$$

$$\therefore \hat{N} = \log \frac{50}{3.57} = 3.06$$

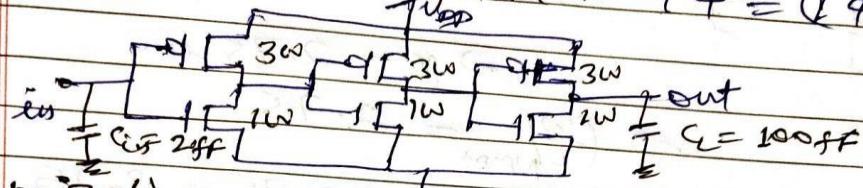


for  $N=3$ ,

$$d = \frac{3x(50)^{1/3}}{1} + 3 \quad \text{for } N=2 \\ = \frac{(14.05)^2}{1} \text{ minimum}$$

for  $N=4$ ,

$$d = \frac{4x(50)^{1/4}}{1} + 4 = (14.63)^2$$



optimization →

~~for  $\frac{C_{in1}}{C_{in2}} = \frac{C_{in2}}{C_{in3}} = \frac{C_{in3}}{C_{out}}$  minimum delay,~~

Here,  $N=3$ ,

$$\Rightarrow g_1 = g_2 = g_3 = 1 \\ \Rightarrow f = (50)^{1/3} = 3.684$$

①

$$g_3 h_3 = f \\ 1 \times \frac{c_1}{c_{in3}} = 3.684$$

$$\Rightarrow c_{in3} = \frac{100fF}{3.684} = 27.144fF$$

$$\Rightarrow c_{in2} = \frac{c_{in3}}{3.684} = 7.368fF$$

$$\text{cross checking } \left\{ c_{in1} = \frac{7.368}{3.684} = 2 = c_{in} \right. \quad \left. \text{verified} \right.$$

Now, calculating ( $w/L$ ) of each MOSFETs,

$$(t_{ox} = 1.4 \times 10^{-8} m) \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times (8.85 \times 10^{-12}) F/m}{1.4 \times 10^{-8} m}$$

$$[C_{ox} = 27.653 \times 10^{-12} F/m^2]$$

$$1\text{fF} = 10^{-15}\text{F}, \quad 1\text{pF} = 10^{-12}\text{F}$$

for Stage-3 Considering.

$$L_{min} = 1\text{nm}$$

$$\left. \begin{array}{l} C_{in3} \\ \downarrow \\ \text{out} \\ \left. \begin{array}{l} 3x \\ \downarrow \\ 1x \end{array} \right. \\ \left. \begin{array}{l} 4x \\ \downarrow \\ 1x \end{array} \right. \end{array} \right\} \Rightarrow (4x) \times (\text{Cox} \cdot L_{min}) = C_{in3} \\ (4x)(24.853 \times 10^{-4}) \times 10^{-6} = 27.19 \text{ pF}$$

$$\Rightarrow x = 2.75 \text{ nm}$$

$$\Rightarrow \frac{(w)}{l_{pmos}} = 2.75$$

$$\Rightarrow \frac{(w)}{l_{pmos}} = 3x2.75 = 8.25$$

for stage-2

$$(4x) \times (\text{Cox} \cdot L_{min}) = C_{in2}$$

$$\Rightarrow x = 0.747 \text{ nm}$$

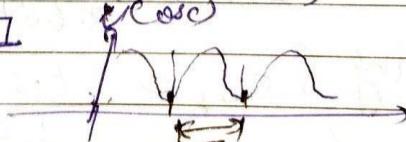
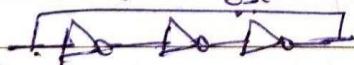
$$\Rightarrow \frac{(w)}{l_{pmos}} = 0.747 \text{ nm}$$

$$\frac{(w)}{l_{pmos}} = 2.241$$

Similarly, for stage-3,

$$\frac{(w)}{l_{pmos}} = 0.2 \text{ nm} \quad \frac{(w)}{l_{nmos}} = 0.6 \text{ nm}$$

Calculating  $\tau$  for delay, Using Ring oscillator calculated  $\tau$ ,



$$\tau = 2\pi n \times T$$

$n$  no of inverters in ring.

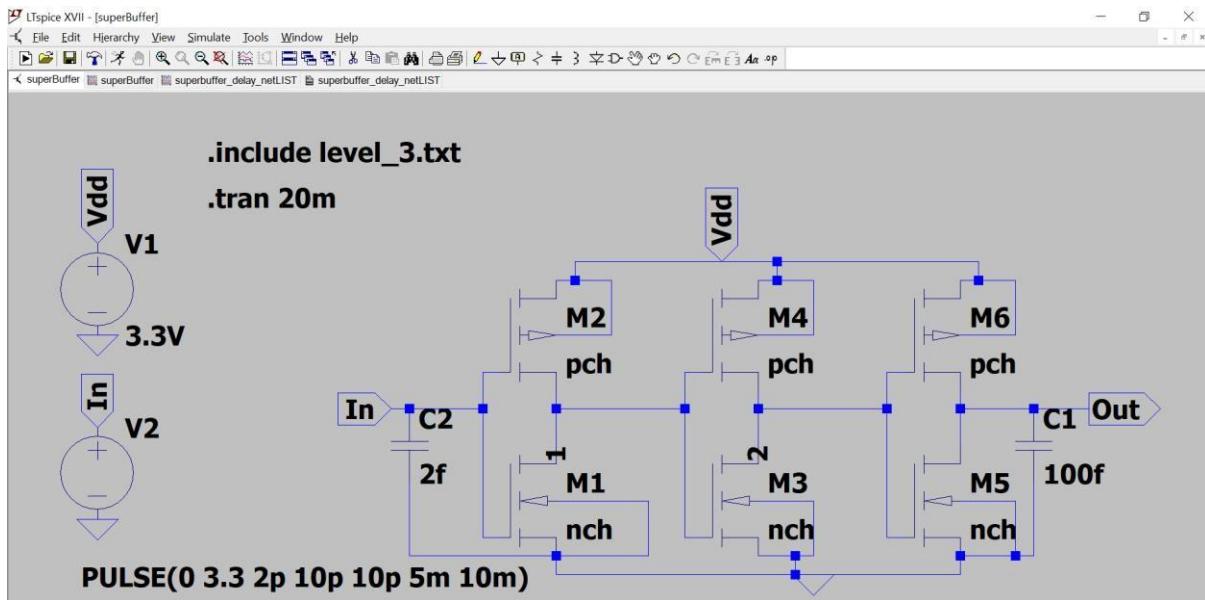
for our case,  $T = 884 \text{ nsec}$

$$\Rightarrow \tau = (6 \times 884) \text{ nsec}$$

$$\Rightarrow 5.3 \text{ nsec}$$

$\Rightarrow$  Delay is of nsec order.

- Schematic of Superbuffer:



- Netlist (Without Optimization) and Spice Error Log:

```
M1 1 In 0 0 nch l=lu w=lu
M2 Vdd In 1 Vdd pch l=lu w=lu
M3 2 1 0 0 nch l=lu w=lu
M4 Vdd 1 2 Vdd pch l=lu w=lu
M5 Out 2 0 0 nch l=lu w=lu
M6 Vdd 2 Out Vdd pch l=lu w=lu
V1 Vdd 0 3.3V
V2 In 0 PULSE(0 3.3 2p 10p 10p 5m 10m)
C1 Out 0 100f
C2 In 0 2f

.param supply=3.3v

.meas tran trise
+TRIG V(out) val='0.1*supply' rise=1
+TARG V(out) val='0.9*supply' rise=1

.meas tran tfall
+TRIG V(out) val='0.9*supply' fall=1
+TARG V(out) val='0.1*supply' fall=1

.measure tran tphl
+TRIG V(in) val='0.5*supply' fall=1
+TARG V(out) val='0.5*supply' rise=1

.measure tran tphl
+TRIG v(in) val='0.5*supply' rise=1
+TARG V(out) val='0.5*supply' fall=1

.measure delay param='(tphl+tplh)/2'
.tran 20m
.include level_3.txt
.end
```

SPICE Error Log: C:\Users\suman\Desktop\LTspice\superbuffer\_delay.netLIST.log

Questionable use of curly braces in ".measure delay param={(tphl+tplh)/2}"  
Error: undefined symbol in: "([tphl]+tplh)/2"  
Circuit: \* SPICE Netlist for Superbuffer

Model "pch": Oxide thickness thinner than recommended for a level 3 MOSFET.  
Model "nch": Oxide thickness thinner than recommended for a level 3 MOSFET.  
Instance "m6": Width narrower than recommended for a level 3 MOSFET.  
Instance "m4": Width narrower than recommended for a level 3 MOSFET.  
Instance "m2": Width narrower than recommended for a level 3 MOSFET.  
Instance "m5": Width narrower than recommended for a level 3 MOSFET.  
Instance "m3": Width narrower than recommended for a level 3 MOSFET.  
Instance "m1": Width narrower than recommended for a level 3 MOSFET.  
Direct Newton iteration for .op point succeeded.

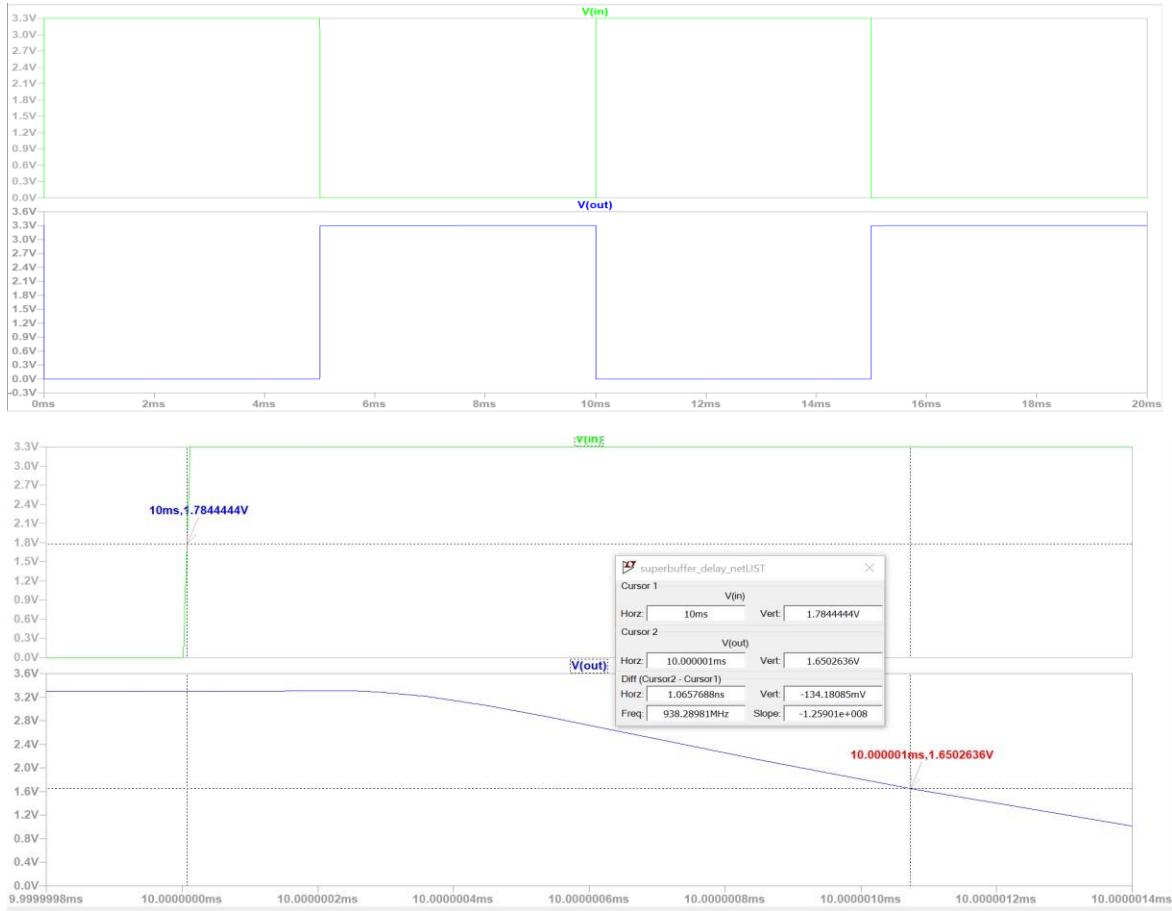
trise=3.54801e-009 FROM 0.005 TO 0.005
tfall=1.3963e-009 FROM 4.91444e-010 TO 1.88775e-009
tplh=2.03663e-009 FROM 0.005 TO 0.005
tphl=1.06711e-009 FROM 7e-012 TO 1.07411e-009
delay: ((tphl+tplh)/2)=1.55187e-009

Date: Sun Feb 20 18:47:36 2022
Total elapsed time: 0.171 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2825
traniter = 2804
tranpoints = 1294
accept = 1251
rejected = 43

Delay=1.55 ns

- Waveform without optimization:



- Optimised Netlist:-

```

M1 1 In 0 0 nch l=lu w=0.2u
M2 Vdd In 1 Vdd pch l=lu w=0.6u
M3 2 1 0 0 nch l=lu w=0.747u
M4 Vdd 1 2 Vdd pch l=lu w=2.241u
M5 Out 2 0 0 nch l=lu w=2.75u
M6 Vdd 2 Out Vdd pch l=lu w=8.25u
V1 Vdd 0 3.3V
V2 In 0 PULSE(0 3.3 2p 10p 10p 5m 10m)
C1 Out 0 100f
C2 In 0 2f

.param supply=3.3v

.meas tran trise
+TRIG V(out) val='0.1*supply' rise=1
+TARG V(out) val='0.9*supply' rise=1

.meas tran tfall
+TRIG V(out) val='0.9*supply' fall=1
+TARG V(out) val='0.1*supply' fall=1

.measure tran tphl
+TRIG V(in) val='0.5*supply' fall=1
+TARG V(out) val='0.5*supply' rise=1

.measure tran tphl
+TRIG V(in) val='0.5*supply' rise=1
+TARG V(out) val='0.5*supply' fall=1

.measure delay param='(tphl+tphl)/2'
.tran 20m
.include level_3.txt
.end

```

SPICE Error Log: C:\Users\suman\Desktop\Ltspice\superbuffer\_delay\_netLIST.log

Questionable use of curly braces in ".measure delay param={(tphl+tphl)/2}"  
 Error: undefined symbol in: "({tphl}+{tphl})/2"  
 Circuit: \* SPICE Netlist for Superbuffer

Model "pch": Oxide thickness thinner than recommended for a level 3 MOSFET.  
 Model "nch": Oxide thickness thinner than recommended for a level 3 MOSFET.  
 Instance "m2": Width narrower than recommended for a level 3 MOSFET.  
 Instance "m3": Width narrower than recommended for a level 3 MOSFET.  
 Instance "m1": Width narrower than recommended for a level 3 MOSFET.  
 Direct Newton iteration for .op point succeeded.

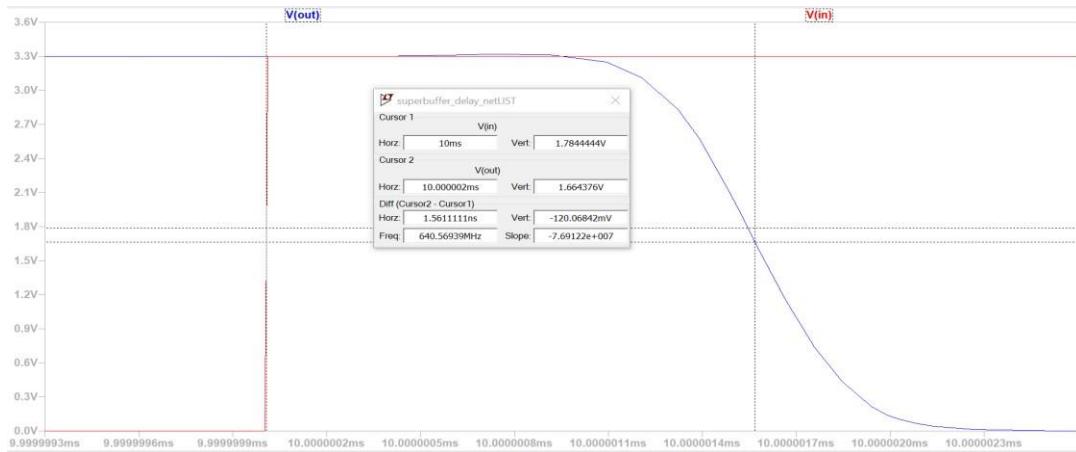
trise=6.06125e-010 FROM 0.005 TO 0.005  
 tfall=6.20552e-010 FROM 1.26797e-009 TO 1.88852e-009  
 tphl=1.16197e-009 FROM 0.005 TO 0.005  
 tphl=1.56381e-009 FROM 7e-012 TO 1.57081e-009  
 delay: ((tphl+tphl)/2)=1.36289e-009

Date: Sun Feb 20 19:00:47 2022  
 Total elapsed time: 0.172 seconds.

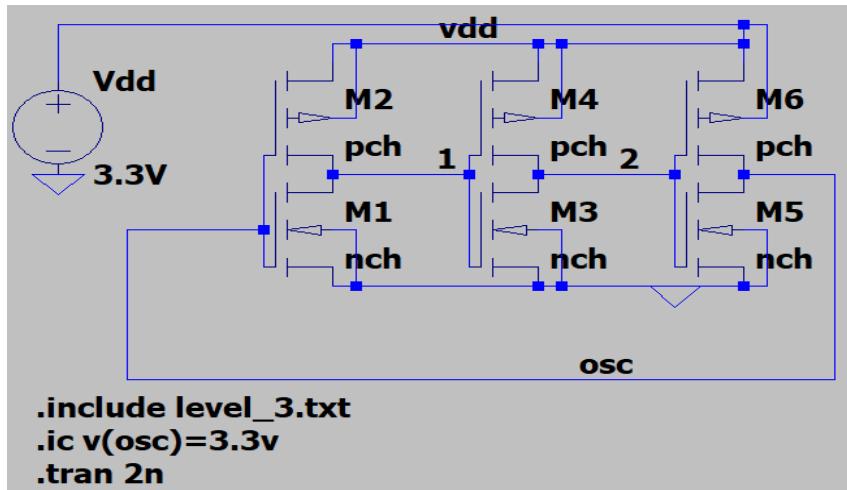
tnom = 27  
 temp = 27  
 method = modified trap  
 totiter = 2791  
 traniter = 2776  
 tranpoints = 1310  
 accept = 1262  
 rejected = 48  
 matrix size = 7  
 fillins = 0  
 solver = Normal

Delay= 1.36 ns

- Optimized Waveform



- Ring Oscillator for Tau Calculation:



- Netlist for Ring Oscillator:

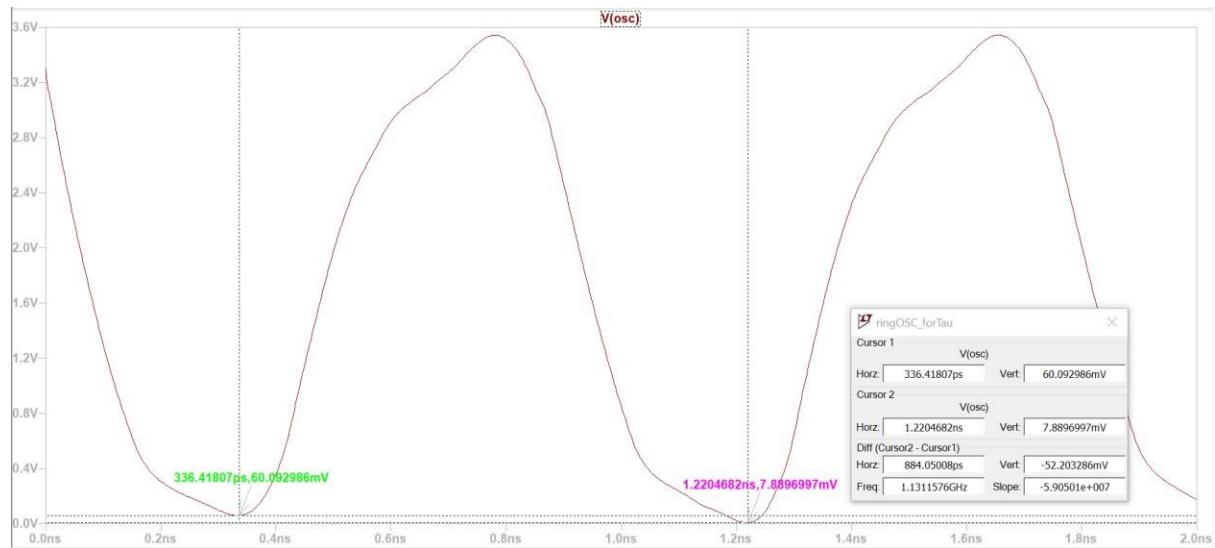
```

* SPICE Netlist for Tau Calculation using Ring Oscillator
M1 1 osc 0 0 nch l=1u w=1u
M2 vdd osc 1 vdd pch l=1u w=3u
M3 2 1 0 0 nch l=1u w=1u
M4 vdd 1 2 vdd pch l=1u w=3u
M5 osc 2 0 0 nch l=1u w=1u
M6 vdd 2 osc vdd pch l=1u w=3u
Vdd vdd 0 3.3V

.include level_3.txt
.ic v(osc)=3.3v
.tran 2n
.end

```

- Waveform for Ring Oscillator:



$\text{Tau} = 2n * (\text{time period}) \quad \{ \text{Here } n \text{ is number of inverters in oscillator ckt., } n=3 \}$

So,  $\text{Tau} = 2*3*(884 \text{ ps}) = 5.3 \text{ ns} \Rightarrow (\text{Delay is of the order of nanosecond})$

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